AKDENİZ UNIVERSITY
CSE 211 – Digital Design

LAB06 Assignment

Your task is to design **4-bit by 3-bit multiplier (Fig.1)** in Proteus Design Suite. A template proteus scheme for only inputs and outputs are shown in the figure below. You must show inputs and outputs with hexadecimal number with seven segment displays as shown in the figure. This displays show hexadecimal values (In the figure below, 6 times 4 is 24 in decimal, but its corresponding hexadecimal value is 18 as shown in the display).

PS: A template project is given in the attached files.

- **74LS83** : 4 bit binary full adder component
- **And Gate**: Logic and gate
- **7SEG-BCD:** Seven Segment Display
- **Logic State, logic probe(big)**

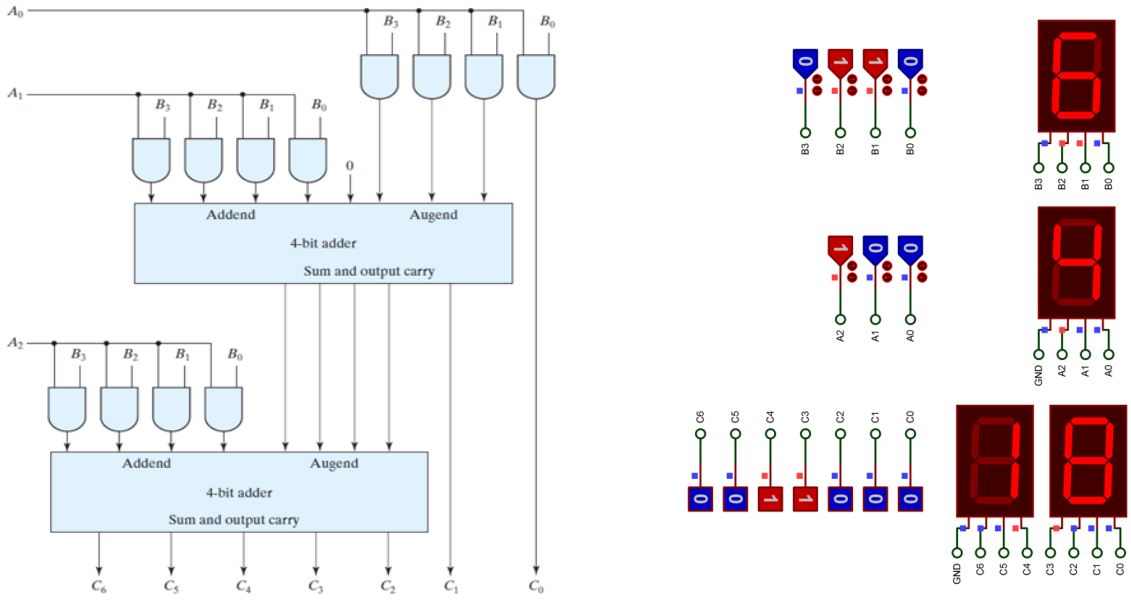

Figure 1. 3-bit by 4-bit multiplier diagram