2018-2019 FALL SEMESTER

CS 223 – DIGITAL DESIGN

LAB 3 – 04.11.2018

SECTION: 1

NAME: MUNIB EMRE

SURNAME: SEVILGEN

STUDENT ID: 21602416

TRAINER PACK: 09

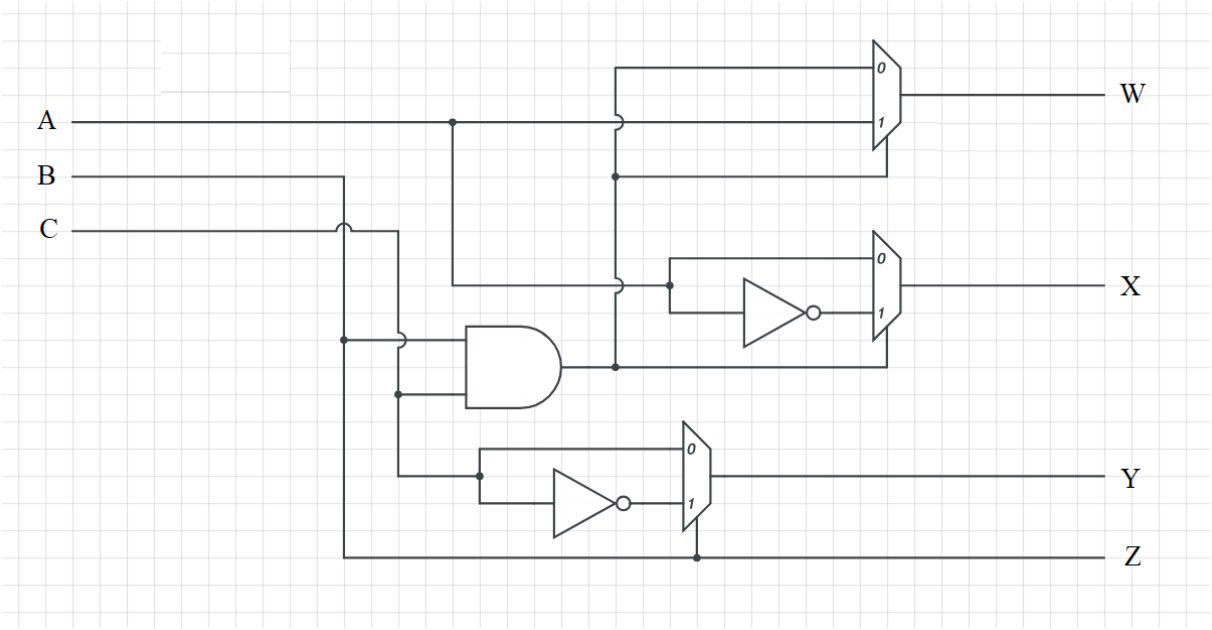

Figure 1 - Schematic for the converter ciruit

// 2:1 Multiplexer module

```
module two_to_one_multiplexer (input logic i0, i1, s, output logic y);
        assign y = s ? i1 : i0;
endmodule
```

// The converter circuit module

```
module converter_circuit (input logic a, b, c, output logic w, x, y, z);
        logic l1;
        and (l1, b, c);
        two_to_one_multiplexer mux1 (l1, a, l1, w);
        two_to_one_multiplexer mux2 (a, ~a, l1, x);
        two_to_one_multiplexer mux3 (c, ~c, b, y);
        assign z = b;
endmodule
```

// Testbench module for the converter circuit module

```
module testbench ();
        logic a, b, c;
        logic w, x, y, z;
        converter_circuit dut(a, b, c, w, x, y, z);
        initial begin
                a = 0; b = 0; c = 0; #10;
                c = 1; #10;
                b = 1; c = 0; #10;
                c = 1; #10;
                a = 1; b = 0; c = 0; #10;
                c = 1; #10;
                b = 1; c = 0; #10;
```

```
            c = 1; #10;
        end
endmodule
```

// Constraint file before seven-segment

```
# Switches
set_property PACKAGE_PIN V17 [get_ports {c}]
   set_property IOSTANDARD LVCMOS33 [get_ports {c}]
set_property PACKAGE_PIN V16 [get_ports {b}]
   set_property IOSTANDARD LVCMOS33 [get_ports {b}]
set_property PACKAGE_PIN W16 [get_ports {a}]
   set_property IOSTANDARD LVCMOS33 [get_ports {a}]

# LEDs
set_property PACKAGE_PIN U16 [get_ports {z}]
   set_property IOSTANDARD LVCMOS33 [get_ports {z}]
set_property PACKAGE_PIN E19 [get_ports {y}]
   set_property IOSTANDARD LVCMOS33 [get_ports {y}]
set_property PACKAGE_PIN U19 [get_ports {x}]
   set_property IOSTANDARD LVCMOS33 [get_ports {x}]
set_property PACKAGE_PIN V19 [get_ports {w}]
   set_property IOSTANDARD LVCMOS33 [get_ports {w}]
```

// The new converter circuit module to show at 7 segment

```
module converter_circuit (input logic a, b, c, clk, output logic w, x, y, z, o_a, o_b, o_c, o_d, o_e,
                                    o_f, o_g, o_dp, [3:0]o_an);
        logic l1;
        logic [3:0] out;

        and (l1, b, c);
        two_to_one_multiplexer mux1 (l1, a, l1, w);
        two_to_one_multiplexer mux2 (a, ~a, l1, x);
        two_to_one_multiplexer mux3 (c, ~c, b, y);
        assign z = b;
        assign out[0] = z;
        assign out[1] = y;
        assign out[2] = x;
        assign out[3] = w;

        SevSeg_4digit seven_segment(clk, out, 0, 0, 0, o_a, o_b, o_c, o_d, o_e, o_f, o_g, o_dp,
                                                o_an);
endmodule
```

// The new constraint file after 7 segment

```
# Clock signal
set_property PACKAGE_PIN W5 [get_ports clk]
        set_property IOSTANDARD LVCMOS33 [get_ports clk]
```

```
# create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]

# Switches
set_property PACKAGE_PIN V17 [get_ports {c}]
   set_property IOSTANDARD LVCMOS33 [get_ports {c}]
set_property PACKAGE_PIN V16 [get_ports {b}]
   set_property IOSTANDARD LVCMOS33 [get_ports {b}]
set_property PACKAGE_PIN W16 [get_ports {a}]
   set_property IOSTANDARD LVCMOS33 [get_ports {a}]

# LEDs
set_property PACKAGE_PIN U16 [get_ports {z}]
   set_property IOSTANDARD LVCMOS33 [get_ports {z}]
set_property PACKAGE_PIN E19 [get_ports {y}]
   set_property IOSTANDARD LVCMOS33 [get_ports {y}]
set_property PACKAGE_PIN U19 [get_ports {x}]
   set_property IOSTANDARD LVCMOS33 [get_ports {x}]
set_property PACKAGE_PIN V19 [get_ports {w}]
   set_property IOSTANDARD LVCMOS33 [get_ports {w}]

# 7 segment display
set_property PACKAGE_PIN W7 [get_ports {o_a}]
      set_property IOSTANDARD LVCMOS33 [get_ports {o_a}]
set_property PACKAGE_PIN W6 [get_ports {o_b}]
      set_property IOSTANDARD LVCMOS33 [get_ports {o_b}]
set_property PACKAGE_PIN U8 [get_ports {o_c}]
      set_property IOSTANDARD LVCMOS33 [get_ports {o_c}]
set_property PACKAGE_PIN V8 [get_ports {o_d}]
      set_property IOSTANDARD LVCMOS33 [get_ports {o_d}]
set_property PACKAGE_PIN U5 [get_ports {o_e}]
      set_property IOSTANDARD LVCMOS33 [get_ports {o_e}]
set_property PACKAGE_PIN V5 [get_ports {o_f}]
      set_property IOSTANDARD LVCMOS33 [get_ports {o_f}]
set_property PACKAGE_PIN U7 [get_ports {o_g}]
      set_property IOSTANDARD LVCMOS33 [get_ports {o_g}]
set_property PACKAGE_PIN V7 [get_ports {o_dp}]
      set_property IOSTANDARD LVCMOS33 [get_ports {o_dp}]
set_property PACKAGE_PIN U2 [get_ports {o_an[0]}]
      set_property IOSTANDARD LVCMOS33 [get_ports {o_an[0]}]
set_property PACKAGE_PIN U4 [get_ports {o_an[1]}]
      set_property IOSTANDARD LVCMOS33 [get_ports {o_an[1]}]
set_property PACKAGE_PIN V4 [get_ports {o_an[2]}]
      set_property IOSTANDARD LVCMOS33 [get_ports {o_an[2]}]
set_property PACKAGE_PIN W4 [get_ports {o_an[3]}]
      set_property IOSTANDARD LVCMOS33 [get_ports {o_an[3]}]
```