CS223 Laboratory Assignment 3

Designing a Code Converter using Multiplexers

Section 1: 5.11.2018 Monday 08:40-12:25
Section 2: 6.11.2018 Tuesday 08:40-12:25
Section 3: 5.11.2018 Monday 13:40-17:25
Section 4: 6.11.2018 Tuesday 13:40-17:25
Section 5: 1.11.2018 Thursday 08:40-12:25
Section 6: 2.11.2018 Friday 08:40-12:25

Location: EA Z04 (in the EA building, straight ahead past the elevators)
Groups: Each student will do the lab individually. Group size = 1

Preliminary Report (30 points)

Today's lab needs considerable advance preparation. These advance designs and Systemverilog models should be prepared in advance, and assembled neatly into a Preliminary Report with a printed cover page and printed pages for the schematics and Systemverilog codes. Each page should have a proper heading. The contents of the report should be as follows:

a) A cover page which includes the following: course name and code number, the number of the lab, your name and student ID, date, number of your trainer pack (remember lab policies. You must always use same pack number).
b) Design of the Code Converter: A company has three directors A, B, and C. While running the company, the directors have to make decisions by voting on propositions about some issues. Each director has different vote according to his/her rank.:
   Mr/Ms A has 4 votes
   Mr/Ms B has 3 vote
   Mr/Ms C has 2 votes

   Each director has a switch to close when voting yes (1) and open when voting no (0). It is necessary to design a combinational circuit that displays the total number of votes that vote yes for a proposition.
   You are required to design a circuit with three inputs A,B,C and four outputs W,X,Y,Z which will show the sum of votes in binary. If all directors vote no, the output of your circuit will be WXYZ=0000. If all vote yes, output will be WXYZ=1001.
   Implement the code converter circuit using three 2-to-1 Multiplexers, one AND gate, and two NOT gates. You will lose 10 points (out of 30) for each extra logic gate you use.
c) Write the Systemverilog code for the code converter circuit. Prepare a test bench to test your circuit. Put your code in your report.
d) Connect the output of your circuit to the LEDs, and inputs to switches, on the BASYS3 board. Put the constraint file in your report.

e) This time, connect the output of your circuit (the 4-bit number) to the 7-segment decoder on the BASYS3 board, so you can see the result as a decimal number. (Systemverilog module is also given in the textbook. You can also download a ready one from here. Use only one of four digits of seven segment). Put the new constraint file in your report.

The Preliminary Report will be turned in at the start of lab. You may need a copy of your designs and Systemverilog programs with you in the lab to refer to or possibly correct and change it. In this lab, you don't need to connect your BASYS-3 board to the Beti board. Working with standalone BASYS-3 board and having it connected to your computer is enough. Create a new Xilinx Vivado Project to do each part. Use appropriate names for files and folders.

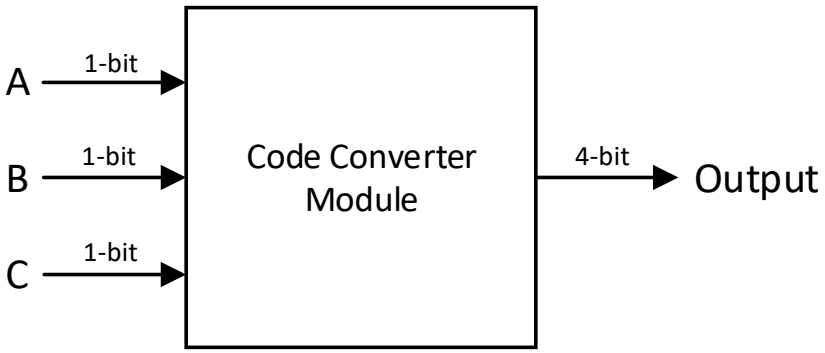

Figure 1: Code Converter Module

Implementation: Multiplexers and Boolean function implementation (70 points)

Create a Vivado project for Code Converter and enter the Systemverilog module to Vivado you prepared in preliminary work part (c).

a) Simulate the CodeConverter. Using the testbench code you prepared in preliminary work part (c), test your circuit, if correct show it to your TA.
b) Implement your code on FPGA. Inputs A, B and C should be applied using the switches on your BASYS3 board. The outputs W,X,Y,Z should be connected to LEDs. Show your implementation on the BASYS3 board to TA.
c) Using Systemverilog module sevenseg, display the output of the code converter on the seven segment displays on the BASYS3 board. Show your implementation on the BASYS3 board to TA.

Submit your code for MOSS similarity testing

Finally, when you are done and before leaving the lab, you need to upload the file *StudentID_SVerilog.txt* created in the Implementation with FPGA part. Be sure that the file contains exactly and only the codes which are specifically detailed above. If you have multiple files, just copy and paste them in order, one after another inside text file. Check the

specifications! Even if you didn't finish, or didn't get the Systemverilog part working, you must submit your code to the Unilica Assignment for similarity checking. Your codes will be compared against all the other codes in all sections of the class, by the MOSS program, to determine how similar it is (as an indication of plagiarism). So be sure that the code you submit is code that you actually wrote yourself! All students must upload their code to the 'Unilica>Assignment' specific for your section. Check submission time and don't miss it before leaving the lab. After taking a backup of your work, don't forget to delete it from computer. Because students of other sections will work with your system too.

Clean Up

1) Clean up your lab station, and return all the parts, wires, the Beti trainer board, etc. Leave your lab workstation for others the way you would like to find it.

2) CONGRATULATIONS! You are finished with this Lab and are one step closer to becoming a computer engineer.

NOTES

--Advance work on this lab, and all labs, is strongly suggested.
--Be sure to read and follow the Policies for CS223 labs, posted in Unilica.

LAB POLICIES

1. There are three computers in each row in the lab. Don't use middle computers, unless you are allowed by lab coordinator.
2. You borrow a lab-board containing the development board, connectors, etc. in the beginning. The lab coordinator takes your signature. When you are done, return it to his/ her, otherwise you will be responsible and lose points.
3. Each lab-board has a number. You must always use the same board throughout the semester.
4. You must be in the lab, working on the lab, from the time lab starts until you finish and leave. (bathroom and snack breaks are the exception to this rule). Absence from the lab, at any time, is counted as absence from the whole lab that day.
5. No cell phone usage during lab. Tell friends not to call during the lab hours--you are busy learning how digital circuits work!
6. Internet usage is permitted only to lab-related technical sites. No Facebook, Twitter, email, news, video games, etc--you are busy learning how digital circuits work!
7. Be on time. If you arrive late, you may lose that session completely.
8. When you are done, DO NOT return IC parts into the IC boxes where you've taken them first. Just put them inside your Lab-board box. Lab coordinator will check and return them later.