Bilkent University

EE102-02 Lab 7 Report:

Finite State Machine

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Purpose:

The purpose of this lab was to build a Finite State Machine (FSM) on the breadboard.

Methodology:

There are two stages in the designed circuit. With the two inputs entered, the result of the FSM will be observed through an output. The state transition diagram and truth table are initially used to build the design. The design is tested with sample inputs once the required logic gates are assembled on the breadboard.

Design Specifications:

The design shows the change in motion of a vehicle depending on the use of the accelerator and the handbrake.

Design details are as follows:

- State = ‘1’ for moving
- State = ‘0’ for motionless
- Input A = ‘1’ for accelerator is active
- Input A = ‘0’ for accelerator is not active
- Input HB = ‘1’ for handbrake is active
- Input HB = ‘0’ for handbrake is not active
- Output = ‘1’ for moving
- Output = ‘0’ for motionless

One D flip-flop was used for data storage in the designed Moore Machine. Two buttons were used for inputs and a LED for output. Also 1 Hz clock is used for the register. The state transition diagram (Figure 1) and output table (Table 1) created as a result of the design are as follows:

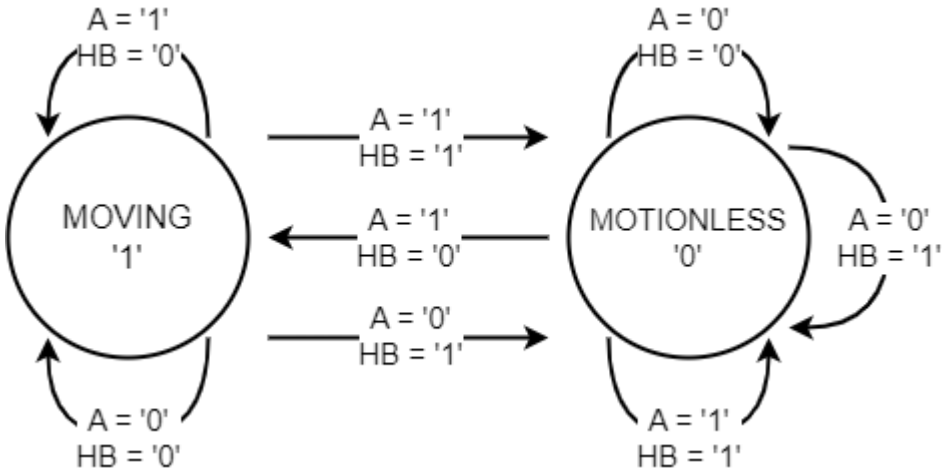

Figure 1: The state transition diagram of the design

M	A	HB	M*	OUT
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	0	1	1
0	0	1	0	0
0	1	1	0	0
1	0	1	0	0
1	1	1	0	0

Table 1:The Truth Table of Design

Finally, the ICs used in circuit design and their codes are as follows:

- (SN74HC74N) Positive-Edge D Flip Flop
- (SN74HC08N) Two input AND gate
- (SN74HC32N) Two input OR gate
- (SN74HC04N) NOT gate

Results:

FSM design created on the breadboard is as follows:

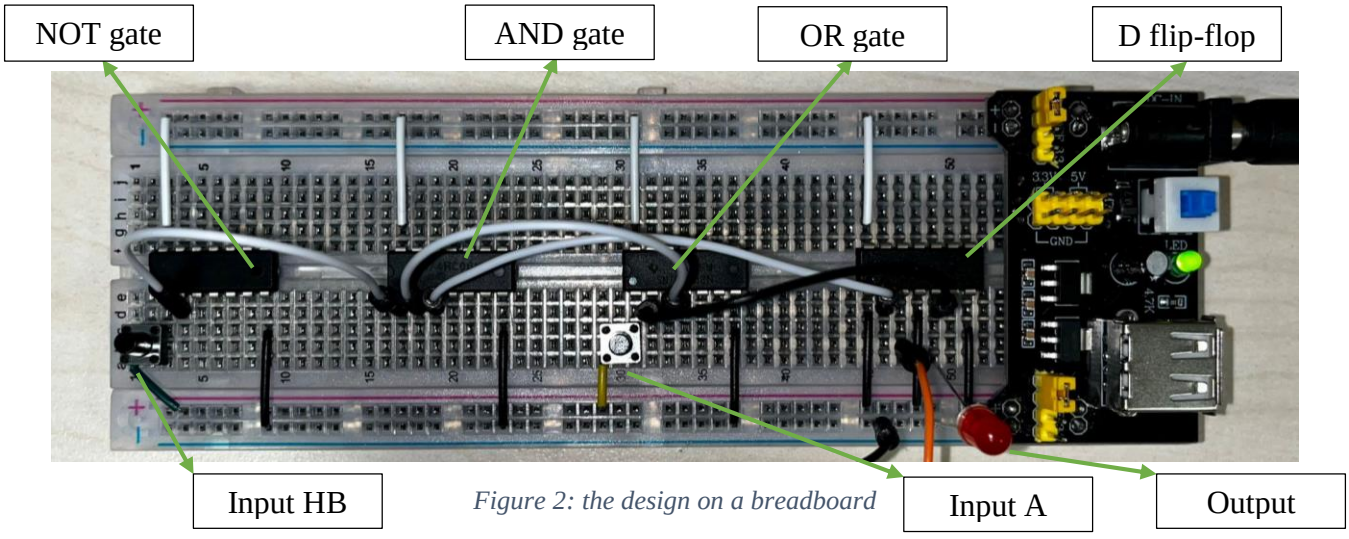

Figure 2: the design on a breadboard

In order to test whether it works correctly, some sample inputs were entered, and the output was created according to the Truth Table.

Sample 1:

State M = ‘0’

Input A = ‘0’

Input HB = ‘0’

State M* = ‘0’

Output = ‘0’

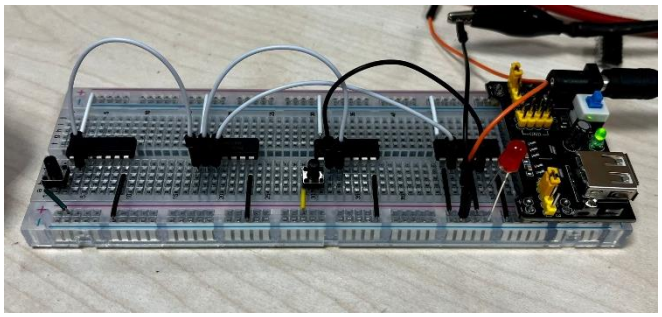

Figure 3: Sample 1 on breadboard

Sample 2:

State M = ‘0’

Input A = ‘1’

Input HB = ‘0’

State M* = ‘1’

Output = ‘1’

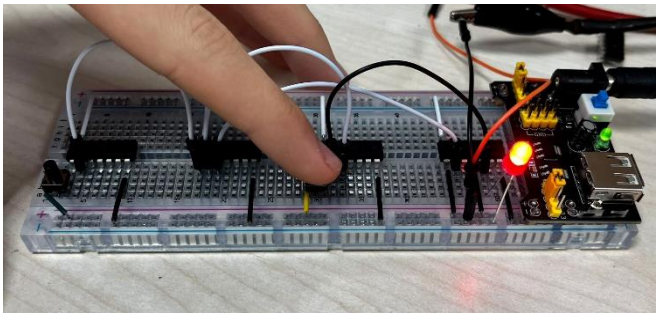

Figure 4: Sample 2 on breadboard

Sample 3:

State M = ‘1’

Input A = ‘0’

Input HB = ‘0’

State M* = ‘1’

Output = ‘1’

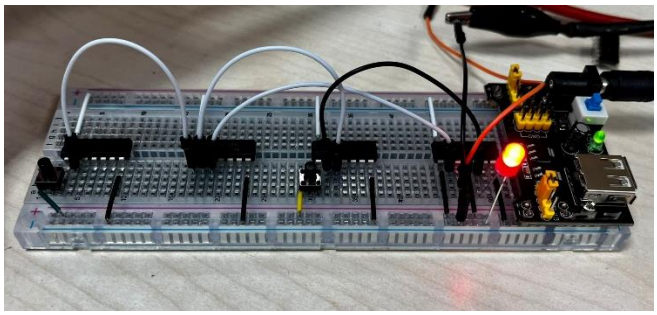

Figure 5: Sample 3 on breadboard

Sample 4:

State M = ‘1’

Input A = ‘0’

Input HB = ‘1’

State M* = ‘0’

Output = ‘0’

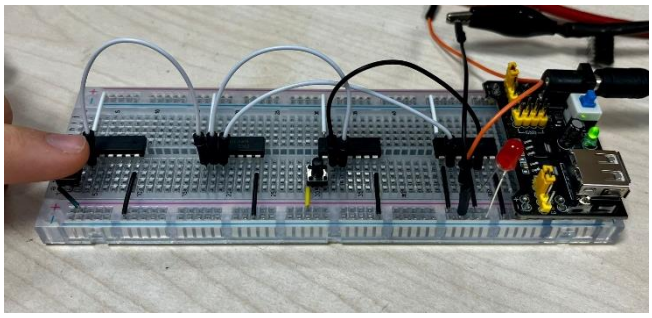

Figure 6: Sample 4 on breadboard

Conclusion:

This lab's objective was to construct an FSM (Finite State Machine) using a breadboard. The circuit was created step by step from simple to complex so that the problems that arose were immediately noticed and fixed. It was observed that the results of the implementation on the breadboard and the results of the Truth Table were compatible. During the construction of the created circuit, no errors were encountered except for human mistakes and non-contact problems. With this lab, with the understanding of the FSM design and logic, the application on the breadboard has been reinforced.