Bilkent University

EEE313 Lab 3 Report

nMOS Common Source Amplifier

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Introduction

This lab aims to characterize an nMOS transistor (2N7000) and then design a single-stage voltage amplifier using characterization results. In the figure below, V_{TH} value will be found using circuit a, and K_N and λ values will be found with circuit b. Afterward, appropriate component values for circuit c will be found, and gain calculation will be made.

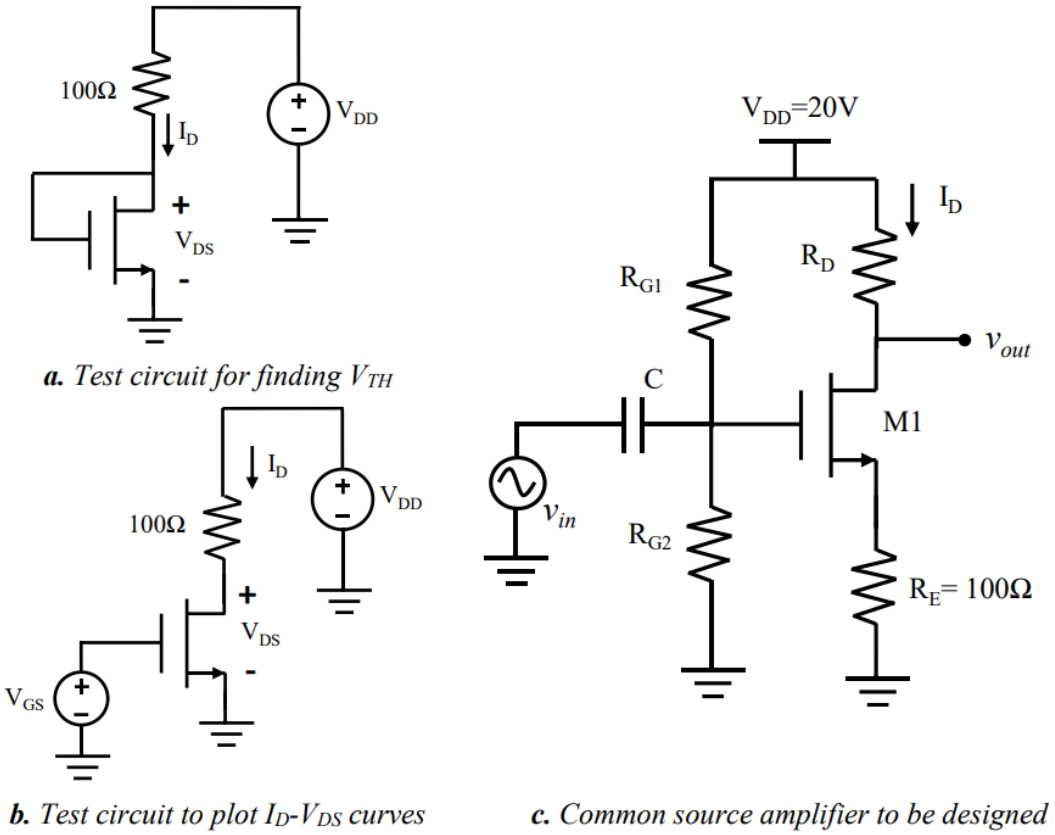

Figure 1: Test circuits and the common source amplifier

Hardware

a) Finding the V_{TH}

In this part, the circuit in figure 1.a was used to find the Vth value. It is assumed that when the current passing through the transistor is 1mA, the transistor is ON. Also, as is known, when the transistor gate-to-source voltage (V_{GS}) value is equal to the threshold voltage (V_{TH}) value, the transistor switches to the ON state. Since the gate and drain are connected to each other in this circuit, gate-to-source voltage (V_{GS}) is equal to drain-to-source voltage (V_{DS}). Additionally, the V_{DS} value can be calculated as follows:

$$V_{DS} = V_{DD} - I_D R_D$$

That is, when all these are used, when the I_D value reaches 1mA, the V_{DD} value will be used in the above equation to obtain the V_{DS}=V_{TH} value. The following plot was created with the values obtained when the V_{DD} value was increased so that the I_D value increased from 0 to 30 mA.

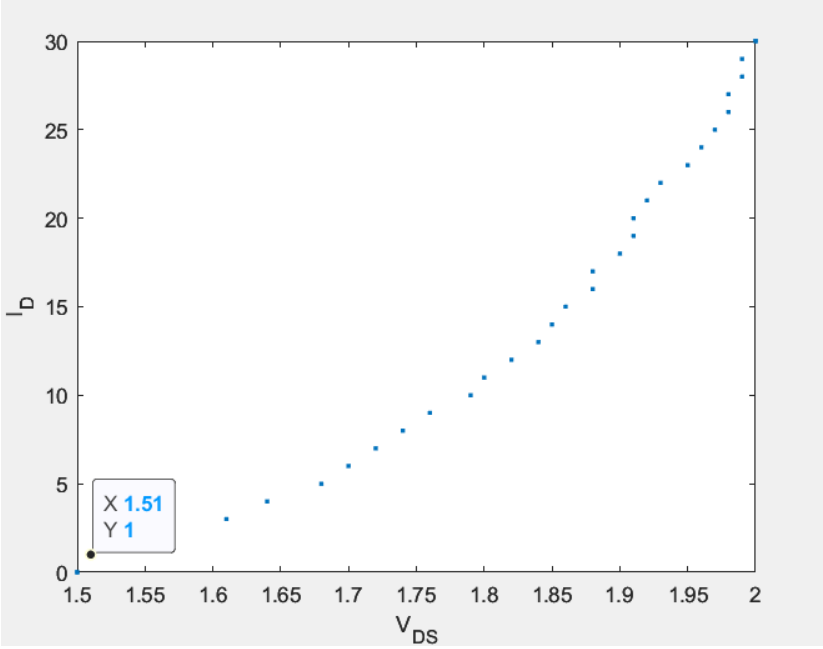

Figure 2: I_D vs V_{DS} plot

In this plot, the I_D value was obtained with a multimeter, and the V_{DS} value was obtained with the above equation with R_D = 100 Ohm. As can be seen at the point marked in the plot, when the I_D value is 1mA, the V_{DS} value is 1.51V; that is, at this value, the transistor switches to the ON state. Therefore, V_{TH} = 1.51V.

b) Finding the K_N and λ

In this part, using the circuit in figure 1.b, three I_D-V_{DS} graphs will be created for $V_{GS}=V_{TH}+0.3V$, 0.4V, and 0.5V. Then, K_N and λ values will be calculated. Since the V_{TH} value in the part is 1.51V, the V_{GS} values to be used are 1.81V, 1.91V, and 2.01V. The three I_D-V_{DS} plots obtained with these values are as follows:

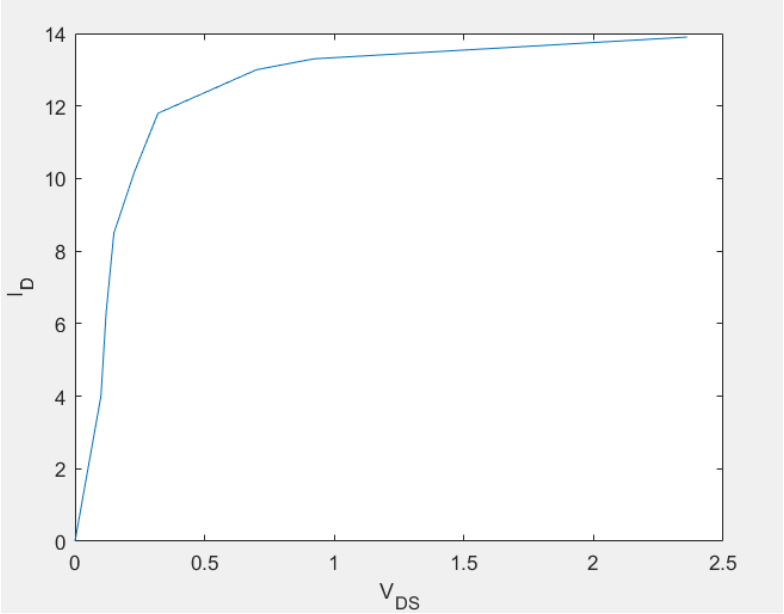

Figure 3: I_D vs V_{DS} plot for V_{GS} = 1.81V

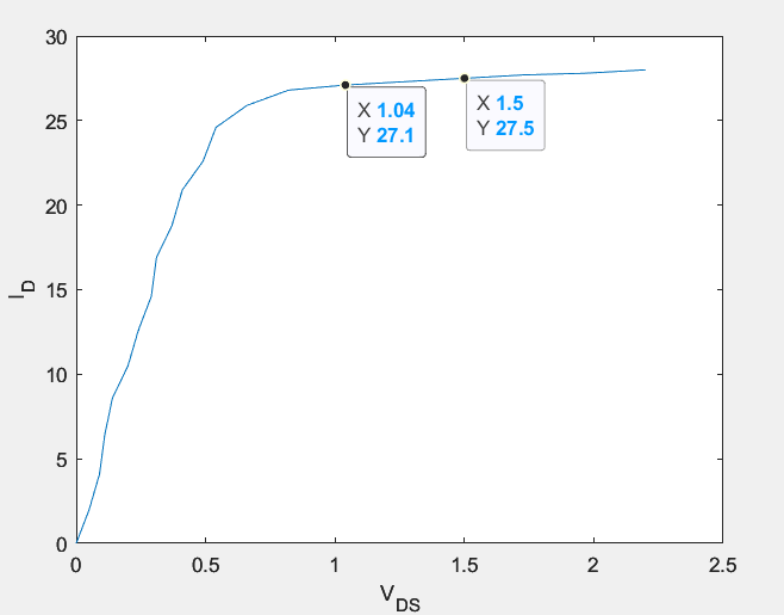

Figure 4: I_D vs V_{DS} plot for V_{GS} = 1.91V

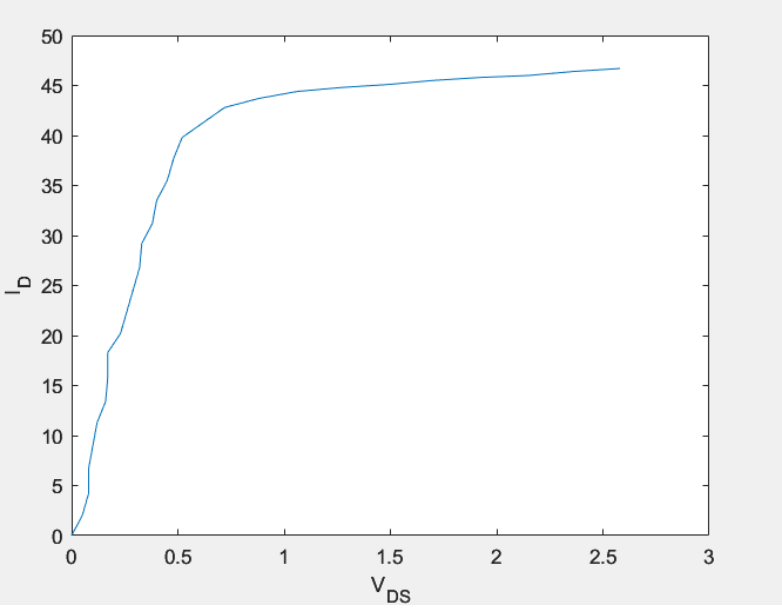

Figure 5: I_D vs V_{DS} plot for V_{GS} = 2.01V

Since $V_{DS(SAT)} = V_{GS} - V_{TH}$, it can be seen in these graphs that the $V_{DS(SAT)}$ values are approximately 0.3V, 0.4V, and 0.5V, respectively. The two values in figure 4 and the equation below were used to calculate K_N and λ.

$$I_D = K_N(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

Since the transistor is not ideal, even if it goes into SAT state, the I_D value is not fixed and continues to increase with a certain slope, so the ideal equation is multiplied by $(1 + \lambda V_{DS})$, and a more realistic equation is obtained. Values obtained after calculations:

$$\lambda = 0.033\ V^{-1}, K_N = 114.621\ mA/V^2$$

c) Finding the gain

In this part, the common source amplifier in figure 1.c will be designed, and gain will be calculated. The specifications given for this circuit are as follows:

$$R_{IN} > 30\ k\Omega$$

$$R_{OUT} < 2\ k\Omega$$

$$10\ mA < I_D < 15\ mA$$

$$|A_V| = |v_{out} / v_{in}| > 9\ when\ v_{in} = 100\ mV_{pp}\ sine\ wave\ @\ 10\ kHz$$

First, the current is selected as to be 11mA. This I_D value and the values in parts b and, g_m and r_0 values can be calculated as follows:

$$g_m = \sqrt{2 I_D K_N} = \sqrt{2 * 11 * 10^{-3} * 114.621 * 10^{-3}}$$

$$g_m = 50.216\, mA/V$$

$$r_0 = \frac{1}{\lambda I_D} = \frac{1}{0.033 * 11 * 10^{-3}}$$

$$r_0 = 2730.003\, \Omega$$

Determining and checking the required component values is as follows:

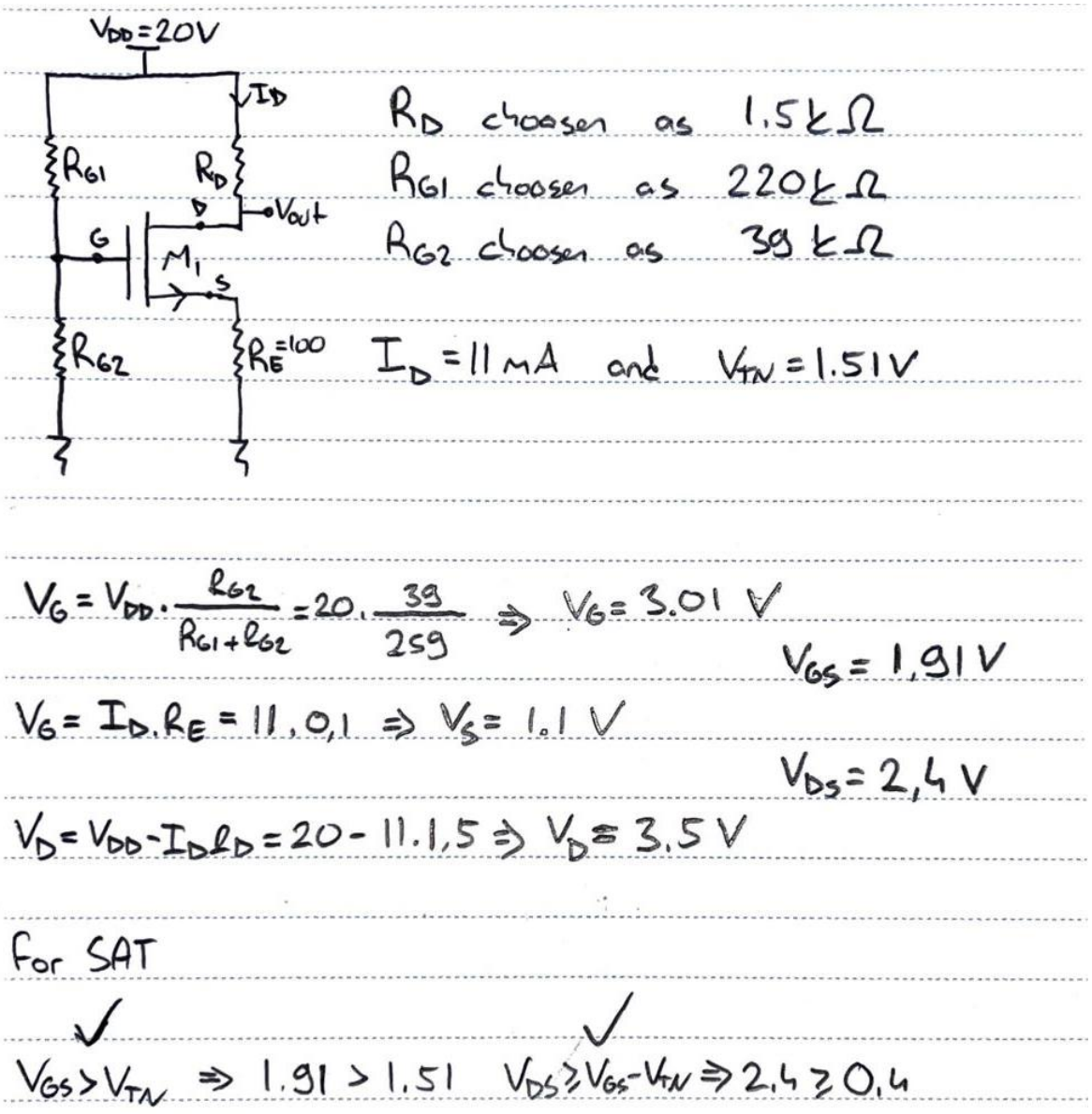

Figure 6: Calculation for component values

A small signal analysis of the circuit is as follows:

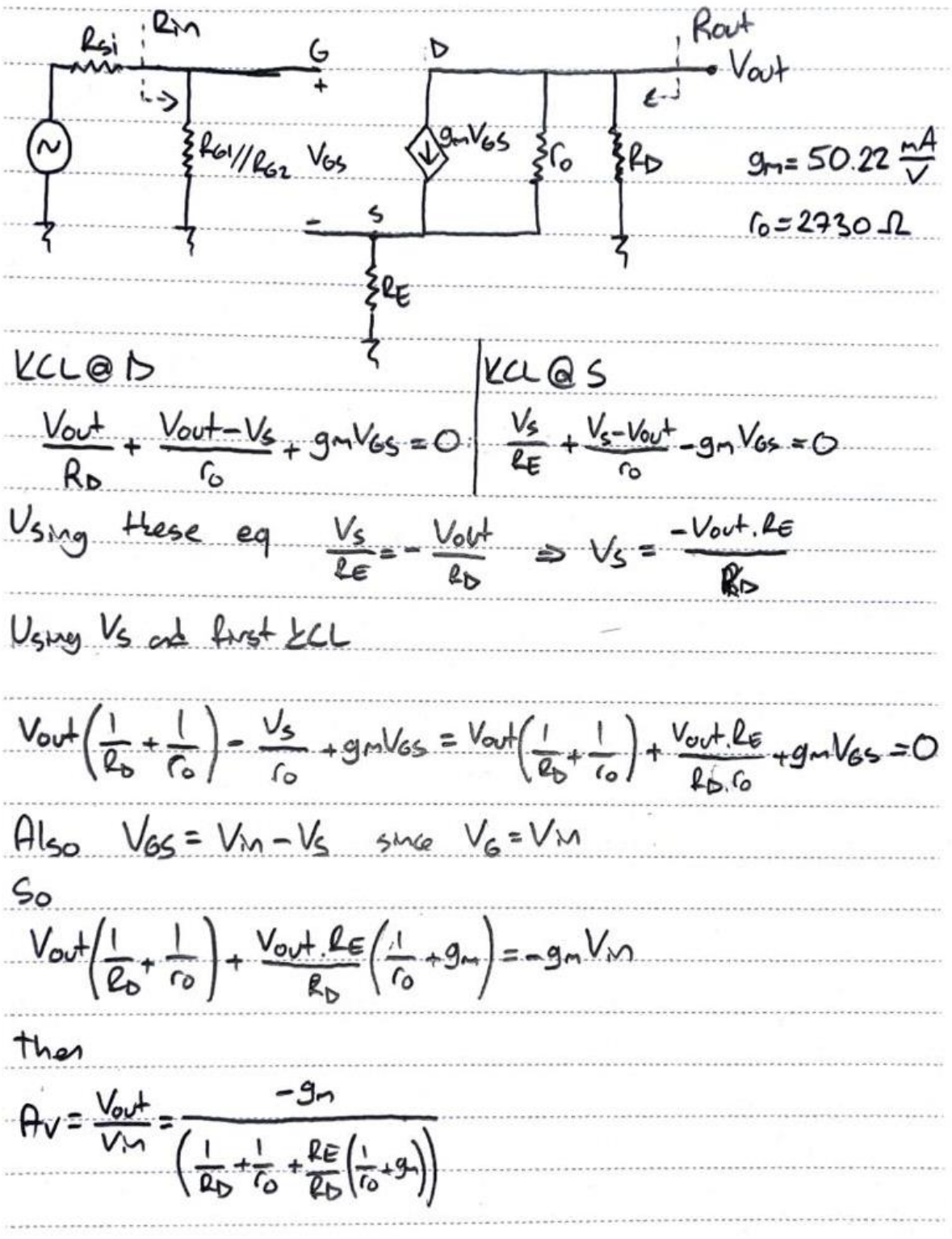

Figure 7: Small signal gain calculation

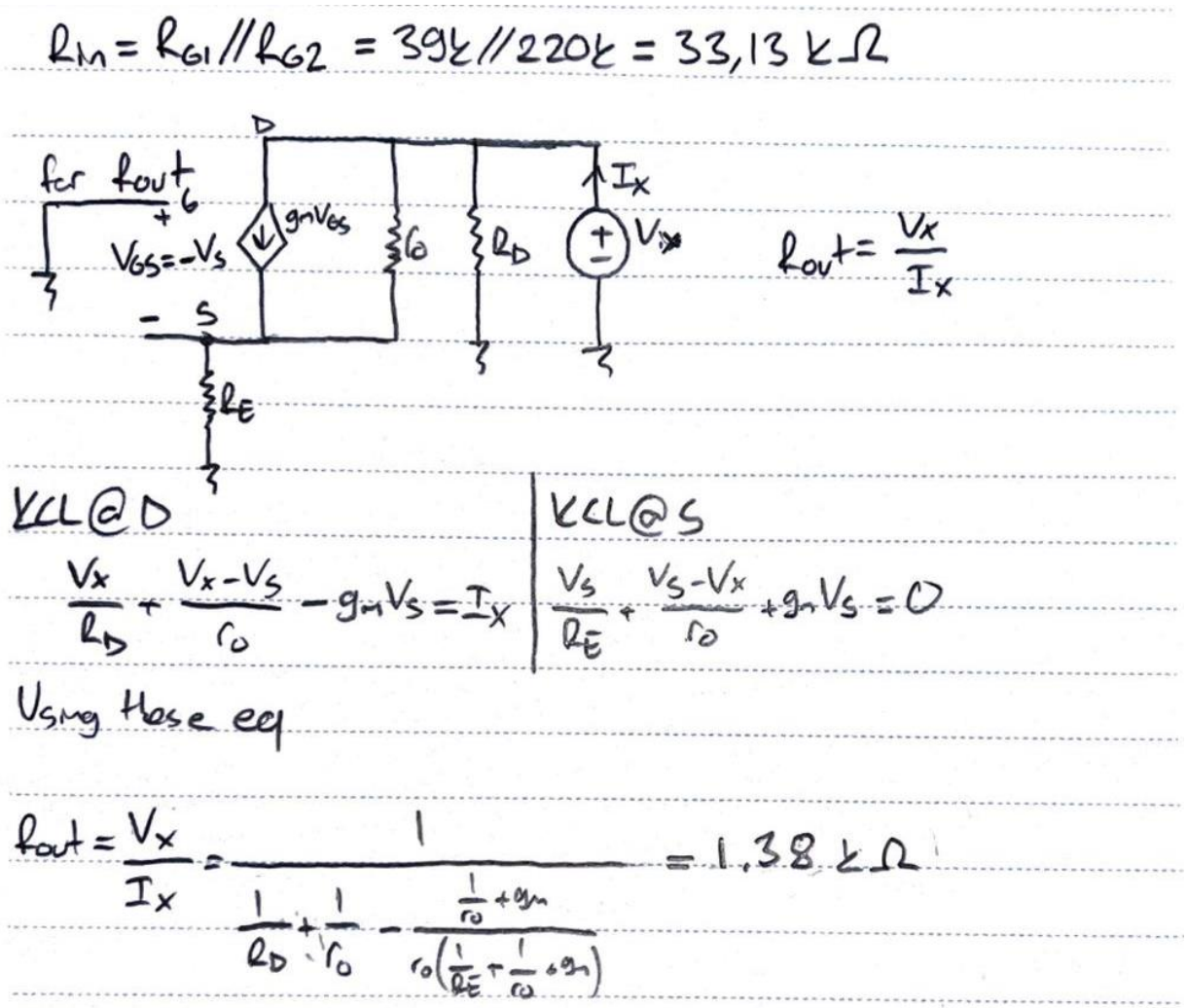

Figure 8: Calculation for R_{out} and R_{in}

Checking the specifications:

$$|A_v| = \frac{50.22}{\frac{1}{1.5} + \frac{1}{2.73} + \frac{0.1}{1.5}\left(\frac{1}{2.73} + 50.22\right)} = 11.39 > 9$$

$$R_{IN} = 33.13\ k\Omega > 30\ k\Omega$$

$$R_{OUT} = 1.38\ k\Omega < 2\ k\Omega$$

$$10\ mA < I_D = 11\ mA < 15\ mA$$

It is seen that the calculated values meet the specifications.

The circuit created with the obtained values is as follows:

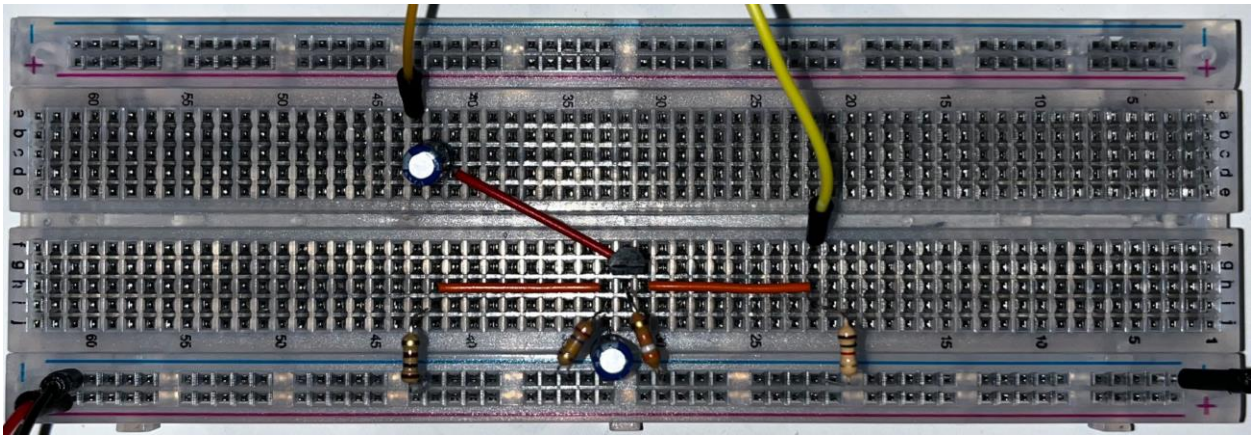

Figure 9: The Common Source Amplifier Circuit

For this part, measurements were made without the capacitor at the bottom in figure 9. The coupling capacitor chosen as 10 µF acts as a short circuit for AC and an open circuit for DC, so separate them. The following result was obtained when the input and output values were measured with an oscilloscope.

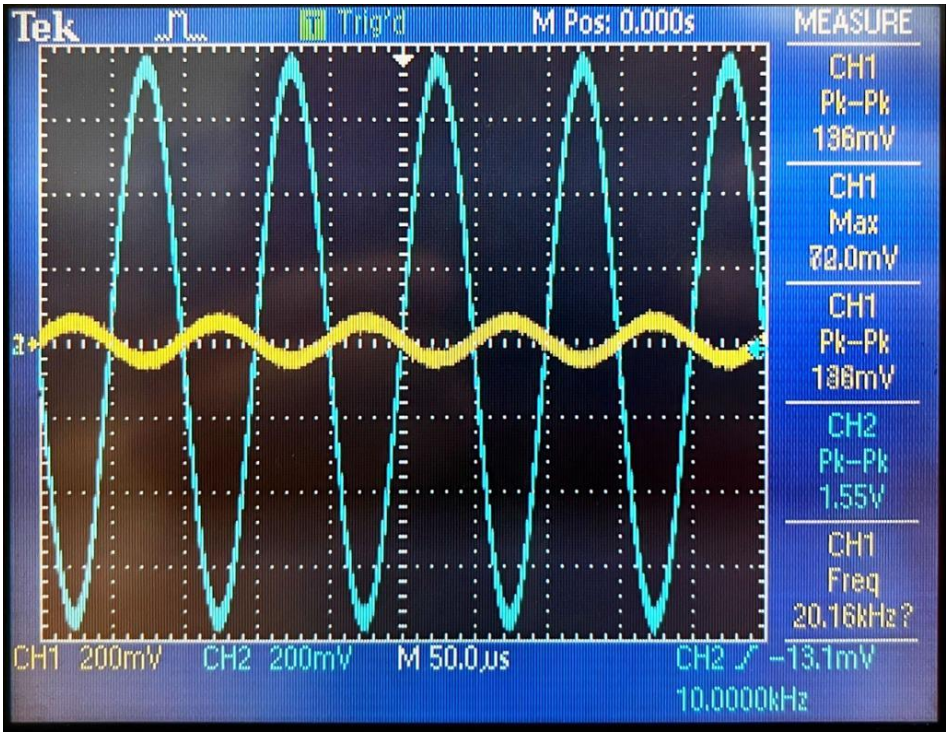

Figure 10: Output(CH2) and Input(CH1) values for part c

When experimental gain is calculated with these values:

$$|A_v| = \frac{V_{out}}{V_{in}} = \frac{1.55}{0.136} = 11.40 > 9$$

Additionally, the following result was obtained when measured with a voltmeter over RD.

Figure 11: Voltage on R_D

When this voltage value is divided by the R_D value, I_D is obtained as follows:

$$10\ mA < I_D = \frac{16.19}{1.5} = 10.79\ mA < 15\ mA$$

The following result was obtained when the input was increased to observe the distortion effect.

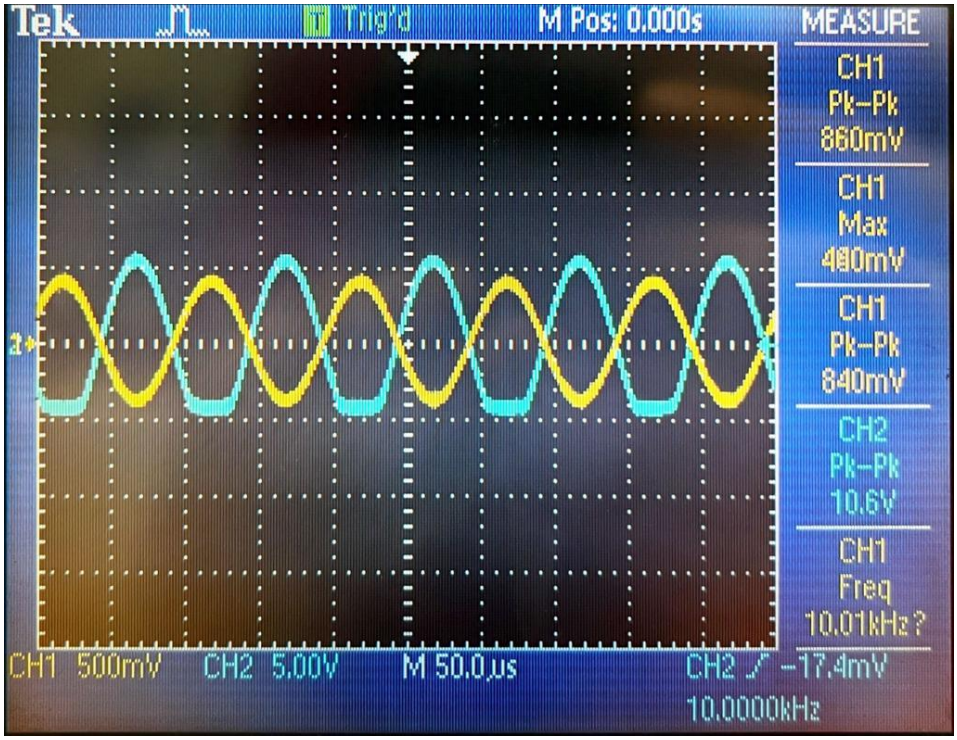

Figure 12: The Distortion Effect

Looking at the plot above, it is observed that when the input is read as 860 mV, the output now looks like a cut-off sine wave, that is, it exceeds the saturation limit and linear region.

d) Finding the gain with the Capacitor

In this part, measurements were repeated with the 10 µF capacitor at the bottom in figure 9. The following result was obtained when the input and output values were measured with an oscilloscope.

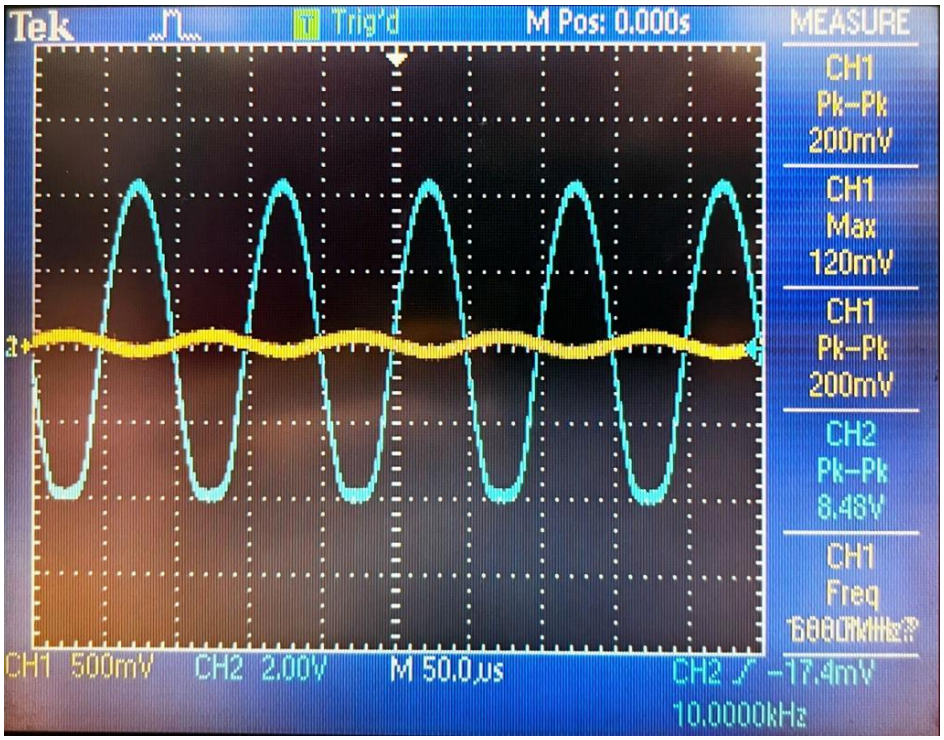

Figure 13: Output(CH2) and Input(CH1) values for part d

In this case, when the experimental gain is calculated:

$$|A_v| = \frac{V_{out}}{V_{in}} = \frac{8.48}{0.2} = 42.2$$

The reason for this change is that the capacitor added in parallel to R_E short circuits the R_E resistor. That is, R_E = 0 Ω, and the theoretical gain calculation in figure 7 can be rewritten as follows:

$$|A_v| = \frac{g_m}{\frac{1}{R_D} + \frac{1}{r_0}} = \frac{50.22}{\frac{1}{1.5} + \frac{1}{2.73}} = 48.62$$

As expected, since R_E was set equal to zero, the value in the denominator decreased, so the gain increased.

Conclusion

The purpose of this lab was to design a common source amplifier. First, the transistor was characterized, and V_{TH} K_N and λ values were obtained. Afterward, DC analysis of the common source amplifier circuit was performed using these values. Thanks to DC analysis, I_D, R_{G1}, $R_{G2,}$ and R_D values that would meet the desired specifications were determined. Afterwards, g_m and r_0 values were calculated with these values. Then, with a small signal analysis, the theoretical gain calculation was made using all these values. The hardware part was started after verifying that the theoretical gain, R_{out}, and R_{in} values were within the desired limitation. While the designed circuit was implemented, the coupling capacitor was selected as 10 µF, and the gain was calculated using an oscilloscope. Then, the input value was increased to observe the distortion effect, and the amplifier was observed to exceed the saturation limit and linear region. Finally, it was observed that the gain increased thanks to the bypass capacitor connected in parallel to the R_E resistor. Afterward, this increase was explained by the decrease in the denominator in the gain equation due to $R_E = 0\ \Omega$.

There were no significant difficulties during the lab. Some minor errors occurred due to the non-ideal MOSFET, imprecise component values, and the material quality or sensitivity of the oscilloscope, signal generator, multimeter, and breadboard. Thanks to this lab, the working logic of MOSFETs was better understood, and the steps in common source amplifier design were learned.

Appendix

```
I_D  = [0:30];
V_DD = [1.50, 1.61, 1.76, 1.91, 2.04, 2.18, 2.30, 2.42, 2.54, 2.66, 2.79, 2.90, 3.02,
3.14, 3.25, 3.36, 3.48, 3.58, 3.70, 3.81, 3.91, 4.02, 4.13, 4.25, 4.36, 4.47, 4.58,
4.68, 4.79, 4.89, 5.00];
V_DS = V_DD - I_D/10;
V_TH = 1.51;

plot(V_DS, I_D, '.')
xlabel('V_D_S')
ylabel('I_D')
%% 0.3-->1.81V
V_DD = [0:0.25:3.75];
I_D  = [0, 2 ,4 ,6.3 ,8.5 ,10.2 ,11.8 ,12.4 ,13.0 ,13.3 ,13.4 ,13.5 ,13.6 ,13.7 ,13.8
,13.9];
V_DS = V_DD - I_D/10;
V_TH = 1.51;

plot(V_DS, I_D)
xlabel('V_D_S')
ylabel('I_D')
%% 0.4-->1.91V
V_DD = [0:0.25:5];
I_D  = [0, 2, 4.1, 6.4, 8.6, 10.5, 12.6, 14.6, 16.9, 18.8, 20.9, 22.6, 24.6, 25.9,
26.8, 27.1, 27.3, 27.5, 27.7, 27.8, 28];
V_DS = V_DD - I_D/10;
V_TH = 1.51;

plot(V_DS, I_D)
xlabel('V_D_S')
ylabel('I_D')
%% 0.5-->2.01V
V_DD = [0:0.25:7.25];
I_D  = [0, 2, 4.2, 6.7, 9, 11.3, 13.4, 15.8, 18.3, 20.2, 22.4, 24.6, 26.8, 29.2,
31.2, 33.5, 35.5, 37.7, 39.8, 41.3, 42.8, 43.7, 44.4, 44.8, 45.1, 45.5, 45.8, 46,
46.4, 46.7];
V_DS = V_DD - I_D/10;
V_TH = 1.51;

plot(V_DS, I_D)
xlabel('V_D_S')
ylabel('I_D')
```