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双葉電子工業株式会社
電子部品事業部
ELECTRONIC COMPONENTS DIVISION
FUTABA CORP.

蛍光表示管規格書
Vacuum Fluorescent Display Specification

Attention PACE

発行月日
The date of issue 2009 . 6 . 3

部品番号
Part No.

双葉電子形名
FUTABA Type No. 16-BD-08GINK

改定記号
Revision Letter A

主旨 (Purpose):
~~新規 (Newly issued)~~
変更 (Revised)

1.Pin connection was changed. (#5～#13, NC → NX)
2.Lead bend was changed. (4.0mm → 5.2mm)
3.Lead edge position was changed. (5.0mm → 4.0mm)

受領印 Signature

記事 Note. 御参考までに、フレーム周波数又はディミング周波数がお決まりでしたら、お知らせ下さい。
For the reference, please note your intended frame frequency or dimming frequency if applicable.

注意事項
NOTE

1. 蛍光表示管(VFD)は下記物質を含有しています。蛍光表示管を破棄する場合は、法律に従い処理をして下さい。
1. Since Vacuum Fluorescent Display (VFD) contents the following environmental control materials, proper disposition complying with regulation is required for its waste.

1-1 硫化ｶﾄﾞﾐｳﾑ
本品種にはカドミウムは一切含まれておりません。
1-1 Cadmium Sulfide
Cadmium Sulfide is not contained in this product.

1-2 ﾊﾞﾘｳﾑ、銀、ｺﾊﾞﾙﾄ
ﾊﾞﾘｳﾑはｹﾞｯﾀｰ及びﾌｨﾗﾒﾝﾄに、ｺﾊﾞﾙﾄは封着ｶﾞﾗｽに、銀は半田及び導電材として、それぞれ微量含有しています。
1-2 Barium, Silver, Cobalt
The Getter and Filament material contain Barium, and Cobalt is contained in frit glass, Silver is used as wiring pattern material and solder.

1-3 鉛
封着ｶﾞﾗｽ及び絶縁ｶﾞﾗｽは鉛系のｶﾞﾗｽが主成分です。
1-3 Lead
Frit glass and isolation paste are the Lead base glass.

2. VFDの外囲器はｿｰﾀﾞﾗｲﾑｶﾞﾗｽで構成され、真空気密が保たれています。従いまして、強い衝撃を与えると破損し、ｶﾞﾗｽが飛び散る事が有りますのでVFDには衝撃を与えないようにして下さい。外周部は鋭くなっていますので、素手で取り扱うとｹｶﾞをする事が有ります。よって手袋、保護ﾒｶﾞﾈ等を着用し、取り扱いを行って下さい。
2. Since the envelope of VFD is fabricated by soda-lime glass to keep vacuum condition , excessive mechanical shock may cause crash of the glass envelop and splash of the glass chip. The edge of the glass package is sharp and can cause injury. Therefore protective glasses and gloves should be used for proper handling of VFD.

3. VFDの構成部品及び製造工程において本スペックの発行時点において規制されている一切のｵｿﾞﾝ層破壊物質、臭素系難燃剤及び水銀は使用しておりません。
3. VFD manufacturing process of articles or parts do not use any ODC(Ozon Depleting Chemicals) or regulated Brominated flame retardant materials or Mercury , that are regulated on this specification issue date.

※ 蛍光表示管規格書(2)枚をお送り致しますので御査収後、御返却下さいます様お願い致します。
After reviewing this material , please send back this cover page with your signature.

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Futaba

A

蛍光表示管製品規格
VACUUM FLUORESCENT DISPLAY SPECIFICATION

双葉電子工業株式会社
電子部品事業部　電子管技術グループ
ENGINEERING GROUP, ELECTRON TUBE
ELECTRONIC COMPONENTS DIVISION
FUTABA CORPORATION

形名 Type No.　16-BD-08GINK

用　途 :Application　STB
外形寸法 :Outer Dimension　110.2 (L) × 18.5 (W) × 6.6 (T) mm
Cadmium Free Phosphor, Lead Free Solder

発 光 色 :Color of Illumination Green (G. x=0.24,y=0.41)

絶対最大定格:Absolute Maximum Rating

項　目　:　Item		Symbol	Terminals	Rating	Unit
フィラメント電圧 :Filament Voltage	*1	Ef	F1-F2	4.9	Vac
ロジック電源電圧 :Logic Supply Voltage	*3	V_{DD}	V_{DD}	−0.3 ～ 6.5	Vdc
ドライバ電源電圧 : Driver Supply Voltage	*4	V_{FL}	V_{FL}	−35 ～ V_{DD}+0.3	Vdc
ロジック信号入力電圧 :Logic Input Voltage		V_{IN}	$\overline{CS}$,CP,DA,$\overline{RESET}$	−0.3 ～ V_{DD}+0.3	Vdc
保存温度 :Storage Temperature		T_{stg}	—	−55 ～ +85	℃

絶対最大定格:瞬時たりとも超えてはならない規格であり、此れを超えた場合恒久的な機能障害を発生する可能性があります。
Absolute Maximum Condition : The value shall not be exceeded in any conditions. Permanent damage to VFD may be expected.

推奨動作条件:Recommended Operating Condition

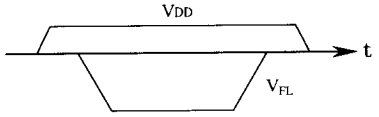
項　目　:　Item		Symbol	Min.	Typ.	Max.	Unit
フィラメント電圧 :Filament Voltage	*1	Ef	3.69	4.1	4.51	Vac
ドライバ電源電圧 : Driver Supply Voltage	*4	V_{FL}	−27	−30	−33	Vdc
ロジック電源電圧 :Logic Supply Voltage	*3	V_{DD}	3.0	3.3	3.6	Vdc
Hレベル入力電圧 :H-Level Input Voltage		V_{IH}	V_{DD}×0.8	—	-	Vdc
Lレベル入力電圧 :L-Level Input Voltage		V_{IL}	-	—	V_{DD}×0.2	Vdc
カットオフバイアス :Cut-off Bias	*2	Ek	5.9	—	-	Vdc
動作温度 :Operating Temperature		T_{opr}	−20	—	+70	℃

内部クロック動作特性:Characteristics of Internal Clock Circuit (条件: Condition R1 = 3.3kΩ、C1 = 39pF)

項　目　:　Item	Symbol	Min.	Typ.	Max.	Unit
発振周波数 :Oscillator Frequency	f_{OSC}	1.5	2.0	2.5	MHz
表示フレーム周波数 :Display Frame Frequency	f_{FR}	183	244	305	Hz

推奨動作条件:信頼性、品質を確保できうる範囲(寿命はTyp.値が最適値です。)
Recommended Operating Condition:Quality and reliability can be assured in this condition.
(Typ.condition is the most optimized value on the life time.)

*1 AC50、60Hzまたは30kHz以上の実効値。50Hz,60Hz or > 30kHz r.m.s.
*2 フィラメントトランスのセンタータップに印加する。Ek is applied to the center tap of the filament transformer.
*3 電源シーケンス　Power Supply Sequence
VFLを印加中はVDDを3.0～3.6Vの間でご使用下さい。
V_{DD} should be 3.0 to 3.6V when applying VFL.
電源投入時はV_{DD}とVFLを同時、またはVDDを投入した後にV_{FL}を投入下さい。
VFL and V_{DD} should be on at the same,or VFL should be on after V_{DD} is on.
電源遮断時はV_{DD}とVFLを同時、またはV_{FL}を遮断した後にV_{DD}を遮断下さい。
VFL and V_{DD} should be off at the same,or V_{DD} should be off after VFL is off.



電源シーケンス
Power Supply Sequence

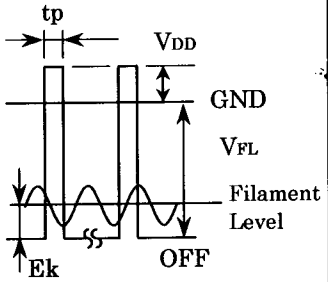
*4 VFLを印加中は推奨動作条件でご使用下さい。Recommended Operating Condition should be used when applying VFL.

本製品は半導体製品ですので静電気のお取り扱いには十分ご注意お願いします。
The VFD is built with C-MOS Ics.Precautions should be taken to minimize the possibility of static charges.
本規格と異なる使い方をされる場合、品質,信頼性を確保出来ない場合がありますので事前にご相談下さい。
Since deviation from this specification may generate quality or reliability concerns, please consult to FUTABA prior to use.
この仕様書の内容はお断りなく変更することがありますのでご了承下さい。
This specification is subject to change without notice.

電気的特性:Electrical Characteristics

指定がない場合は、推奨動作条例のTyp値、全点灯、f_C=1.0MHz、PGND=LGND=0Vとする。

Unless otherwise specified, The test condition should be Typ value of recommended condition and all segments on, f_C=1.0MHz,PGND=LGND=0V.

項目 : Item	Test Condition	Symbol	Min.	Typ.	Max.	Unit.
フィラメント電流 Filament Current	Ef = 4.1 Vac VFL=VDD=0V	If	113	125	138	mAac
ロジック電源電流 Logic Supply Current	全点灯 All Segments on	IDD	—	-	5.0	mA
ドライバ電源電流 Driver Supply Current	全点灯 All Segments on	IEE(AVG)	—	| 7 |	| 14 |	mA
	全点灯 All Segments on	IEE(PEAK) T1、T16	—	| 7 |	| 14 |	mA
Hレベル入力電流 H-Level Input Current	VIN=VDD $\overline{CS}$,CP,DA $\overline{RESET}$	IIH	-1.0	—	1.0	μA
Lレベル入力電流 L-Level Input Current	VIN=0V $\overline{CS}$,CP,DA $\overline{RESET}$	IIL	-1.0	—	1.0	μA
輝 度 Luminance	Ef = 4.1 Vac VDD = 3.3 Vdc f_{OSC} = 2.0 MHz V_{FL} = -30.0 Vdc Ek = 5.9 Vdc (Grid Duty=1/17.1) tp = 240 μs tb = 16 μs  	L(G.)	350 (102)	700 (204)	—	cd/m^2 (ft-L)
		L( )			—	cd/m^2
		L( )			—	cd/m^2
		L( )			—	cd/m^2
		L( )			—	cd/m^2
		L( )			—	cd/m^2
		L( )			—	cd/m^2
		L( )			—	cd/m^2
輝度比 Luminance Ratio between Digits		$\frac{Lmax}{Lmin}$	—	—	2	

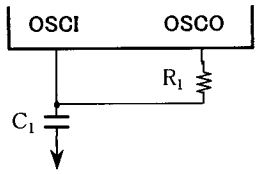
形名 Type No. 16-BD-08GINK

●機能表:Function Table

機能 Function	記号 Symbol	入力／出力 Input／Output	内容 Description
シフトクロック入力端子 Shift Clock Input	CP	入力 Input	CPの立ち上がりでシリアルデータがシフトします。 Serial data is shifted on the rising edge of CP
シリアルデータ入力 Serial Data Input	DA	入力 Input	LSB側より入力します。 Input from LSB.
チップセレクト入力端子 Chip Select Input	$\overline{CS}$	入力 Input	$\overline{CS}$をハイレベルにするとデータのシリアル転送が禁止されます。 Serial data transfer is disabled when CS pin is "H" level.
リセット入力端子 Reset Input	$\overline{RESET}$	入力 Input	$\overline{RESET}$をローレベルにすると全ての機能を初期化します。 "Low" initializes all the functions. Initial status is as follows. . Address of each RAM . . . . . Address "00"H . Data of each RAM . . . . . Content is undefined. . Display digit . . . . . 16 digits . Contrast adjustment . . . . . 8/16 . All lights ON or OFF . . . . . OFF mode . All outputs . . . . . "LOW" level
発振用入力端子 Input for oscillation.	OSCI	入力 Input	発振用入力端子です。 Input Pin for oscillation.
発振用出力端子 Output for oscillation.	OSCO	出力 Output	発振用出力端子です。 Output Pin for oscillation.
ロジック電源端子 Logic Supply Pin	VDD	入力 Output	ロジック回路のための電源端子 Power Supply pin for Logic Circuit
ロジックグランド端子 Logic GND Pin	GND	入力 Input	ロジックのグランド GND for Logic Circuit
ドライバ電源端子 Driver Supply Pin	V_{FL}	入力 Input	蛍光表示管駆動のための電源端子 Vacuum Fluorescent Display driving voltage pin
フィラメント端子 Filament Pin	F1,F2	入力 Input	フィラメント電圧入力端子 Filament Voltage input
ノーピン No Pin	NP	—	NP部にはピンはありません。 There is no pin.
ノーエクステンド No Extend Pin	NX	—	ノーコネクションのピンです。 There is no connection.

Oscillation Circuit

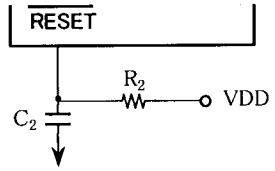
An oscillation circuit may be constructed by connecting extemal Resistor (R1) and Capacitor (C1) between the oscillator pins -- OSCI and OSCO. The RC time constant depends on the value of VDD voltage used.
The target oscillation frequency is 2MHz. Please refer to the diagram below.



Power Supply Voltage	R1	C1
VDD = 3.3Vdc	3.3KΩ	39pF

Reset Circuit

For reset control, both input reset signal from microcontroller and extemal RC circuit can be available.
In case of power-on- reset circuit, resistor and capacitor are connected externally for resetting CIG.

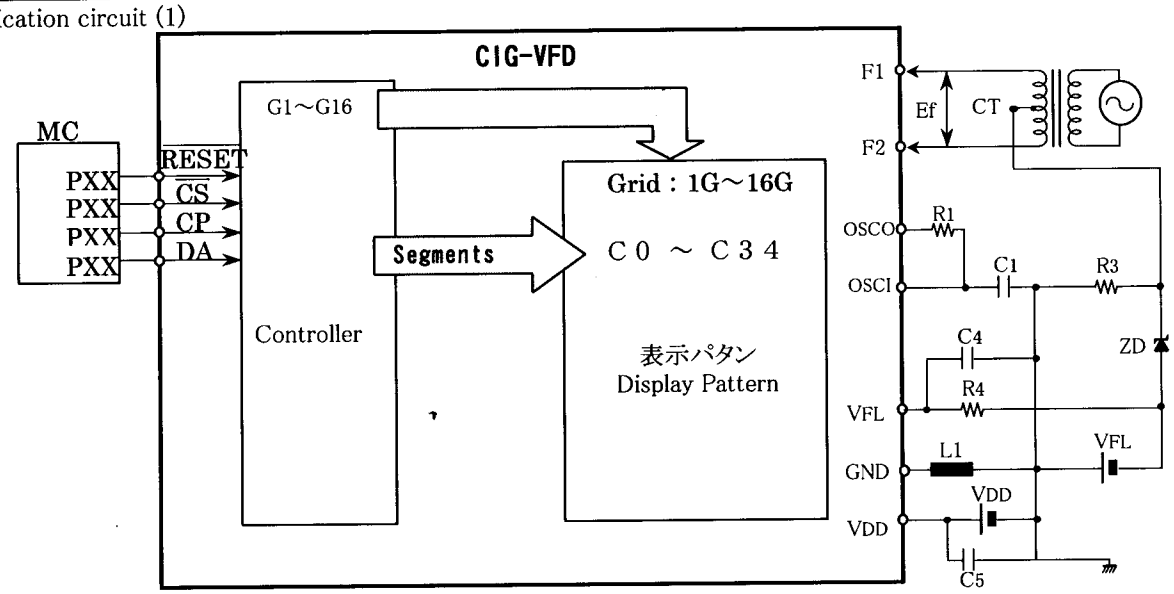


Power Supply Voltage	R2	C2
VDD = 3.3Vdc	1.0KΩ	0.1μF

形名 Type No. 16-BD-08GINK

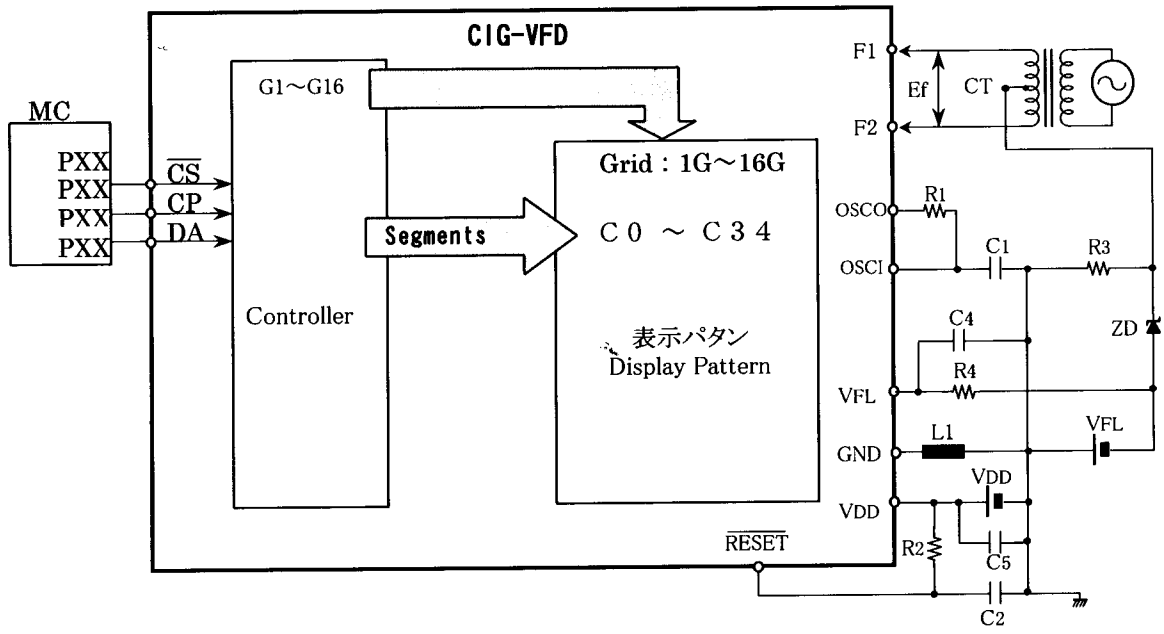
接続回路(例1)

Application circuit (1)



接続回路(例2)

Application circuit (2)



注1)本製品はICを含むデバイスです。ICの破壊モード(ショートモード)に対応する回路設計を推奨します。

Note1)This product is the device with built－in IC. The design of the PWB should be considered for the destructive mode (short mode) of IC.

Note2)Passive components relating oscillation and reset are required to be located as close as possible to VFD.

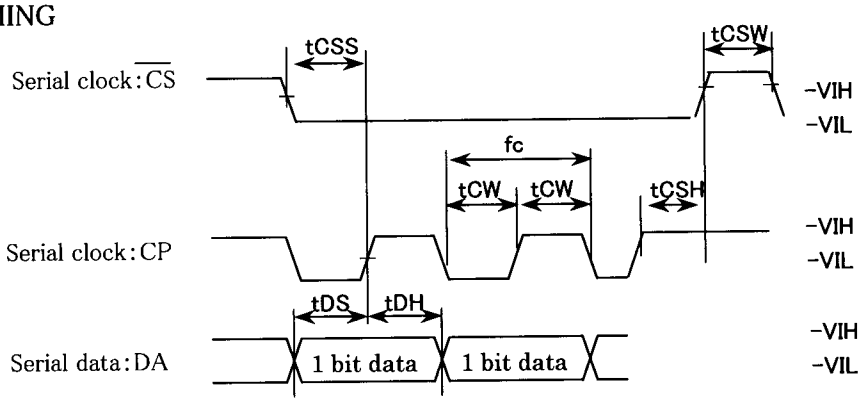
- ●R4: Current Limiting Resistor (470Ω)
- ●L1: Bead (Inductor) for improving ESD . . . CIC21J601NE (Maker :SEM) equivalent
- ●C4: Bypass Capacitor for High Voltage (0.1μF ,60V)
- ●C5: Bypass Capacitor for Logic Voltage (0.1μF)

形名 Type No. 16-BD-08GINK

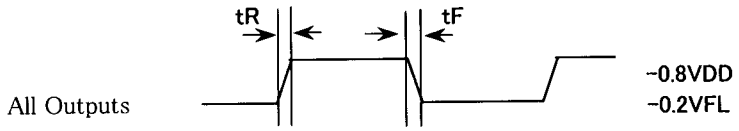
● Timing condition

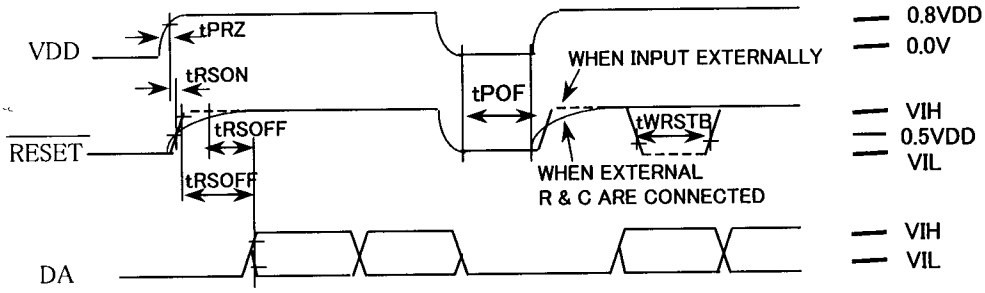
The timing condition for serial transfer is shown below.

. Data TIMING



. Output Timing





Timing Characteristics

Parameter	Symbol	VDD = 3.3 ± 10%
High Level Input Voltage	VIH	0.8 VDD
Low Level Input Voltage	VIL	0.2 VDD

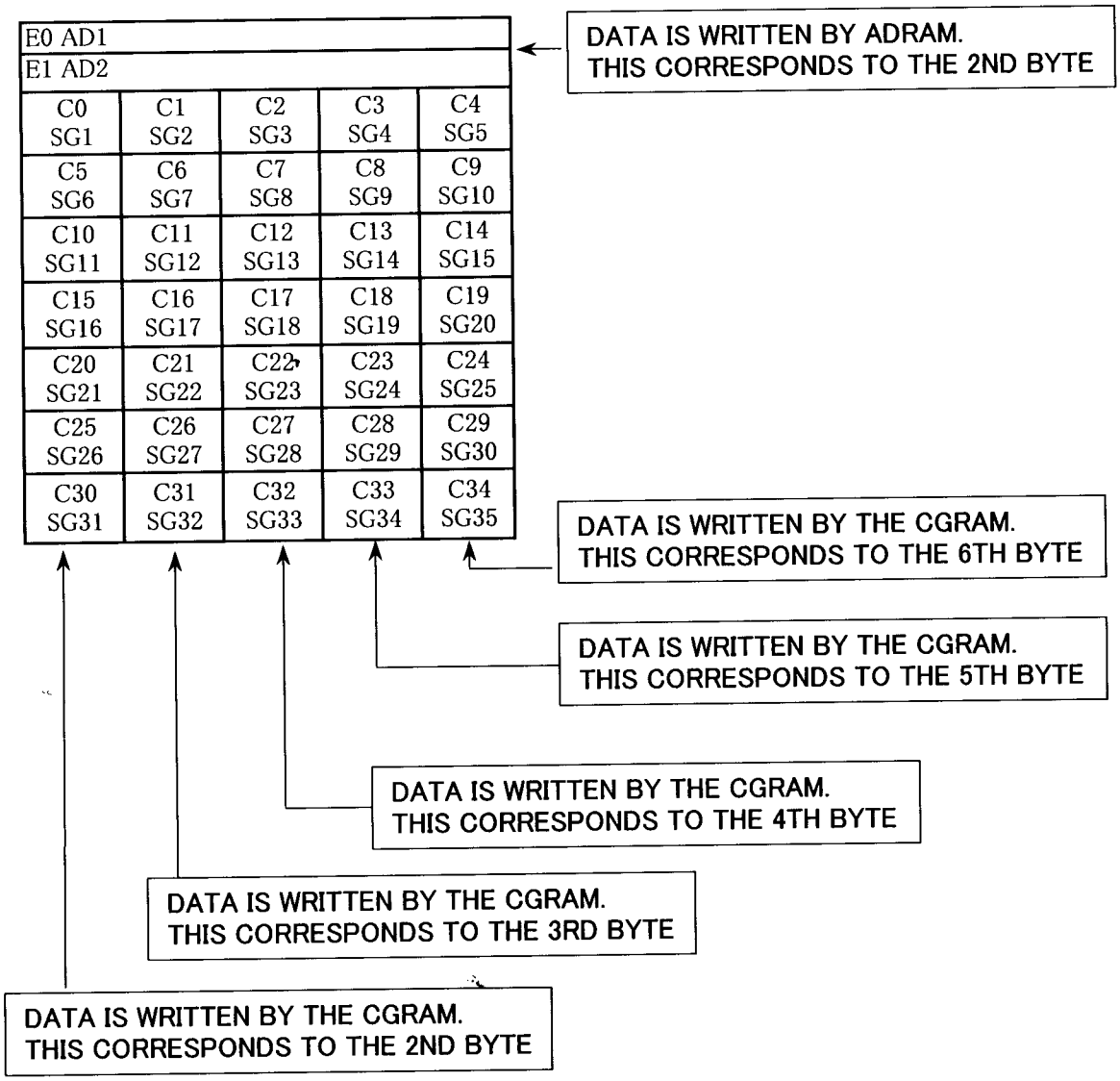
Timing Condition

Item	Symbol	Condition	Min	Max	Unit
CP Cycle Time	fc	-	-	1.0	MHz
CP Pulse Width	t_{CW}	-	300	-	ns
DA Setup Time	t_{DS}	-	300	-	ns
DA Hold Time	t_{DH}	-	300	-	ns
$\overline{CS}$ Setup Time	t_{CSS}	-	300	-	ns
$\overline{CS}$ Hold Time	t_{CSH}	R1 = 3.3kΩ,C1 = 39pF	16	-	μs
$\overline{CS}$ Wait Time	t_{CSW}	-	300	-	ns
Data Processing Time	t_{DOFF}	R1 = 3.3kΩ,C1 = 39pF	8	-	μs
$\overline{RESET}$ Pulse Width	t_{WRSTB}	When $\overline{RESET}$ Signal is input from microcontroller etc. extemally	300	-	ns
DA Wait Time	t_{RSOFF}	-	300	-	ns
All Output Slew Rate	t_R	Cl=100pF,tR=20% to 80%	-	4.0	μs
	t_F	Cl=100pF,tF=80% to 20%	-	4.0	μs
VDD Rise Time	t_{PRZ}	Mounted in the Unit	-	100	μs
VDD Off Time	t_{POF}	VDD=0V, Mounted in the Unit	5.0	-	ms

形名 Type No. 16-BD-08GINK

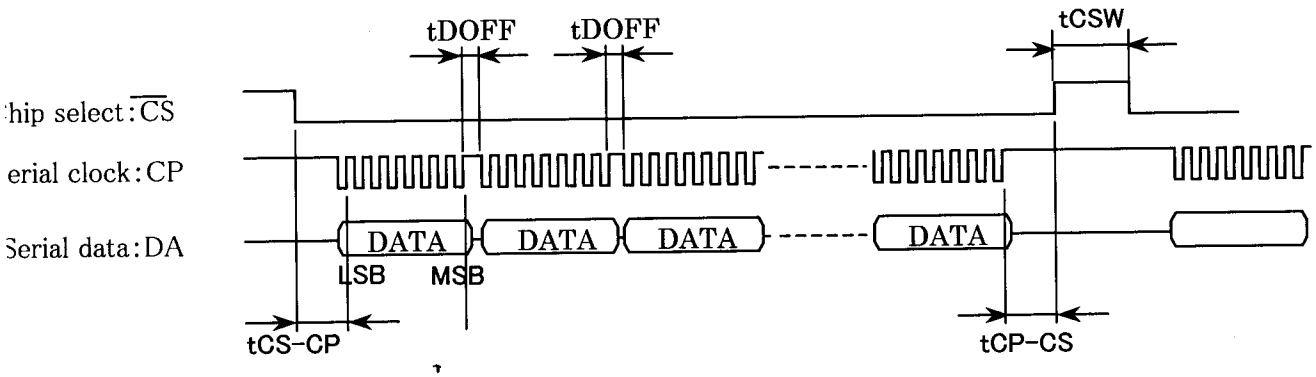
● RELATIONSHIP BETWEEN SEGMENT DRIVERS SGN AND ADN (ONE DIGIT)

The following diagram best describes the relationship between the Segment Drivers --SGn and ADn.



● DATA TRANSFER

The Display Control Command and the data are written by an-8-bit serial data transfer. Please refer to the Write Timming Diagram below.



Note: When data is written into the RAM (DCRAM , ADRAM , CGRAM) in a continuous manner , the address are automatically incremented. Therefore it is not necessary to specify the first byte of the 2nd and later bytes when writing the RAM data.

When the $\overline{CS}$ pin is set to "LOW" level, data transfer operation is enabled. 8 bits of data are sequentially inputted into the DA Pin (LSB first). The shift register reads the data at the rising edge of generated and the data is written to each register and RAM. Thus, it is not necessary to input load signals externally.

When the $\overline{CS}$ Pin is set to "HIGH" level, the data transfer operation is disabled. The data input when the $\overline{CS}$ Pin changes from "HIGH" to "LOW" is recognized in 8-bit units.

● Commands

1. List of commands.

The following are the list of commands issued by PT6302. When data is written into the RAM (DCRAM, CGRAM, or ADRAM) in a continuous manner, the addresses are automatically incremented internally. It is therefore not necessary to specify the first byte.

Table 1 shows the list of commands.

Table 1 Commands

NO.	Command	LSB 1st Byte							MSB	LSB 2nd Byte							MSB	
		B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	
1	DCRAM DATA WRITE	X0	X1	X2	X3	1	0	0	0	C0	C1	C2	C3	C4	C5	C6	C7	
2	CGRAM DATA WRITE	X0	X1	X2	*	0	1	0	0	C0	C5	C10	C15	C20	C25	C30	*	2nd Byte
										C1	C6	C11	C16	C21	C26	C31	*	3rd Byte
										C2	C7	C12	C17	C22	C27	C32	*	4th Byte
										C3	C8	C13	C18	C23	C28	C33	*	5th Byte
										C4	C9	C14	C19	C24	C29	C34	*	6th Byte
3	ADRAM DATA WRITE	X0	X1	X2	X3	1	1	0	0	E0	E1	*	*	*	*	*	*	
4	GENERAL OUTPUT PORT SET	P1	P2	*	*	0	0	1	0									
5	DUTY SET OF DISPLAY	D0	D1	D2	*	1	0	1	0									
6	NO. OF DIGITS SET	K0	K1	K2	*	0	1	1	0									
7	ALL LIGHTS ON/OFF	L	H	*	*	1	1	1	0									

*: arbitrary

Xn: To set the address for RAM, n= 0 to 3

Cn: To set the CGRAM character code, n= 0 to 34

En: To set ON/OFFof AD1～AD2outputs, n= 0 to 1

Dn: To set display duty, n= 0 to 2

Kn: To set the value for digits bit, n= 0 to 2

H: To set to all lights ON, H=1: all lights ON (all segments at H) H=0: normal lighting mode

L: To set to all lights OFF, L=1: all lights OFF (all segments at L) L=0: normal lighting mode

Pn: To set General output port status bit, n=0 to 1

The Test Mode is not a user function, but an IC internal function.

2 Description of commands

2.1 DCRAM data write command

The DCRAM (data control RAM) has a 5-bit address to store the character codes of the CGROM and the CGRAM. The character codes specified by the DCRAM are converted into the character pattern of 5x7 dot matrix via the CGROM or the CGRAM.

To write-in the DCRAM, specify the DCRAM address and write-in the character codes of the CGROM and the CGRAM. For the setting relationship of the DCRAM address to the display timing, refer to section 2.5, Display duty set command. The command format is

【Command Format】

	LSB							MSB
	B0	B1	B2	B3	B4	B5	B6	B7
1st byte (1st)	X0	X1	X2	X3	1	0	0	0

The DCRAM data write mode is selected and the DCRAM address is specified.
(Ex. The DCRAM address 0H is specified.)

	LSB							MSB
	B0	B1	B2	B3	B4	B5	B6	B7
2nd byte (2nd)	C0	C1	C2	C3	C4	C5	C6	C7

The CGROM and CGRAM character codes are specified. (The specified character codes are written into the DCRAM address 0H.)

●To continuously specify the CGROM and CGRAM character codes, specify character codes only as shown below. As the DCRAM addresses are automatically incremented, it is not necessary to specify the first byte. Addresses are specified from 00H to 13H incrementing 1 by 1. It is possible to continuously transfer up to 24 addresses.

	LSB							MSB
	B0	B1	B2	B3	B4	B5	B6	B7
2nd byte (3rd)	C0	C1	C2	C3	C4	C5	C6	C7

The CGROM and CGRAM character codes are specified.
(The data are written into the DCRAM address 1H.)

	LSB							MSB
	B0	B1	B2	B3	B4	B5	B6	B7
2nd byte (4th)	C0	C1	C2	C3	C4	C5	C6	C7

The CGROM and CGRAM character codes are specified.
(The data are written into the DCRAM address 2H.)

:

	LSB							MSB
	B0	B1	B2	B3	B4	B5	B6	B7
2nd byte (17th)	C0	C1	C2	C3	C4	C5	C6	C7

The CGROM and CGRAM character codes are specified.
(The data are written into the DCRAM address FH.)

	LSB							MSB
	B0	B1	B2	B3	B4	B5	B6	B7
2nd byte (18th)	C0	C1	C2	C3	C4	C5	C6	C7

The CGROM and CGRAM character codes are specified.
(The data are written into the DCRAM address 0H.)

X0(LSB)～X3(MSB) : DCRAM address (5bit: 16 characters)
C0(LSB)～C7(MSB) : CGROM and CGRAM codes (8bit: 256 characters)

Hex	X0	X1	X2	X3	Grid position
0	0	0	0	0	GR1
1	1	0	0	0	GR2
2	0	1	0	0	GR3
3	1	1	0	0	GR4
4	0	0	1	0	GR5
5	1	0	1	0	GR6
6	0	1	1	0	GR7
7	1	1	1	0	GR8
8	0	0	0	1	GR9
9	1	0	0	1	GR10
A	0	1	0	1	GR11
B	1	1	0	1	GR12
C	0	0	1	1	GR13
D	1	0	1	1	GR14
E	0	1	1	1	GR15
F	1	1	1	1	GR16

2.2 CGRAM data write command

The CGRAM (character generator RAM) has a 3-bit address to store character Patterns of 5x7 dot matrix. Character patterns stored in the CGRAM can be outputted by specifying the character code (address) of DCRAM. The CGRAM addresses are assigned from 00H

The CGRAM can be written-in by specifying its address.
The command format is shown below.

【Command Format】

	LSB							MSB	
	B0	B1	B2	B3	B4	B5	B6	B7	
1st byte (1st)	X0	X1	X2	*	0	1	0	0	The CGRAM data write command and the CGRAM address are specified. (Ex: The CGRAM address 00H is specified.)
2nd byte (2nd)	C0	C5	C10	C15	C20	C25	C30	*	The data in the first row is specified. (The data is written into the CGRAM address 00H.)
3rd byte (3rd)	C1	C6	C11	C16	C21	C26	C31	*	The data in the second row is specified. (The data is written into the CGRAM address 00H.)
4th byte (4th)	C2	C7	C12	C17	C22	C27	C32	*	The data in the third row is specified. (The data is written into the CGRAM address 00H.)
5th byte (5th)	C3	C8	C13	C18	C23	C28	C33	*	The data in the fourth row is specified. (The data is written into the CGRAM address 00H.)
6th byte (6th)	C4	C9	C14	C19	C24	C29	C34	*	The data in the fifth row is specified. (The data is written into the CGRAM address 00H.)

●To continuously specify character pattern data, specify the character pattern data only as shown below. As the DCRAM addresses are automatically incremented, it is not necessary to specify the first byte. The character pattern data of the 2nd to the 6th byte are considered as one data. The time between bytes tDOFF is 2us(min).

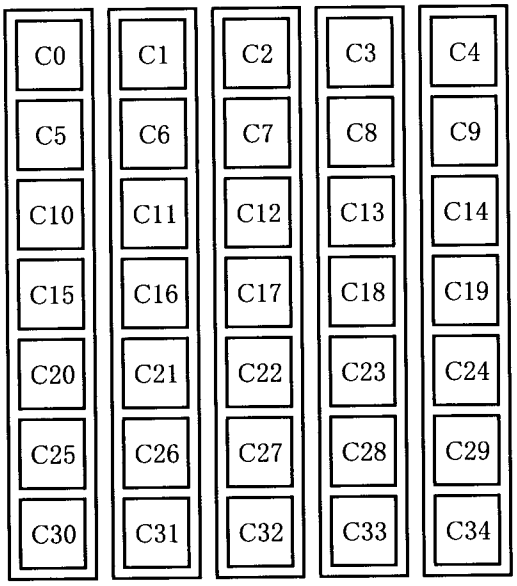
	LSB							MSB	
	B0	B1	B2	B3	B4	B5	B6	B7	
2nd byte (7th)	C0	C5	C10	C15	C20	C25	C30	*	The data in the first row is specified. (Written into the CGRAM address 01H.)
	:								
6th byte (11th)	C4	C9	C14	C19	C24	C29	C34	*	The data in the fifth row is specified. (Written into the CGRAM address 01H.)

X0(LSB)～X2(MSB) : CGRAM address (3 bits: for 8 characters)
C0(LSB)～C34(MSB): character pattern data (35 bits: 35 outputs for a digit)
*: Don't Care

【Setting relationship of CGRAM Addresses】

HEX	X2	X1	X0	指定CGRAM
0	0	0	0	RAM00 (00H)
1	0	0	1	RAM01 (01H)
2	0	1	0	RAM02 (02H)
3	0	1	1	RAM03 (03H)
4	1	0	0	RAM04 (04H)
5	1	0	1	RAM05 (05H)
6	1	1	0	RAM06 (06H)
7	1	1	1	RAM07 (07H)

【Setting relationship CGRAM Outputs】



- The setting relationship of CGRAM outputs may very depending of the VFD product.
- Refer to the individual specification.

2.3 ADRAM data write command

The ADRAM (Additional Data RAM) has a 5-bit address to store data.
The signal data specified by the ADRAM is directly outputted. The ADRAM stores up to 2 output patterns (AD1 to AD2) for each digit.
To write the ADRAM data, specify the ADRAM address before writing-in data.
Please refer to the Page8 anode connection for the position of set ADRAM address and display timing.
The command format is shown below.

【Command Format】

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
1st byte (1st)	X0	X1	X2	X3	1	1	0	0	To select the ADRAM data write and to specify the ADRAM address. (Ex: To specify the ADRAM address 00H.)
2nd byte (2nd)	E0	E1	*	*	*	*	*	*	To specify the signal data. (Ex: To write-in the data to the ADRAM address 00H.)

●To continuously specify the signal data, specify the character codes only as shown below.
Since the ADRAM addresses are automatically incremented, it is not necessary to specify the 1st byte.
Addresses are specified from 00H to 13H incrementing 1 by 1.

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7	
2nd byte (3rd)	E0	E1	*	*	*	*	*	*	To specify the signal data. (The data is written into the ADRAM address 01H.)
2nd byte (4th)	E0	E1	*	*	*	*	*	*	To specify the signal data. (The data is written into the ADRAM address 02H.)
⋮									
2nd byte (17th)	E0	E1	*	*	*	*	*	*	To specify the signal data. (The data is written into the ADRAM address FH.)
2nd byte (18th)	E0	E1	*	*	*	*	*	*	To specify the signal data. (The data is written into the ADRAM address 00H.)

X0 (LSB) ~ X3 (MSB) : ADRAM address (4-bit)
E0 (LSB) ~ E1 (MSB) : Symbol data bits (2 symbol data per digit)
* : Don't Care

2.4 GENERAL OUTPUT PORT SET COMMAND

The General Output Port Set Command is used to specify the general output port status. The general output port is used to control other input / output devices as well as turn on the LED Display. When th general output port is set to "HIGH", the output is equivalent to the VDD voltage. When the general output port is set to "LOW" Level, the output becomes ground potential. The command form is given below.

【Command Format】

	LSB							MSB
	B0	B1	B2	B3	B4	B5	B6	B7
1st byte (1st)	P1	P2	*	*	0	0	1	0

A General Output Port is selected and the output status is specified.

Where :

1. P1 , P2 : General output port
2. * : Don't Care

The following table shows the data setting in relation to the Status of the General Output Port.

P1	P2	General Output Port Display Status
0	0	P1 = "LOW", P2= "LOW" (see Note)
1	0	P1 = "HIGH", P2= "LOW"
0	1	P1 = "LOW", P2= "HIGH"
1	1	P1 = "HIGH", P2= "HIGH"

NOTE: The state when the power is applied or when $\overline{\text{RESET}}$ is inputted.

2.5 Display duty set command

The display duty command sets is used to write the'display duty value to the duty cycle register. Using a 3-bit data, the display duty adjusts the contrast in 8 stages. When the power is turned ON or when the RSTB signals is inputted, the duty cycle register value is set to "0". It is advisable to always execute this command before turning on the display, after which the desired duty value may be set. The command format is given below.

【Command Format】

	LSB							MSB	
	B0	B1	B2	B3	B4	B5	B6	B7	
1st byte (1st)	D0	D1	D2	*	1	0	1	0	To select the display duty set.

where:

1. D0(LSB) to D2 (MSB) : Display duty data bits (8 stages)
2. *: Don't Care

The Relationship between the Setup Data and the Controlled GRID Duty is given in the table below:

Hex	D2	D1	D0	Grid Duty
0	0	0	0	8/16
1	0	0	1	9/16
2	0	1	0	10/16
3	0	1	1	11/16
4	1	0	0	12/16
5	1	0	1	13/16
6	1	1	0	14/16
7	1	1	1	15/16

← The state when the Power is tumed ON or when the $\overline{\text{RESET}}$ signal is inputted.

2.6 NUMBER OF DIGITS SET COMMAND

The Number of Digits Set Command is used to write the number of display digits into the display digit register. Using a 3-bit data, the Number of Digits Set Command can display 9 to 16 digits. When the power is turned ON or when the RSTB signals is inputted, the value is set to "0". It is advisable to always execte this command before the turning on the display. The command format is given bellow.

【Command Format】

	LSB							MSB
	B0	B1	B2	B3	B4	B5	B6	B7
1st byte (1st)	K0	K1	K2	*	0	1	1	0

The Number of Digits Set Mode is selected and the number of digit value is specified.

The table below shows the relationship between the setup data and controlled GR.

Hex	K2	K1	K0	Number of Digits of GR
0	0	0	0	GR1～GR16
1	0	0	1	GR1～GR9
2	0	1	0	GR1～GR10
3	0	1	1	GR1～GR11
4	1	0	0	GR1～GR12
5	1	0	1	GR1～GR13
6	1	1	0	GR1～GR14
7	1	1	1	GR1～GR15

← **The state when the power is turned ON or when the $\overline{\text{RESET}}$ signal is inputted.**

2.7 Display light ON/OFF set command

The display light ON/OFF set command are used to turn on all the display lights or turn them off. The all display lights OFF mode is mainly used for blinking or protecting the display from any misoperation to be aused when the power is supplied.The command format is shown below.

【Command Format】

	LSB B0	B1	B2	B3	B4	B5	B6	MSB B7
1st byte (1st)	L	H	*	*	1	1	1	0

To select the all display light ON/OFF and specify operation.

L,H : display operation data.

* : Don't Care.

●Set value and display status

L	H	Display status	
0	0	Normal operation	
1	0	All display lights OFF	← The state when the power is applied or when the $\overline{\text{RESET}}$ signal is inputted.
0	1	All display lights ON	
1	1	All display lights ON	← All Display Light ON Mode has the first priority.

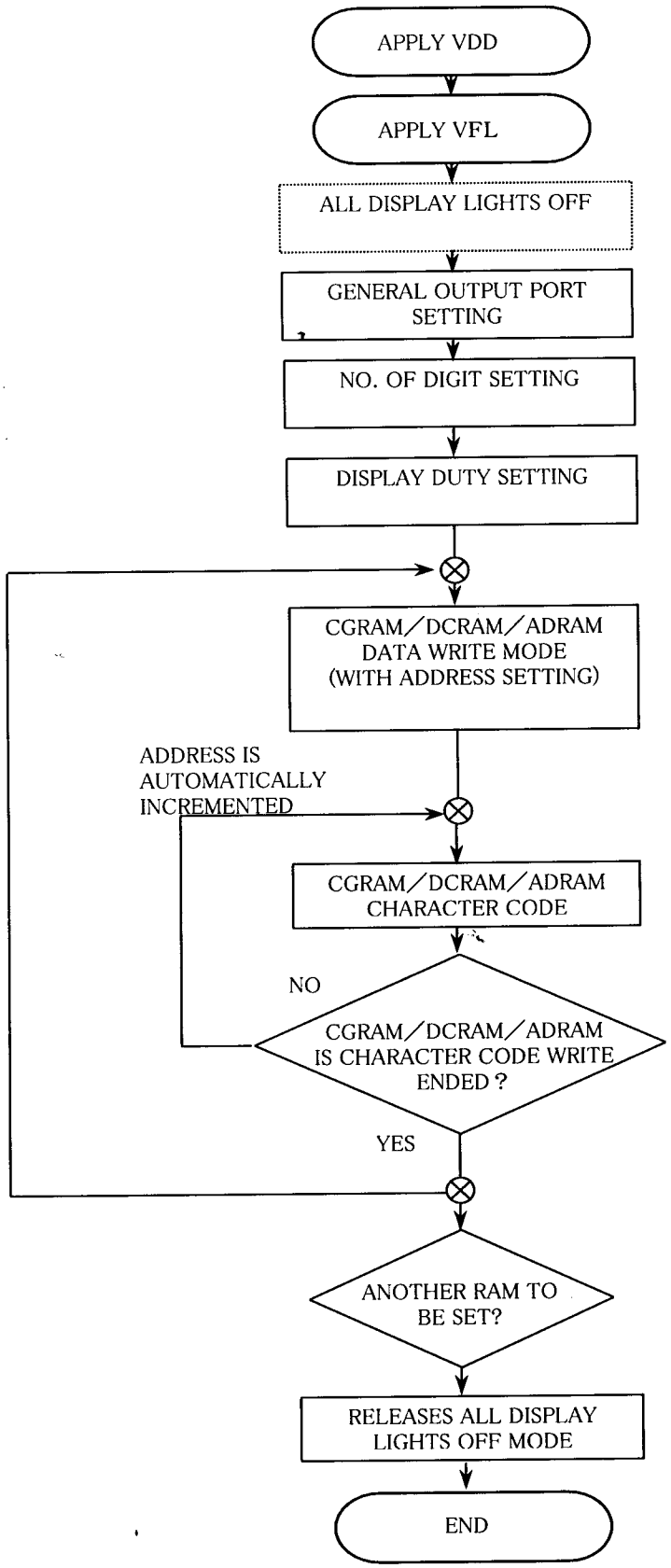
2.8 CGROM codes

MSB / LSB	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	RAM0															
0001	RAM1															
0010	RAM2															
0011	RAM3															
0100	RAM4															
0101	RAM5															
0110	RAM6															
0111	RAM7															
1000																
1001																
1010																
1011																
1100																
1101																
1110																
1111																

形名 Type No. 16-BD-08GINK

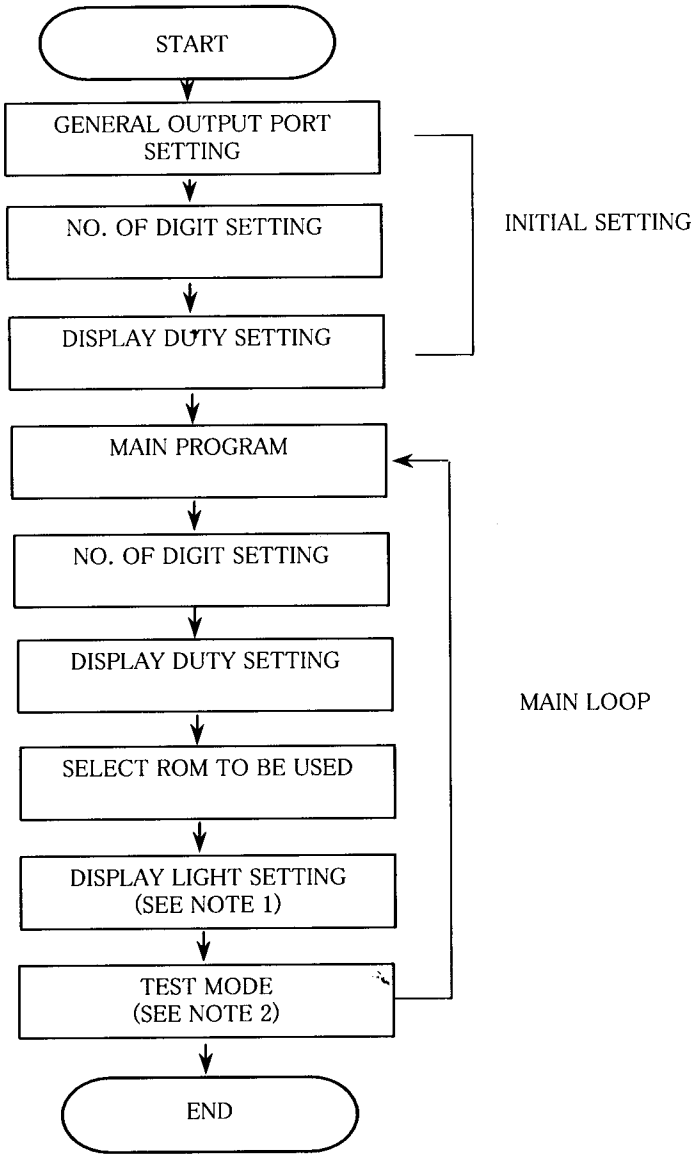
● Flowchart of Commands

1.SETTING FLOWCHART
(Power applying included)



● Flowchart of Commands

2.RECOMMENDED SOFTWARE FOLWCHART



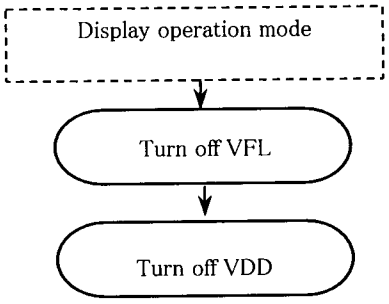
Note:

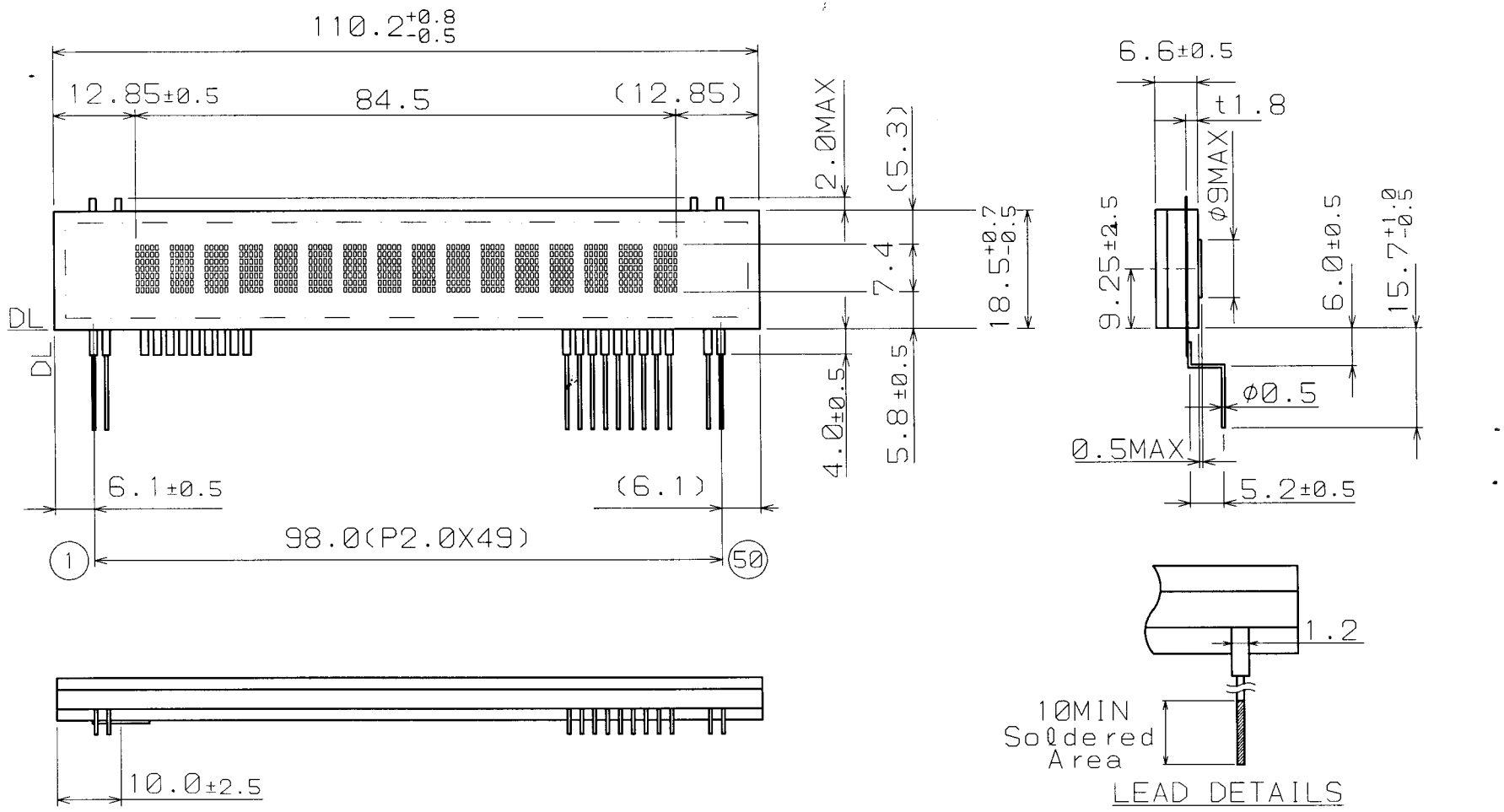
1.Display light active mode.(ex. 0111XX00B)

2.Test mode off (ex. 1000X000B)

● Flowchart of Commands

3.Power-off Flowchart





LEAD FREE SOLDER

(unit in mm)

16-BD-08GINK
OUTER DIMENSION

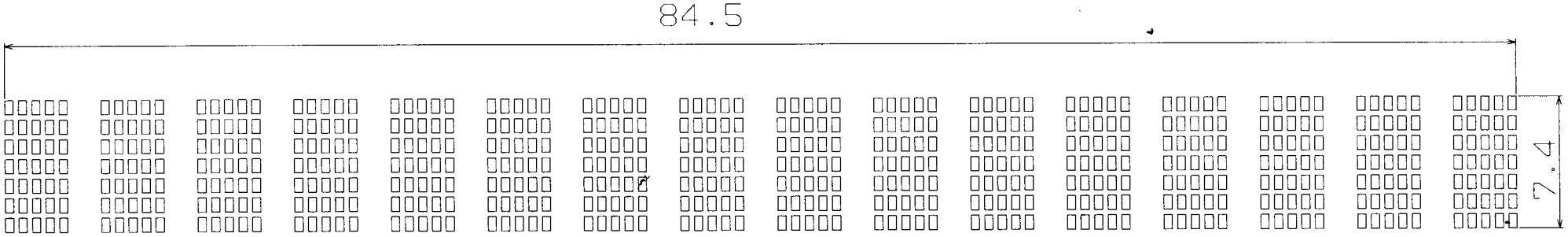
PIN CONNECTION

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
CONNECTION	F1	F1	NP	NP	NX	NX	NX	NX	NX	NX	NX	NX	NX	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	NP	ND	VDD	DA	CP	-CS	-RESET	OSCO	OSCI	GND	VFL	NP	NP	F2	F2

NOTE
1) F1,F2 --- Filament
2) NP ------ No pin
3) NX ------ No extend pin
4) DL ------ Datum Line
5) VFL ----- VFD Driving Voltage sink pin
6) GND ----- GND pin
7) OSCI ----- Input Pin for oscillation
8) $\overline{\text{OSCO}}$ ----- Output Pin for oscillation
9) $\overline{\text{RESET}}$ --- Reset Input
10) $\overline{\text{CS}}$ ------ Chip Select Input pin
11) CP ------ Shift Register Clock
12) DA ------ Serial Data Input
13) VDD ----- Logic Voltage Supply pin
14) Solder composition is Sn-3Ag-0.5Cu.

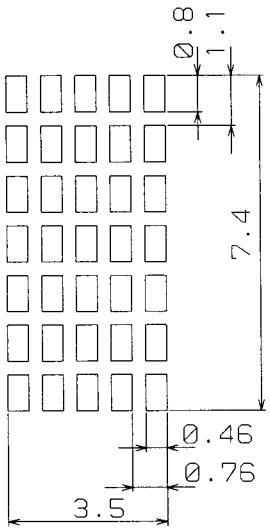
16-BD-08GINK
OUTER DIMENSION

PATTERN DETAIL



COLOR OF ILLUMINATION

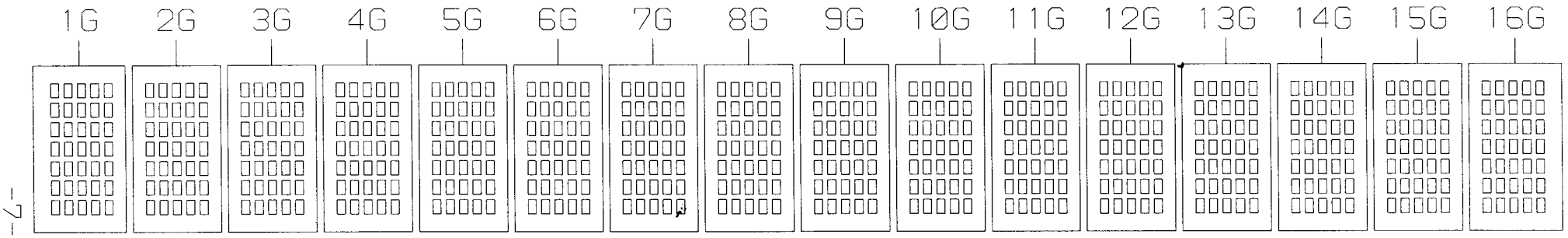
Green (G. x=0.24, y=0.41) - - - - - AQQ graphics.

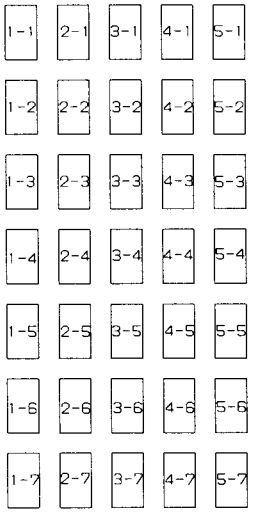


(unit in mm)

16-BD-08GINK
PATTERN DETAIL
COLOR OF ILLUMINATION

GRID ASSIGNMENT





(1G~16G)

16-BD-08GINK
GRID ASSIGNMENT

ANODE CONNECTION

	1G~16G
C0	1-1
C1	2-1
C2	3-1
C3	4-1
C4	5-1
C5	1-2
C6	2-2
C7	3-2
C8	4-2
C9	5-2
C10	1-3
C11	2-3
C12	3-3
C13	4-3
C14	5-3
C15	1-4
C16	2-4
C17	3-4
C18	4-4
C19	5-4
C20	1-5
C21	2-5
C22	3-5
C23	4-5
C24	5-5
C25	1-6
C26	2-6
C27	3-6
C28	4-6
C29	5-6
C30	1-7
C31	2-7
C32	3-7
C33	4-7
C34	5-7

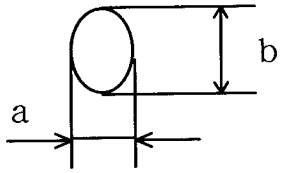
16-BD-08GINK
ANODE CONNECTION

Vacuum Fluorescent Display Quality Inspection Standard
蛍光表示管品質判定基準

General 一般

This standard should be adapted to the VFD quality inspection.
本仕様書は蛍光表示管の品質検査規格に適用される。

Inspection Condition 検査条件

Item	Condition
①VFD Operating Condition. VFD 駆動条件	Typ. Recommended Condition 推奨TYP. 駆動条件
②Inspection Aide 検査付帯条件	The inspection is to be performed with Futaba standard filter*1 or a applicable customer's filter and unaided eyes from 30cm distance under brightness of 90－110 lx. Futaba標準フィルター*1または顧客指定フィルターを通して30cmの距離から、90－110 lx の周囲照度にて、目視判定する。
③Defect Point Definition 不良点の測定方法	 $\phi S = \frac{a+b}{2}$

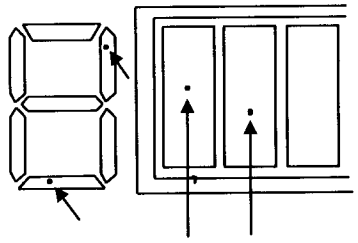
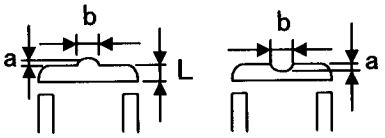
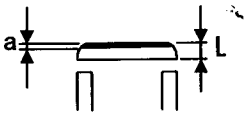
Limit sample should be provided upon mutual agreement by both parties when necessary.
限度見本は必要に応じ、両者協議の上設定するものとする。

Note *1
Futaba standard filter
双葉標準フィルター

Standard filter 標準フィルター	Type No. 型名	Manufacturer メーカー	Application 用途				
			Automotive 車載	Home Appliance 民生			
				Office machine 事務機	Consumer 家電用	Audio 音響	VTR
Gray smoke グレイスモーク	#530	MITSUBISHI RAYON 三菱レーヨン製	○	○	○		
Wine red ワインレッド	PZ-1123-R	DIATEC (株)ダイヤテック製				○	○

形名 Type No. 16-BD-08GINK

Individual Quality Standard 個別品質基準

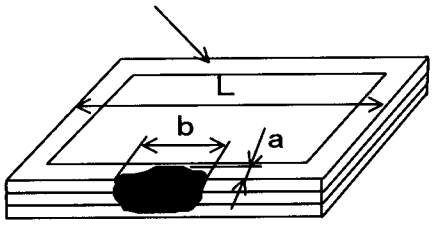
Item 項目	Phenomena 現象	Criterion 判定基準
①Foreign Particles・ Black Spot・ Printing Error 異物・黒点・ 印刷不良	Spots(Black spot)on the lighted segment due to dirt or dust. セグメントの斑点状の発光ムラ(黒点)。 	1.A black spot of over Φ0.3mm is counted as defected point. s=Φ0.3mmを超える物は不良とする。 2.In case of spot size is over Φ0.2mm,less than 0.3mm,one spot on the same segment, or maximum 3 spots in a display is to be allowed. Φ0.2mm以上Φ0.3mm以下は、セグメントに1箇まで、全セグメントに3箇所までを良品とする。 3.A spot of less than Φ0.2mm should not be counted as defect point. Φ0.2mm未満の物は個数に拘わらず良品とする。
②Irregularity of segment shape by printing error. ｾｸﾞﾒﾝﾄ凹凸・ 印刷不良	Partial irregularity on a segment. セグメント形状の部分的凹凸 	1.Acceptable size of irregularities with respect to the segment width(L). セグメント幅(L)に対する凹凸の許容寸法。 a=0.3mm max., b=0.3mm max.,acceptable. a=0.3mm 以下、b=0.3mm 以下を良品とする。 2.In case of the (L) below 0.5mm wide,the acceptable irregularities is a=1/2max. of the segment width(L). 尚、セグメント幅(L)が0.5mm以下の場合は、a≦1/2Lを良品とする。
③Uneven luminance 輝度ムラ	Partial dark area on the lighted segment. 発光面の部分的な輝度差	No significant irregularity of luminance is acceptable. 著しい物は無き事。
④Shaded Segment 字カケ	Shaded area appeared on the edge of segments セグメント端部の半影 	1.Shaded Segments up to 1/3 of the segment width are accepted. セグメント幅(L)の1/3までを良品とする。 2.In case of a segment below 0.5mm wide, the acceptable shaded segment should be up to 1/2 of the segment width. 但し、L≦0.5mmの場合は、1/2迄を良品とする。
⑤Extra lighting モレ発光	Undesirable lighting area or points, a star dust or a bright spot due like to extra phosphor particle. 発光パタン以外への蛍光体付着による星屑状、輝点状の不要発光	Extra lighting which can be clearly observed through the specified filter should be judged as a defect. 指定フィルターを通して不要発光のはっきり判る物を不良とする。
⑥Scratch/Stain on/in glass ガラス傷・汚れ	A scratch,dent,or foreign particles such as stain,attached on the surface or the inside of the front glass. フロントガラス内面・表面のガラス面の傷、シミ等の異物付着	1.Scratch which can be clearly observed through the specified filter should be judged as defect. 指定ﾌｨﾙﾀｰを通して傷のはっきり判る物を不良とする。 2.The criterion for the dent and foreign particle are the same as the specified in ①. 打痕状の傷、異物等は、①頁と同等判定とする。
⑦Chip on the front glass and base plate ガラス欠け	For chip on the front glass and base plate,refer to the next page. ガラス欠けについては、次頁参照	Refer to the next page. 次頁参照

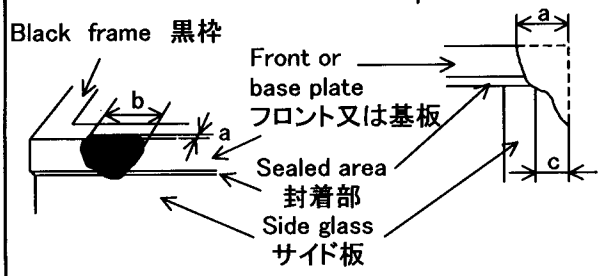
形名 Type No. 16-BD-08GINK

Criterion for the glass chip on the front glass or the base plate.

Definition 定義	Judgment Criterion 判定基準

Black frame 黒枠





a : depth of chipping
欠けの奥行き寸法

b : length of chipping
欠けの長さ寸法

c : chipping size in relation to thickness of the side glass.
サイド板厚に対する欠け寸法

L : package width (length wide)
パッケージ幅（長辺方向）

1) Chipping size Spec. 欠けの寸法規格(mm)

	VFD:a	FLVFD:a	b	c
L≦100	within the black frame 黒枠以内	3.0max.	10max.	1/3max.
L>100	within the black frame 黒枠以内	3.5max.	15max.	1/3max.

VFD : vacuum fluorescent display
蛍光表示管

FLVFD :Front Luminous Vacuum Fluorescent Display
前面発光型蛍光表示管

2) A chip with "a" less than 1mm should not be counted as defect point.
a寸法が1mm未満の場合は欠点としない。

3) A chip area covered with sealing cement should not be counted as defect point.
封着前の欠けは、欠けの中に封着セメントが流入していれば欠点としない。

4) Up to 3 chips within this specification in a same display to be allowed.
表示管全体で規格内の欠け数は3ケまで良品とする。

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