2024-1 Computer Architecture Homework #1

Due: 3/31 (Sun) 11:59 p.m.

1. [15] Compilers can have a profound impact on the performance of an application. Assume that for a program, compiler A results in a dynamic instruction count of 1.0E9 and has an execution time of 1.1 s, while compiler B results in a dynamic instruction count of 1.2E9 and an execution time of 1.5 s.

   a. [5] Find the average CPI for each program given that the processor has a clock cycle time of 1 ns.

   b. [5] Assume the compiled programs run on two different processors. If the execution times on the two processors are the same, how much faster is the clock of the processor running compiler A's code versus the clock of the processor running compiler B's code?

   c. [5] A new compiler is developed that uses only 6.0E8 instructions and has an average CPI of 1.1. What is the speedup of using this new compiler versus using compiler A or B on the original processor?

2. [35] Assume for arithmetic, load/store, and branch instructions, a processor has CPIs of 1, 12, and 5, respectively. Also assume that on a single processor a program requires the execution of 2.56E9 arithmetic instructions, 1.28E9 load/store instructions, and 256 million branch instructions. Assume that each processor has a 2 GHz clock frequency. Assume that, as the program is parallelized to run over multiple cores, the number of arithmetic and load/store instructions per processor is divided by 0.7 x p (where p is the number of processors) but the number of branch instructions per processor remains the same.

   a. [15] Find the total execution time for this program on 1, 2, 4 processors, and show the relative speedup of the 2, 4 processor result relative to the single processor result.

   b. [10] If the CPI of the arithmetic instructions was doubled, what would the

impact be on the execution time of the program on 1, 2, 4 processors?

c. [10] To what should the CPI of load/store instructions be reduced in order for a single processor to match the performance of four processors using the original CPI values?

3. [30] The Pentium 4 Presco processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power. The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

a. [5] For each processor find the average capacitive loads.

b. [5] Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.

c. [20] If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? Note: power is defined as the product of voltage and current.

4. [20] Another pitfall cited in Section 1.11 is expecting to improve the overall performance of a computer by improving only one aspect of the computer. Consider a computer running a program that requires 250 s, with 70 s spent executing FP instructions, 85 s executed L/S instructions, and 40 s spent executing branch instructions.

a. [5] By how much is the total time reduced if the time for FP operations is reduced by 20%?

b. [10] By how much is the time for INT operations reduced if the total time is reduced by 20%?

c. [5] Can the total time can be reduced by 20% by reducing only the time for branch instructions?