2024-1 Computer Architecture Homework #2

Due: 4/19 (Fri) 11:59 p.m.

1. [25] Translate the following C code to MIPS. Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3, and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7, respectively. Assume that the elements of the arrays A and B are 8-byte words:

```
B[8] = A[i] + A[j];
```

2. [10] Provide the type and assembly language instruction for the following binary value:0000 0010 0001 0000 1000 0000 0010 0000two . Hint: Figure 2.20 may be helpful.

3. [25] Consider a proposed new instruction named rpt. This instruction combines a loop's condition check and counter decrement into a single instruction. For example, rpt $s0, loop would do the following:

```
if (x29 > 0) {
        x29 = x29 − 1;
        goto loop
}
```

a. [10] If this instruction were to be implemented in the MIPS instruction set, what is the most appropriate instruction format?

b. [15] What is the shortest sequence of MIPS instructions that performs the same operation?

4. [20] Translate the following loop into C. Assume that the C-level integer i is held in register $t1, $s2 holds the C-level integer called result, and $s0 holds the base address of the integer MemArray.

```
        addi $t1, $0, 0
LOOP: lw $s1, 0($s0)
        add $s2, $s2, $s1
        addi $s0, $s0, 4
        addi $t1, $t1, 1
        slti $t2, $t1, 100
        bne $t2, $s0, LOOP
```

5. [20] For the following code:

```
lbu $t0, 0($t1)
sw $t0, 0($t2)
```

Assume that the register $t1 contains the address 0x10000000 and the data at address is 0x11223344.

a. [10] What value is stored in 0x10000004 on a big-endian machine?

b. [10] What value is stored in 0x10000004 on a lile-endian machine?