Integrated Circuit Systems, Inc.

ICS94211

Programmable System Frequency Generator for PII/III™

Recommended Application:

440BX/VIA Apollo Pro133/ ALI 1631 style chipset.

Output Features:

- 2 - CPUs @2.5V
- 1 - IOAPIC @ 2.5V
- 13 - SDRAM @ 3.3V
- 6 - PCI @3.3V,
- 1 - 48MHz, @3.3V
- 1 - 24MHz @ 3.3V
- 2 - REF @3.3V, 14.318MHz.

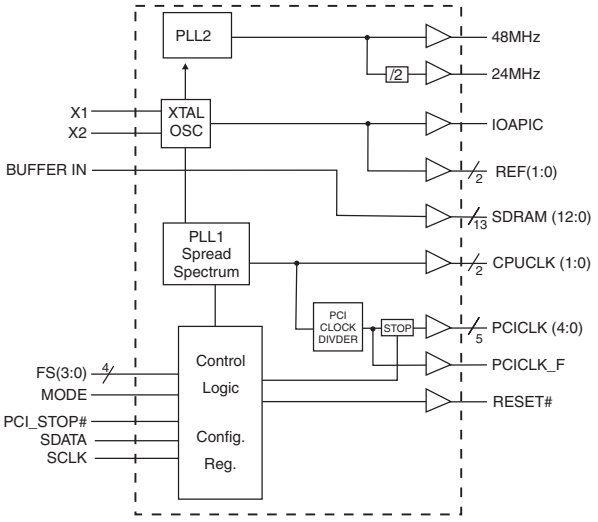
Features:

- Programmable ouput frequency.
- Programmable ouput rise/fall time.
- Programmable PCICLK, PCICLK_F, SDRAM skew.
- Real time system reset output
- Spread spectrum for EMI control typically by 7dB to 8dB,
  with programmable spread percentage.
- Watchdog timer technology to reset system if over-clocking causes malfunction.
- Uses external 14.318MHz crystal.
- FS pins for frequency select

Key Specifications:

- CPU – CPU: <175ps
- SDRAM - SDRAM: <500ps
- PCI – PCI: <500ps
- CPU(early)-PCI: Min=1.0ns, Typ=2.0ns, Max=4.0ns

Block Diagram



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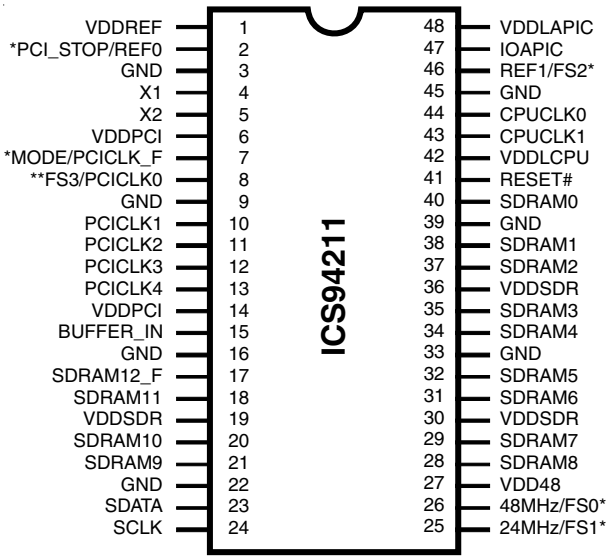
Pin Configuration



48-Pin 300mil SSOP

* Internal Pull-up Resistor of 120K to VDD
** Internal Pull-down resistor of 120K to GND

Functionality

FS3	FS2	FS1	FS0	CPU (MHz)	PCICLK (MHz)
0	0	0	0	80.00	40.00
0	0	0	1	75.00	37.50
0	0	1	0	83.31	41.65
0	0	1	1	66.82	33.41
0	1	0	0	103.00	34.33
0	1	0	1	112.01	37.34
0	1	1	0	68.01	34.01
0	1	1	1	100.23	33.41
1	0	0	0	120.00	40.00
1	0	0	1	114.99	38.33
1	0	1	0	109.99	36.66
1	0	1	1	105.00	35.00
1	1	0	0	140.00	35.00
1	1	0	1	150.00	37.50
1	1	1	0	124.00	31.00
1	1	1	1	132.99	33.25

General Description

The **ICS94211** is a single chip clock solution for desktop designs using the BX/Apollo Pro133/ALI 1631 style chipset. It provides all necessary clock signals for such a system.

The **ICS94211** belongs to ICS new generation of programmable system clock generators. It employs serial programming I^2C interface as a vehicle for changing output functions, changing output frequency, configuring output strength, configuring output to output skew, changing spread spectrum amount, changing group divider ratio and dis/enabling individual clocks. This device also has ICS propriety 'Watchdog Timer' technology which will reset the frequency to a safe setting if the system become unstable from over clocking.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
2	REF0	OUT	14.318 Mhz reference clock.
	PCI_STOP#[1]	IN	Halts PCICLK(0:4) clocks at logic 0 level, when input low (In mobile mode, MODE=0)
3, 9, 16, 22, 33, 39, 45	GND	PWR	Ground
4	X1	IN	Crystal input, has internal load cap (36pF) and feedback resistor from X2
5	X2	OUT	Crystal output, nominally 14.318MHz. Has internal load cap (36pF)
6, 14	VDDPCI	PWR	Supply for PCICLK_F and PCICLK (0:4), nominal 3.3V
7	PCICLK_F	OUT	Free running PCI clock not affected by PCI_STOP# for power management.
	MODE[1, 2]	IN	Pin 7 function select pin, 1=Desktop Mode, 0=Mobile Mode. Latched Input.
8	FS3	IN	Frequency select pin. Latched Input. Internal Pull-down to GND
	PCICLK0	OUT	PCI clock outputs. Syncheronous to CPU clocks with 1-48ns skew (CPU early)
13, 12, 11, 10	PCICLK (4:1)	OUT	PCI clock outputs. Syncheronous to CPU clocks with 1-48ns skew (CPU early)
15	BUFFER IN	IN	Input to Fanout Buffers for SDRAM outputs.
17, 18, 20, 21, 28, 29, 31, 32, 34, 35, 37, 38, 40	SDRAM (12:0)	OUT	SDRAM clock outputs, Fanout Buffer outputs from BUFFER IN pin (controlled by chipset)
19, 30, 36	VDDSDR	PWR	Supply for SDRAM (0:12) and CPU PLL Core, nominal 3.3V.
23	SDATA	I/O	Data input for I^2C serial input, 5V tolerant input
24	SCLK	IN	Clock input of I^2C input, 5V tolerant input
25	24MHz	OUT	24MHz output clock
	FS1[1, 2]	IN	Frequency select pin. Latched Input.
26	48MHz	OUT	48MHz output clock
	FS0[1, 2]	IN	Frequency select pin. Latched Input
27	VDD48	PWR	Power for 24 & 48MHz output buffers and fixed PLL core.
41	RESET	OUT	Real time system reset signal for frequency ratio change or watchdog timmer timeout. This signal is active low.
42	VDDLCPU	PWR	Supply for CPU clocks, 2.5V nominal
43	CPUCLK1	OUT	CPU clock outputs, powered by VDDL2. Low if CPU_STOP#=Low
44	CPUCLK0	OUT	Free running CPU clock. Not affected by the CPU_STOP#
46	REF1	OUT	14.318 MHz reference clock.
	FS2[1, 2]	IN	Frequency select pin. Latched Input
47	IOAPIC	OUT	IOAPIC clock output. 14.318 MHz Powered by VDDL.
48	VDDLAPIC	PWR	Power pin for the IOAPIC outputs. 2.5V.

Notes:

1: Internal Pull-up Resistor of 120K to 3.3V on indicated inputs

2: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.

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General I²C serial interface information for the ICS94211

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte 0 through Byte 20*** (see Note)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
○	
○	○
○	○
	○
Byte 18	
	ACK
Byte 19	
	ACK
Byte 20	
	ACK
Stop Bit	

*See notes on the following page.

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends ***Byte 0 through byte 8 (default)***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8).***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
If 7_H has been written to B6	***Byte 7***
ACK	
○	○
○	○
○	○
If 12_H has been written to B6	***Byte18***
ACK	
If 13_H has been written to B6	***Byte 19***
ACK	
If 14_H has been written to B6	***Byte 20***
ACK	
Stop Bit	

Brief I²C registers description for ICS94211 Programmable System Frequency Generator

Register Name	Byte	Description	PWD Default
Functionality & Frequency Select Register	0	Output frequency, hardware / I²C frequency select, spread spectrum & output enable control register.	See individual byte description
Output Control Registers	1-6	Active / inactive output control registers/latch inputs read back.	See individual byte description
Vendor ID & Revision ID Registers	7	Byte 11 bit[7:4] is ICS vendor id - 1001. Other bits in this register designate device revision ID of this part.	See individual byte description
Byte Count Read Back Register	8	Writing to this register will configure byte count and how many byte will be read back. Do not write 00_H to this byte.	08_H
Watchdog Timer Count Register	9	Writing to this register will configure the number of seconds for the watchdog timer to reset.	10_H
Watchdog Control Registers	10 Bit [6:0]	Watchdog enable, watchdog status and programmable 'safe' frequency' can be configured in this register.	000,0000
VCO Control Selection Bit	10 Bit [7]	This bit select whether the output frequency is control by hardware/byte 0 configurations or byte 11&12 programming.	0
VCO Frequency Control Registers	11-12	These registers control the dividers ratio into the phase detector and thus control the VCO output frequency.	Depended on hardware/byte 0 configuration
Spread Spectrum Control Registers	13-14	These registers control the spread percentage amount.	Depended on hardware/byte 0 configuration
Group Skews Control Registers	15-16	Increment or decrement the group skew amount as compared to the initial skew.	See individual byte description
Output Rise/Fall Time Select Registers	17-20	These registers will control the output rise and fall time.	See individual byte description

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. Readback will support standard SMBUS controller protocol. **The number of bytes to readback is defined by writing to byte 8.**
2. **When writing to byte 11 - 12, and byte 13 - 14, they must be written as a set.** If for example, only byte 14 is written but not 15, neither byte 14 or 15 will load into the receiver.
3. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
4. The input is operating at 3.3V logic levels.
5. The data byte format is 8 bit bytes.
6. To simplify the clock generator I²C interface, the protocol is set to use only Block-Writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
7. At power-on, all registers are set to a default condition, as shown.

Byte 0: Functionality and frequency select register (Default=0)

Bit	Description									PWD
Bit (2,7:4)	Bit2	Bit7 FS3	Bit6 FS2	Bit5 FS1	Bit4 FS0	VCO/REF Divider	VCO MHz	CPUCLK MHz	PCICLK MHz	Note 1
	0	0	0	0	0	447/40	160.01	80.00	40.00	
	0	0	0	0	1	440/42	150.00	75.00	37.50	
	0	0	0	1	0	512/44	166.61	83.31	41.65	
	0	0	0	1	1	392/42	133.64	66.82	33.41	
	0	0	1	0	0	446/31	206.00	103.00	34.33	
	0	0	1	0	1	485/31	224.01	112.01	37.34	
	0	0	1	1	0	513/54	136.02	68.01	34.01	
	0	0	1	1	1	518/37	200.45	100.23	33.41	
	0	1	0	0	0	352/21	240.00	120.00	40.00	
	0	1	0	0	1	514/32	229.99	114.99	38.33	
	0	1	0	1	0	507/33	219.98	109.99	36.66	
	0	1	0	1	1	484/33	210.00	105.00	35.00	
	0	1	1	0	0	352/18	280.00	140.00	35.00	
	0	1	1	0	1	440/21	300.00	150.00	37.50	
	0	1	1	1	0	433/25	247.99	124.00	31.00	
	0	1	1	1	1	483/26	265.99	132.99	33.25	
	1	0	0	0	0	396/21	270.00	135.00	33.75	
	1	0	0	0	1	345/19	259.99	129.99	32.50	
	1	0	0	1	0	440/25	252.00	126.00	31.50	
	1	0	0	1	1	478/29	236.00	118.00	39.33	
	1	0	1	0	0	486/30	231.95	115.98	38.66	
	1	0	1	0	1	491/37	190.01	95.00	31.67	
	1	0	1	1	0	440/35	180.00	90.00	30.00	
	1	0	1	1	1	463/39	169.98	85.01	28.34	
	1	1	0	0	0	371/16	332.00	166.00	41.50	
	1	1	0	0	1	447/20	320.01	160.01	40.00	
	1	1	0	1	0	433/20	309.99	154.99	38.75	
	1	1	0	1	1	310/15	295.91	147.95	36.99	
	1	1	1	0	0	469/23	291.97	145.98	36.50	
	1	1	1	0	1	362/18	287.95	143.98	35.99	
	1	1	1	1	0	476/24	283.98	141.99	35.50	
	1	1	1	1	1	347/18	276.02	138.01	34.50	
Bit 3	0-Frequency is selected by hardware select, latched inputs 1- Frequency is selected by Bit 2,7:4									0
Bit 1	0- Normal 1- Spread spectrum enable ± 0.35% Center Spread									1
Bit 0	0- Running 1- Tristate all outputs									0

Notes:

1. Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

Byte 1: CPU, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Latched FS2#
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	40	1	SDRAM0
Bit 2	-	1	(Reserved)
Bit 1	43	1	CPUCLK1
Bit 0	44	1	CPUCLK0

Byte 2: PCI, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	7	1	PCICLK_F
Bit 5	-	1	(Reserved)
Bit 4	13	1	PCICLK4
Bit 3	12	1	PCICLK3
Bit 2	11	1	PCICLK2
Bit 1	10	1	PCICLK1
Bit 0	8	1	PCICLK0

Byte 3: SDRAM, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	X	Latched FS0#
Bit 5	26	1	48MHz
Bit 4	25	1	24 MHz
Bit 3	-	1	(Reserved)
Bit 2	17, 21, 20, 18	1	SDRAM (9:12)
Bit 1	28, 32, 31, 29,	1	SDRAM (5:8)
Bit 0	34, 38, 37, 35	1	SDRAM (1:4)

Byte 4: Reserved , Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	-	1	(Reserved)
Bit 3	-	X	Latched FS1#
Bit 2	-	1	(Reserved)
Bit 1	-	X	Latched FS3#
Bit 0	-	1	(Reserved)

Byte 5: Peripheral , Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	(Reserved)
Bit 6	-	1	(Reserved)
Bit 5	-	1	(Reserved)
Bit 4	47	1	IOAPIC
Bit 3	-	1	(Reserved)
Bit 2	-	1	(Reserved)
Bit 1	46	1	REF1
Bit 0	2	1	REF0

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Byte 6: Peripheral , Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved (Note)
Bit6	-	0	Reserved (Note)
Bit5	-	0	Reserved (Note)
Bit4	-	0	Reserved (Note)
Bit3	-	0	Reserved (Note)
Bit2	-	1	Reserved (Note)
Bit1	-	1	Reserved (Note)
Bit0	-	0	Reserved (Note)

Note: This is an unused register writing to this register will not affect device performance or functinality.

Byte 7: Vendor ID and Revision ID Register

Bit	PWD	Description
Bit 7	0	Vendor ID
Bit 6	0	Vendor ID
Bit 5	1	Vendor ID
Bit 4	X	Revision ID
Bit 3	X	Revision ID
Bit 2	X	Revision ID
Bit 1	X	Revision ID
Bit 0	X	Revision ID

Byte 8: Byte Count and Read Back Register

Bit	PWD	Description
Bit 7	0	Reserved
Bit 6	0	Reserved
Bit 5	0	Reserved
Bit 4	0	Reserved
Bit 3	1	Reserved
Bit 2	0	Reserved
Bit 1	0	Reserved
Bit 0	0	Reserved

Byte 9: VCO Control Selection Bit & Watchdog Timer Control Register

Bit	PWD	Description
Bit 7	0	0=Hw/B0 freq / 1=B14&15 freq
Bit 6	0	WD Enable 0=disable / 1=enable
Bit 5	0	WD Status 0=normal / 1=alarm
Bit 4	0	WD Safe Frequency, Byte 0 bit 2
Bit 3	0	WD Safe Frequency, FS3
Bit 2	0	WD Safe Frequency, FS2
Bit 1	0	WD Safe Frequency, FS1
Bit 0	0	WD Safe Frequency, FS0

Note: FS values in bit [0:4] will correspond to Byte 0 FS values. Default safe frequency is same as 00000 entry in byte0.

Byte 10: Watchdog Timer Count Register

Bit	PWD	Description
Bit 7	0	The decimal representation of these 8 bits correspond to 290ms or 1ms the watchdog timer will wait before it goes to alarm mode and reset the frequency to the safe setting. Default at power up is 16X 290ms = 4.6 seconds.
Bit 6	0	
Bit 5	0	
Bit 4	1	
Bit 3	0	
Bit 2	0	
Bit 1	0	
Bit 0	0	

Byte 11: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit0
Bit 6	X	REF Divider Bit6
Bit 5	X	REF Divider Bit5
Bit 4	X	REF Divider Bit4
Bit 3	X	REF Divider Bit3
Bit 2	X	REF Divider Bit2
Bit 1	X	REF Divider Bit1
Bit 0	X	REF Divider Bit0

Note: The decimal representation of these 7 bits (Byte 11 [6:0]) + 2 is equal to the REF divider value .

Notes:

1. PWD = Power on Default

Byte 12: VCO Frequency Control Register

Bit	PWD	Description
Bit 7	X	VCO Divider Bit8
Bit 6	X	VCO Divider Bit7
Bit 5	X	VCO Divider Bit6
Bit 4	X	VCO Divider Bit5
Bit 3	X	VCO Divider Bit4
Bit 2	X	VCO Divider Bit3
Bit 1	X	VCO Divider Bit2
Bit 0	X	VCO Divider Bit1

Note: The decimal representation of these 9 bits (Byte 12 bit [7:0] & Byte 11 bit [7]) + 8 is equal to the VCO divider value. For example if VCO divider value of 36 is desired, user need to program 36 - 8 = 28, namely, 0, 00011100 into byte 12 bit & byte 11 bit 7.

Byte 13: Spread Sectrum Control Register

Bit	PWD	Description
Bit 7	X	Spread Spectrum Bit7
Bit 6	X	Spread Spectrum Bit6
Bit 5	X	Spread Spectrum Bit5
Bit 4	X	Spread Spectrum Bit4
Bit 3	X	Spread Spectrum Bit3
Bit 2	X	Spread Spectrum Bit2
Bit 1	X	Spread Spectrum Bit1
Bit 0	X	Spread Spectrum Bit0

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 14: Spread Sectrum Control Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Spread Spectrum Bit12
Bit 3	X	Spread Spectrum Bit11
Bit 2	X	Spread Spectrum Bit10
Bit 1	X	Spread Spectrum Bi 9
Bit 0	X	Spread Spectrum Bit8

Note: Please utilize software utility provided by ICS Application Engineering to configure spread spectrum. Incorrect spread percentage may cause system failure.

Byte 15: Output Skew Control

Bit	PWD	Description
Bit 7		PCICLK_F Skew Control
Bit 6		
Bit 5		PCICLK [0:4} Skew Control
Bit 4		
Bit 3		SDRAM_F Skew Control
Bit 2		
Bit 1		SDRAM [0:7} Skew Control
Bit 0		

Byte 16: Output Skew Control

Bit	PWD	Description
Bit 7		SDRAM [8:11] Skew Control
Bit 6		
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Byte 17: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7		CPUCLK_F: Slew Rate Control
Bit 6		
Bit 5		CPUCLK1: Slew Rate Control
Bit 4		
Bit 3		SDRAM [0:11] Slew Rate Control
Bit 2		
Bit 1		SDRAM_F: Slew Rate Control
Bit 0		

Byte 18: Output Rise/Fall Time Select Register

Bit	PWD	Description
Bit 7		PCI {0:4]: Slew Rate Control
Bit 6		
Bit 5		PCI_F Slew Rate Control
Bit 4		
Bit 3		48MHz: Slew Rate Control
Bit 2		
Bit 1		24MHz: Slew Rate Control
Bit 0		

Notes:

1. PWD = Power on Default
2. The power on default for byte 13-20 depends on the harware (latch inputs FS[0:4]) or I^2C (Byte 0 bit [1:7]) setting. Be sure to read back and re-write the values of these 8 registers when VCO frequency change is desired for the first pass.

Byte 19: Reserved Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Byte 20: Reserved Register

Bit	PWD	Description
Bit 7	X	Reserved
Bit 6	X	Reserved
Bit 5	X	Reserved
Bit 4	X	Reserved
Bit 3	X	Reserved
Bit 2	X	Reserved
Bit 1	X	Reserved
Bit 0	X	Reserved

Note: Byte 19 and 20 are reserved registers, these are unused registers writing to these registers will not affect device performance or functinality.

VCO Programming Constrains

VCO Frequency ..... 150MHz to 500MHz

VCO Divider Range ..... 8 to 519

REF Divider Range ..... 2 to 129

Phase Detector Stability ..... 0.3536 to 1.4142

Useful Formula

VCO Frequency = 14.31818 x VCO/REF divider value

Phase Detector Stabiliy = 14.038 x (VCO divider value)$^{-0.5}$

To program the VCO frequency for over-clocking.

0. Before trying to program our clock manually, consider using ICS provided software utilities for easy programming.

1. Select the frequency you want to over-clock from with the desire gear ratio (i.e. CPU:SDRAM:3V66:PCI ratio) by writing to byte 0, or using initial hardware power up frequency.

2. Write 0001, 1001 (19_H) to byte 8 for readback of 21 bytes (byte 0-20).

3. Read back byte 11-20 and copy values in these registers.

4. Re-initialize the write sequence.

5. Write a '1' to byte 9 bit 7 and write to byte 11 & 12 with the desired VCO & REF divider values.

6. Write to byte 13 to 20 with the values you copy from step 3. This maintains the output spread, skew and slew rate.

7. The above procedure is only needed when changing the VCO for the 1st pass. If VCO frequency needed to be changed again, user only needs to write to byte 11 and 12 unless the system is to reboot.

Note:

1. User needs to ensure step 3 & 7 is carried out. Systems with wrong spread percentage and/or group to group skew relation programmed into bytes 13-16 could be unstable. Step 3 & 7 assure the correct spread and skew relationship.

2. If VCO, REF divider values or phase detector stability are out of range, the device may fail to function correctly.

3. Follow min and max VCO frequency range provided. Internal PLL could be unstable if VCO frequency is too fast or too slow. Use 14.31818MHz x VCO/REF divider values to calculate the VCO frequency (MHz).

4. ICS recommends users, to utilize the software utility provided by ICS Application Engineering to program the VCO frequency.

5. Spread percent needs to be calculated based on VCO frequency, spread modulation frequency and spreadamount desired. See Application note for software support.

Absolute Maximum Ratings

Supply Voltage . . . . . 7.0 V
Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature . . . . . 0°C to +70°C
Case Temperature . . . . . 115°C
Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			
Operating Supply Current	$I_{DD3.3OP}$	C_L = max cap loads; CPU=66-133 MHz, SDRAM=100 MHz		124	350	mA
		CPU=133 MHz, SDRAM=133 MHz		135	500	
	$I_{DD2.5OP}$	C_L = max cap loads;		18	70	
Powerdown Current	$I_{DD3.3PD}$	C_L = 0 pF; Input address to VDD or GND			600	mA
Input Frequency	F_i	V_{DD} = 3.3 V		14.318		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition time[1]	T_{trans}	To 1st crossing of target frequency			3	ms
Settling time[1]	T_s	From 1st crossing to 1% target frequency			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target frequency			3	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		10	ns
Skew[1]	tcpu-pci	V_T = 1.5V; VTL=1.25V		2.45	4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70°C;VDD = 3.3V; V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP2B}	Vo=V_{DD}*(0.5)	13.5	15	45	Ω
Output Impedance[1]	R_{DSN2B}	Vo=V_{DD}*(0.5)	13.5	16.5	45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2	2.48		V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA		0.04	0.4	V
Output High Current	I_{OH2B}	$V_{OH@MIN}$ = 1 V		-60	-27	mA
		$V_{OH@MAX}$ = 2.375V	-27	-7		
Output Low Current	I_{OL2B}	$V_{OL@MIN}$ = 1.2 V	27	63		mA
		$V_{OL@MAX}$ =0.3V		20	30	
Rise Time[1]	t_{r2B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.2	1.6	ns
Fall Time[1]	t_{f2B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	0.9	1.6	ns
Duty Cycle[1]	d_{t2B}	V_T = 1.25 V	45	46.9	55	%
Skew[1]	t_{sk2B}	V_T = 1.25 V		12.7	175	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	V_T = 1.25 V, CPU 66, SDRAM 100		150	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%, C_L = 40 pF for PCI0-1, C_L = 10 - 30 pF for other PCIs (unless otherwise st

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP1}	Vo=V_{DD}*(0.5)	12		55	Ω
Output Impedance[1]	R_{DSN1}	Vo=V_{DD}*(0.5)	12		55	Ω
Output High Voltage	V_{OH1}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH1}	$V_{OH@MIN}$ = 1 V			-33	mA
		$V_{OH@MAX}$ = 3.135V	-33			
Output Low Current	I_{OL1}	$V_{OL@MIN}$ = 1.95 V	30			mA
		$V_{OL@MAX}$ =0.4V			38	
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V,	0.5	1.5	2	ns
Fall Time[1]	t_{f1}	V_{OL} = 2.4 V, V_{OH} = 0.4 V, PCI0-3	0.5	1.5	2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45	52.5	55	%
Skew[1]	t_{sk1}	V_T = 1.5 V		49	500	ps
Jitter, cycle-to-cycle[1]	$t_{jcyc-cyc1}$	V_T = 1.5 V		200	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70°C; VDD = 3.3V; V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP4B}	Vo=V_{DD}*(0.5)	9		3	Ω
Output Impedance[1]	R_{DSN4B}	Vo=V_{DD}*(0.5)	9		30	Ω
Output High Voltage	V_{OH4B}	I_{OH} = -5.5 mA	2			V
Output Low Voltage	V_{OL4B}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH4B}	$V_{OH@MIN}$ = 1.4 V			-21	mA
		$V_{OH@MAX}$ = 2.5V	-36			
Output Low Current	I_{OL4B}	$V_{OL@MIN}$ = 1.0 V	36			mA
		$V_{OL@MAX}$ =0.2V			31	
Rise Time[1]	t_{r4B}	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	0.7	1.6	ns
Fall Time[1]	t_{f4B}	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.1	1.6	ns
Duty Cycle[1]	d_{t4B}	V_T = 1.25 V	45	53.7	55	%

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%, C_L = 20 - 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP3}	Vo=V_{DD}*(0.5)	10		24	Ω
Output Impedance[1]	R_{DSN3}	Vo=V_{DD}*(0.5)	10		24	Ω
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH3}	$V_{OH@MIN}$ = 2 V			-46	mA
		$V_{OH@MAX}$ = 3.135V	-54			
Output Low Current	I_{OL3}	$V_{OL@MIN}$ = 1 V	54			mA
		$V_{OL@MAX}$ =0.4V			53	
Rise Time[1]	t_{r3}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	0.8	1.6	ns
Fall Time[1]	t_{f3}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	0.8	1.6	ns
Duty Cycle[1]	d_{t3}	V_T = 1.5 V	45	51.7	55	%
Skew[1]	t_{sk3}	V_T = 1.5 V		166	250	ps
Propagation Delay	Tprop	V_T = 1.5 V		3.1	5	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 24_48MHz, 48MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance[1]	R_{DSP5}	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output Impedance[1]	R_{DSN5}	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH5}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH5}	$V_{OH @ MIN}$ = 1.0 V			-23	mA
		$V_{OH @ MAX}$ = 3.135 V	-29			
Output Low Current	I_{OL5}	$V_{OL @ MIN}$ = 1.95 V	29			mA
		$V_{OL @ MAX}$ = 0.4 V			27	
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.4	2	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.4	2	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45	53	55	%
Jitter, cycle-to-cycle[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, Fixed clocks		200	500	ps
		V_T = 1.5 V, Ref clocks		1032	1250	

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS94211 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

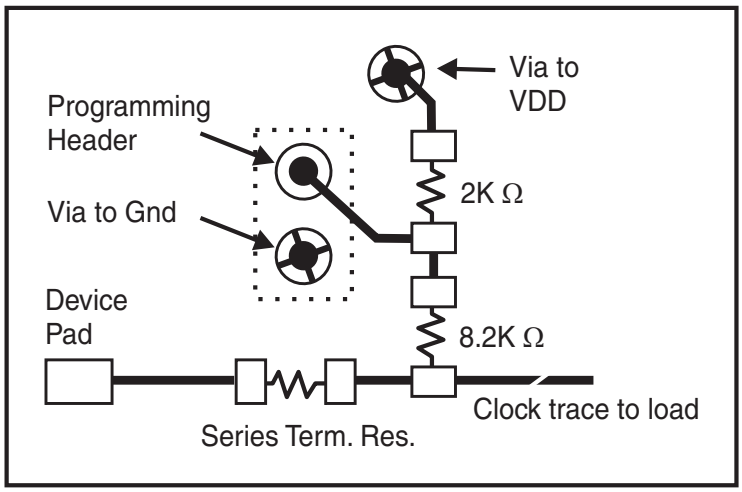
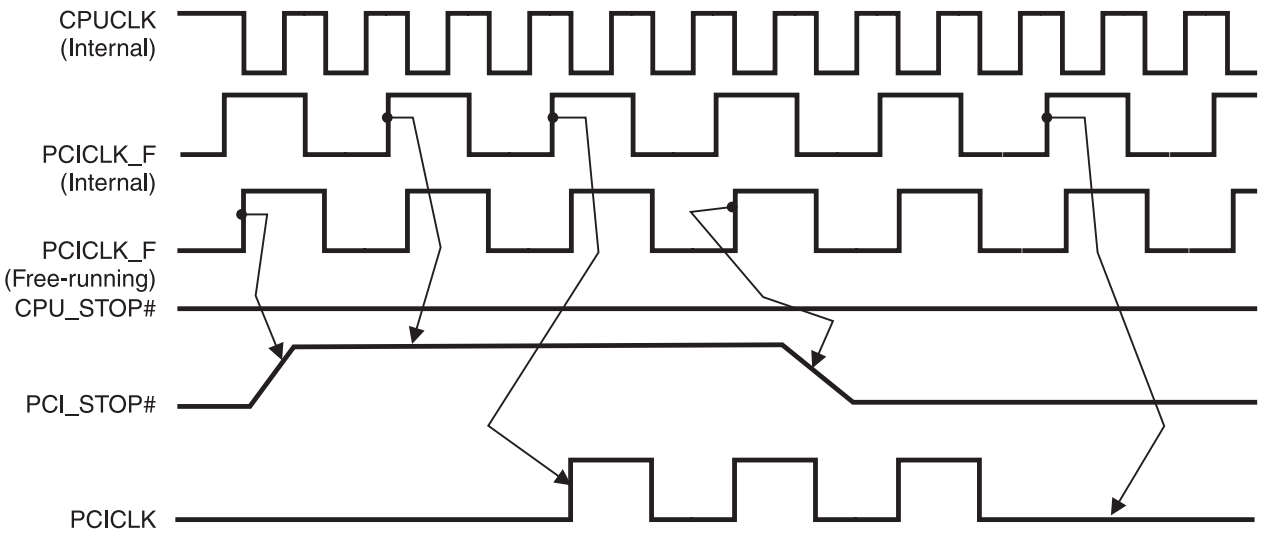


Fig. 1

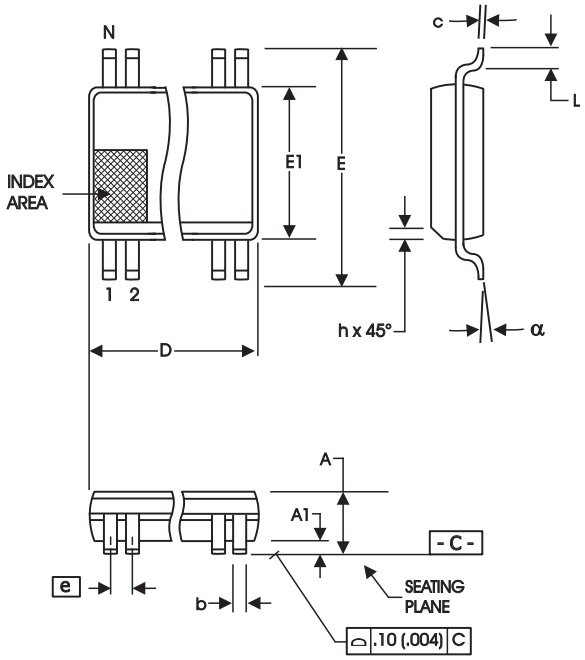
PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS94211**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS94211** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS94211 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS94211.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS94211yFLF-T

Example:

ICS XXXX y F LF -T

- **Designation for tape and reel packaging**
- **Lead Free, RoHS Compliant (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS, AV = Standard Device

0441F—08/24/05

Revision History

Rev.	Issue Date	Description	Page #
F	8/24/2005	Added LF Ordering Information.	16

94211 (Desktop Chipsets)

Description
440BX/VIA Apollo Pro133/ ALI 1631 style chipset.
Market Group
PC CLOCK
Additional Info
The ICS94211 is a single chip clock solution for desktop designs using the BX/Apollo Pro133/ALI 1631 style chipset. It provides all necessary clock signals for such a system. The ICS94211 belongs to ICS new generation of programmable system clock generators. It employs serial programming I2C interface as a vehicle for changing output functions, changing output frequency, configuring output strength, configuring output to output skew, changing spread spectrum amount, changing group divider ratio and dis/ enabling individual clocks. This device also has ICS propriety 'Watchdog Timer' technology which will reset the frequency to a safe setting if the system become unstable from over clocking. • Programmable ouput frequency. • Programmable ouput rise/fall time. • Programmable PCICLK, PCICLK_F, SDRAM skew. • Real time system reset output • Spread spectrum for EMI control typically by 7dB to 8dB, with programmable spread percentage. • Watchdog timer technology to reset system if over-clocking causes malfunction. • Uses external 14.318MHz crystal. • FS pins for frequency select

Related Orderable Parts

Attributes	94211AF	94211AFLF	94211AFLFT	94211AFT
Voltage	3.3 V (PV48)	3.3 V (PVG48)	3.3 V (PVG48)	3.3 V (PV48)
Package	SSOP 48	SSOP 48	SSOP 48	SSOP 48
Speed	NA	NA	NA	NA
Temperature	C	C	C	C
Status	Active	Active	Active	Active
Sample	Yes	Yes	No	No
Minimum Order Quantity	90	90	1000	1000
Factory Order Increment	30	30	1000	1000

Related Documents

Type	Title	Size	Revision Date
Datasheet	94211 Datasheet	165 KB	11/08/2006

Node: www.idt.com