CSE 360-Computer Architecture

Lecture-5

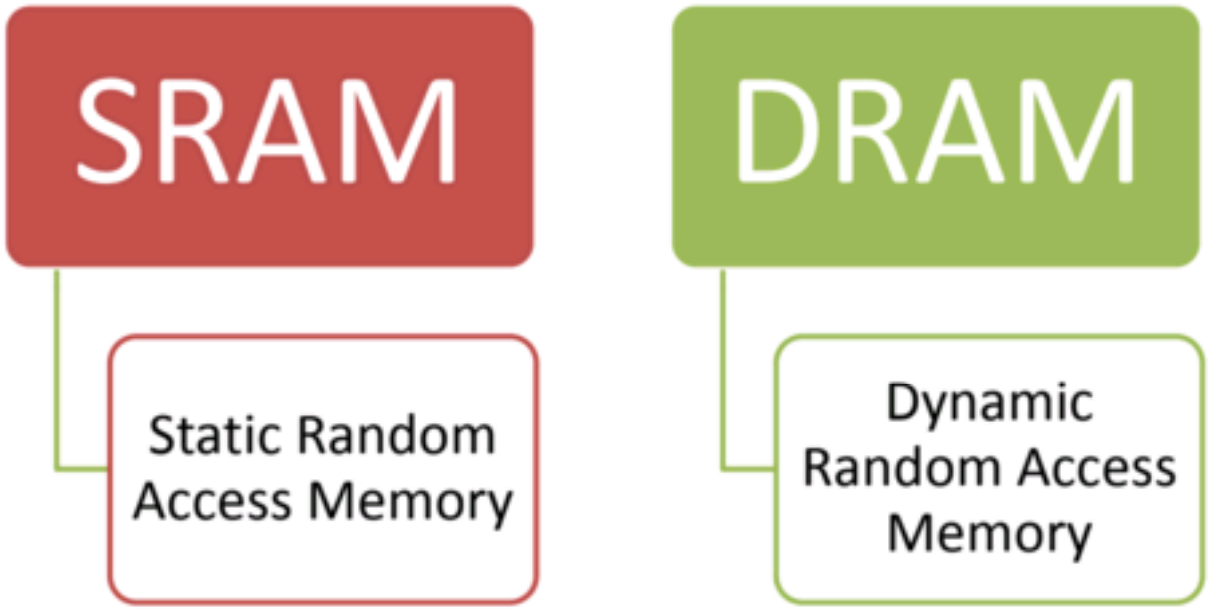
Internal Memory

Dr. Shamim Akhter

Computer Science and Engineering

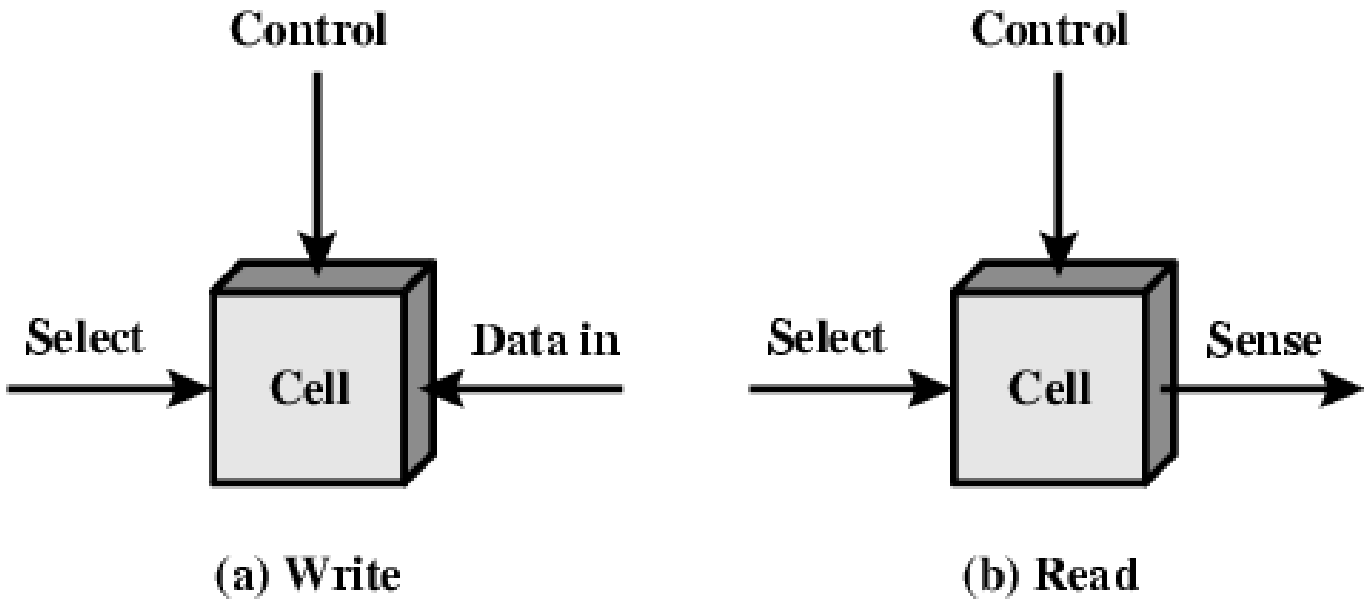
EAST WEST UNIVERSITY

Random Access Memory (RAM)
Volatile Memory



1) What is the meaning of "Static" and "Dynamic"
2) Why is SRAM faster than DRAM?
3) Why is DRAM denser than SRAM?
4) Structure of SRAM and DRAM

Semiconductor Memory Cell

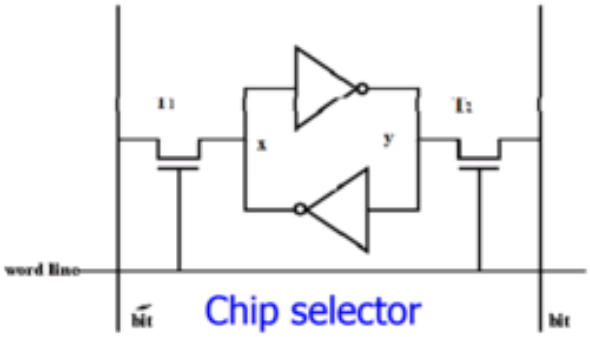


Three(3) functional terminals carry electrical signal:

- **Select terminal:** selects a memory cell for read and write operation.
- **Control terminal : i**ndicates **read or write**
- **Data in /out(sense) terminal:**
  - For writing, the Data in terminal provides an electrical signal that sets the state of the cell to 1 or 0.
  - For reading, the data out terminal is used for output of the cell's state.

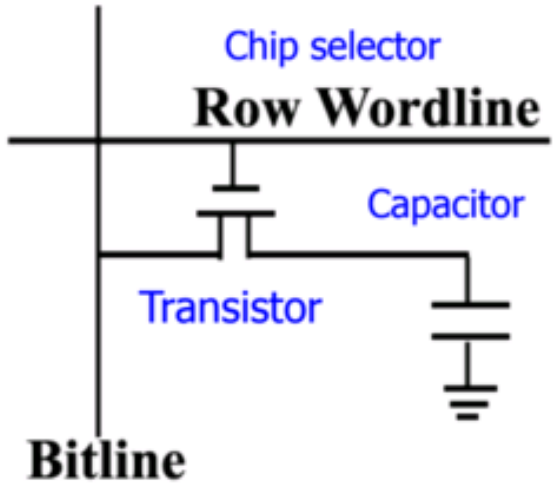
Static and Dynamic

- SRAM
  - Large array of storage cells (registers)
  - Requires **4-6 transistors per bit**
  - Costly (per bit cost)
  - Holds the stored data as long as power on



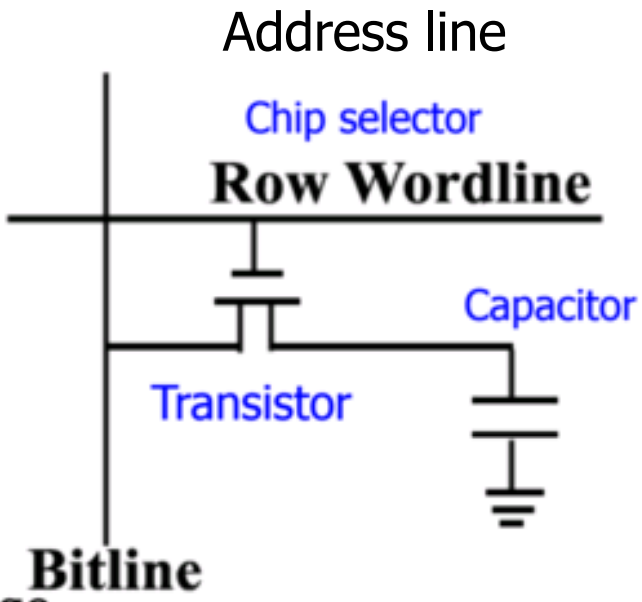
Address line

- DRAM
  - Requires 1 transistor per bit
  - Cheaper than SRAM (per bit cost)
  - Density is higher than SRAM
  - Periodically refreshed to prevent loss of stored data



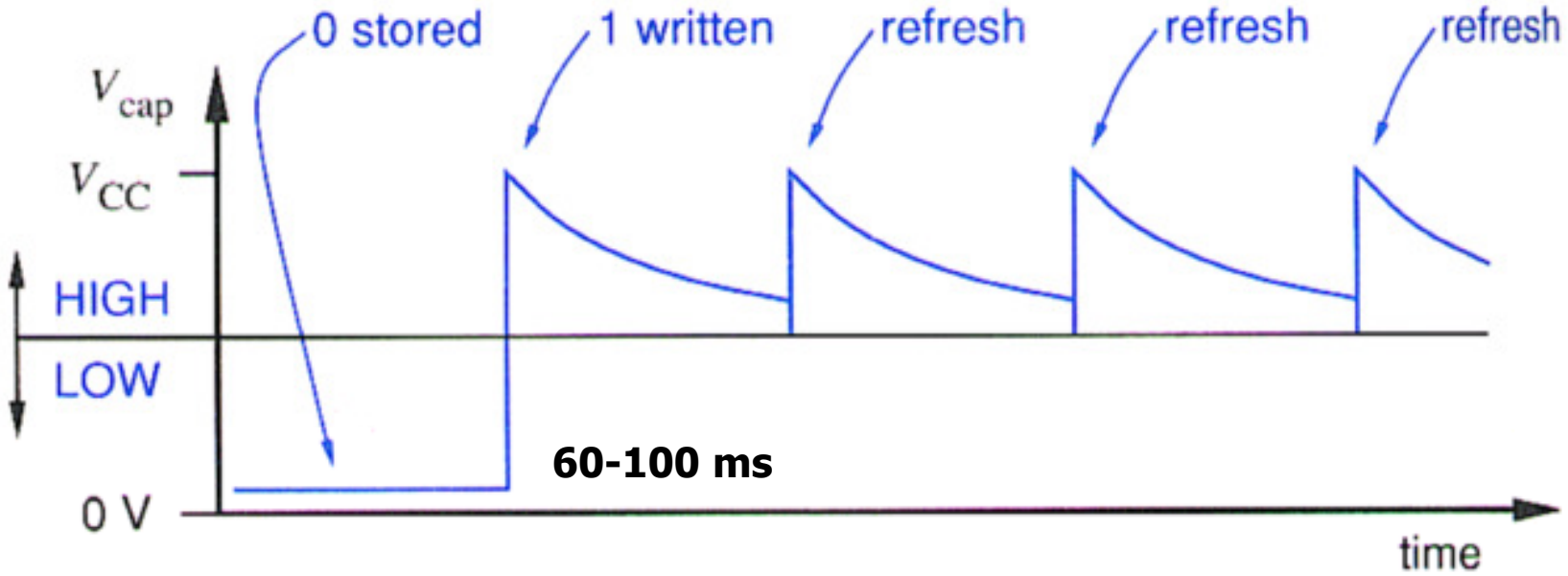
Reading and Writing with DRAM cell

- Store
  - Asserted Wordline
  - Bitline 0/1
  - Capacitor discharged/charged



- Destructive Read
  - Bitline is precharged to a halfway voltage
  - Asserted Wordline
  - Bitline voltage is then pulled slightly lower/higher depending on whether the cell stores 0 or 1
  - Sense amplifier detects the change and recovers 0/1
  - Destructive readout of data must be followed by a write operation to restore the original value.

Why is SRAM faster than DRAM?
Why is DRAM denser than SRAM?



- Single-transistor memory cell, leads to highest possible storage density
- Reduce per bit cost

Impossible to build a bit stable element with only one transistor

DRAM consists Semi Conducting Transistor
-leaks a small amount of electricity
-capacitor slowly discharge
-information eventually fades (requires periodically refreshed)

Capacitor have a natural tendency to discharge

SRAM – Static Random access memory

Read Operation

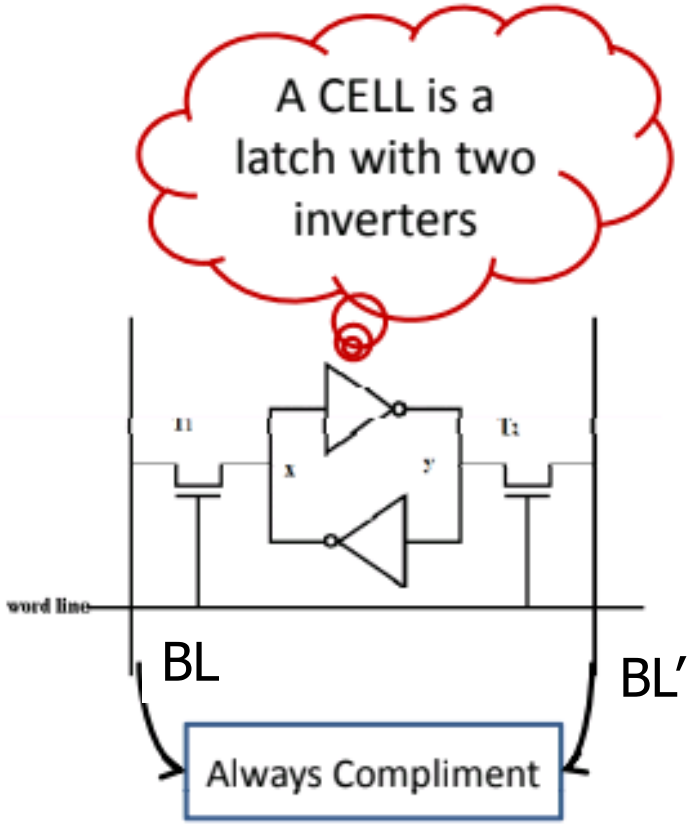
Wordline activates T1 and T2 Transistors
- If CELL has 1
  - bitline (BL) is high and bitline(BL') is low
- If CELL has 0
  - bitline (BL) is low and bitline(BL') is high

Sense amplifier senses the two bit lines and sets the corresponding output

Write Operation

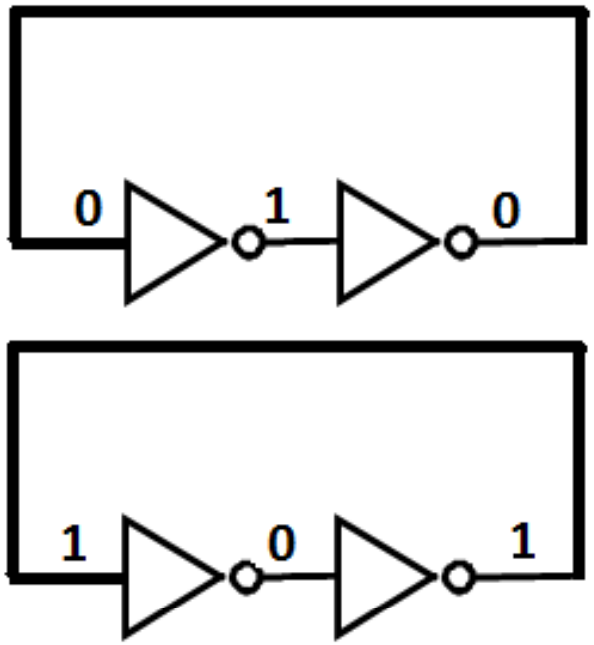
Instead of sensing, drives bit lines (BL and BL')
- Appropriate value at BL and its compliment in BL'
- and activated word line

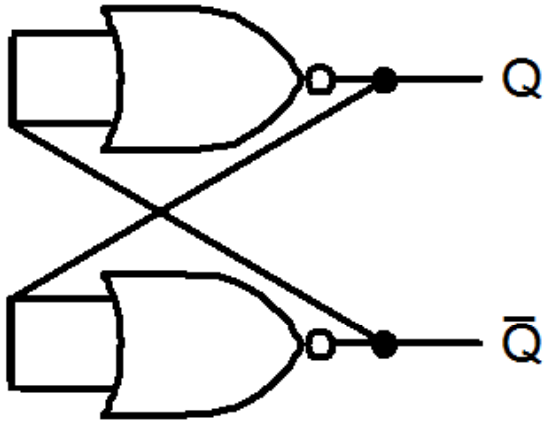
Force the cell to corresponding state and cell retains when the word line is deactivated.



Question: SRAM has 4-6 transistors but we are watching two.
Where are the others?

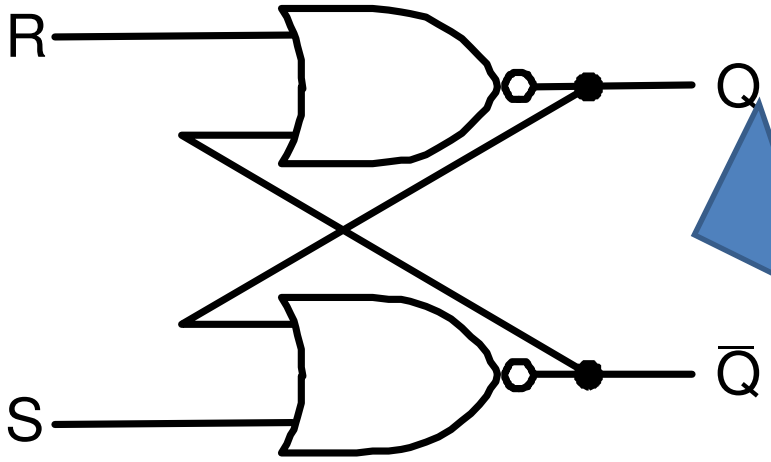
- Stable Circuit (same input always same output)
  - 1 input -> 1 output
  - 0 input -> 0 output





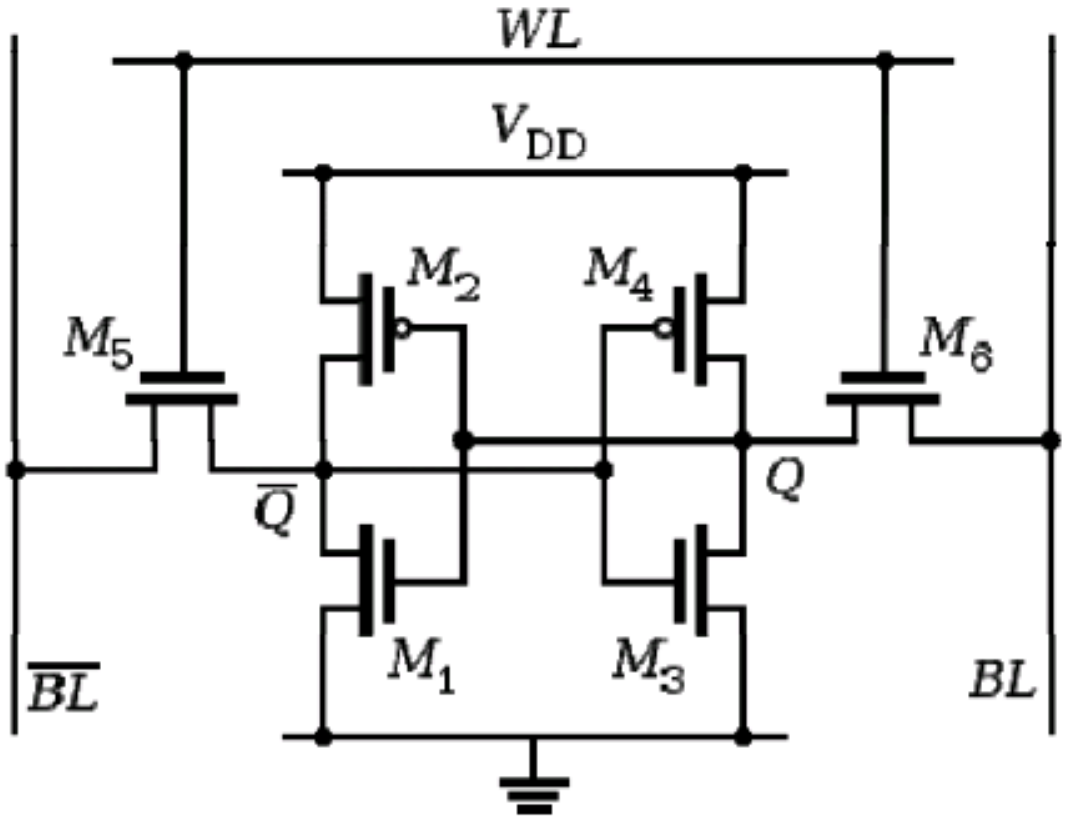
Storing Capability but Infinite Looping

How do we control this circuit??



S-R Latch

SRAM Cell with Six(6) Transistors

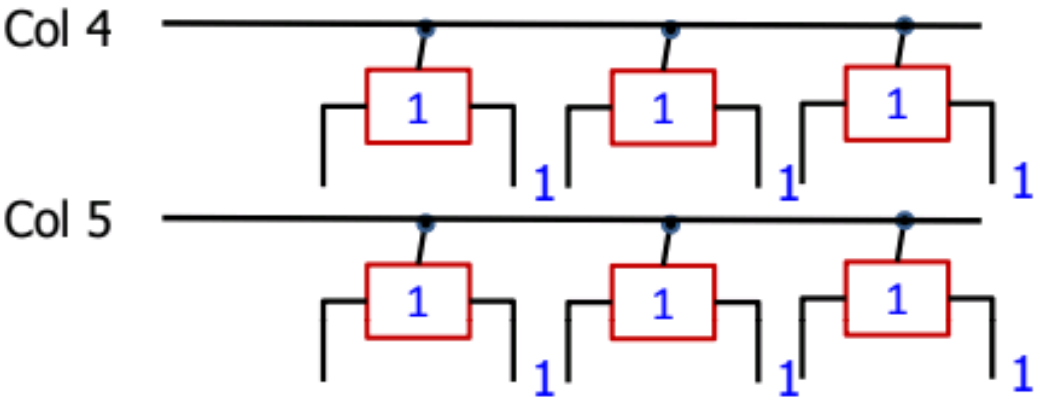


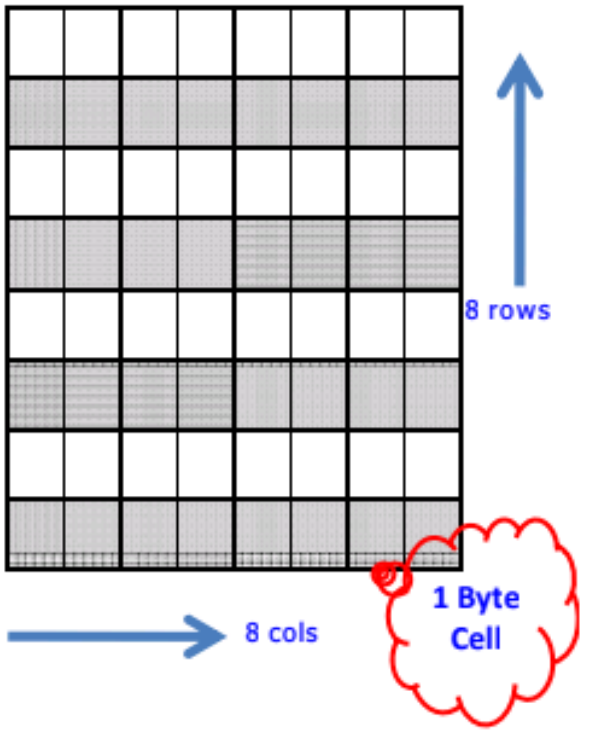
Using CMOS Inverters

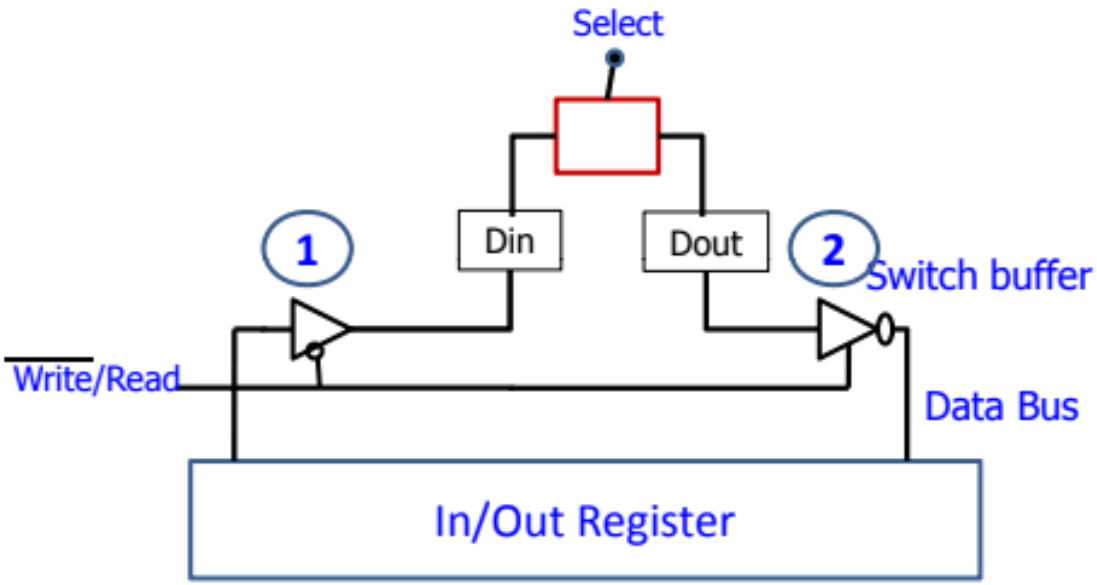
Types of ROM

- **Programmable read-only memory (PROM)**
  - Semiconductor memory whose contents are set at once.
  - The writing process is performed electrically and performed by the user at a time of original chip fabrication
  - Needs special equipment to program
  - Read "mostly" – read operations are far more frequent than write operations but for which non-volatile storage is required
- **Erasable Programmable (EPROM)**
  - Read and write electrically, as with PROM
  - Before writing**, all storage cells must be erased by ultraviolet (UV) radiation**. [20 minutes take to erase]
  - EPROM is more expensive than PROM but it has advantage of multiple update capability.
- **Electrically Erasable (EEPROM)**
  - Can be written into anytime without erasing whole contents; only byte or bytes addressed are updated
  - Takes much longer to write than read
  - EEPROM has advantage of non-volatility with flexibility of being updatable
  - More expensive than EPROM and also less dense (supporting fewer bits per cheap)
- **Flash memory**
  - Erase whole memory or a section (block) electrically within one or a few seconds (in a single action or "**flash**"), which is **much faster than EPROM but slower than EEPROM** but achieves highest density (1 transistor/bit)

SRAM – Read/Write operation

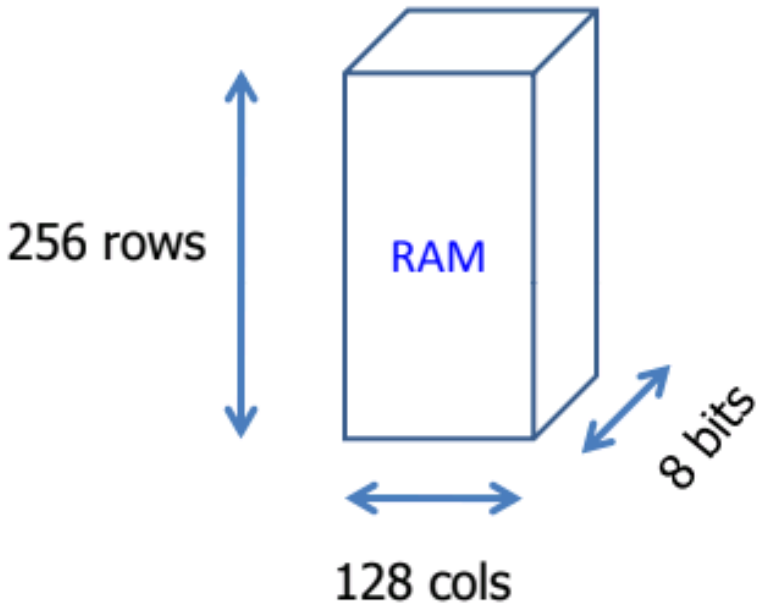






Write	Read
W'/R =0	W'/R=1
1 Enable 2 Disable	1 Disable 2 Enable

32K X 8 RAM

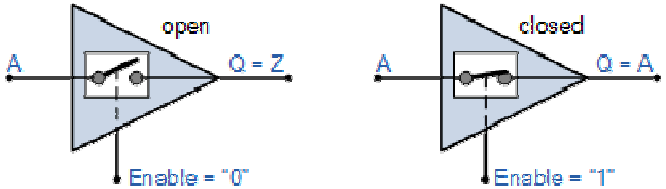


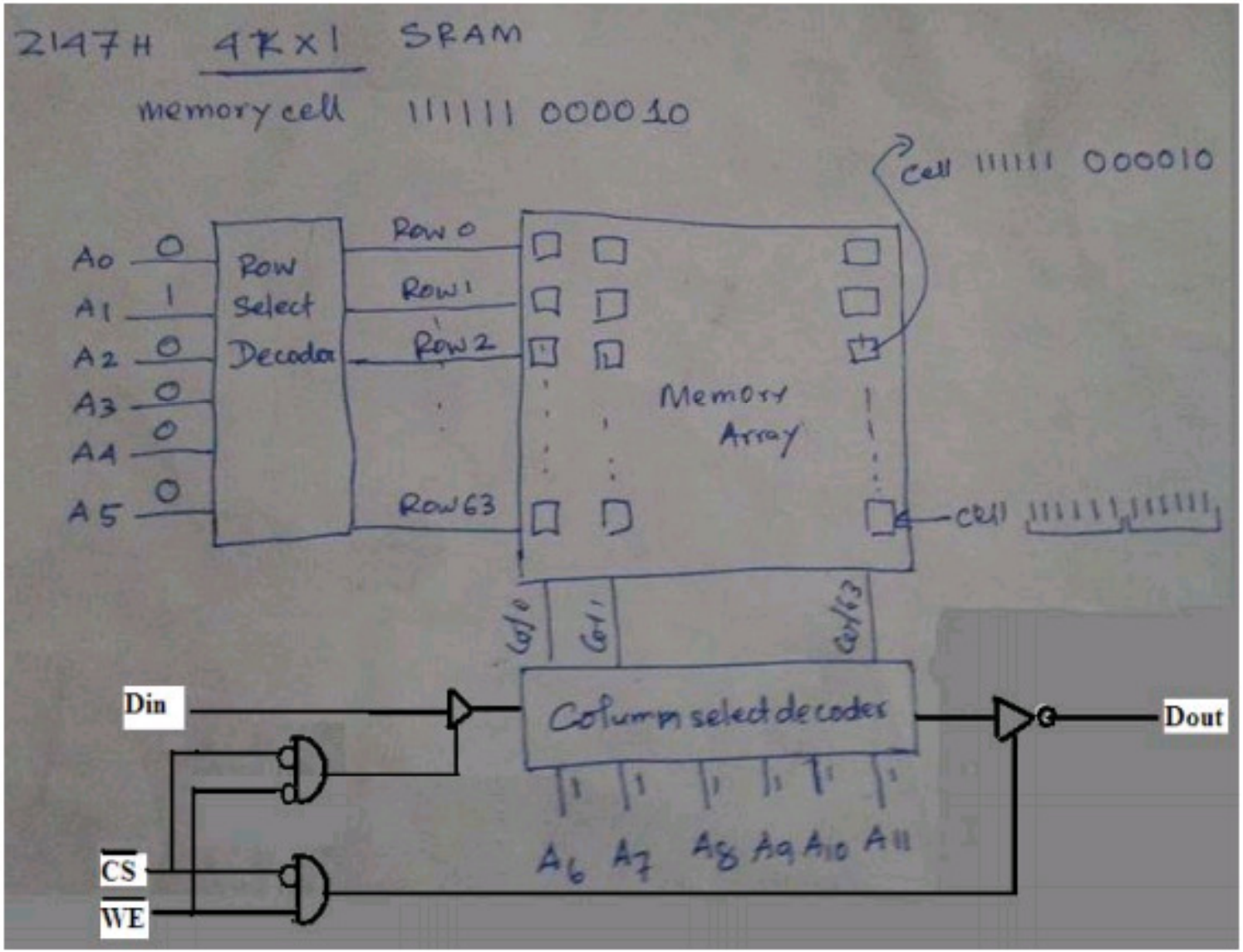
256x128=32768 cells

=32KB

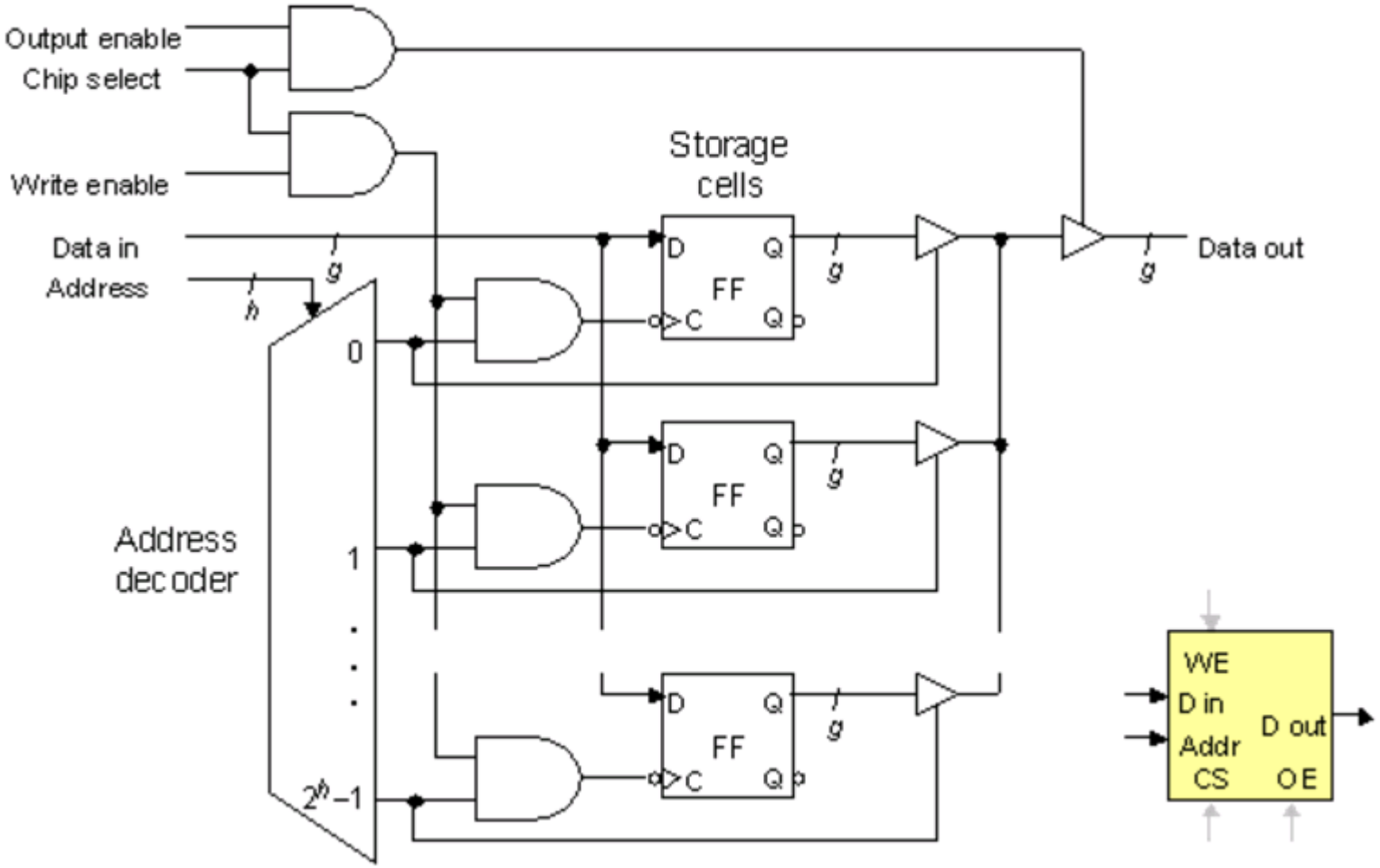
=32K X 8 bits
= 262,144 bits

4k x 1 SRAM


open
A
Q = Z
Enable = "0"
closed
A
Q = A
Enable = "1"


2147H 4K x 1 SRAM
memory cell 111111 000010
Cell 111111 000010
A0
A1
A2
A3
A4
A5
Row Select Decoder
Row 0
Row 1
Row 2
Row 63
Memory Array
Cell
Col 0
Col 1
Col 63
Din
Column select decoder
Dout
CS
WE
A6 A7 A8 A9 A10 A11

Conceptual inner structure of a 2^h x g SRAM chip and its shorthand represantation



Multiple-Chip SRAM

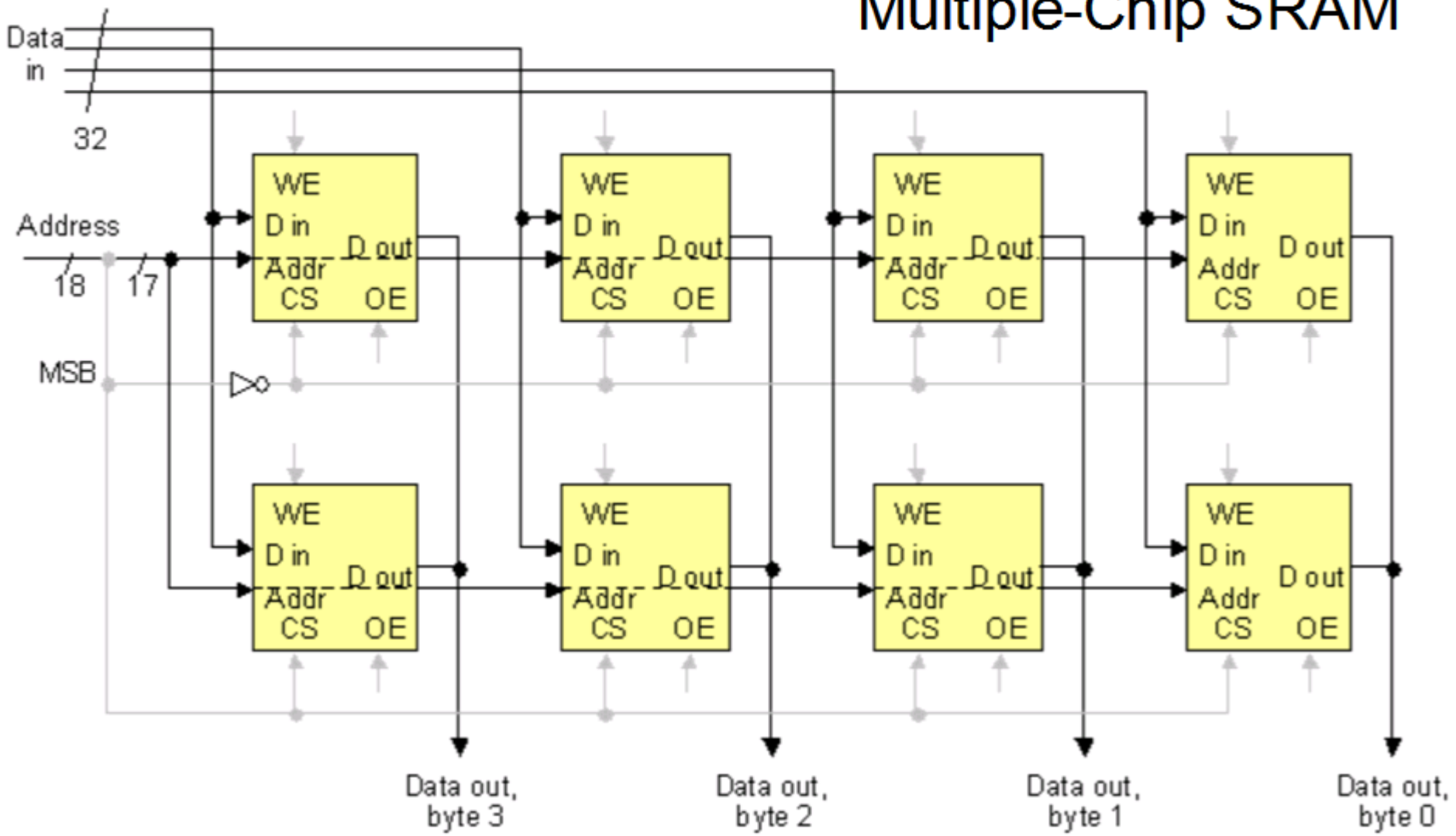
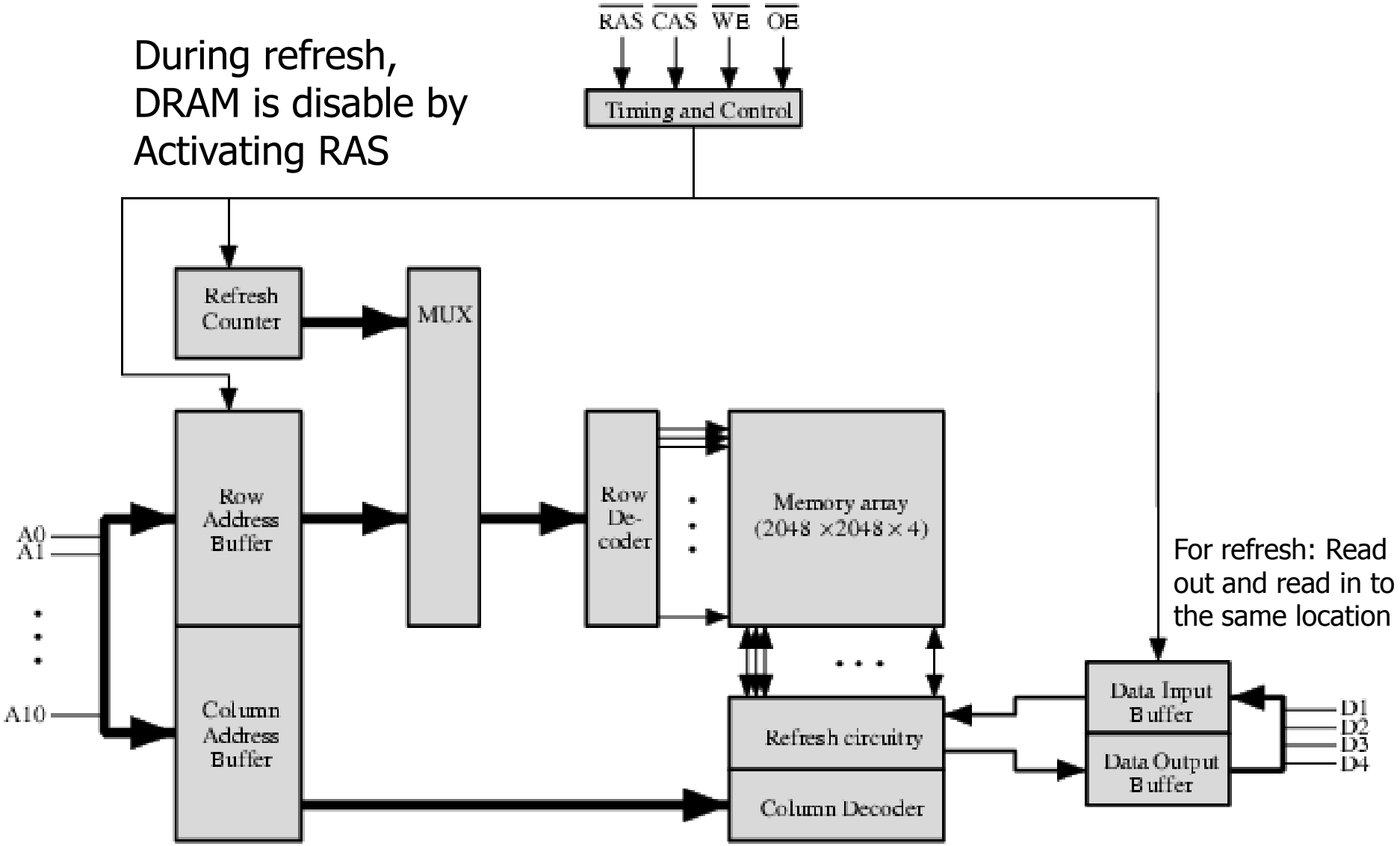


Fig. 17.2 Eight 128K × 8 SRAM chips forming a 256K × 32 memory unit.

Typical 16 Mb DRAM (4M x 4)

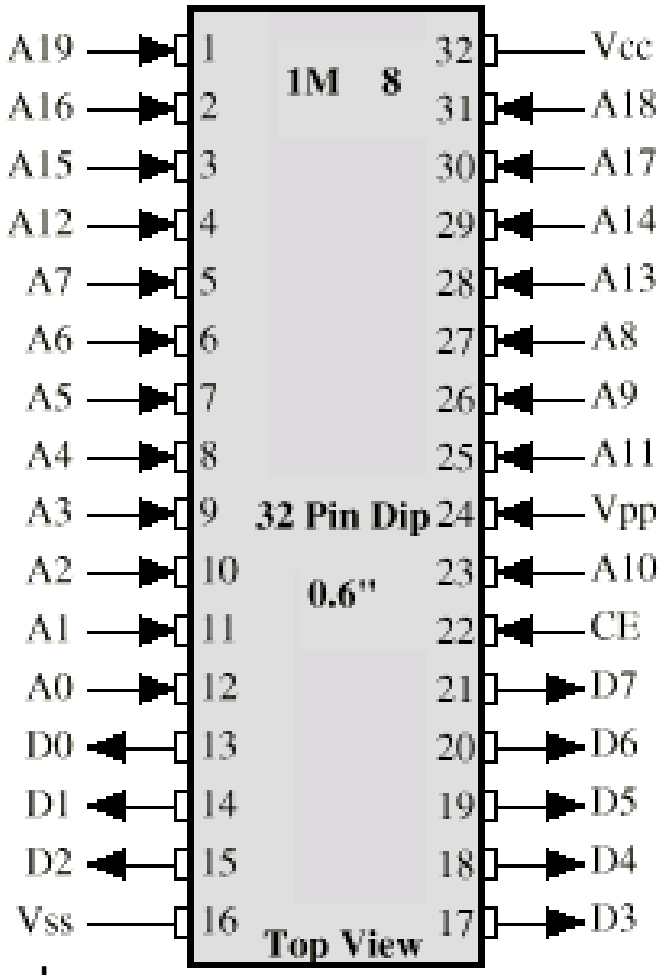
During refresh, DRAM is disable by Activating RAS



For refresh: Read out and read in to the same location

Chip Packaging- IC

consists pins for connection to the outside world



power

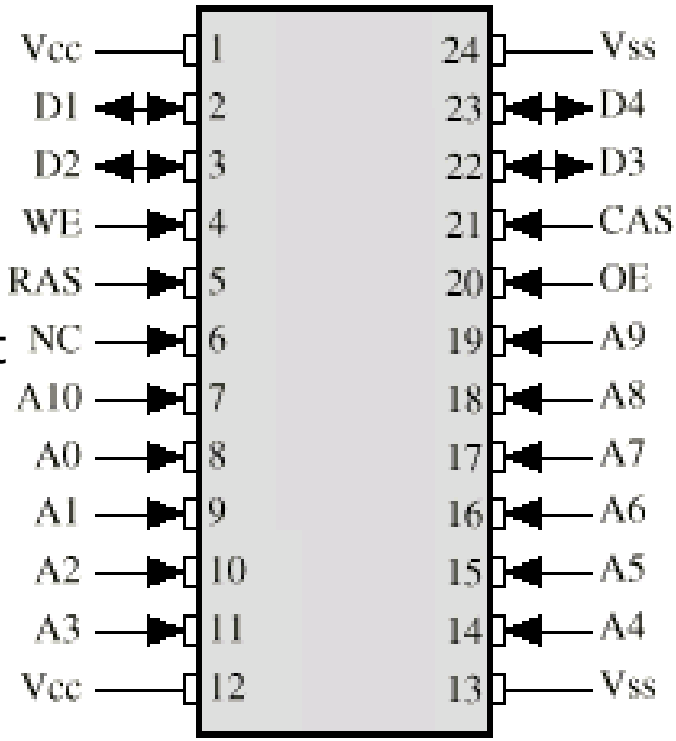
Write Enable

No Connect

Program voltage

ground

(a) 8 Mbit EPROM



Output Enable

Multiplexed Address line (row, col)

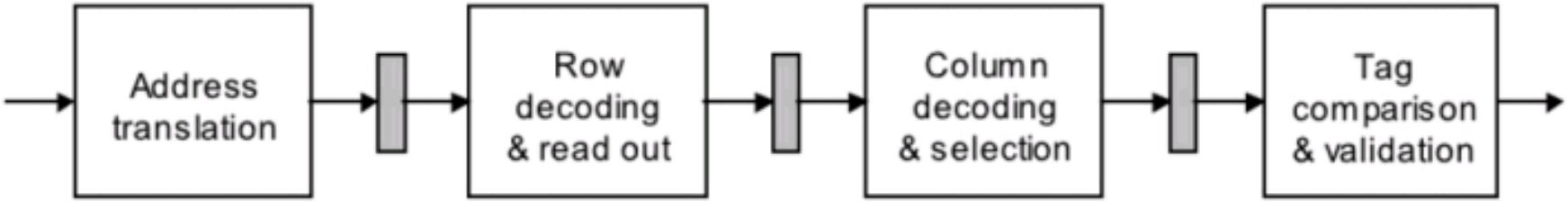
(b) 16 Mbit DRAM

1Mx 8 bit = 2^{20} x 8 bit

4 M x 4 bits

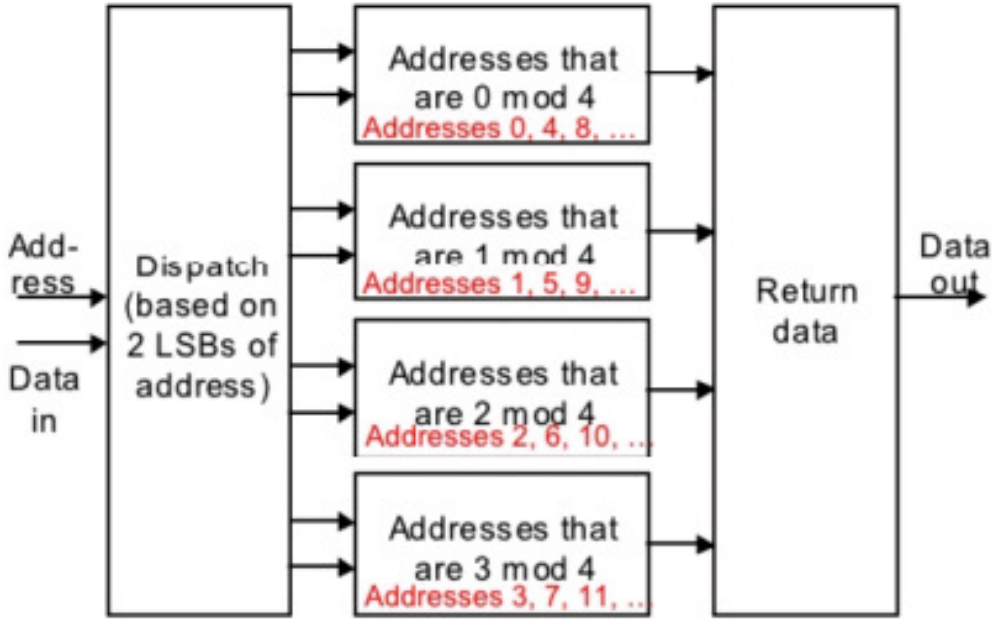
Pipelined and Interleaved Memory

- Simple memory units-> sequential accesses (one at a time)
- How about memory with multiports?
- How can we increase memory throughput? -> more data can access at once

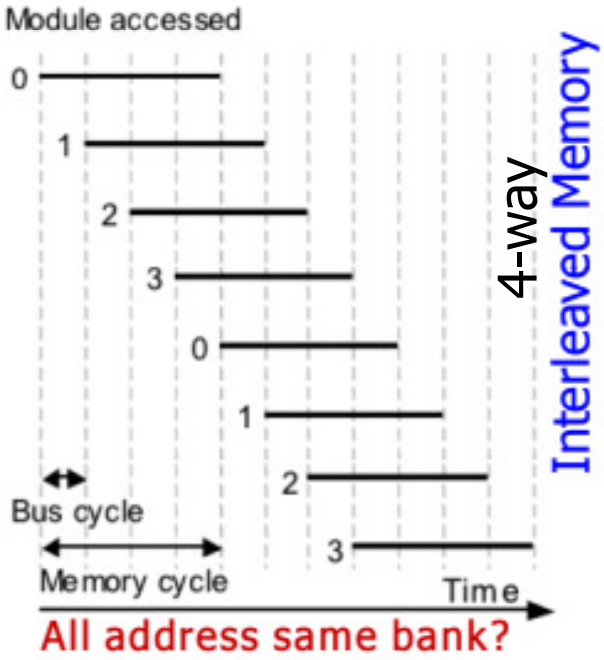


Pipelined Cache memory/ Memory

Incase memory no tag comparison



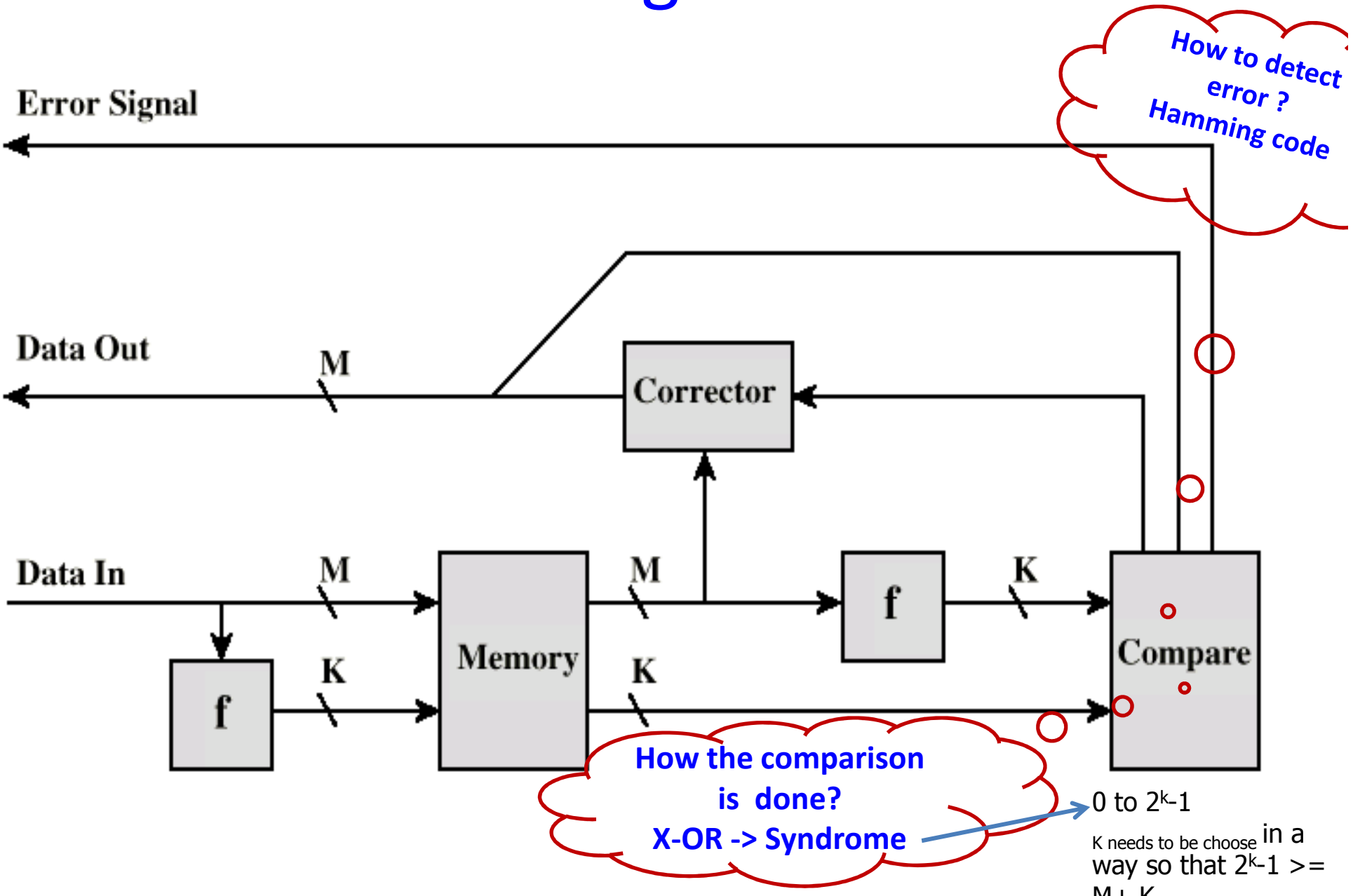
Memory Bank



All address same bank?

Consecutive words of memory are stored in diff[n] banks, transfer of a block of memory is speed up

Error Correcting Code Function



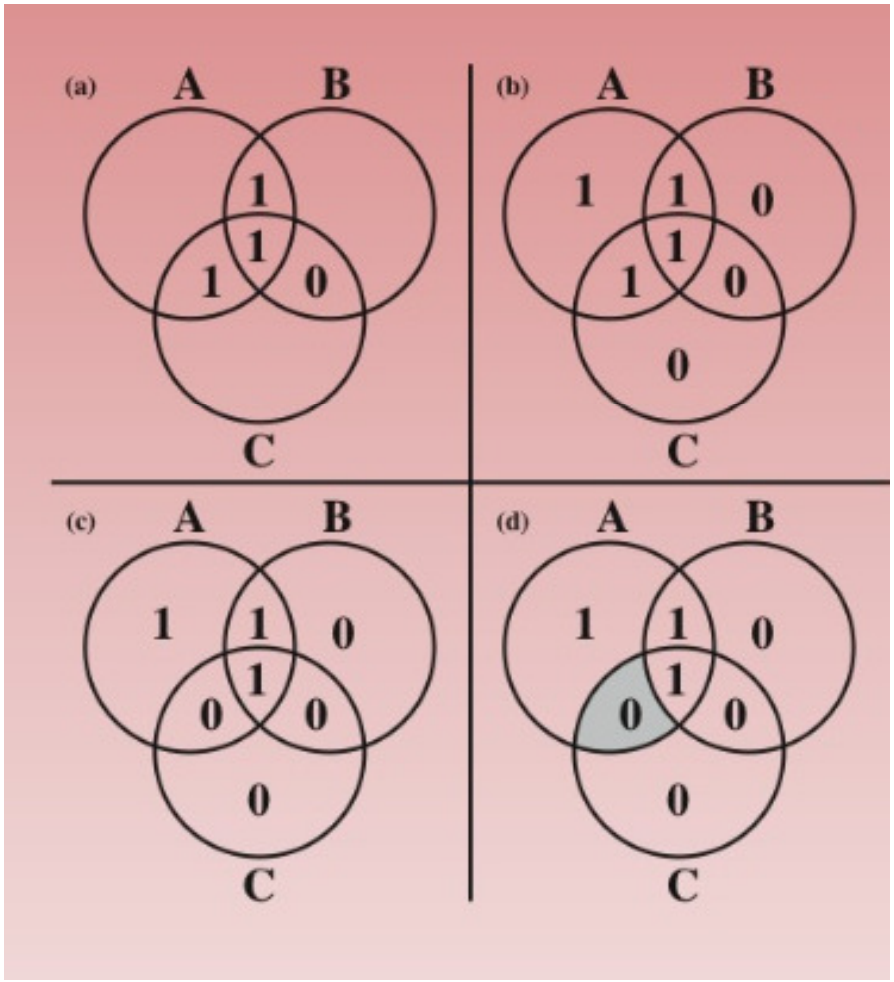
Hamming Code

- 4 bits Words (M=4)
- Choosing Parity bit=1/0
  - so that total # of 1 in circle is **even**

How many k bits for total M bit data that $2^k-1 >= M+ K$

M	K	
8	3	$2^3-1 < M+ K$
8	4	$2^4-1 >= M+ K$, 4 bits OK

Venn Diagrams



Discrepancies in A and C but not in B

Layout of Data Bits and Check Bits

Bit Position	12	11	10	9	8	7	6	5	4	3	2	1
Position Number	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001
Data Bit	D8	D7	D6	D5		D4	D3	D2		D1		
Check Bit					C8				C4		C2	C1

Single-Error-Correcting (SEC) Example

- 8 bits input- 0 0 1 1 1 0 0 1
- Check bits Calculation:
- C1=D1 ⊕ D2 ⊕ D4 ⊕D5 ⊕D7
- = 1 ⊕ 0 ⊕ 1 ⊕ 1 ⊕ 0 =1
- C2= D1 ⊕ D3 ⊕D4 ⊕D6 ⊕D7
- =1 ⊕ 0 ⊕ 1 ⊕ 1 ⊕ 0 =1
- C4= D2 ⊕D3 ⊕D4 ⊕D8
- = 0 ⊕ 0 ⊕ 1 ⊕ 0 =1
- C8=D5 ⊕D6 ⊕D7 ⊕D8
- = 1 ⊕ 1 ⊕ 0 ⊕ 0 =0
- C1=1, C2=1, C4=1, C8=0

- 8 bits input- 0 0 1 1 1 **1** 0 1
- Check bits Calculation:
- C1=D1 ⊕ D2 ⊕ D4 ⊕D5 ⊕D7
- = 1 ⊕ 0 ⊕ 1 ⊕ 1 ⊕ 0 =1
- C2= D1 ⊕ D3 ⊕D4 ⊕D6 ⊕D7
- =1 ⊕ 1 ⊕ 1 ⊕ 1 ⊕ 0 =0
- C4= D2 ⊕D3 ⊕D4 ⊕D8
- = 0 ⊕ 1 ⊕ 1 ⊕ 0 =0
- C8=D5 ⊕D6 ⊕D7 ⊕D8
- = 1 ⊕ 1 ⊕ 0 ⊕ 0 =0
- C1=1, C2=0, C4=0, C8=0

	C8	C4	C2	C1
	0	1	1	1
⊕	0	0	0	1
	0	**1**	**1**	**0**

6 # bit has error