EAST WEST UNIVERSITY BANGLADESH
Department of Computer Science & Engineering

CSE360: Computer Architecture

Term II Examination **Fall 2014**

Total Marks: 40 | Instructor: Dr. Md. Shamim Akhter | Time: 90 minutes

PART: A (20)

Consider the **single-cycle** and **multi-cycle** implementations (for your reference the datapaths for the single-cycle and the multi-cycle are provided on the last page).

1. Why does the **single-cycle implementation** use more hardware resources than the **multi-cycle implementation**? (3)

2. Answer the following questions for the **single-cycle implementation**:

   a) The **MemWrite** signal must be set to 1 for one particular supported instruction. Describe what could go wrong if it was set to 1 for any of the other instructions. (2)

   b) For which of the supported MIPS assembly instruction(s) must set 1 for the select line, **MemtoReg**? Explain why. (2)

   c) For which of the supported MIPS assembly instruction(s) is (are) the **Shift-Left-2** unit necessary? Explain why? (2)

3. Suppose each stage of the instruction takes the following times:
   IF = 7 ns, ID = 8 ns, EX = 15 ns, MA = 10 ns, WB = 8 ns

   a) What is the cycle time for the **single-cycle implementation**? Explain. (2)

   b) What is the cycle time for the **multi-cycle implementation**? Explain. (2)

4. Given the below MIPS assembly code, answer the following questions. *Assume the mul is as fast as an add and a blt is the same as a beq.*

```
loop:   lw    $t0, 0($a0)
        mul   $t0, $t0, $a3
        sw    $t0, 0($a1)
        add   $a0, $a0, 4
```

```
add    $a1, $a1, 4
add    $t1, $t1, 1
beq    $t1, $t2, loop
```

a) How many cycles would one iteration of this loop take to execute on the **single-cycle datapath**? (2)

b) How many cycles would one iteration take on the **multi-cycle datapath**? (2)

c) What is going on during the **12th cycle** of execution (in multi-cycle datapath)? (3)

PART: B (10)

Consider the **single-cycle implementations** (for your reference the single-cycle datapath is provided on the last page).

1. Write the procedure to generate **ALU (3 bit) control signals**. (2)

2. List the value of the **control signals** associated with the following instructions: (8)

Instructions	Reg Dst	ALU Src	MemtoReg	RegWrite	MemRead	MemWrite	ALU OP1	ALU OP0
sw $t0,0($t1)								
add $t1, $t2, $t3								
lw $t1, 4($t2)								
beq $t1, $t2, Label								

PART: C (10)

1. Suppose we have two implementations of the same instruction set architecture (ISA). For some program: **machine A** has a clock cycle time of 10 ns and a CPI of 2.0, **machine B** has a clock cycle time of 20 ns and a CPI of 1.2. Which machine is faster for this program, and by how much? (5)

2. Suppose a machine- M1 contains same instruction set. The following given table contains information regarding four classes of instructions (R-type, Load, Store and Branch) with their average number of cycles and frequency.(5)

Op	Freq	CPI_i	Freq x CPI_i
R-Type	50%	1	
Load	20%	5	
Store	10%	3	
Branch	20%	2	
Overall effective CPI			Σ =

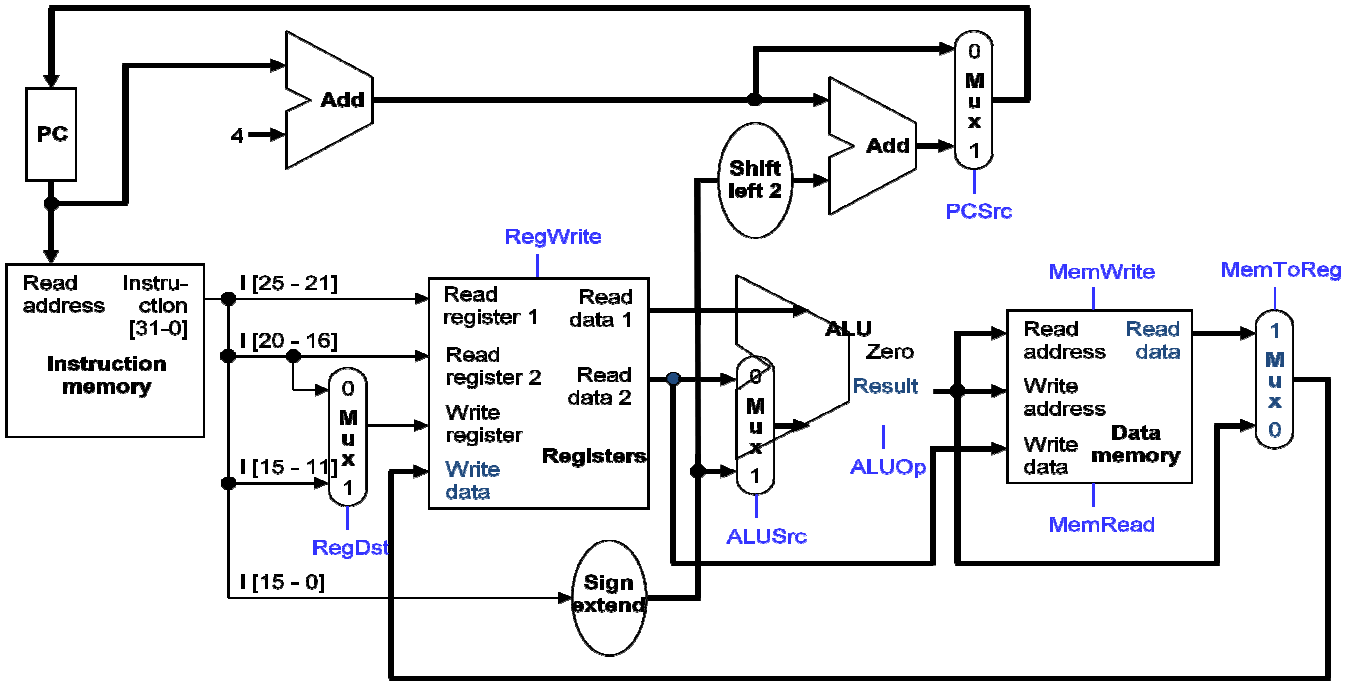
a) Generate the **Overall effective CPI**.

b) How much faster would the machine be if a better data cache reduced **the average load time** to 2 cycles?

c) How does this compare with using branch prediction to **save a cycle off the branch time**?

d) What if **two R-Type instructions** could be executed at once?

Single Cycle Datapath:



Multi-Cycle Datapath: