

# Andromeda XZU65 Module

## Reference Design for Andromeda PE5 Base Board User Manual

### Purpose

The purpose of this document is to present to the user the overall view of the Andromeda XZU65 module reference design and to provide the user with a step-by-step guide to the complete AMD® MPSoC design flow used for the Andromeda XZU65 module.

### Summary

This document gives an overview of the Andromeda XZU65 module reference design and then guides through the complete AMD MPSoC design flow for the Andromeda XZU65 module in the getting started section. In addition, the internals and the boot options of the Andromeda XZU65 module reference design are described.

Product Information	Code	Name
Module	AM-XZU65	Andromeda XZU65 Module
Baseboard	AM-PE5	Andromeda PE5 Base Board

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# 1 Overview

## 1.1 Introduction

The Andromeda XZU65 module reference design demonstrates a system using the Andromeda XZU65 module in combination with the Andromeda PE5 base board. It presents the basic configuration of the device and contains a getting started tutorial.

A troubleshooting section is included at the end of the document to help users resolve potential issues related to board connectivity and system functionality.

This reference design does not include any source code for software examples. Instead, Enclustra provides application notes [6] for selected applications.

An introduction to the AMD tools is available online:

- Vivado Design Suite User Guide [9]
- Vitis Unified Software Platform Documentation [11]
- Embedded Design Tutorials [12]
- Zynq Ultrascale+ MPSoC Embedded Design Tutorial [15]

More information on the module and the base board can be found in the Andromeda XZU65 Module User Manual [2] and the Andromeda PE5 Base Board User Manual [3]. The following directory structure applies to the reference design:

Directory	Description
doc	Reference design documentation
scripts	Scripts directory required for project creation and settings
src	Design pinout, timing constraints and VHDL source code directory

Table 1: Directory Structure

## 1.2 Variables Paths

The following variables are used to substitute the full path to directories relevant for the reference design build process. Paths not already present in the reference design directory will be created during the build process.

Variable	Full Path	Description
<base_dir>	<base_dir>/reference_design	Reference design root directory as described in Table 1
<vivado_dir>	<base_dir>/reference_design/Vivado/<module_name>	Vivado project directory

Table 2: Path Variables

## 1.3 Prerequisites

- IT infrastructure
  - Computer with a microSD card slot (optional<sup>1</sup>)
  - Supported OS<sup>2</sup>
- Software
  - AMD Vitis 2024.2 Core Development Kit
  - Enclustra Module Configuration Tool (MCT) [\[4\]](#) (optional<sup>3</sup>)
  - a terminal emulation program, for example, Tera Term
- Hardware
  - Enclustra Andromeda XZU65 module
  - Enclustra Andromeda PE5 base board
- Accessories
  - 12 V DC power supply
  - microSD card (optional<sup>1</sup>)
  - USB-C cable

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<sup>1</sup>Only required for SD card boot mode.

<sup>2</sup>A comprehensive list of supported operating systems is given in the Vivado Design Suite Installation Guide [\[10\]](#).

<sup>3</sup>May be used for MPSoC device configuration or for FTDI configuration.

## 2 Reference Design Description

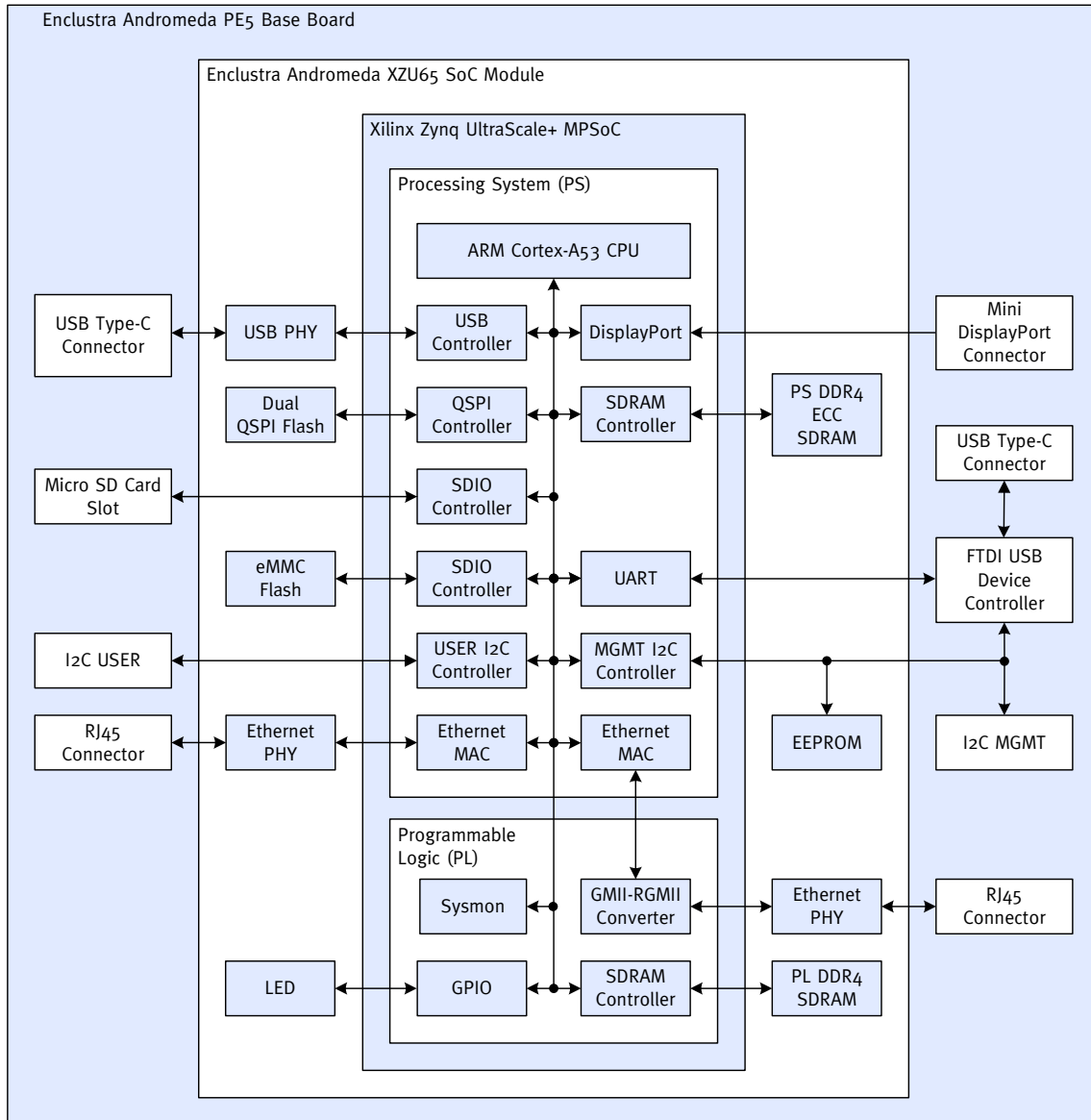


Figure 1: Hardware block diagram

### 2.1 Processing System (PS)

#### 2.1.1 Clocks

The PS input clock frequency is configured to 33.33 MHz. The CPU clock frequency is configured to its corresponding maximum APU clock frequency, as specified in the Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics [14]. The maximum CPU (APU) clock performance depends on the device speed grade and package.

A 50 MHz clock and a 100 MHz clock are exported from the PS to the PL. These clocks can be modified

in the settings of the PS in the Vivado block design.

### 2.1.2 DDR4 SDRAM

The DDR4 SDRAM memory is configured as specified in the Andromeda XZU65 Module User Manual [2]. ECC is enabled on product models with ECC support. The DDR configuration can be modified in the settings of the processing system in Vivado.

### 2.1.3 microSD Card

The SD1 controller is mapped to MIO[39, 46:51]. This enables microSD card access and booting from the microSD card. In order to boot from a microSD card the configuration DIP switches on the base board must be set according to Section 4.3.2.

### 2.1.4 eMMC

The SD0 controller is mapped to MIO[13:22]. This enables eMMC device access and booting from the eMMC device. In order to boot from eMMC the configuration DIP switches on the base board must be set according to Section 4.4.3.

### 2.1.5 I2C

The I2C0 controller is mapped to MIO[30:31]. It is connected to the I2C MGMT bus on the base board. The I2C1 controller is mapped to MIO[24:25]. It is connected to the I2C USER bus on the base board. The available I2C devices on each bus are listed in the Andromeda XZU65 Module User Manual [2] and the Andromeda PE5 Base Board User Manual [3].

### 2.1.6 Quad SPI Flash Controller

The quad SPI flash controller is mapped to MIO[0:12] in dual parallel mode. In order to boot from the QSPI flash the configuration DIP switches on the base board must be set according to Section 4.2.2. Refer to the Andromeda XZU65 Module User Manual [2] for details about flash programming and usage.

### 2.1.7 UART

The UART0 controller is mapped to MIO[26:27] and connected to the FTDI USB device controller on the base board. The UART is configured as shown in Table 3.

Parameter	Value
Baud rate	115'200 Bd
Data width	8 bit
Parity	None
Stop	1 bit
Flow control	None

Table 3: UART configuration



### 2.1.8 Ethernet

The Ethernet MAC GEM3 controller is mapped to MIO[64:75] and the GEM1 controller is mapped to EMIO pins. Each interface is connected to a Microchip KSZ9131 RGMII Ethernet PHY on the module. The PHYs are on separate MDIO busses. The PS MDIO is mapped to MIO[76:77]. The other interface is routed to PL pins. The PHYs can be configured via the MDIO interface on address 3 (GEM3) and address 7 (GEM1).

#### Tip

The RGMII delays need to be configured before the Ethernet interface can be used. Further details on PHY delay configuration are given in the Enclustra Gigabit Ethernet Application Note [6].

### 2.1.9 USB

The USB controller USB0 is mapped to MIO[52:63]. It is connected to a USB3320C USB2.0 PHY on the module. This interface can be configured in USB host, USB device and USB On-The-Go (OTG) mode. The GTR configuration for USB 3.0 is given in Section 2.1.13.

### 2.1.10 GPIOs

The unused MIO pins are available as GPIOs. For details on the I/O assignment, refer to the Andromeda XZU65 Module User Manual [2], Section "Multiplexed I/O (MIO) Pins". For details on the combination of the I/O assignment with the base board, refer to the Andromeda PE5 Base Board User Manual [3].

### 2.1.11 Status LEDs

The module has two status LEDs labeled **E** and **S**. Refer to the Andromeda XZU65 Module User Manual [2], Section "Top and Bottom Views" for the exact location. Both LEDs should be off when booting from a device containing a suitable boot image. The **E** LED will turn on when no bootable image can be loaded. This might indicate a problem with either the boot image or the boot mode settings. Refer to Section 4 for boot image generation and valid boot mode settings.

### 2.1.12 DisplayPort

The AUX channel of the DisplayPort is mapped to MIO[34:37]. The GTR configuration is given in Section 2.1.13.

### 2.1.13 GTR Settings

The GTR configuration is given in Table 4.

Lane Number	Function	Reference Clock Number	Reference Clock Frequency [MHz]
0	DP Lane 1	3	135
1	DP Lane 0	3	135
2	USB0 3.0	2	100
3	unused	-	-

Table 4: PS GTR Configuration

## 2.2 Programmable Logic (PL)

### 2.2.1 DDR4 SDRAM

The DDR4 SDRAM memory in the PL is configured as specified in the Andromeda XZU65 Module User Manual [2]. The maximum DDR performance depends on the device speed grade, the package, the VCC\_INT voltage and the memory chips equipped on the module. The DDR clock frequency can be modified in the settings of the Memory Interface Generator (MIG) IP core in Vivado.

### 2.2.2 Ethernet

The Ethernet MAC GEM1 is mapped to EMIO pins providing a GMII interface to the PL. This PHY can be configured via the MDIO interface on PHY address 7. The GMII-to-RGMII converter IP core is provided as-is without further documentation or source files.

### 2.2.3 LEDs and GPIOs

The PL firmware contains a 24-bit counter freely running at 50 MHz. The MSB of this counter is used to blink XZU65\_LED0\_N with a frequency of approximately 3 Hz. The pin mapping is given in Table 5.

Pin	Signal	Function
AD20	XZU65_LED0_N	Blinking LED counter MSB

Table 5: PL Blinking LED Configuration

In addition, the block design instantiates an AXI GPIO IP block to control the LEDs described in Table 6.

PL Pin	Signal	Function
AE20	XZU65_LED1_N	GPIO 1
AK20	XZU65_LED2_N	GPIO 2
AJ21	XZU65_LED3_N	GPIO 3

Table 6: PL AXI GPIO Configuration

### 2.2.4 System Management

A System Management IP core instance is connected via AXI bus to the PS in order to monitor the temperature of the device. The temperature threshold for the FPGA is configured to its maximum allowed temperature. The constraints provided in the reference design enable FPGA bitstream power-down when the temperature increases above the threshold. In this case, the PL will be reset while the ARM processor will still be running.

## 3 Getting Started

This section describes the steps required to configure the Andromeda XZU65 module and the Andromeda PE5 base board in order to run a simple HelloWorld application example:

1. Install the module and configure the base board.
2. Generate the bitstream.
3. Prepare the software workspace.
4. Run a software application.

Read the Andromeda XZU65 Module User Manual [2] and the Andromeda PE5 Base Board User Manual [3] carefully before proceeding.

### 3.1 Essential Information

Pre-generated binaries may be used instead of building them manually as described in the following sections. The binaries for any supported XZU65 product model and boot mode are released on the reference design Github release page [5].

#### Tip

Workarounds and fixes for potential issues can be found in Section 5.

#### NOTICE



##### Damage to the device due to overheating

Depending on the user application, the Andromeda XZU65 module may consume more power than can be dissipated without additional cooling measures.

- Ensure that the MPSoC is always adequately cooled by installing a heat sink and/or providing air flow.

### 3.2 Setting up the Hardware

#### NOTICE



##### Damage to the device when mounting or removing the module

Mounting or removing the module while the base board is powered can lead to damage to the module or the base board.

- Ensure that the base board is not powered before mounting or removing the module.

The assembly drawing of the Andromeda PE5 base board is shown in Figure 2. The relevant interfaces are marked in red in the figure as well as in the instructions below.



- (g) Click **Set device mode**.
- (h) Wait for completion.
- (i) Close MCT.
- (j) Disconnect and reconnect the USB-C cable.

#### Tip

Alternatively, an AMD JTAG USB programmer can be used. Connect the JTAG signals to the JTAG connector on the base board.

- 9. Four new serial ports should be detected by the OS (or three if FTDI is configured in Xilinx JTAG mode).
- 10. Open the serial port with the second highest number of the newly detected ports and configure it using the parameters specified in Section 2.1.7. Any suitable utility for establishing a serial connection can be used
- 11. The output of the HelloWorld application will be printed in this terminal after running a software application, as presented in Section 3.4.4.

## 3.3 Generating the FPGA Bitstream

Follow the steps described in this section to generate the reference design bitstream manually. Refer to the troubleshooting section 5.1 in case of problems.

#### Tip

Pre-generated bitstreams for all supported XZU65 product models are available on the XZU65 reference design Github release page [5]. These can be used directly instead of generating the bitstream manually. If using those files directly, the bitstream does not need to be generated manually and this section can be skipped.

1. Configure the `<base_dir>/reference_design/scripts/settings.tcl` file:
  - (a) Set the `module_name` variable to the desired product model<sup>4</sup>.
  - (b) Save the file after editing<sup>5</sup>.
2. Start AMD Vivado 2024.2.
3. Create the Andromeda XZU65 module reference design project:
  - (a) Click on the **Tcl Console** at the bottom of the Vivado window.
    - i. Type `cd {<base_dir>/reference_design}`  
Note the curly brackets around the path.
    - ii. Type `source ./scripts/create_project.tcl`
    - iii. Wait for completion (the created project opens automatically).
4. Compile the design and generate the programming files:
  - (a) Click on **Generate Bitstream**.
  - (b) Click **Yes** in the next window.
  - (c) Click **Launch runs on local host** with the default number of jobs. This will run all design steps from synthesis to implementation and bitstream generation.
  - (d) Wait for completion.
  - (e) Select **View Reports** and click **OK**.
5. Export the hardware platform:
  - (a) Select **File > Export > Export Hardware...**
  - (b) Click **Next**.
  - (c) Select **Include bitstream** and click **Next**.
  - (d) Leave the default settings and click **Next**.

<sup>4</sup>Valid values for the variables are listed at the beginning of the file.

<sup>5</sup>The Vivado project directory can be set to a custom value by adjusting the `<vivado_dir>` variable. However, the documentation assumes that the default path is used.

(e) Click **Finish**.

The build output is located in `<base_dir>/reference_design/Vivado/<module_name>` and is described in Table 7:

File	Description
Andromeda_XZU65_PE5.xsa	Handoff file for the Vitis IDE
Andromeda_XZU65_PE5.runs/impl_1/Andromeda_XZU65_PE5.bit	Generated bitstream

Table 7: Vivado Programming Files

## 3.4 Preparing the Boot Binaries

This section describes the whole build flow for generating a bootable binary image file. The AMD Vitis IDE 2024.2 is used in the following sections.

### Tip

Pre-generated binaries for all supported XZU65 product models are available on the reference design Github release page [5]. These can be used directly instead of generating the binaries manually. In this case, the following section can be skipped.

### 3.4.1 Preparing the Vitis Workspace

Follow these steps to create a new workspace:

1. Create an empty folder for the workspace.
2. Open the AMD Vitis IDE 2024.2:
  - (a) Click **Set Workspace**.
  - (b) Select the previously created empty folder for the Vitis workspace and click **OK**.

The workspace setup for the HelloWorld application is complete.

### 3.4.2 Creating the Hardware Platform

Add a new hardware platform to the workspace created in Section 3.4.1:

1. In the **Welcome** splash screen, select **Create Platform Component**.
2. Use `Andromeda_XZU65_PE5` as the **Component name**.
3. Select the workspace folder as the **Component location**.
4. Click **Next**.
5. Choose **Hardware Design**.
6. Click **Browse** and select the XSA file generated in Section 3.3.
7. Click **Next**.
8. Wait for completion on the next screen. **Operating system** and **Processor** should be filled automatically.
9. Ensure that **Generate Boot artifacts** is enabled.
10. Click **Next**.
11. In the summary screen, click **Finish**.
12. Wait until Vitis has completed all tasks and the created platform is available in the **Vitis Components** window.
13. In the **Flow** window, click **Build**.
14. Wait for completion.

The hardware platform for running bare-metal applications on the Andromeda XZU65 module is ready. The FSBL is located in the <workspace>/Andromeda\_XZU65\_PE5/export/Andromeda\_XZU65\_PE5/sw/boot directory (Table 8):

File	Description
fsbl.elf	Bootloader

Table 8: Vitis Platform Output

### 3.4.3 Building the HelloWorld Application

Create a new application from a template and build it by following these steps:

1. Select **View > Examples > Hello World**.
2. Click **Create Application Component from Template**.
3. Select HelloWorld for the **Component name** and click **Next**.
4. Select the platform created in Section 3.4.2 and click **Next**.
5. Leave the default settings and click **Next**.
6. Click **Finish**.
7. In the **Flow** window, click **Build**.
8. Wait for completion.

The build output is located in <workspace>/HelloWorld/build/ and is described in Table 9:

File	Description
HelloWorld.elf	Executable bare-metal application file

Table 9: Vitis Application Build Output

### 3.4.4 Running Software Applications

This section describes how to run software applications.

1. Start AMD Vitis 2024.2.
2. Open the workspace created in Section 3.4.1.
3. In the **Vitis Components** window, select the HelloWorld application project.
4. Prepare the run configuration:
  - (a) In the **Flow** window, click the gear icon on the right side while hovering over the **Run** button.
  - (b) Use HelloWorld as the **Launch Config Name**.
  - (c) Select **TCL** for **Board initialization**.
  - (d) Enable **PL Powerup**.
5. Ensure that the hardware setup is done according to Section 3.2.
6. Click the **Run** button.

The expected output in the serial terminal console is given in Figure 6. For troubleshooting refer to Section 5.2.

```
Hello World
Successfully ran Hello World application
```

Figure 3: Example of the Terminal Output for the HelloWorld Application

## 4 Boot Configurations

A boot image can be created containing the previously generated binaries to enable booting from various boot modes. The boot image contains the bootloader, the bitstream for programming the FPGA logic and the software bare-metal application.

### Tip

Pre-generated images may be used for booting instead of rebuilding the image. The binaries for any supported XZU65 product model and boot mode are released on the reference design Github release page [5].

### 4.1 Generating the Image File

This section describes how to generate a boot image for the Andromeda XZU65 module using the AMD Vitis IDE. The workspace, hardware platform and application from Sections 3.4.1, 3.4.2 and 3.4.3 are used. To create a bootable image file in the AMD Vitis IDE, follow these steps:

1. In the **Flow** window, click **Create Boot Image**.
2. Click **Browse** next to **Output BIF File Path\***.
3. Create a new folder called `output`.
4. Rename the `.bif` file to `HelloWorld.bif` and click **Save**.
5. The **Output Image\*** path should point to the `output` folder automatically.
6. Click **Create Image**.

The build output is located in the previously created output folder and is described in Table 10. The `BOOT.BIN` file is the same for all boot modes.

File	Description
<code>BOOT.BIN</code>	Bootable image containing the HelloWorld application
<code>HelloWorld.bif</code>	Source file describing the individual components of the boot image

Table 10: Boot Image

### 4.2 QSPI Flash Boot

#### 4.2.1 Programming the QSPI Flash

There are several ways of programming the QSPI flash memory with the `BOOT.BIN` created in Section 4.1. Only **one** method needs to be followed in order to program the QSPI flash.

#### JTAG Boot Mode

Programming flash memory devices such as QSPI or eMMC using Vivado or Vitis requires setting the JTAG boot mode first. Set the DIP switch on the Andromeda PE5 base board as follows:

- `BOOT` = [1: OFF, 2: OFF, 3: OFF, 4: OFF]

After setting the JTAG boot mode, follow the steps described in the Vitis section or the Vivado section below.



## Vitis

In order to program the QSPI flash using Vitis, follow these steps:

1. In Vitis, open the workspace created in Section 3.4.1.
2. Select **Vitis > Program Flash**. A dialog as the one shown in Figure 4 appears.
3. In the **Program Flash Memory** window, click **Browse** next to the **Image File** field.
4. Select the `BOOT.BIN` file created in Section 4.1.
5. Click **Browse** next to the **Init File** field.
6. Select the `fsbl.elf` file created as part of the hardware platform in Section 3.4.2.
7. Select **qspi-x8-dual-parallel** for the **Flash Type**.
8. Click **Program**.

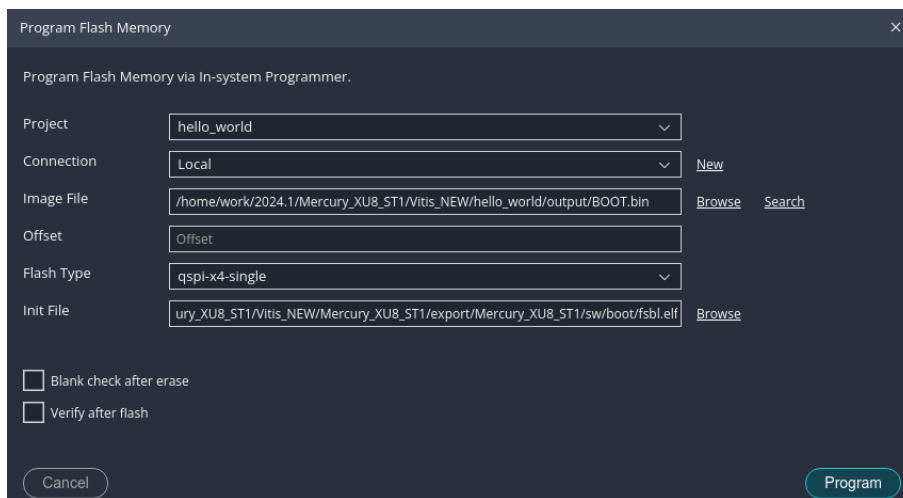


Figure 4: Example Dialog Vitis Program Flash Memory (QSPI)

## Vivado

In order to program the QSPI flash using Vivado, follow these steps:

1. Open Vivado.
2. Click **Open Hardware Manager**.
3. Select **Open target > Auto Connect**. The hardware manager should be able to connect to the device as shown in Figure 5.
4. Right-click the MPSoC and select **Add Configuration Memory Device....** A dialog as the one shown in Figure 5 appears.
5. In the new window, select the following:
  - (a) Manufacturer: Cypress/Spansion
  - (b) Type: qspi
  - (c) Density: 512
  - (d) Width: x8-dual-parallel
6. Select part **s25fl512s-1.8v** from the listed options.
7. Click **OK**.
8. In the new window, click **OK** again to program the configuration memory.
9. In the **Program Configuration Memory Device** dialog, do the following:
  - (a) Select the `BOOT.BIN` file created in Section 4.1 as the **Configuration file**.
  - (b) Select the `fsbl.elf` file created as part of the hardware platform in Section 3.4.2.
  - (c) Leave the default settings for the rest of the options.
  - (d) Click **OK**.
  - (e) Wait for completion.

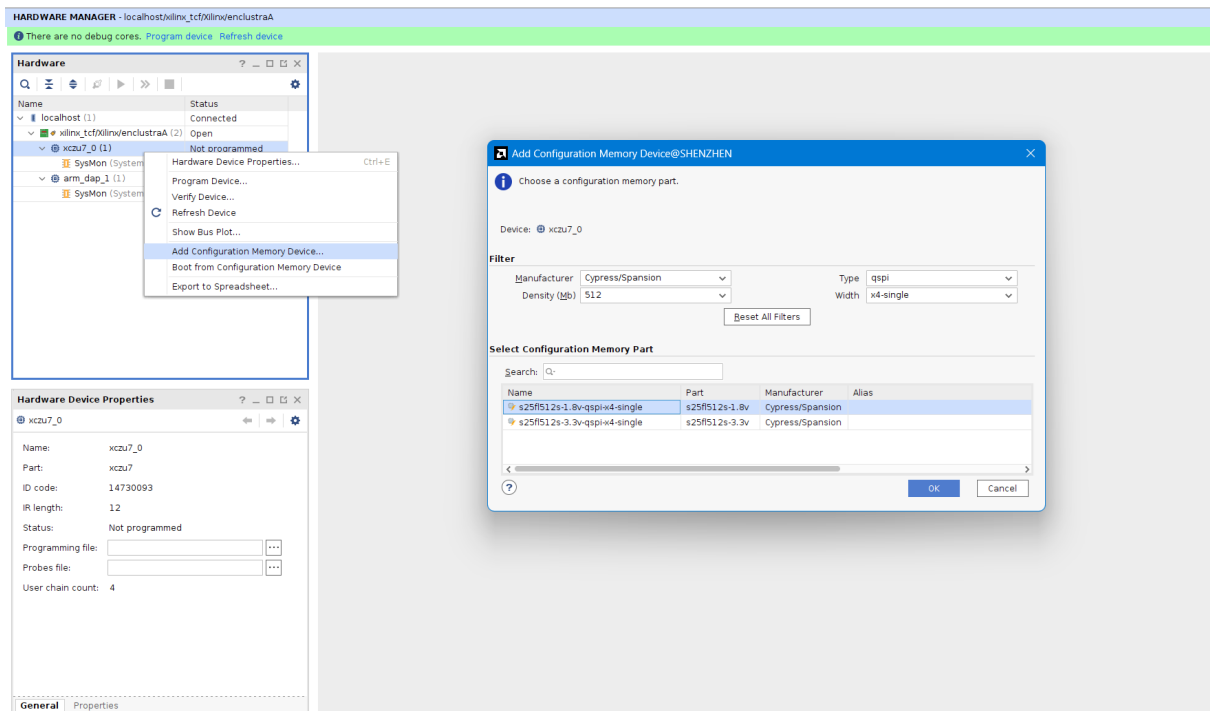


Figure 5: Example Dialog Vivado Configuration Memory (QSPI)

### Tip

Alternatively, Linux running directly on the target can be used to program flash memory devices such as QSPI or eMMC. Refer to the Enclustra Linux Documentation [16] for details.

## 4.2.2 Preparing the Hardware

Refer to Figure 2 to locate the labels on the base board.

1. Disconnect the power supply of the base board (label **12 V DC**).
2. Disconnect all USB cables from the base board.
3. Set the boot mode DIP switch on the base board to [1: OFF, 2: ON, 3: OFF, 4: OFF] (label **BOOT**).
4. Connect the USB-C cable between the computer and the base board using the USB-C port labeled **USB D**.
5. Reconnect the power supply of the base board (label **12 V DC**).

## 4.2.3 Booting from the QSPI Flash

Refer to Figure 2 to locate the labels on the base board.

1. Ensure that the hardware configuration is done according to Section 4.2.2.
2. Reconnect the serial terminal.
3. Press the power-on reset button (label **POR**) and release it after 1 s.
4. The DONE LED (label **LEDs**) lights up after the bitstream has been loaded.
5. The LED on the module starts blinking as described in Section 2.2.3.

The expected output in the serial terminal console is given in Figure 6.

```
Zynq MP First Stage Boot Loader
Release 2024.1 Sep 2 2024 - 10:32:56
PMU-FW is not running, certain applications may not be supported.
Hello World
Successfully ran Hello World application
```

Figure 6: Example of the Terminal Output

## 4.3 SD Card Boot

### 4.3.1 Preparing the SD Card

1. Insert an SD card into the SD card slot of the computer.
2. Ensure that the SD card has a FAT32 formatted partition.
3. Copy the `BOOT.BIN` file created in Section 4.1 to the FAT32 partition of the SD card.

### 4.3.2 Preparing the Hardware

Refer to Figure 2 to locate the labels on the base board.

1. Disconnect the power supply of the base board (label **12 V DC**).
2. Disconnect all USB cables from the base board.
3. Set the boot mode DIP switch on the base board to [1: OFF, 2: ON, 3: ON, 4: ON] (label **BOOT**).
4. Connect the USB-C cable between the computer and the base board using the USB-C port labeled **USB-D**.
5. Insert the SD card into the SD card slot of the base board (label **SD Card**).
6. Reconnect the power supply of the base board (label **12 V DC**).

### 4.3.3 Booting from the SD Card

Refer to Figure 2 to locate the labels on the base board.

1. Ensure that the hardware configuration is done according to Section 4.3.2.
2. Press the power-on reset button (label **POR**) and release it after 1 s.
3. The DONE LED (label **LEDs**) lights up after the bitstream has been loaded.
4. The LED on the module starts blinking as described in Section 2.2.3.

The expected output in the serial terminal console is given in Figure 6.

## 4.4 eMMC Boot

### 4.4.1 Programming the eMMC

#### JTAG Boot Mode

Programming flash memory devices such as QSPI or eMMC using Vivado or Vitis requires setting the JTAG boot mode first. Set the DIP switch on the Andromeda PE5 base board as follows:

- BOOT = [1: OFF, 2: OFF, 3: OFF, 4: OFF]

After setting the JTAG boot mode, follow the steps described in the Vitis section or the Vivado section below.

#### Vitis

In order to program the eMMC memory using Vitis, follow these steps:

1. Open the workspace created in Section 3.4.1 in Vitis.
2. Select **Vitis > Program Flash**.

3. In the **Program Flash Memory** window, click **Browse**.
4. Select the `BOOT.BIN` file created in Section 4.1.
5. Select **emmc** for the **Flash Type**.
6. Select **32** for the **Partition Size (in MB)**. Figure 7 is given for reference.
7. Click **Program**.

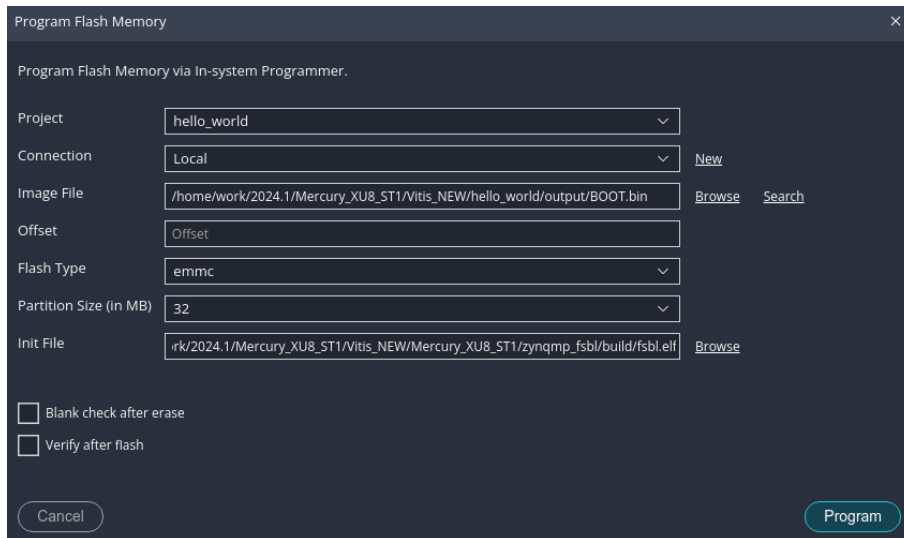


Figure 7: Vitis Program Flash Memory (eMMC)

## Vivado

In order to program the eMMC memory using Vivado, follow these steps:

1. Open Vivado.
2. Click **Open Hardware Manager**.
3. Select **Open target > Auto Connect**. The hardware manager should be able to connect to the device as shown in Figure 8.
4. Right-click the MPSoC and select **Add Configuration Memory Device...**
5. In the new window, select the following:
  - (a) Manufacturer: All
  - (b) Type: emmc
  - (c) Density: All
  - (d) Width: All
6. Select **jedec4.51-16gb-emmc** from the listed options. See Figure 8 for reference.
7. Click **OK**.
8. In the new window, click **OK** again to program the configuration memory.
9. In the **Program Configuration Memory Device** dialog, do the following:
  - (a) Add the `BOOT.BIN` file created in Section 4.1 to the **Files to load** field.
  - (b) Select the `fsbl.elf` file created as part of the hardware platform in Section 3.4.2 in the **Zynq FSBL** field.
  - (c) Leave the default settings for the rest of the options.
  - (d) Click **OK**.
  - (e) Wait for completion.

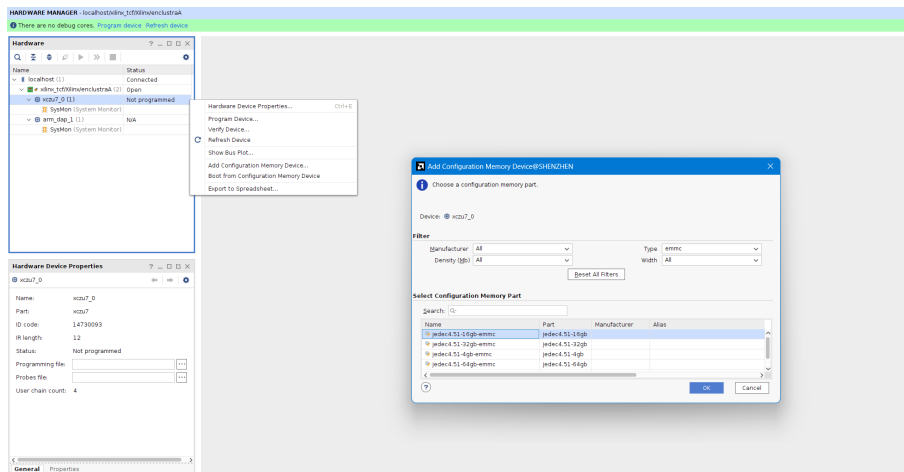


Figure 8: Vivado Configuration Memory (eMMC)

### Tip

Alternatively, Linux running directly on the target can be used to program flash memory devices such as QSPI or eMMC. Refer to the Enclustra Linux Documentation [16] for details.

## 4.4.2 Preparing the Hardware

Refer to Figure 2 to locate the labels on the base board.

1. Disconnect the power supply of the base board (label **12 V DC**).
2. Disconnect all USB cables from the base board.
3. Set the boot mode DIP switch on the base board to [1: OFF, 2: ON, 3: ON, 4: OFF] (label **BOOT**).
4. Connect the USB-C cable between the computer and the base board using the USB-C port labeled **USB-D**.
5. Connect the power supply to the base board (label **12 V DC**).

## 4.4.3 Booting from the eMMC

Refer to Figure 2 to locate the labels on the base board.

1. Check that the hardware configuration is done according to Section 4.4.2.
2. Press the power-on reset button (label **POR**) and release it after 1 s.
3. The DONE LED (label **LEDs**) lights up after the bitstream has been loaded.
4. The LED on the module starts blinking as described in Section 2.2.3.

The expected output in the serial terminal console is the same as in Section 4.3.3.

# 5 Troubleshooting

Ensure the issues are not listed in the Andromeda XZU65 Module Known Issues and Changes [7] or the Andromeda PE5 Base Board Known Issues and Changes [8].

## 5.1 Vivado Issues

### The Windows OS Path is too Long.

The path length limitation of Windows OS can lead to seemingly random errors during the build process.

- Reduce the path length to the Vivado project upon project creation. Refer to [AR52787](#) for further details.

### The Block Design Changes Are Not Propagated into the Implementation Step.

Regenerate the block design files:

1. Right-click the block design ( .bd ) file.
2. Click **Reset Output Products** > **Reset**.
3. Right-click the block design ( .bd ) file.
4. Click **Generate Output Products** > **Generate**.

### The Hardware Manager gives a Critical Warning upon Connection to the Device.

PL Power Status OFF, cannot program PL. Check that POR\_B signal is LOW or BOOT mode is JTAG.

This warning appears when the device has not been configured yet and the internal PL power is disabled. The warning can be ignored and disappears after the device has been programmed.

## 5.2 Vitis Issues

### The Platform Component Generation Fails.

Use a clean workspace:

1. Close Vitis.
2. Delete the workspace folder.
3. Restart Vitis and retry the steps described in Sections [3.4.1](#) and [3.4.2](#).

### The Software Application Launch Fails.

After launching a software application as described in Section [3.4.4](#), launching a second run might fail with the following error:

ERROR : Failed to initialize the hardware Invalid target. Use "connect" command to connect to hw\_server/TCF agent

The problem is usually fixed by clicking the **Run** button again.

## 5.3 JTAG Issues

### The JTAG Is Not Recognized.

- Ensure that the hardware configuration complies with Section [3.2](#).
- Ensure that only **one** JTAG adapter is active and connected to the hardware. Using an AMD JTAG Programmer and the built-in JTAG via FTDI simultaneously will not work. Refer to the Andromeda PE5 Base Board User Manual [3] for details regarding the built-in JTAG functionality.
- Ensure that the device is powered when trying to connect via JTAG.

## 5.4 UART Connection Issues

- If the computer is not able to recognize the USB UART on the Andromeda PE5 base board:
  1. Check that the USB cable is connected properly
  2. Check that the FTDI VCP drivers are installed
    - (a) Disconnect all JTAG connections
    - (b) Open Device Manager
    - (c) Universal Serial Bus controllers → USB Serial Converter A/B/C/D → Properties → Advanced tab → enable Load VCP checkbox
    - (d) Reboot the computer if the COM port is still not detected
  3. Reinstall the FTDI drivers if the problem persists
- If the computer does not output any character in the terminal program:
  1. Check that the FTDI device is set to UART mode:
    - (a) Download and open FT\_Prog utility (this is a third party tool offered by the FTDI company to configure FTDI devices)
    - (b) DEVICES → Scan and Parse
    - (c) Check that for Port A,B,C and D of the RS232 UART property is true
  2. Check that the baud rate for the UART in the block design matches the baud rate set in the terminal program
  3. Make sure that Enclustra MCT software is not open. After closing it, unplug and plug in again the USB cable corresponding to the UART communication.

## 5.5 QSPI Issues

### The QSPI Programming Fails.

- Try any of the other methods described in Section [4.2.1](#).
- Use an SD card image containing a Linux system to program the QSPI flash:
  1. Prepare the SD card image as described in the Enclustra Linux documentation [[16](#)].
  2. Create a folder named `QSPI` on the FAT32 partition of the SD card.
  3. Copy the `BOOT.BIN` created in Section [4.1](#) to the `QSPI` folder.
  4. Boot the system from the SD card as described in Section [2.1.3](#).
  5. Stop the boot process in u-boot by pressing any key during the 3s countdown.
  6. Program the QSPI flash using the following commands:

```
sf probe
sf erase 0x0 0x4000000
fatload mmc 1:1 0x2000000 QSPI/BOOT.BIN
sf write 0x2000000 0x0 $filesize
```

### The QSPI Boot Fails.

Ensure that the hardware setup complies with Section [4.2.2](#).

## 5.6 eMMC Issues

### The eMMC Programming Fails.

Try any of the other methods described in Section [4.4.1](#).

### 5.6.1 The eMMC Boot Fails.

Ensure that the hardware setup complies with Section [4.4.2](#).

## 5.7 MCT Issues

### The Module Enumeration Fails.

1. Disconnect all USB cables.
2. Ensure that all tools are closed that may be connected to the FTDI (Vivado Hardware Manager, Vitis, any serial terminal).
3. Ensure that no leftover instances of the hw\_server process are running using the Windows task manager.
4. Configure the DIP switches according to Section [3.2](#).
5. Reconnect the USB cable.
6. Ensure that VCP is enabled as described in Section [5.4](#).
7. Click **Enumerate** again.

If enumeration is still unsuccessful, select **Settings > Enable Diagnostic Logging**. Click **Enumerate** and send the log file to the Enclustra Support Channel [\[1\]](#) for further analysis.



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# References

- [1] Enclustra Support Channel  
[support@enclustra.com](mailto:support@enclustra.com)
- [2] Andromeda XZU65 Module User Manual  
<https://www.enclustra.com/am-xzu65-user-manual>
- [3] Andromeda PE5 Base Board User Manual  
<https://www.enclustra.com/am-pe5-user-manual>
- [4] Enclustra Module Configuration Tool (MCT)  
<https://www.enclustra.com/module-configuration-tool>
- [5] Andromeda XZU65 PE5 Reference Design Releases  
[https://github.com/enclustra/Andromeda\\_XZU65\\_PE5\\_Reference\\_Design/releases](https://github.com/enclustra/Andromeda_XZU65_PE5_Reference_Design/releases)
- [6] Enclustra Application Notes  
<https://github.com/enclustra/I2CAppNote>  
<https://github.com/enclustra/GigabitEthernetAppNote>
- [7] Andromeda XZU65 Module Known Issues and Changes  
<https://www.enclustra.com/am-xzu65-known-issues-and-changes>
- [8] Andromeda PE5 Base Board Known Issues and Changes  
<https://www.enclustra.com/am-pe5-known-issues-and-changes>
- [9] Vivado Design Suite User Guide, UG910, AMD Xilinx, 2024  
<https://docs.amd.com/r/en-US/ug910-vivado-getting-started>
- [10] Vivado Design Suite User Guide: Release Notes, Installation, and Licensing, UG973, AMD Xilinx, 2024  
<https://docs.amd.com/r/en-US/ug973-vivado-release-notes-install-license/Release-Notes>
- [11] Vitis Unified Software Platform, UG1416, AMD Xilinx, 2024  
<https://docs.amd.com/v/u/en-US/ug1416-vitis-documentation>
- [12] Embedded Design Tutorials  
<https://github.com/Xilinx/Embedded-Design-Tutorials/tree/master>
- [13] Zynq UltraScale+ Device Technical Reference Manual, UG1085, AMD Xilinx, 2023  
<https://docs.amd.com/r/en-US/ug1085-zynq-ultrascale-trm>
- [14] Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics, DS925, AMD Xilinx, 2024  
<https://docs.amd.com/r/en-US/ds925-zynq-ultrascale-plus>
- [15] Zynq UltraScale+ MPSoC Embedded Design Tutorial, UG1209, AMD Xilinx, 2024  
<https://docs.amd.com/v/u/en-US/ug1209-embedded-design-tutorial>
- [16] Enclustra Linux Documentation  
<https://github.com/enclustra/meta-enclustra-amd>