

axis_data_gen

Documentation

Content

Table of Contents

1	Introduction.....	3
1.1	Feature List.....	3
1.2	Modes of Operation.....	3
1.2.1	Continuous Trigger Generation.....	3
1.2.2	Sporadic Trigger Generation.....	5
2	Interfaces.....	6
2.1	GUI	6
2.1.1	General Configuration	6
2.1.2	Reset Values	7
2.2	Registers	8
2.2.1	Overview.....	8
2.2.2	Register Descriptions	8

1 Introduction

The purpose of this IP is to generate AXI-stream traffic in a controlled way for testing purposes. The traffic generated contains counter values with configurable trigger/TLAST flags.

1.1 Feature List

- Up to 32-bit data width
- Configurable data- and trigger-rate
- Different trigger generation schemes
 - Continuous: Generate a trigger every N samples
 - Sporadic: Generate X triggers, N samples apart and then stop generating triggers
- Generate single cycle triggers and/or TLAST (handshake)
- Static configuration possible
 - In this case no software to configure the core is required
 - Feature-set is slightly reduced
- Backpressure can be handled (data topped if TREADY low) or ignored

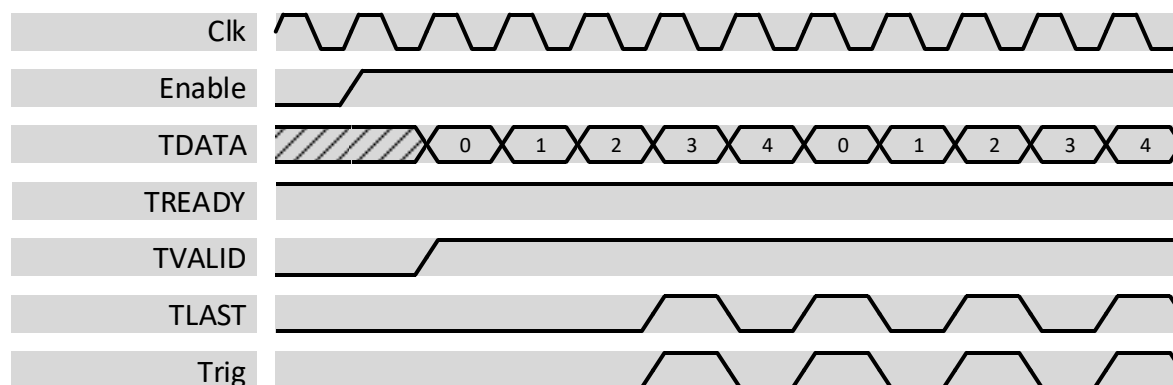
1.2 Modes of Operation

1.2.1 Continuous Trigger Generation

1.2.1.1 Back-to-Back data

The figure below shows an example waveform for the following settings:

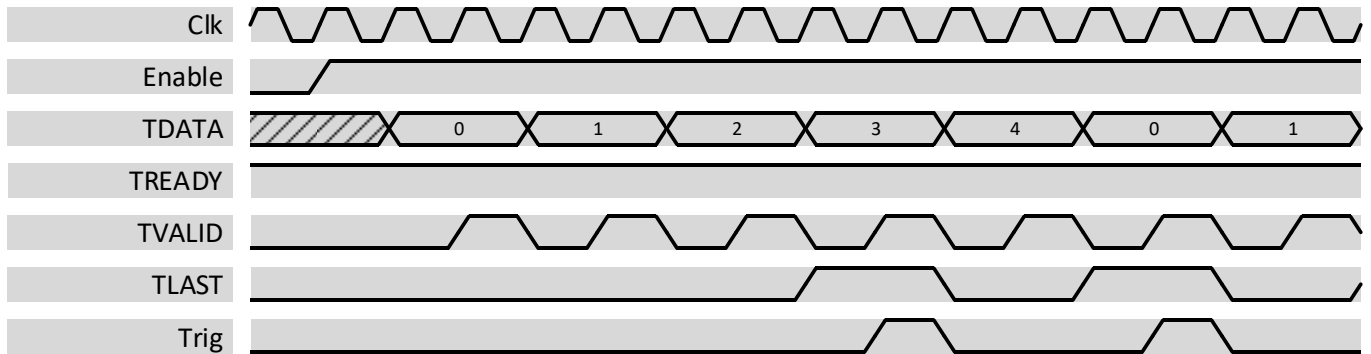
DATA_SPAC 0
 DATA_WRP 4
 TRIG_OFFS 3
 TRIG_SPAC 1



1.2.1.2 Reduced Data-Rate

The figure below shows an example waveform for the following settings:

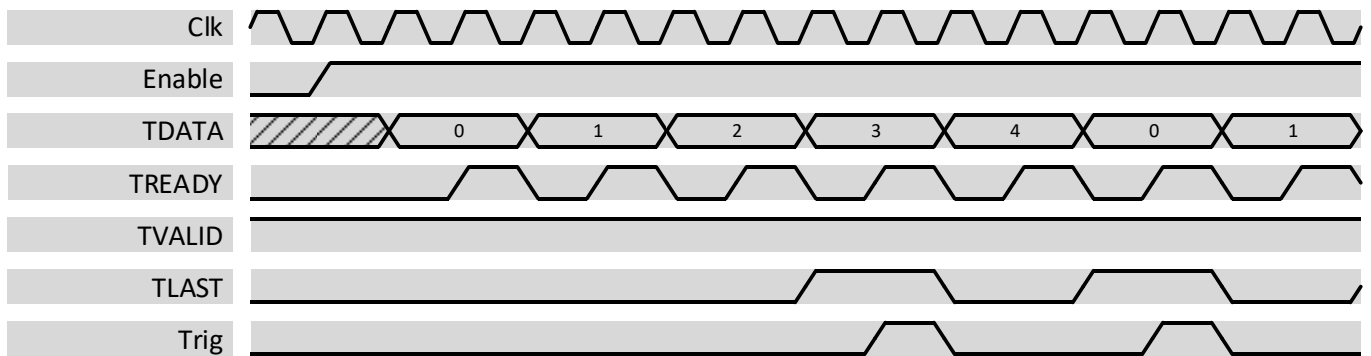
DATA_SPAC 1
DATA_WRP 4
TRIG_OFFS 3
TRIG_SPAC 1



1.2.1.3 Reduced Back-Pressure

The figure below shows an example waveform for the following settings:

DATA_SPAC 1
DATA_WRP 4
TRIG_OFFS 3
TRIG_SPAC 1
CFG_USERDY 1

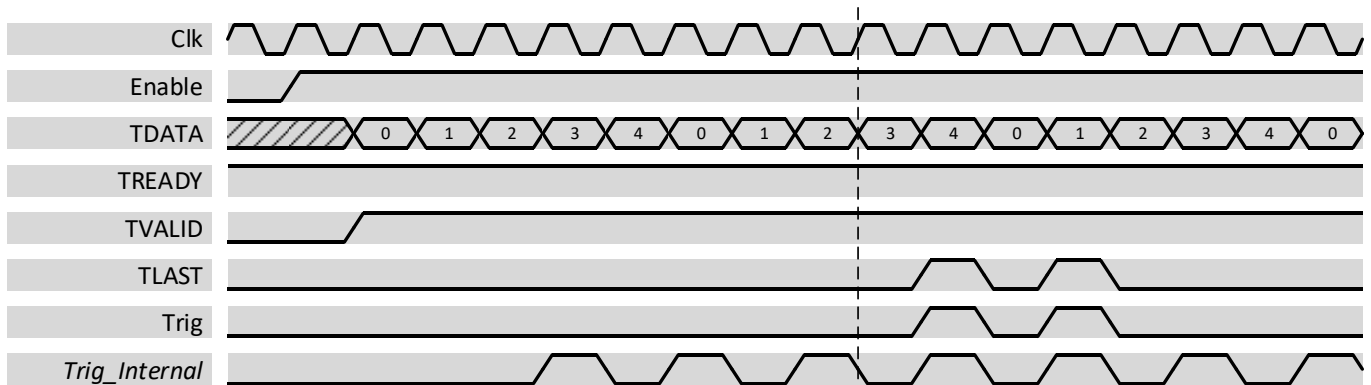


1.2.2 Sporadic Trigger Generation

The figure below shows an example waveform for the following settings:

DATA_SPAC 0
DATA_WRP 4
TRIG_OFFS 3
TRIG_SPAC 1

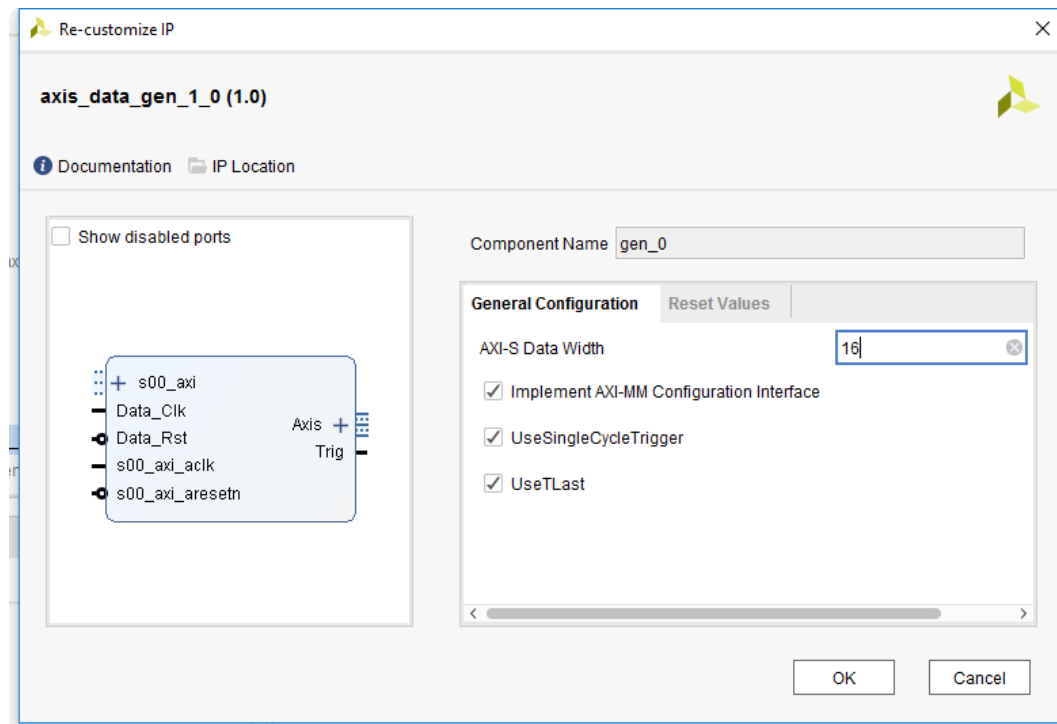
At the point marked with a dashed line, the trigger counter is set to two. The signal *Trig_Internal* shows the internal trigger signal (unsuppressed trigger) that is not visible to the ports. It is only shown to depict that the trigger alignment does not change if sporadic triggering is used.



2 Interfaces

2.1 GUI

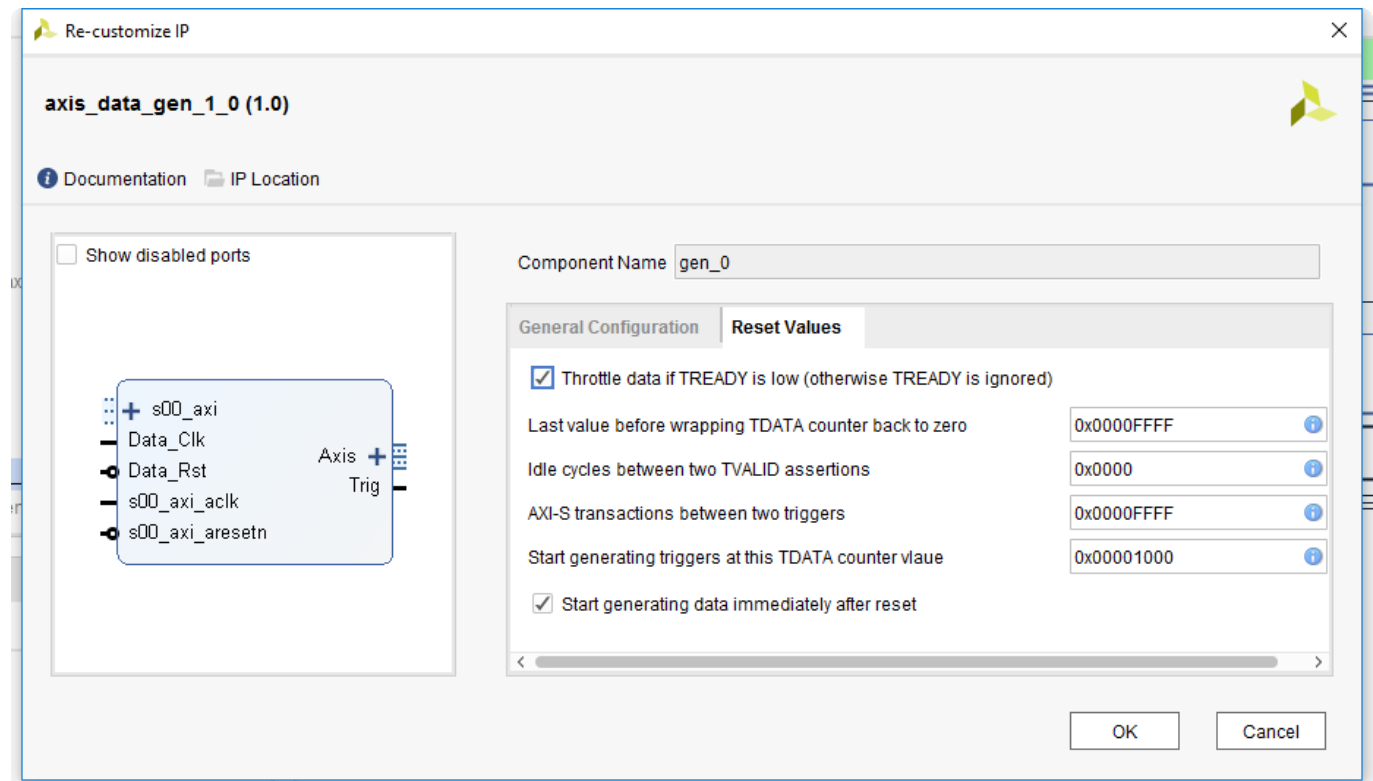
2.1.1 General Configuration



This page contains the following parameters

- AXI-S Data Width
 - Width of the AXI-S data port in bits
- Implement AXI-MM Configuration interface
 - If set, the core can be configured via an AXI-MM register bank
 - If not set, no runtime configuration is possible and the core starts generating data directly after the reset according to the settings on the page *Reset Values*
- UseSingleCycleTrigger
 - If set, a *Trig* output port is generated that contains trigger pulses that are exactly one clock cycle long.
 - If not set, the *Trig* output is omitted
- UseTlast
 - If set, the trigger signal is applied to TLAST (synchronous to the handshaking of course) according to the AXI-S specification
 - If not set, the TLAST port is omitted

2.1.2 Reset Values



This page of the GUI contains the reset values for all registers required to generate data without an AXI-MM interface.

If an AXI-MM port is implemented, it is recommended to do all settings over this port instead of using the parameters in this GUI page.

Note that data can be entered in hex (*0x1234ABCD*), binary (*0b00100111*) or decimal (*0d1234*). Vivado detects the prefix automatically and does the conversion.

2.2 Registers

2.2.1 Overview

Byte Address Offset	Name	Description
0x000	CFG_ENA	Enable data generator
0x004	CFG_USERDY	Use TREADY signal for back-pressure handling
0x010	DATA_WRP	Last value before wrapping the data counter
0x014	DATA_SPAC	Number of clock cycles between two samples
0x020	TRIG_OFFS	Counter value to generate the first trigger at
0x024	TRIG_SPAC	Number of samples between two triggers
0x028	TRIG_SPOR_EN	Enable sporadic triggering
0x02C	TRIG_SPOR_LD	Load sporadic trigger counter
0x030	TRIG_SPOR_CNT	Sporadic trigger counter
0x040	RDYLO	Ready-low detection
0x050	STAT_DATACNT	Current data counter
0x054	STAT_TRIGLEFT	Number of triggers left to generate in sporadic mode

2.2.2 Register Descriptions

2.2.2.1 CFG_ENA – Enable data generator (0x00)

Field	Bit(s)	Type	Reset	Description
ENA	0	RW	See GUI	1 Data generator enabled 0 Data generator disabled

If the data generator is disabled, all values are set to their initial value. So the data counter starts at zero and the first trigger is generated at *TRIG_OFFS* after re-enabling.

2.2.2.2 CFG_USERDY – Use TREADY signal for back-pressure handling (0x04)

Field	Bit(s)	Type	Reset	Description
USERDY	0	RW	See GUI	1 TREADY is used, when TREADY is '0', the data counter is stopped. 0 TREADY is ignored

This register must not be changed while the data generator is running.

2.2.2.3 DATA_WRP – Last value before wrapping the data counter (0x10)

Field	Bit(s)	Type	Reset	Description
WRP	31:0	RW	See GUI	Last counter value before the data counter is wrapped back to zero. Example: WRP = 13 leads to the counter sequence ..., 10, 11, 12, 13, 0, 1, 2, ...

This register must not be changed while the data generator is running.

2.2.2.4 DATA_SPAC – Number of clock cycles between two samples (0x14)

Field	Bit(s)	Type	Reset	Description
SPAC	15:0	RW	See GUI	Number of clock cycle TVALID is held low between two samples. Apply 0 for back-to-back data generation.

This register must not be changed while the data generator is running.

2.2.2.5 TRIG_OFFS – Counter value to generate the first trigger at (0x20)

Field	Bit(s)	Type	Reset	Description
OFFS	31:0	RW	See GUI	Counter value the trigger generation is started at. The first trigger is generated together with the sample number given in this register.

This register must not be changed while the data generator is running.

2.2.2.6 TRIG_SPAC – Number of samples between two triggers (0x24)

Field	Bit(s)	Type	Reset	Description
SPAC	31:0	RW	See GUI	Number of samples between two triggers. Apply 0 for generating a trigger with each sample.

This register must not be changed while the data generator is running.

2.2.2.7 TRIG_SPOR_EN – Enable sporadic triggering (0x28)

Field	Bit(s)	Type	Reset	Description
ENA	0	RW	0	0 Triggers are generated continuously 1 Triggers are only generated when requested by the sporadic trigger settings.

This register is always reset to zero since sporadic triggering only makes sense if an AXI-MM interface is present. Otherwise the triggering would never be started (because it is started through the AXI-MM interface).

2.2.2.8 TRIG_SPOR_LD – Load sporadic trigger counter (0x2C)

Field	Bit(s)	Type	Reset	Description
LOAD	0	W	-	Write 1 to set the sporadic trigger counter.

After the sporadic trigger counter is set, triggers are generated and the counter is decremented until it arrived at zero. After N triggers, the counter is zero and no more triggers are generated.

The *TRIG_SPAC* settings stay valid during sporadic triggering. Also do the trigger still occur at the positions given by *TRIG_OFFS* and *TRIG_SPAC*. If the sporadic trigger counter is zero, triggers are just suppressed but their alignment does not change.

2.2.2.9 TRIG_SPOR_CNT – Sporadic trigger counter (0x30)

Field	Bit(s)	Type	Reset	Description
CNT	31:0	RW	-	Number of triggers to generate after <i>TRIG_SPOR_LD</i> is asserted

2.2.2.10 RDYLO – Ready-low detection (0x40)

Field	Bit(s)	Type	Reset	Description
WASLO	0	RCW1	0	This bit is set when TREADY='0' delayed the data generation. Write 1 to clear the bit.

This functionality is very useful to see if the downstream logic (logic receiving the values generated) can handle the data-rate. If it cannot, pulls TREADY low which is detected here.

2.2.2.11 STAT_DATACNT – Current data counter (0x50)

Field	Bit(s)	Type	Reset	Description
CNT	31:0	R	0	Current value of the data counter

2.2.2.12 STAT_TRIGLEFT – Current trigger counter (0x54)

Field	Bit(s)	Type	Reset	Description
CND	31:0	R	0	Current value of the trigger counter used for sporadic trigger generation.