AMERICAN INTERNATIONAL UNIVERSITY-BANGLADESH (AIUB)

Faculty of Engineering
Department of Electrical and Electronic Engineering
Undergraduate Program

PART A

1.	Course No/Course Code	EEE 3101
2.	Course Title	Digital Logic and Circuits
3.	Course Type	Core Course
4.	Year/Level/Semester/Term	Third year (5th Semester)
5.	Academic Session	Fall 2023-24
6.	Course Teachers/Instructors	Mr. Nafiz Ahmed Chisty, Dr. Shahriyar Masud Rizvi, Dr. Tanbir Ibne Anowar, Dr. Gour Chand Mazumder, Mr. Abir Ahmed, Mr. Md. Shahariar Parvez, Mr. Tamim Hossain, Mr. Richard Victor Biswas, Mr. Abrar Fahim Liaf
7.	Pre-requisite (If any)	EEE 2103: Electronic Devices
8.	Credit Value	3 credit hours
9.	Contact Hours	2 hours 30 mins of theory per week
10.	Total Marks	100
11.	Mission of EEE Department	• Educate young leaders for academia, industry, entrepreneurship, and public and private organization through theory and practical knowledge to solve engineering problems individually and in teams. • Create knowledge through innovative research and collaboration with multiple disciplines and societies. • Serve the communities at national, regional, and global levels with ethical and professional responsibilities.
12.	Vision of EEE Department	To become a front runner in preparing Electrical and Electronics Engineering graduates to be nationally and globally competitive and thereby contribute value for the knowledge-based economy and welfare for the people of the world.
13.	Rationale of the Course (Course Description)	This is core course of Electrical and Electronic Engineering & Computer Engineering program that presents basic tools for the design of digital circuits. It serves as a building block in many disciplines that utilize data of digital nature like digital control, data communication, digital computers etc.
14.	Course Content	The course is designed to provide students with: • Perform arithmetic operations in many number systems, Manipulate Boolean algebraic structures, Implement the Boolean Functions using NAND and NOR gates, Simplify the Boolean expressions using Karnaugh Map. • Analyze and design various combinational logic circuits, Study of Storage Elements: Introduction to the behavior and structure of latches, flip-flops, and registers, Understand the importance of state diagram representation of sequential circuits, Study Sequential Circuits: Analyze and design clocked sequential circuits, Perform Timing Analysis: • Introduction to timing analysis of combinational and sequential circuits. Special characteristics of Digital logic families and their comparative discussion. Definition and Problem solving on Fan out, Noise Margin, Propagation Delay, Power Dissipation, Duty Cycle and Speed Power Product. Diode Logic Gates.

- Basic Diode Transistor Logic Gates: RTL, DTL, Modified DTL and HTL with operational detail. MOS and CMOS Logic with operational detail. Basic memory units and operations.

15. Course Outcomes (CO)/Course Learning Outcomes (CLOs):

By the end of this course, students should be able to –

COs/ CLOs Number	COs/CLOs Statements	K	P	A	Assessed Program Outcome Indicator	BNQF Indicator	Teaching - Learning Strategy	Assessment Strategy
1	**Apply** laws of Boolean Algebra for implementing combinational digital logic circuits (gate and transistor level) and for the calculation of performance parameters (Fan-out, Fan-in, Power dissipation, Speed power products, Noise margin) along with along with Adders, Magnitude Comparators, Encoder, Decoder, Multiplexer and Demultiplexer with the familiarity of issues.	2			P.a.2.C3	FS.2		Quiz 1, Quiz 2, Quiz 3 Assignment, Midterm Exam
2	**Develop** a system in context of Digital logic circuits with 555 timer and transistors for **conflicting requirements** of complex engineering problem.	**3**	**P1, P2 P6**		**P.a.3.C3**	**FS.1**		**OBE Assignment (Final Term)**
3	**Apply** basic digital signal techniques, latches and flip-flops with the familiarity of issues for different signal converter and sequential logic circuits.	1			P.a.1.C3	FS.1		Quiz 4, Quiz 5, Final term Exam
4	**Demonstrate** individual skills as a leader in solving combinational or sequential digital circuits.				P.i.2.A5	FS.5		Presentation

16. Mapping with Course Learning Outcomes (CLOs) with Program Learning Outcomes (PLOs)

CLOs	PLO 1	PLO 2	PLO 3	PLO 4	PLO 5	PLO 6	PLO 7	PLO 8	PLO 9	PLO 10	PLO 11	PLO 12
1	FS.2											
2	FS.1											
3	FS.1											
4									FS.5			

PART B

17. Course plan:

By the end of this course, students should be able to –

Time Frame (Week)	Topics	Teaching Learning Strategy	Assessment Strategy	Corresponding COs /CLOs	Assessment Tools
Week 1	Mission & Vision of AIUB, Dept. of EEE, Digital Logic Design meaning and objectives of this course *Introduction to Integrated Circuit (IC). *Special Characteristics of digital logic families *Binary Logic, Logic gates and their truth table *Diode Logic gates Basics of semiconductor memory * Logic Gates: using RTL, Solutions of RTL Logic family mathematical problems	Lecture Tutorial	*Calculation-based question: test/ mid-term exam *Theoretical-based question: test/ mid-term exam	1	Quiz, Term Exam
Week 2	*Logic Gates: using DTL and Modified DTL. *Problem solving on Fan of DTL gate. and Modified DTL gate *Logic Gates: using HTL *MOS and CMOS logic with operation detail. *Negative temperature co-efficient *Design CMOS logic circuits from equation	Lecture Tutorial		1 2	Quiz, Term Exam
Week 3	Boolean algebra, Simplification of logic function using Boolean Algebra, Implementing circuit from Boolean expressions. De-Morgan's law Universal gates and Implementation of Basic Combinational Logic Circuits using Universal Gates only	Lecture Tutorial		1	Quiz, Term Exam
Week 4	Simplifying Boolean Expression using algebraic manipulation Boolean expression in Sum of Product (SOP) and Product of Sum (POS) form, Canonical forms Standardization of SOP/POS expressions and conversions between them Simplifying Boolean Expressions using K – map	Lecture Tutorial		1	Quiz, Term Exam
Week 5	*Adder: Half adder, Full adder, 2's complement *Magnitude Comparators *Decoders, Encoders,	Lecture Tutorial		1	Quiz, Term Exam, Assignment
Week 6	Priority Encoders, Cascading of Decoders,	Lecture Tutorial		1	Quiz, Term Exam,

					Assignment
Week 7	*Multiplexers, De-Multiplexer Boolean Function implementation using Multiplexers, Cascading of Multiplexers, De-Multiplexers	Lecture Tutorial		1	Quiz, Term Exam
Week 8	**MID-TERM EXAM WEEK**				
Week 9	*Sequential Logic Circuit, *Different types of Flip – flop (S-R, J-K, D and T), Timing Diagram	Lecture Tutorial	*Calculation-based question: test/ final exam *Theoretical-based question: test/ final exam	3	Quiz, Term Exam
Week 10	*Counters: Asynchronous (Cascading and Modulus Counter) and Synchronous (Cascading) [State Diagram, Table, Equation]	Lecture Tutorial		3	Quiz, Term Exam
Week 11	Binary Up-Down counter [State Diagram, Table, Equation] *Designing Irregular Counters using State Diagram and State Equation	Lecture Tutorial		3	Quiz, Term Exam
Week 12	*Shift registers: Basic Shift Register Functions, Different types of Shift Registers *Shift register Counters: Johnson counter, Ring counter	Lecture Tutorial		3	Quiz, Term Exam
Week 13	*Operation of 555 integrated timer circuit: Monostable, A stable multivibrator	Lecture Tutorial		2 3	Quiz, Term Exam
Week 14	Digital Signal Processing Basics, Sample and Hold Circuits *Different types of A/D Converter with application *Different types D/A converter with application. **Special Assignment for assessing P.a.3.C3**	Lecture Tutorial		3	Quiz, Term Exam, OBE Assignment
Week 15	Digital Signal Processing Basics, Sample and Hold Circuits *Different types of D/A converter with application.	Lecture Tutorial		3	Quiz, Term Exam
Week 16	**FINAL-TERM EXAM WEEK**				
Week 17	**FINAL-TERM SET B EXAM WEEK**				

* The faculty reserves the right to change, amend, add or delete any of the contents.

PART C

18. Assessment and Evaluation

1. Assessment Strategy:

	CO/CLO 1 (marks)	CO/CLO 2 (marks)	CO/CLO 3 (marks)	CO/CLO 4 (marks)	Marks for Grading
Quiz (Mid)	**Q1(20) Q2(20)**				
Mid Assignment	**10**				
Quiz (Final)			**Q3(5)**		

			Q4(5)		
OBE Assignment (Final)		**Q1(15) Q2(15)**			
Presentation & Viva (Final)				**10**	

2. Table of Specification (TOS)

Mid-Term Exam

Topics	CO No.	No. of Days	No. of Items	No. of COs	Level of Bloom's Taxonomy																		POI
					Remember			Understand			Apply			Analyze			Evaluate			Create			
					Item No.	Test Type	Marks	Item No.	Test Type	Marks	Item No.	Test Type	Marks	Item No.	Test Type	Marks	Item No.	Test Type	Marks	Item No.	Test Type	Marks	
Special Characteristics of digital logic families, Binary Logic, Logic gates, their truth table and design of logic circuit	CO1	3	5								1.a	PS	5										P.a.2.C3
											4.b	PS	5										
Boolean algebra, Simplification, Circuit implementation	CO1	2	3								2.a	PS	5										P.a.2.C3
SOP, POS, KMAP, Universal gates	CO1	3	4								2.b	PS	5										P.a.2.C3
											3.a	PS	5										
											5.b	PS	5										
Adder, 2's complement, Comparator, Encoder, Decoder, MUX, DeMUX	CO1	6	8								1.b	PS	5										P.a.2.C3
											3.b	PS	5										
											4.a	PS	5										
											5.a	PS	5										
Total		14	20										50										

Final Exam

Topics	CO No.	No. of Days	No. of Items	No. of COs	Level of Bloom's Taxonomy																		POI
					Remember			Understand			Apply			Analyze			Evaluate			Create			
					Item No.	Test Type	Marks	Item No.	Test Type	Marks	Item No.	Test Type	Marks	Item No.	Test Type	Marks	Item No.	Test Type	Marks	Item No.	Test Type	Marks	
Flip- flops, Timing diagram	CO3	2	2								3.b	PS	5										P.a.1.C3
Counters and Shift register	CO3	6	6								1.b	PS	5										P.a.1.C3
											2.a	PS	5										
											3.a	PS	5										
											4.a	PS	5										
Timer	CO3	4	2								2.b	PS	5										P.a.1.C3
											5.b	PS	5										
Digital Signal Processing	CO3	4	4								1.a	PS	5										P.a.1.C3
											4.b	PS	5										
											5.a	PS	5										
Total		16	14										50										

***Test Type Legend**: **AS:** Assignment; **BQ**: Broad question; **SQ**: Short question; D: Derivation; **ES:** Essay; **EX:** Exercise; **GE:** Group Exercise; **ID:** Identification; **MC**: Multiple Choice; **MT**: Matching Type; **OB:** Observation; **PS**: Problem Solving; **SA**: Short Answer; **TF**: True or False; **VV:** Viva Voce; **Other please specify**:*

3. Marks Distribution:

The evaluation system will be strictly followed as par the AIUB grading policy. The following grading system will be strictly followed in this class.

Assessment Type	Marking system For Theory Classes (Midterm)	
Continuous	Attendance	10%
Continuous	Quiz (Best 2 out of 3)	40%
Continuous	Assignment	10%
Summative	Midterm Exam	40%
	Total	100%
	Marking system For Theory Classes (Final term)	
Continuous	Attendance	10%
Continuous	Quiz	10%
Continuous	OBE Assignment	30%
Summative	Presentation & VIVA	10%
Summative	Final Exam	40%
	Total	100%
	Final Grade/ Grand Total	
Grand Total	Midterm:	40%
	Final Term:	60%

4. Grading Policy

Letter	Grade Point	Numerical %
A+	4.00	90-100
A	3.75	85-<90
B+	3.50	80-<85
B	3.25	75-<80
C+	3.00	70-<75
C	2.75	65-<70
D+	2.50	60-<65
D	2.25	50-<60
F	0.00	<50(Failed)

5. Makeup Procedure:

Students who fail to maintain the requirements and deadlines needed to contact faculty with reasoning. Continuous assessments will be taken with agreement with the student and faculty. For the make-up of Summative assessments students need to apply for SET – B exam according to the AIUB policy.

PART D

19. Learning Materials

Formal lectures will provide the theoretical base for the subject as well as covering its practical application. A set of lecture notes, tutorial examples, with subsequent discussion and explanation, together with suggested reading will support and direct the students in their own personal study. Maximum topics will be covered from the textbook. For the rest of the topics, reference books will be followed. Some Class notes will be uploaded on the web. White board will be used for most of the time. For some cases, multimedia projector will be used for the convenience of the students.

Students must study up to the last lecture before coming to the class and it is suggested that they should go through the relevant chapter before coming to the class. Just being present in the class is not enough- students must participate in classroom discussions.

Few assignments will be given to the students based on that class to test their class performance.

1. Recommended Readings (Textbook);

[1] Thomas L. Floyd, "Digital Fundamentals" 9th edition, Prentice Hall.
[2] M. Morris Mano, "Digital Logic & Computer Design" Prentice Hall.

2. Supplementary Readings (Reference Book);

[1] Ronald J. Tocci & Neal S. Widmer, "Digital Systems" 7th edition, Prentice Hall.
[2] Digital design – Karim and Johnson
[3] Brian Holdsworth and Clive Woods, "Digital Logic Design"-Fourth Edition.
[4] Stephen Brown and Zvonko Vranesic, "Fundamentals of Digital Logic with VHDL Design with CD-ROM"
[5] William J. Dally and R. Curtis Harting, "Digital Design: A Systems Approach"
[6] Victor P. Nelson, H. Troy Nagle, Bill D. Carroll and David Irwin, "Digital Logic Circuit Analysis and Design"
[7] John P. Hayes, "Introduction to Digital Logic Design"
[8] Norman Balabanian and Bradley Carlson, "Digital Logic Design Principles"
[9] Enoch O. Hwang, "Digital Logic and Microprocessor Design with VHDL"
[10] Joseph Cavanagh, "Digital Computer Arithmetic: Design and Implementation (Computer Science)"

PART E

Verification: **EEE 3101: Digital Logic and Circuits**		
Prepared by: …….. Mr. Md. Shahariar Parvez (Course Co-ordinator) Date:	Checked and certified by: ..... Nafiz Ahmed Chisty Head (UG), Department of EEE, Faculty of Engineering Date:	Approved by: ..... Prof. Dr. A B M Siddique Hossain Dean, Faculty of Engineering Date: .....
	Moderated by: …… Date: …….	Moderated by: …… Date: …….