AMERICAN INTERNATIONAL UNIVERSITY BANGLADESH

Faculty of Engineering

Laboratory Report Cover Sheet

Students must complete all details except the faculty use part.

Please submit all reports to your subject supervisor or the office of the concerned faculty.

Lab Title: Construction of different Logic Gates using various types of semiconductor devices..

Experiment Number: **05** Due Date: 25/10/2023 Semester: Fall 2022-2023

Subject Code: **EEE3102** Subject Name: DIGITAL LOGIC AND CIRCUITS LAB Section: **L**

Course Instructor: **NUZAT NUARY ALAM** Degree Program: **B.Sc. CSE**

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Group Number (if applicable): 6 Individual Submission Group Submission

No.		Student Name	Student Number	Student Signature	Date
Submitted by:					
1		**ABIR BOKHTIAR**	**22-47038-1**		22/10/2023
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3		MD SHOHANUR RAHMAN SHOHAN	**22-46013-1**		
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For faculty use only:

Total Marks: _____ Marks Obtained: _____

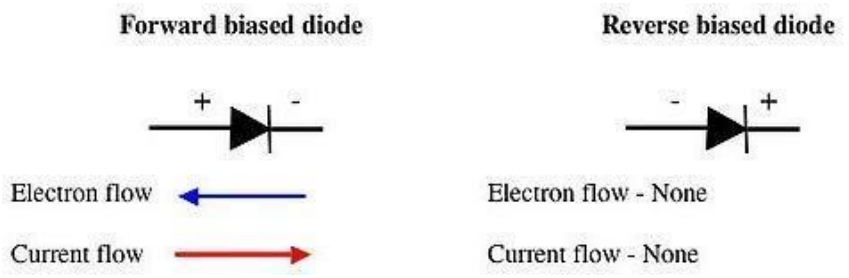
Faculty comments_____

Title: Construction of different Logic Gates using various types of semiconductor devices.

Part I: Construction of Diode Logic Gates

Introduction:

A diode is a two-terminal electrical device that allows current to flow in one direction but not the other. It is like a pipe with an internal valve that allows water to flow freely in one direction but shuts down if the water tries to flow backward. The diode's two terminals are called the anode and cathode. In the diode symbol, the arrow points from the anode (flat part of triangle) toward the cathode (point of the triangle).



The device operates by allowing current to flow from anode to cathode, basically in the direction of the triangle. Recall that current is defined to flow from the more positive voltage toward the more negative voltage (electrons flow in the opposite direction). If the diode's anode is at a higher voltage than the cathode, the diode is said to be forward biased, its resistance is very low, and current flows. If the anode is at a lower voltage than the cathode, the diode is reverse-biased, its resistance is very high, and no current flows. The diode is not a perfect conductor, so there is a small voltage drop, approximately 0.7 V, across it.

In this group of experiments we will implement some logic functions using the DL circuits and discover the potential benefits and problems of using the DL logic.

Theory and Methodology:

***Diode Logic OR Gate*:**

A Diode Logic OR gate consists of nothing more than diodes (one for each input signal) and a resistor. Here, the 10KΩ resistor (R) is added to provide a ground reference for the output signal. If there are no input signals connected to the diodes, the output will be ground, or logic 0. Thus, an open input is equivalent to a logic 0 input, and will have no effect on the operation of the rest of the circuit.

It is possible to add any number of input diodes to this circuit, each with its separate input signal. However, two inputs are quite sufficient to demonstrate the operation of the circuit.

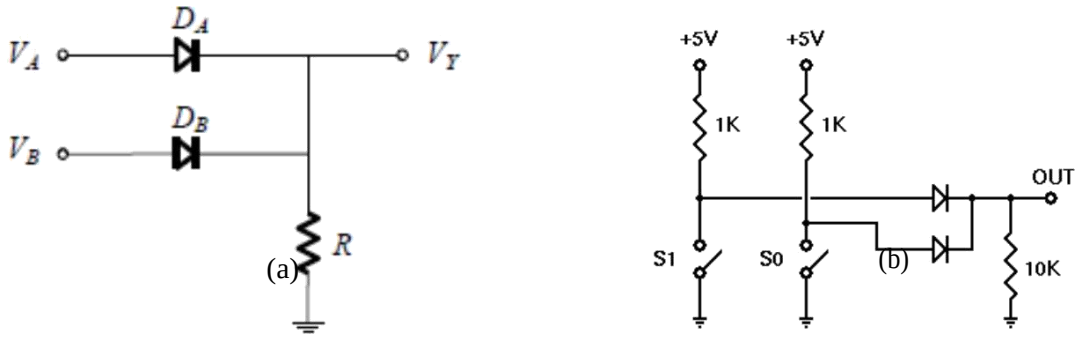


Fig.1 DL-OR Gate

Assuming the diodes are ideal, the voltage truth table as given in Table 1(a) is obtained. The corresponding logic truth table is given in Table 1(b):

V_A (volt)	V_B (volt)	V_Y (volt)
0	0	0
0	5	5
5	0	5
5	5	5

(a)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(b)

Table 1

Diode Logic AND Gate:

A Diode Logic AND gate consists of diodes (one for each input signal) and a resistor. As with the DL OR gate, the 10KΩ resistor (R) provides a reference connection. Unlike the OR gate, however, this is a reference to +5 volts, rather than to ground. If there are no input signals connected to the diodes, the output will be +5 volts, or logic 1. Thus, an open input will not affect the rest of the circuit, which will continue to operate normally.

As with DL-OR gates, it is possible to add any number of input diodes to this circuit, each with its separate input signal. However, two inputs are quite sufficient to demonstrate the operation of the circuit.

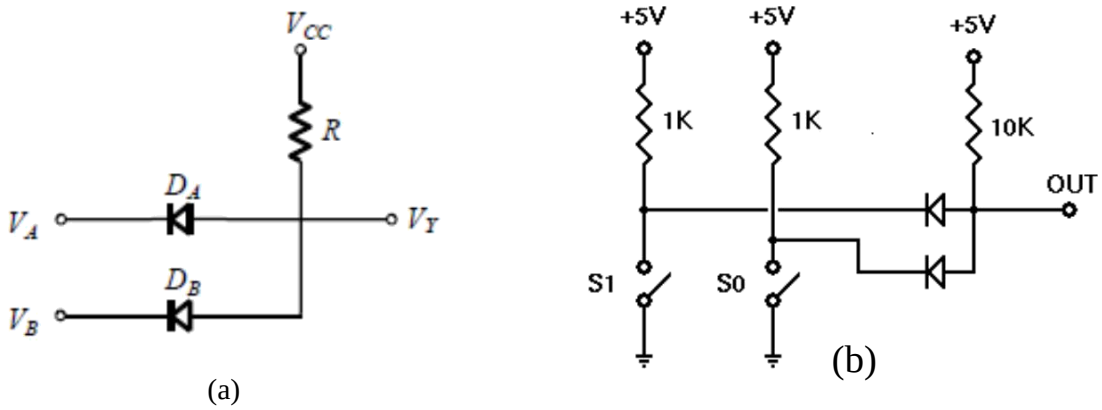


Fig.2 DL-AND Gate

Assuming the diodes are ideal, the voltage truth table of the above AND gate is as given in Table 2(a). The corresponding logic truth table is in Table 2(b).

V_A (volt)	V_B (volt)	V_Y (volt)
0	0	0
0	5	0
5	0	0
5	5	5

(a)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(b)

Table 2

Two-Input DL AND –OR Gate:

After looking at both the Diode Logic (DL) OR gate and AND gate and evaluating whether their operations were within acceptable parameters, the AND and OR gates will be cascaded. The OR gate will be used to combine the outputs of two AND gates and how well this combination works will be observed.

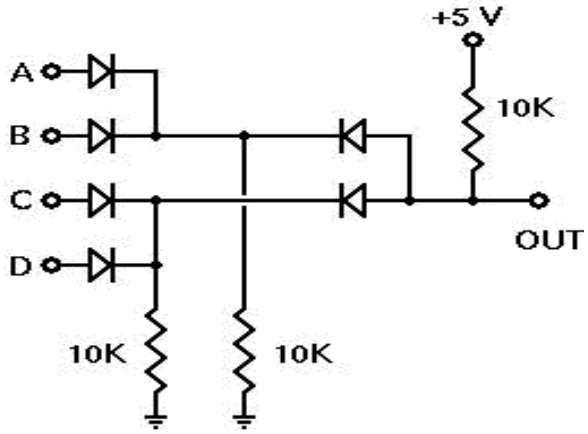


Fig.3 DL-AND-OR Gate

Diode polarity:

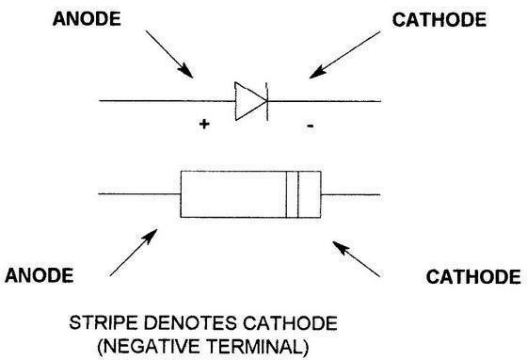


Fig.4 Diode polarity

Apparatus:

(1) 10K ohm resistor (brown-black-orange).

(2) 1N914/1N4002 diodes or equivalent.

(3) Connecting wires.

(4) Trainer Board

Precautions:

Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply only enough voltage (within V_{DD}) to turn on the transistors and/or chip, otherwise it may get damaged.

Experimental Procedure:

1. We have constructed the DL-OR gate on the breadboard as shown in Fig. 1. Then drew a Truth Table similar to the one provided and filled in our experimental results.

2. We constructed the DL-AND gate on the breadboard as shown in Fig. 2. Then drew a Truth Table similar to the one provided and filled in your experimental results.

3. We constructed the DL-AND-OR gate on the breadboard as shown in Fig. 3. Before beginning the experiment, we calculated the expected results for all the different input combinations and put them

in a Truth Table similar to the one provided. Then drew a second Truth Table and filled it with your experimental output values.

Part 2: Construction of Bipolar Transistor Logic Gate Introduction:

A bipolar transistor is a three-terminal semiconductor device. Under the control of one of the terminals, called the base, current can flow selectively from the collector terminal to the emitter terminal.

Fig 5: Bipolar junction transistor circuit symbols

In this experiment we examine how to build logic gates from bipolar transistors using the RTL, DTL and TTL design.

Theory and Methodology:

Resistor-Transistor Logic (RTL):

Resistor-Transistor Logic (RTL) is a large step beyond Diode Logic (DL). Basically, RTL replaces the diode switch with a transistor switch. If a +5v signal (logic 1) is applied to the base of the transistor (through an appropriate resistor to limit base-emitter forward voltage and current), the transistor turns fully on and grounds the output signal. If the input is grounded (logic 0), the transistor is off and the output signal is allowed to rise to +5 volts. In this way, the transistor not only inverts the logic sense of the signal, but it also ensures that the output voltage will always be a valid logic level under all circumstances. Because of this, RTL circuits can be cascaded indefinitely, where DL circuits cannot be cascaded reliably at all.

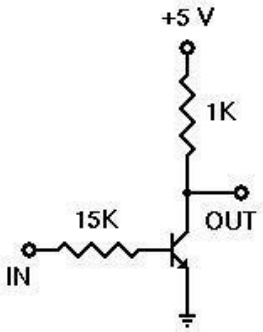


Fig.6: RTL Inverter

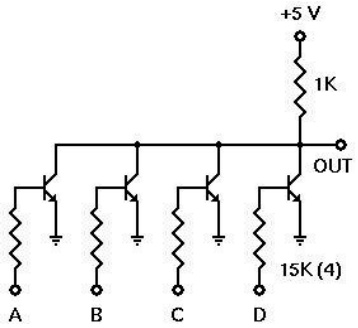


Fig .7: 4-input RTL Inverter

Diode-Transistor Logic:

Diode–Transistor Logic (DTL) is a class of digital circuits built from bipolar junction transistors (BJT), diodes and resistors; it is the direct ancestor of transistor–transistor logic (TTL).
DTL offers better noise margins and greater fan-outs than RTL, but suffers from low speed (especially in comparison to TTL).

RTL allows the construction of NOR gates easily, but NAND gates are relatively more difficult to get from RTL. DTL, however, allows the construction of simple NAND gates from a single transistor, with the help of several diodes and resistors.

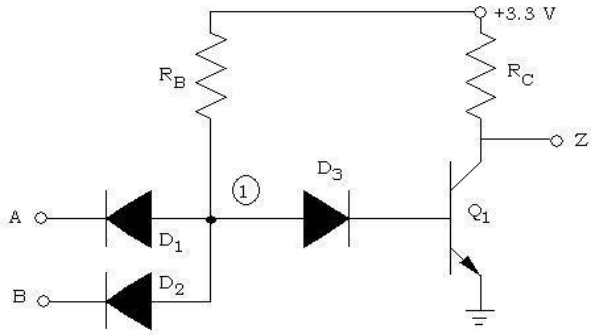


Fig 8: 2-input DTL NAND Gate

Transistor-Transistor Logic:

We can think of a bipolar transistor as two diodes placed very close together, with the point between the diodes being the transistor base. Thus, we can use transistors in place of diodes to obtain logic gates that can be implemented with transistors and resistors only; this is called transistor-transistor logic (TTL).

One problem that DTL doesn't solve is its low speed, especially when the transistor is being turned off. Turning off a saturated transistor in a DTL gate requires it to first pass through the active region before going into cut-off. Cut-off, however, will not be reached until the stored charge in its base has been removed. The dissipation of the base charge takes time if there is no available path from the base to ground. This is why some DTL circuits have a base resistor that's tied to ground, but even this requires some trade-offs. Another problem with turning off the DTL output transistor is the fact that the effective capacitance of the output needs to charge up through Rc before the output voltage rises to the final logic '1' level, which also consumes a relatively large amount of time. TTL, however, solves the speed problem of DTL elegantly.

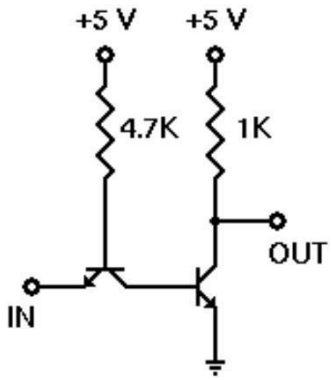


Fig 9: TTL Inverter

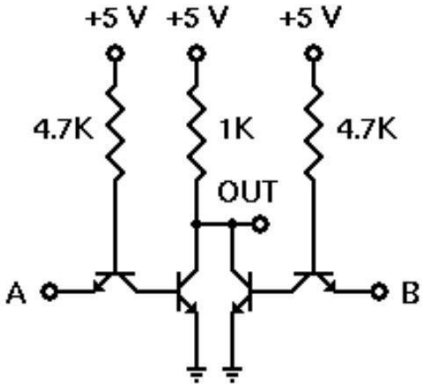
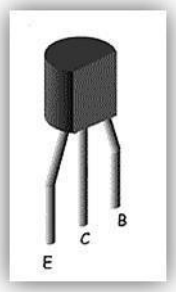


Fig 10: 2-input TTL NOR gate

BJT pin configuration:



Pre-Lab Homework:

Explain how n-p-n BJT transistors work?

Students must install PSpice/LTSpice/ Psim software and MUST present the simulation results using transistors to the instructor before the start of the experiment.

Apparatus:

1. 2N4124 NPN silicon transistor (or equivalent).
2. Resistors 15KΩ, 1KΩ, 4.7 KΩ
4. Connecting wires.
5. Trainer Board

Precautions:

We have our instructor check all our connections after we were done setting up the circuit and made sure that we have applied only enough voltage (within V_{DD}) to turn on the transistors and/or chip, otherwise it may get damaged.

Experimental Procedure:

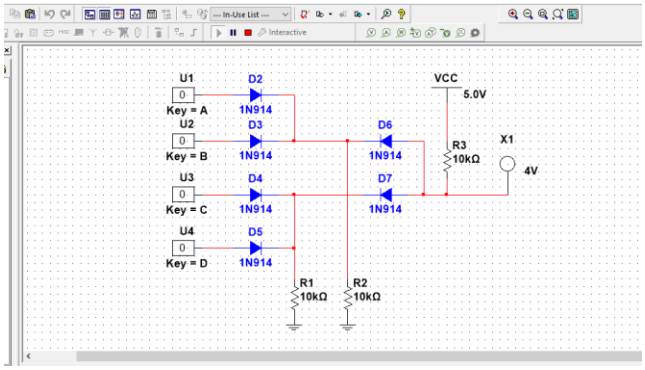
(1) We have set up the circuit for 2-input DL AND -OR gate as shown in Fig.3, 2-input DTL NAND Gate as shown in Fig.8 and 2-input TTL NOR gate as shown in Fig.10
(2) For each input combination, we have found the output and placed them in a Truth Table.
(3) Lastly, we have simulated the circuit and compared experimental and simulated outputs.

Truth Table (2-Input DL AND –OR Gate):

For equation, Y = (A+B) (C+D)

A	B	C	D	(A+B) (C+D)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Simulation and Measurement (2-Input DL AND –OR Gate):



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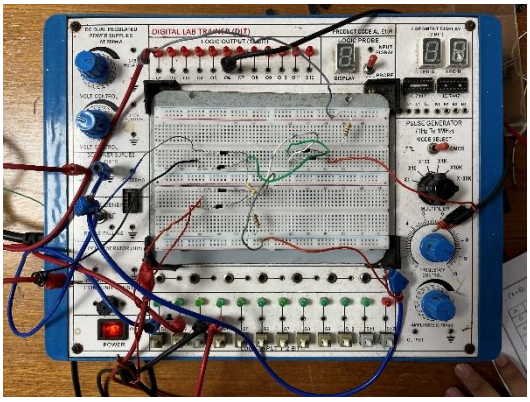

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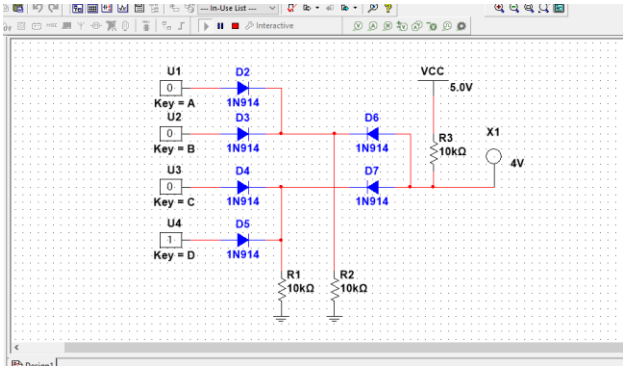

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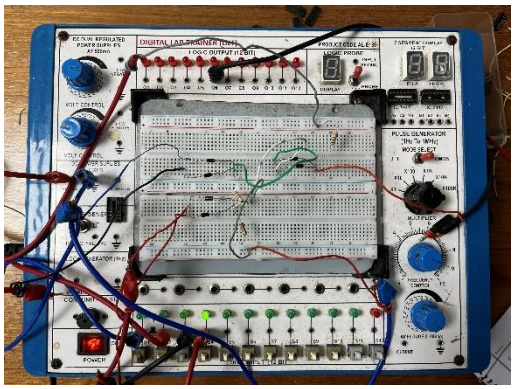

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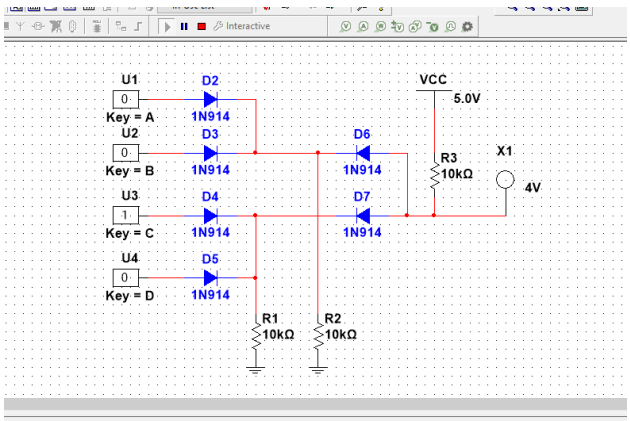

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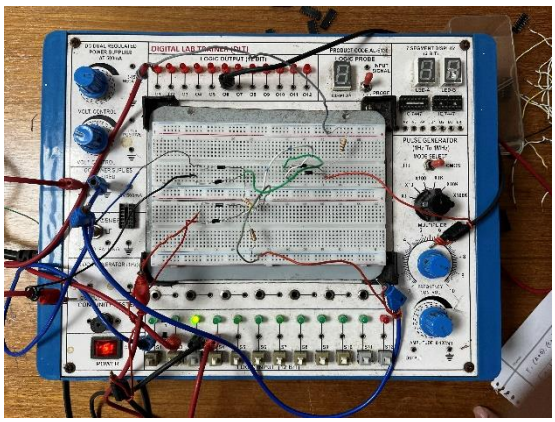

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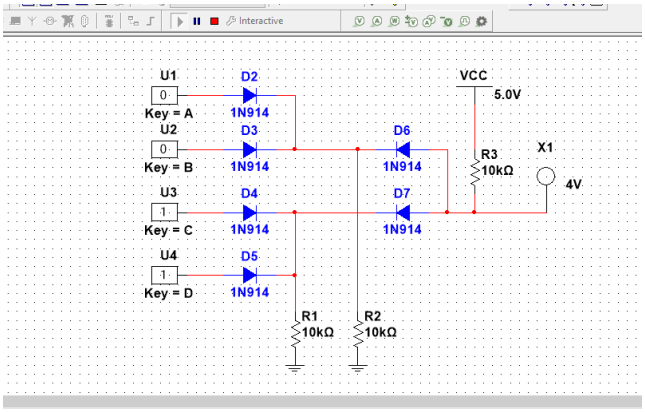

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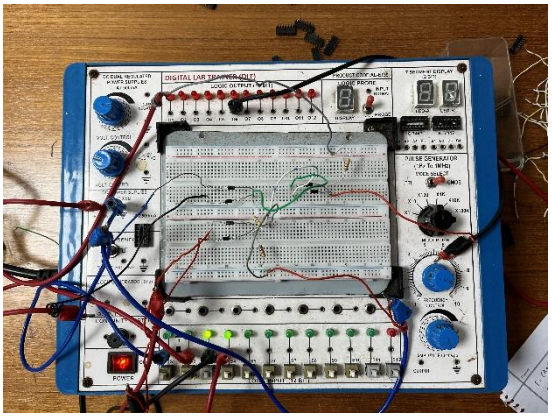

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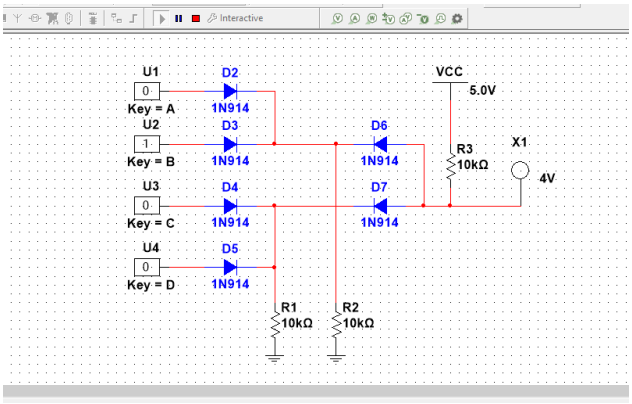

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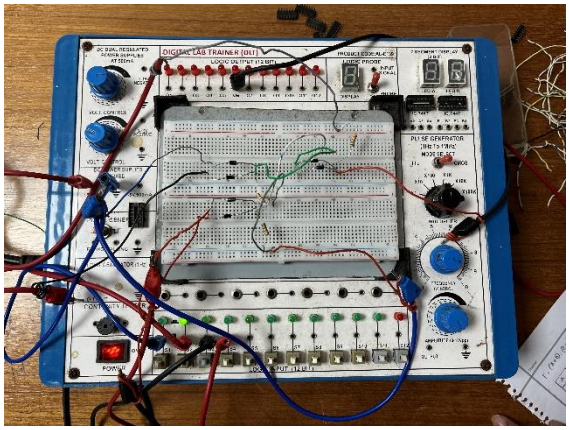

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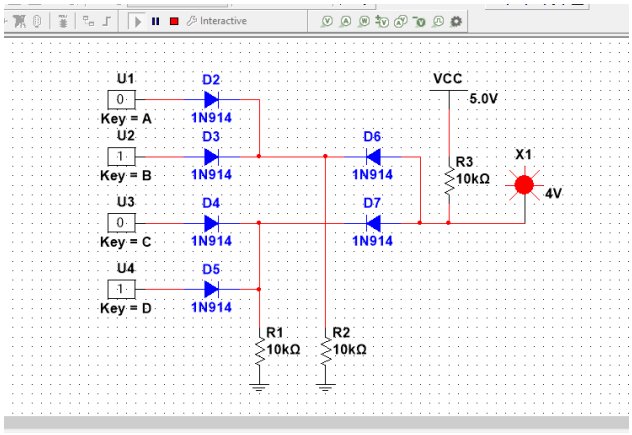

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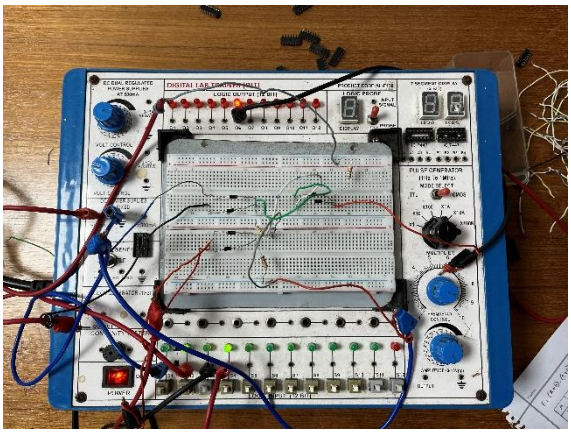

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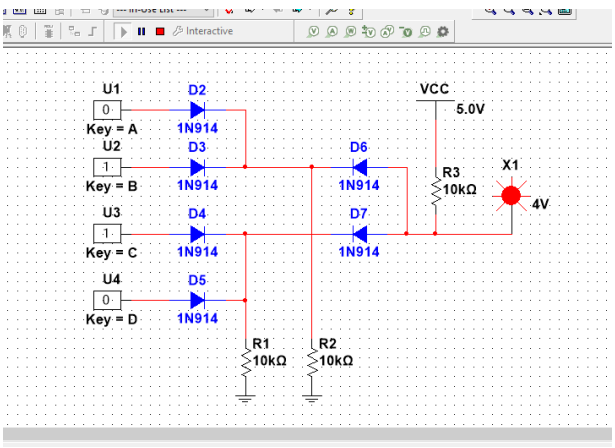	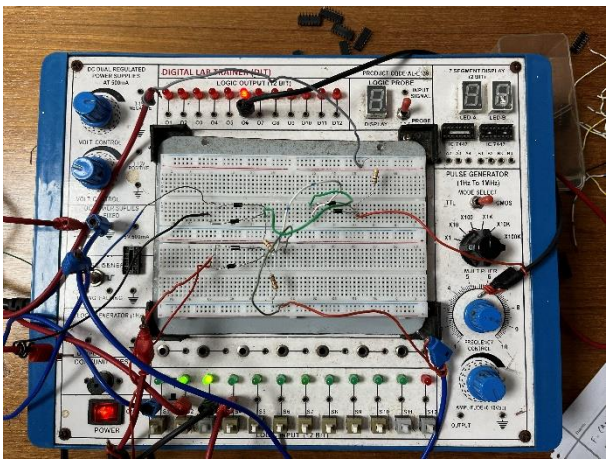
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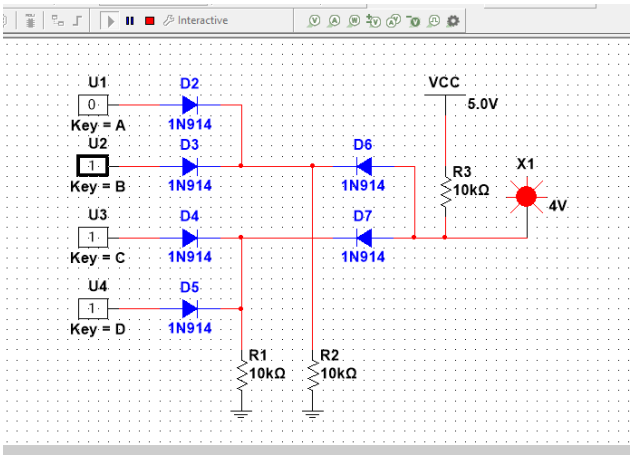	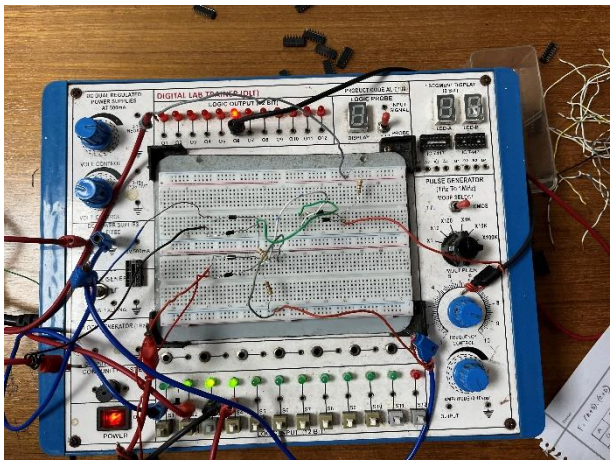
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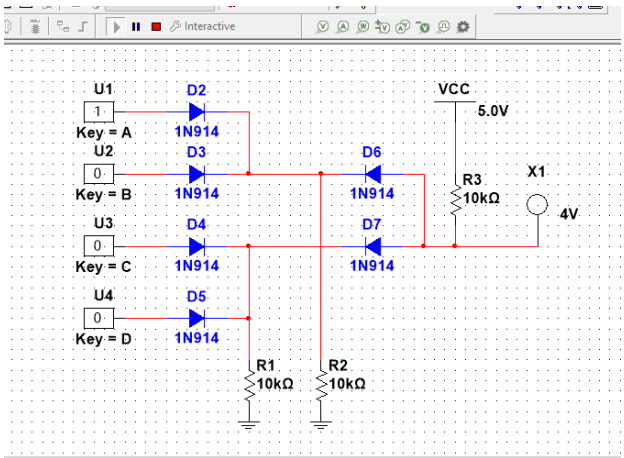	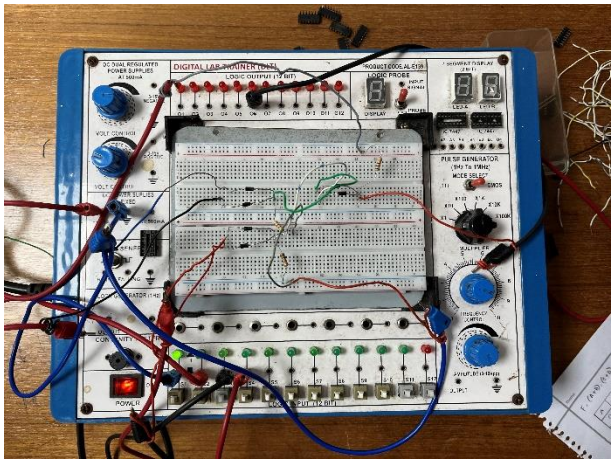
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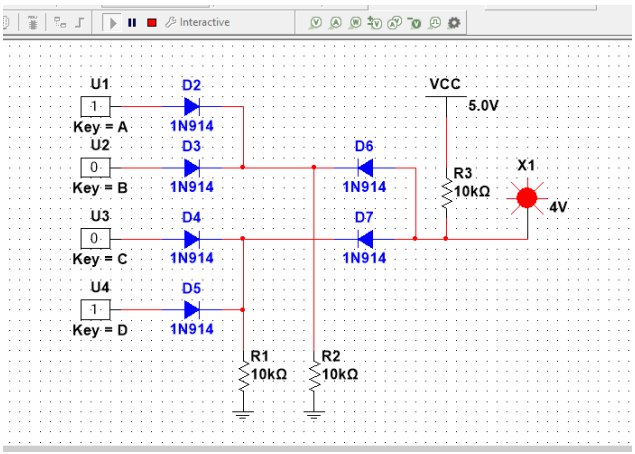

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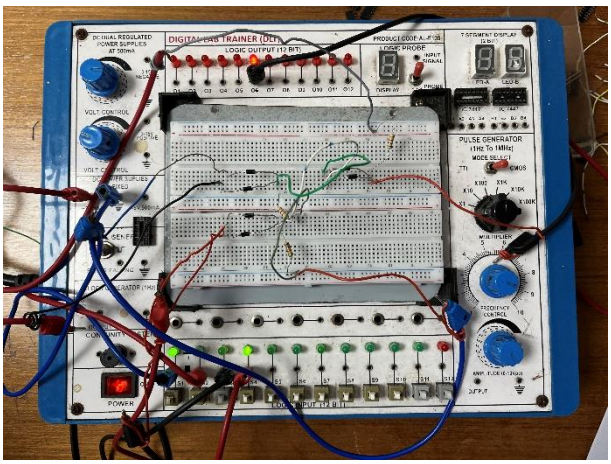

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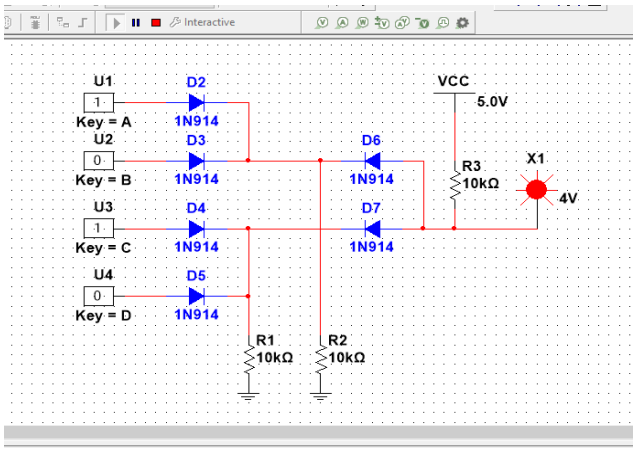

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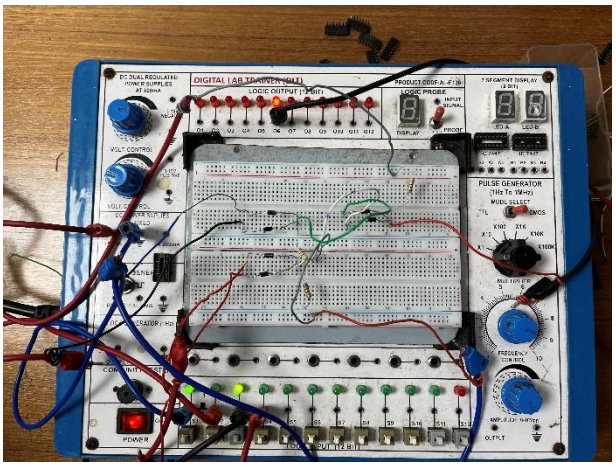

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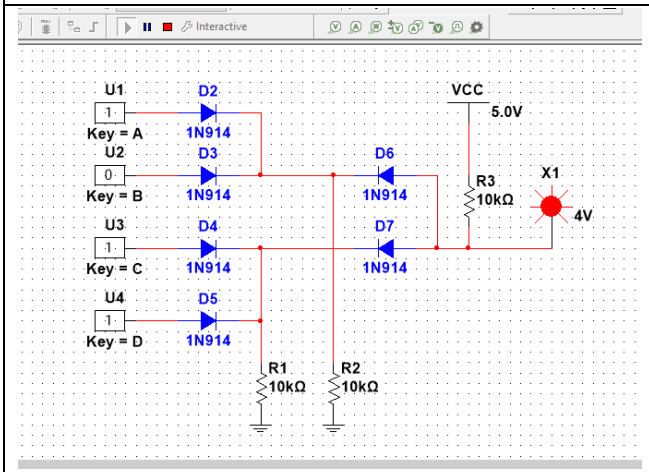

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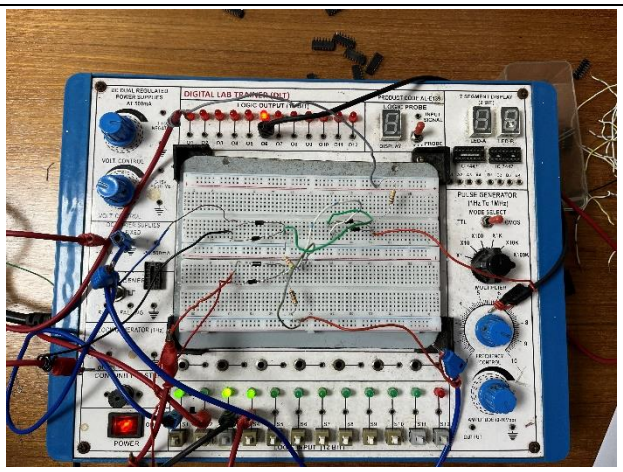

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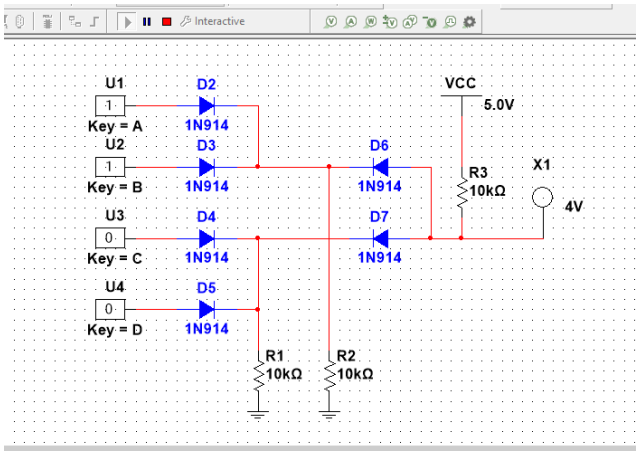

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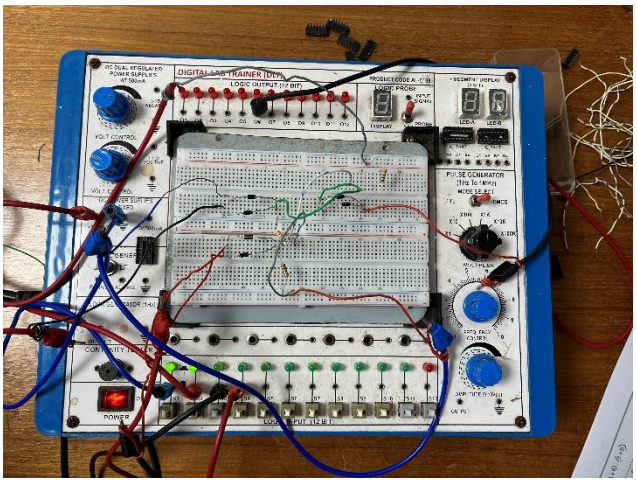

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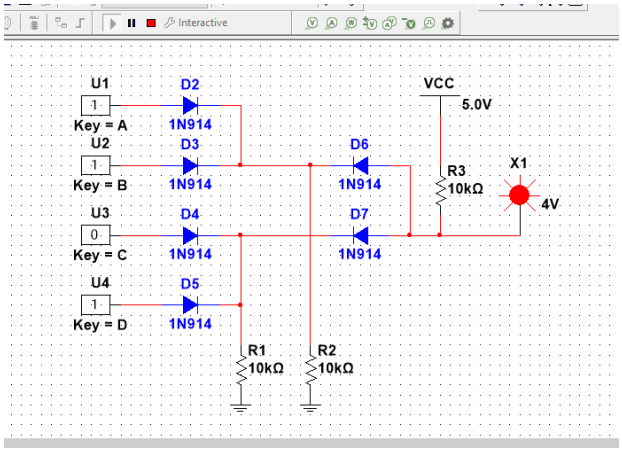

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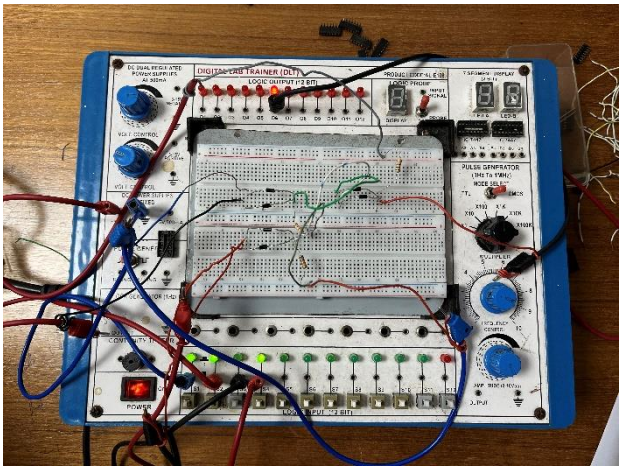
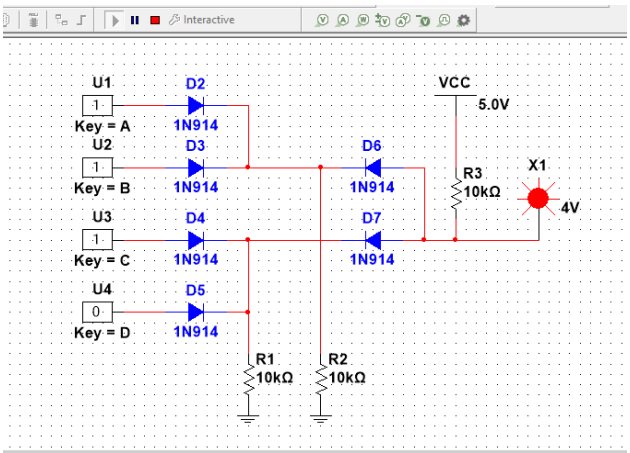


A=1, B=1, C=0, D=1



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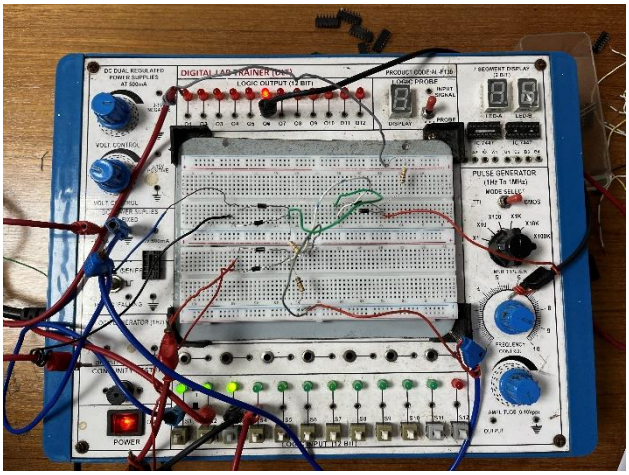
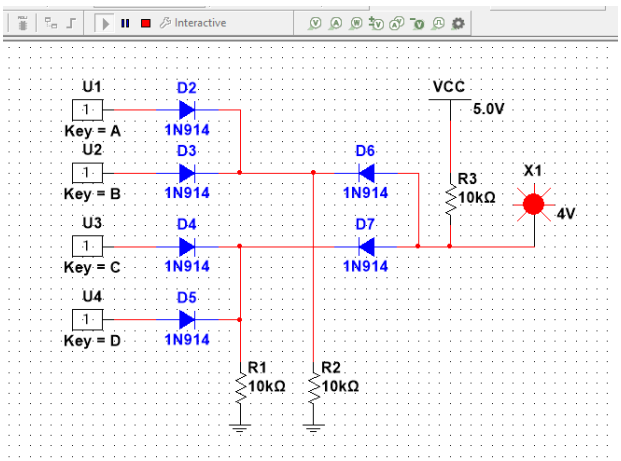
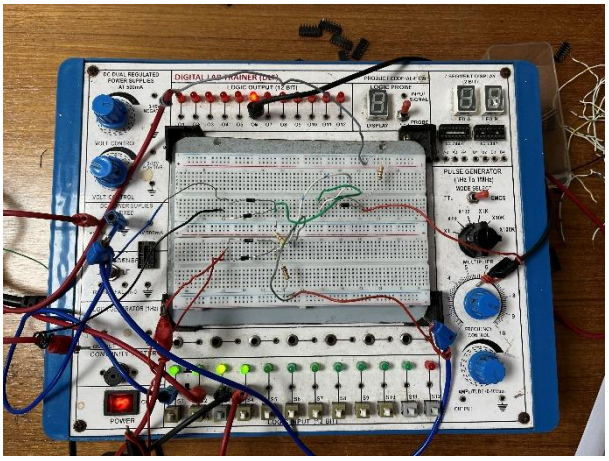


A=1, B=1, C=1, D=0



A=1, B=1, C=1, D=1



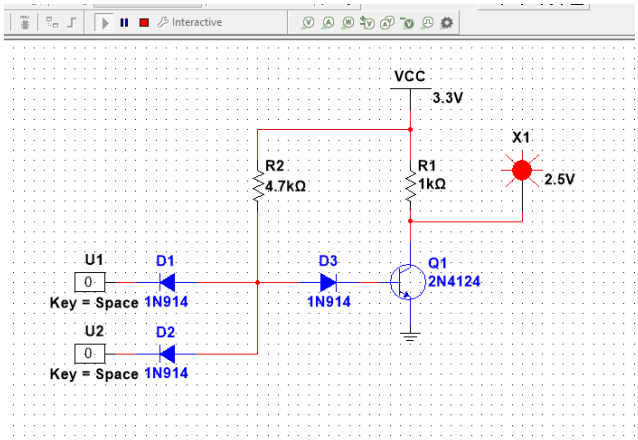
A=1, B=1, C=1, D=1

Truth Table (2-input DTL NAND Gate):

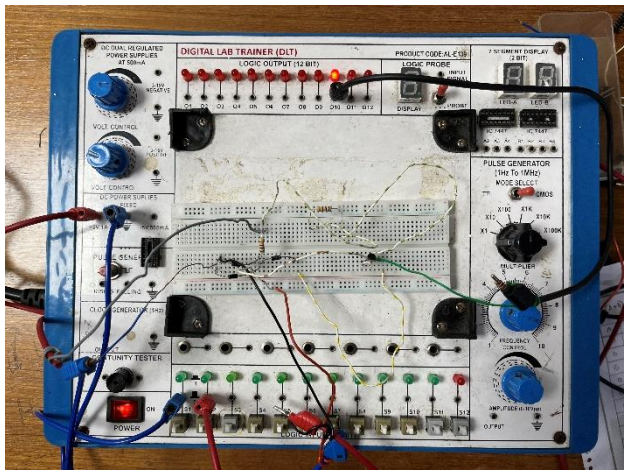
For equation, Y = $\overline{A.B}$

A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

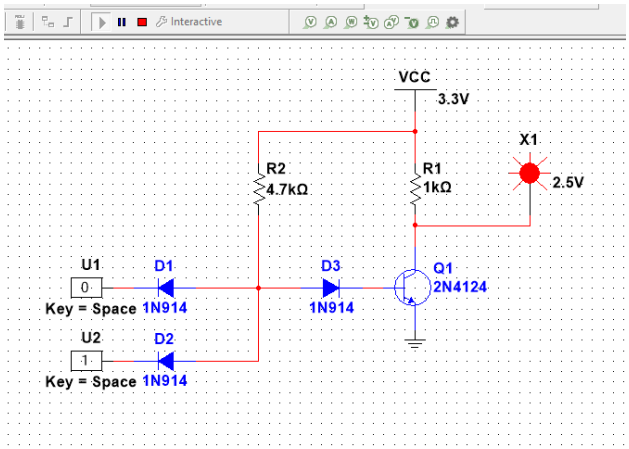
Simulation and Measurement (2-input DTL NAND Gate):



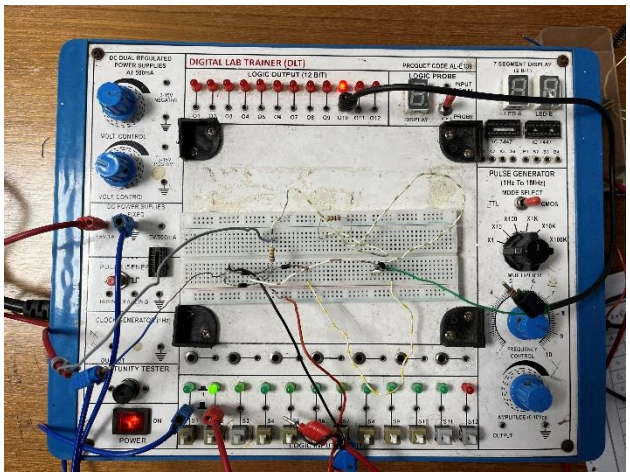
A=0, B=0



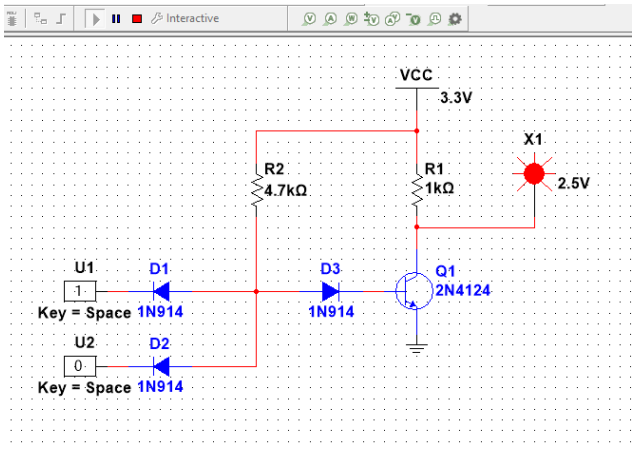
A=0, B=0



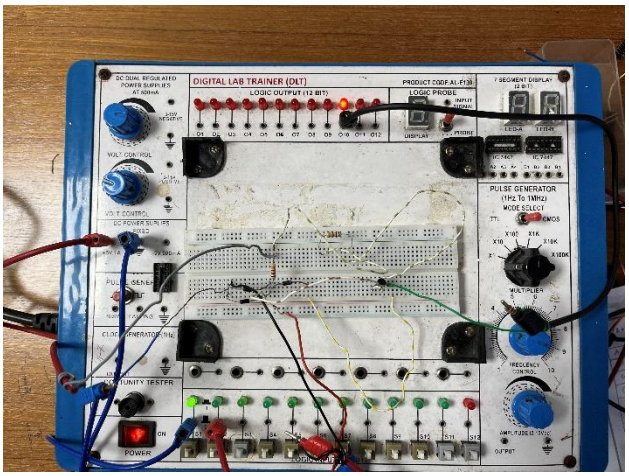
A=0, B=1



A=0, B=1



A=1, B=0



A=1, B=0

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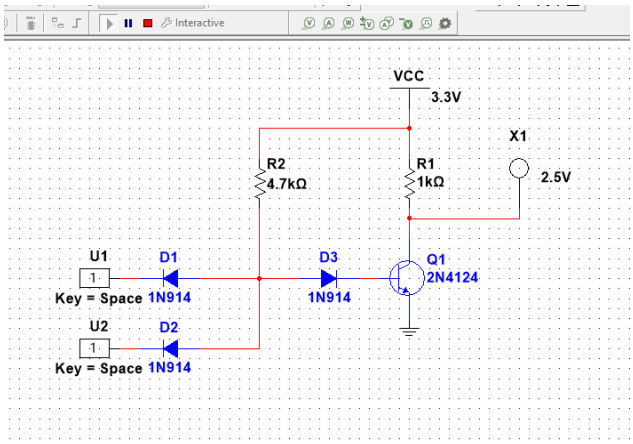
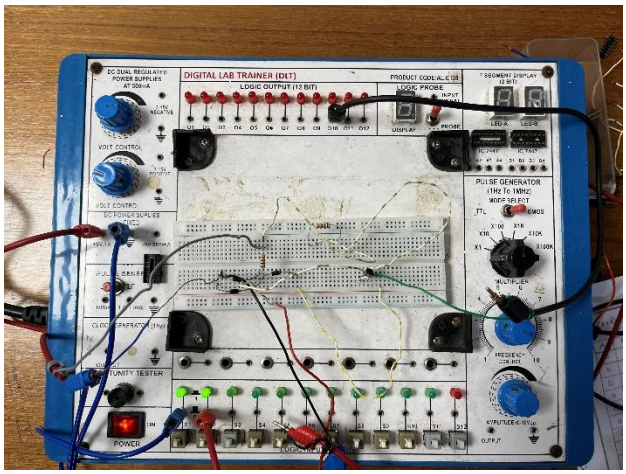
<td> 

A=1, B=1</td>
<td> 

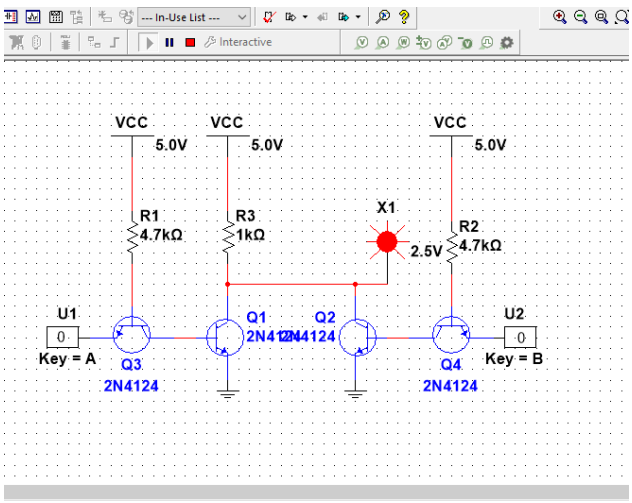
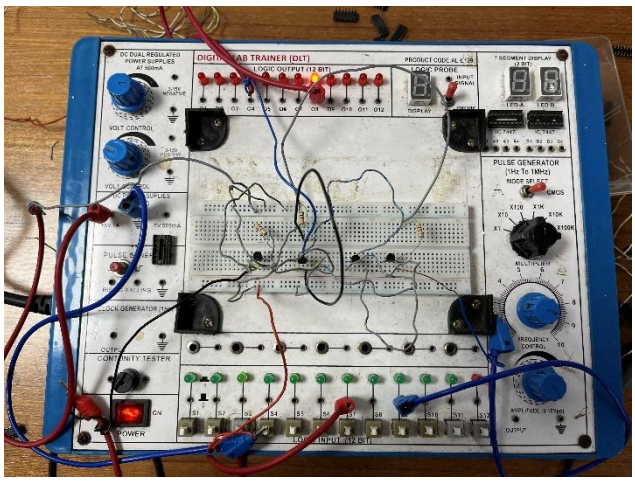
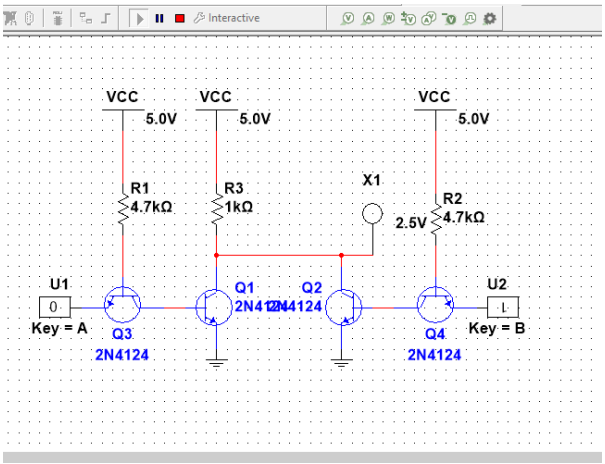
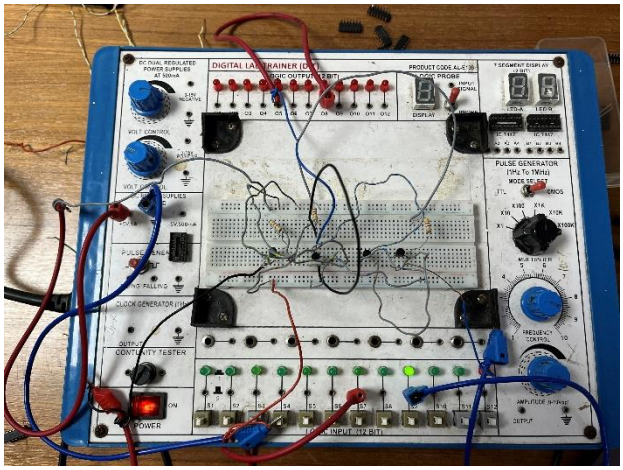
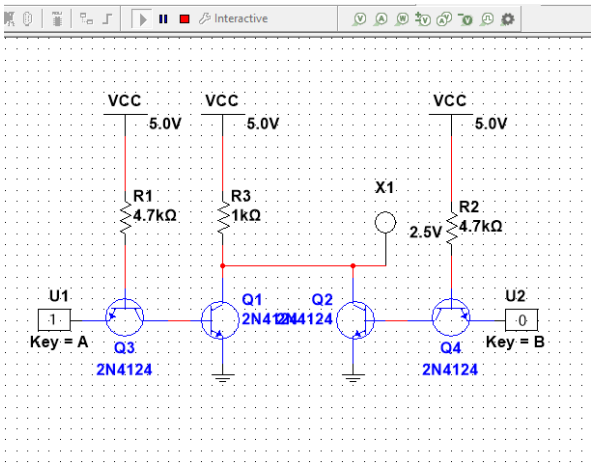
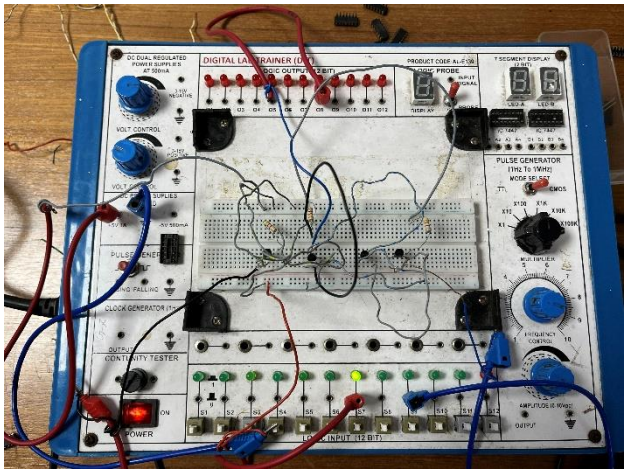
A=1, B=1</td>
</tr>
</table>

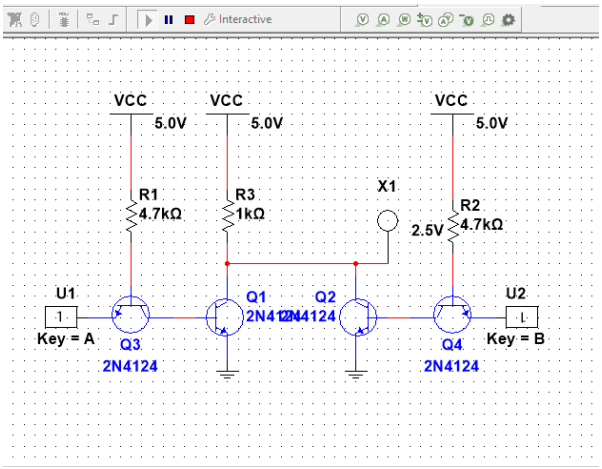
Truth Table (2-input TTL NOR gate) :

For equation, Y = $\overline{A + B}$

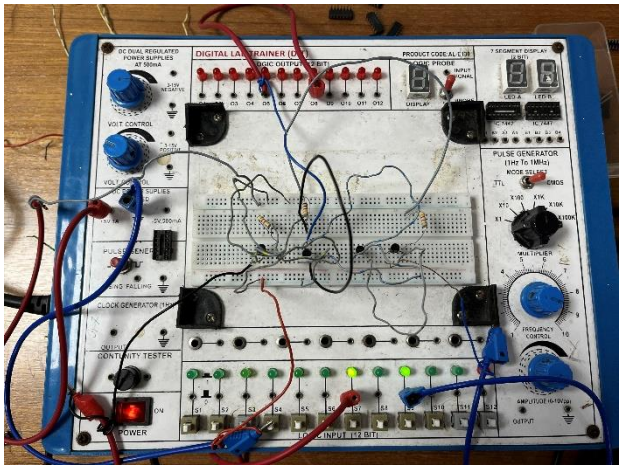
A	B	$\overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

Simulation and Measurement (2-input TTL NOR gate):

	
A=0, B=0	A=0, B=0
	
A=0, B=1	A=0, B=1
	
A=1, B=0	A=1, B=0



A=1, B=1



A=1, B=1

Results and Discussion:

From the first part of the experiment, we have learned about constructing different logic gates using semiconductor devices. Using diode logic circuits, we constructed OR gate, AND gate and combination of both.

From second part of experiment, we examined how to build logic gates from bipolar transistors using the RTL, DTL and TTL design. We can now successfully construct RTL inverter, NAND gate using DTL, NOR gate using TTL and with as many inputs as we need to construct our expected circuits.

In this group of experiments, we implemented some logic functions using the DL and Bipolar Transistor logic circuits and discovered the potential benefits and problems of using them.

RTL allows the construction of NOR gates easily, but NAND gates are relatively more difficult to get from RTL. DTL, however, allows the construction of simple NAND gates from a single transistor, with the help of several diodes and resistors.

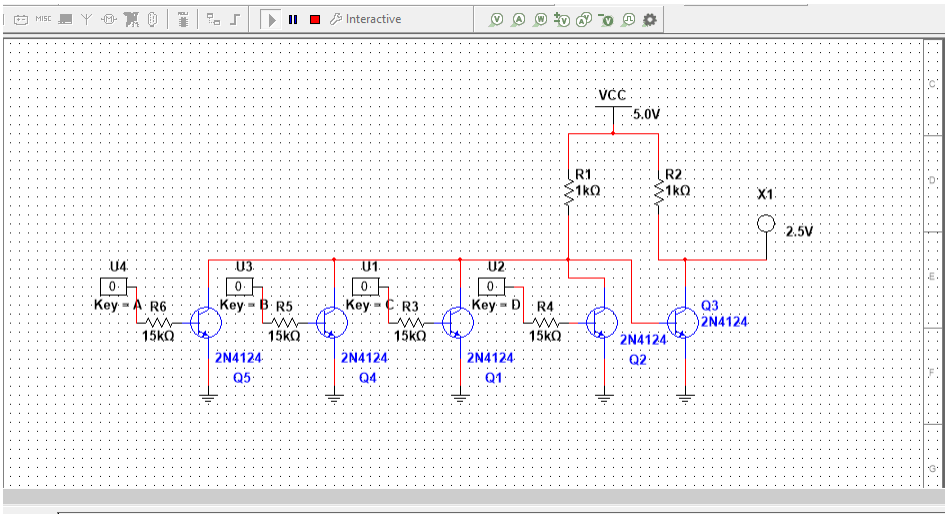
DTL is low on speed because the dissipation of the base charge takes time if there is no available path from the base to ground. DTL effective capacitance of the output needs to charge up through Rc before the output voltage. TTL, however, solves the speed problem of DTL elegantly.

Report:

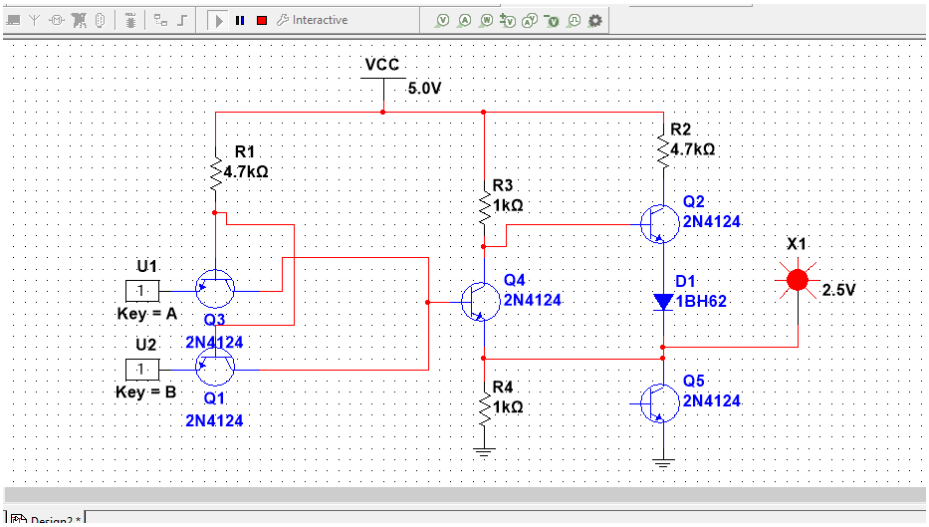
4. For, each of the above set-ups, describe in words what the data means. Did your results match the expected ideal outputs? If not, explain why?
5. Design RTL 4-input OR gates.
6. Design 2-input TTL NAND and NOR gates.

Solution:

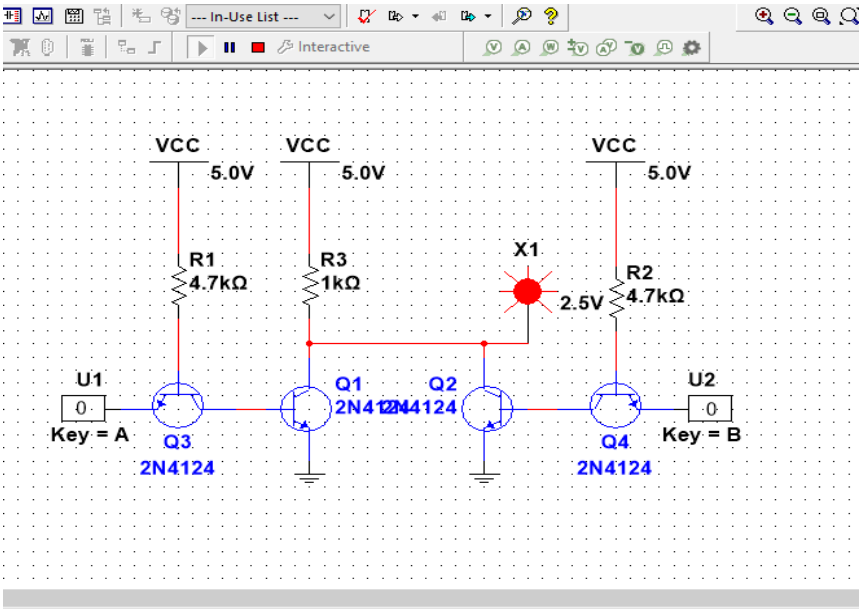
4. For each above set-ups, for various inputs we have found different outputs, where we considered low level voltage as ‘0’ logic and High level voltage as ‘1’ logic. Therefore we determined that the results match with ideal outputs using truth table.



5. Figure: RTL 4-input OR gates.



6. Figure: 2-input TTL NAND and 2-input TTL OR Gates



Reference(s):

1. Thomas L. Floyd, *Digital Fundamentals*, 9th Edition, 2006, Prentice Hal