AMERICAN INTERNATIONAL UNIVERSITY BANGLADESH
Faculty of Engineering

Laboratory Report Cover Sheet
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Please submit all reports to your subject supervisor or the office of the concerned faculty.

Lab Title: Implementation of Asynchronous and synchronous counters using flip-flops.

Experiment Number: **07** Due Date: 09 /12/2023 Semester: Fall 2023-2024

Subject Code: **EEE3102** Subject Name: DIGITAL LOGIC AND CIRCUITS LAB Section: **L**

Course Instructor: **NUZAT NUARY ALAM** Degree Program: **B.Sc. CSE**

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Title: Implementation of Asynchronous and synchronous counters using flip-flops.

Introduction:

Counters are combinations of flip-flops arranged so that they can remember how many clock pulses have been applied over some specified interval. The flip-flops are often interconnected so that only a portion of their available binary states can be supported. If there are N flip-flops being used in a counter, the number of states available is 2N. If the counter proceeds cyclically through K of these states, where $K \leq 2N$, it is said to be a modulo K (or MOD K) counter. Some applications will require a separate output to indicate each of the counter's states, alternatively, other applications may require only one output pulse for every Kth state.

Counters are classified into two broad categories according to the way they are clocked: asynchronous and synchronous. In asynchronous counters, commonly called ripple counters, the first flip-flop is clocked by the external clock pulse and then each successive flip flop is clocked by the output of the preceding flip-flop. In synchronous counters, the clock input is connected to all the flip-flops so that they are clocked simultaneously.

The objective of this experiment is designing of the following counters using J-K Flip-Flops (IC 74LS76)

(a)n-bit Binary Asynchronous Counter
(b)n-bit Binary Synchronous Counter

Theory and Methodology:

Asynchronous counter:

A three-bit asynchronous counter is shown in figure 9.1. The external clock is connected to the clock input of the first flip-flop (FF0) only. So, FF0 changes state at the falling edge of each clock pulse, but FF1 changes only when triggered by the falling edge of the Q output of FF0. Because of the inherent propagation delay through a flip-flop, the transition of the input clock pulse and a transition of the Q output of FF0 can never occur at the same time. Therefore, the flip-flops cannot be triggered simultaneously, producing an asynchronous operation.

Figure 9.1 gives a three-bit counter capable of counting from 0 to 7. The clock inputs of the three flip-flops are connected in cascade. The T input of each flip-flop is connected to a constant 1, which means that the state of the flip-flop will be reversed (toggled) at each positive edge of its clock. We are assuming that the purpose of this circuit is to count the number of pulses that occur on the primary input called Clock. Thus, the clock input of the first flip-flop is connected to the Clock line. The other two flip-flops have their clock inputs driven by the Q output of the preceding flip-flop. Therefore, they toggle their state whenever the preceding flip-flop changes its state from Q = 1toQ = 0, which results in a positive edge of the Q signal.
Figure 9.1 shows a timing diagram for the counter. The value of Q0 toggles once each clock cycle. The change takes place shortly after the positive edge of the Clock signal. The delay is caused by the propagation delay through the flip-flop. Since the second flip-flop is clocked by Q0, the value of Q1 changes shortly after the negative edge of the Q0 signal. Similarly, the

value of Q2 changes shortly after the negative edge of the Q1 signal. If we look at the values Q2Q1Q0 as the count, then the timing diagram indicates that the counting sequence is 0, 1, 2, 3, 4, 5, 6, 7, 0, 1, and so on. This circuit is a modulo-8 counter. Because it counts in the upward direction, we call it an up-counter.

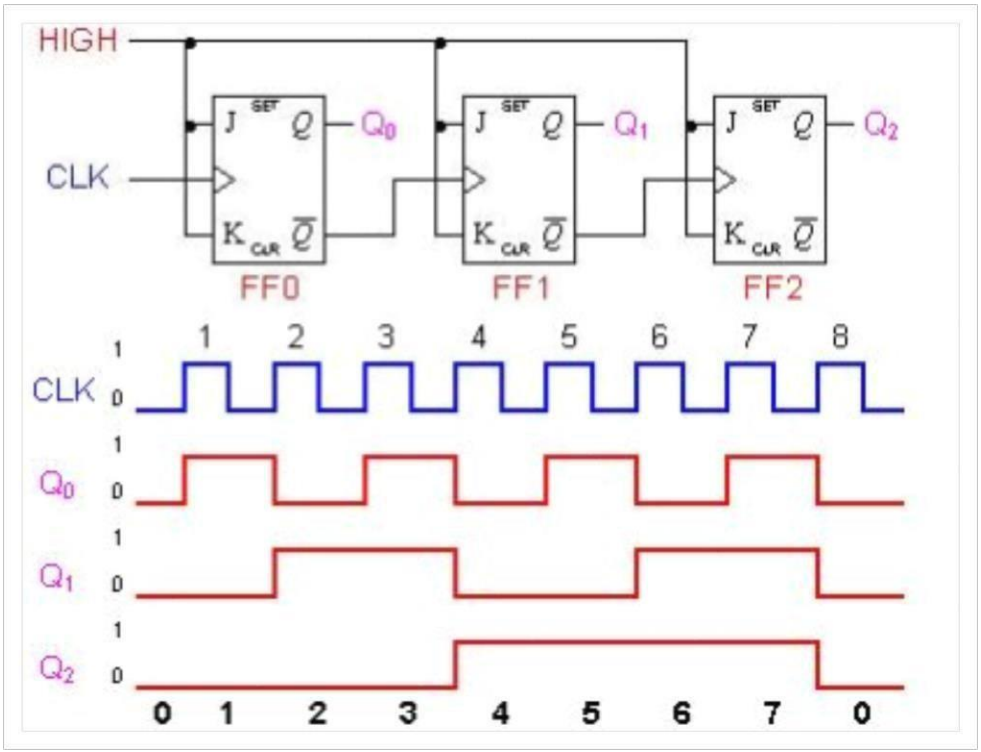

Figure 9.1: 3-bit Asynchronous counter and its timing diagram Synchronous

Table 9.1 shows the contents of a four-bit up-counter for eight consecutive clock cycles, assuming that the count is initially 0. Observing the pattern of bits in each row of the table, it is apparent that bit Q0 changes on each clock cycle. Bit Q1 changes only when Q0 = 1. Bit Q2 changes only when both Q1 and Q0 are equal to 1. In general, for an n-bit up-counter, a given flip-flop changes its state only when all the preceding flip-flops are in the state Q = 1.

Table 9.1

T0 = 1

Clock cycle	Q_2 Q_1 Q_0
0	0 0 0
1	0 0 1
2	0 1 0
3	0 1 1
4	1 0 0
5	1 0 1
6	1 1 0
7	1 1 1
8	0 0 0

Q_1 changes

Q_2 changes

The Circuit diagram of a four-bit counter based on these expressions is given in Figure 9.2a. Figure 9.2b gives a timing diagram. It shows that the circuit behaves as a modulo-16 up- counter. Because all changes take place with the same delay after the active edge of the Clock signal, the circuit is called a synchronous counter.

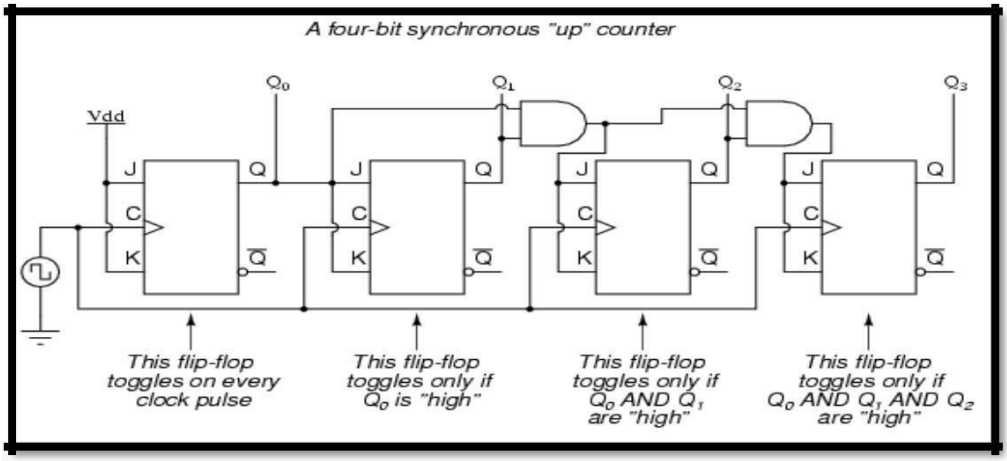

Figure 9.2a: A four-bit Synchronous Up Counter

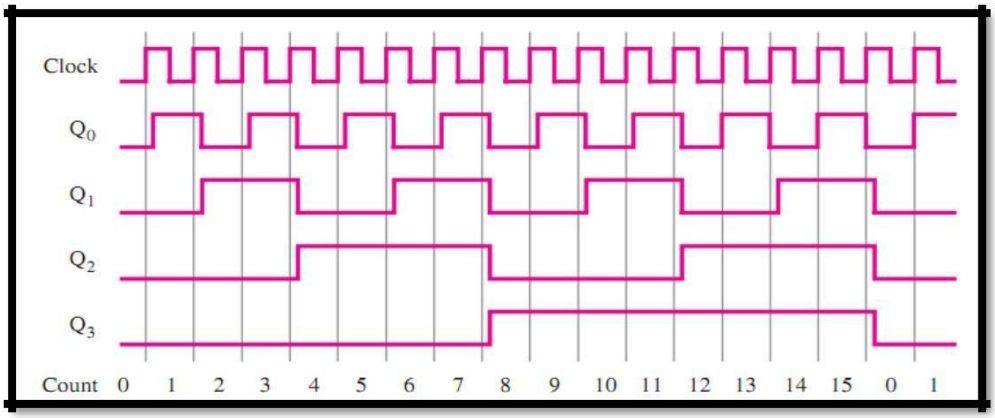

Figure 9.2b: The timing diagram of a four-bit Synchronous Up Counter

Pin Configuration of 74LS76 and 7408:

There are 2 J-K Flip Flops in one IC. Here is the pin configuration of the IC 74LS76:

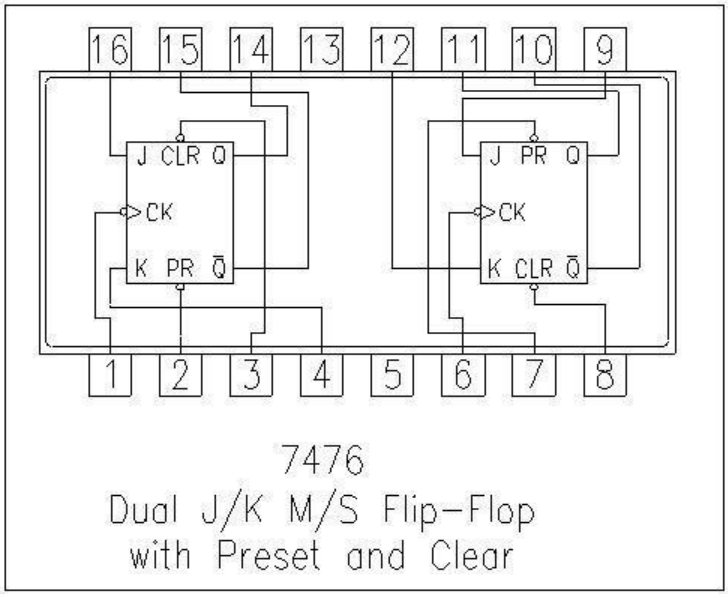

Figure 9.3: IC 74LS76

IC 7408 contains 4 AND gates in it. The pin configuration is shown below:

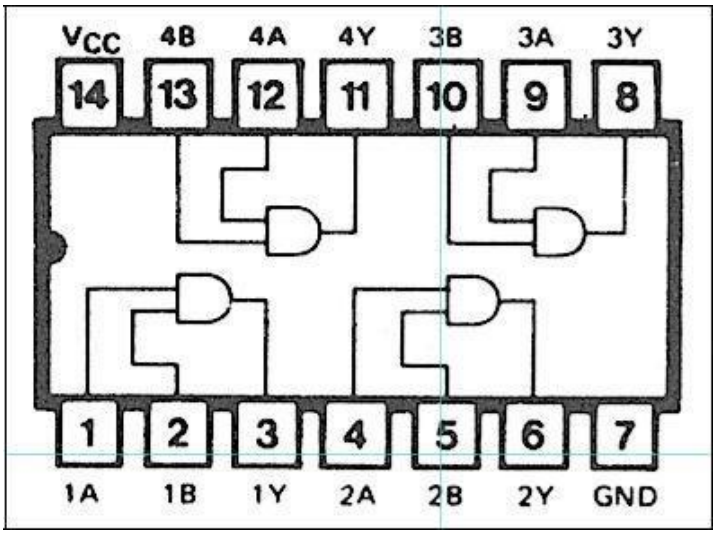

Figure 9.4: IC 7408

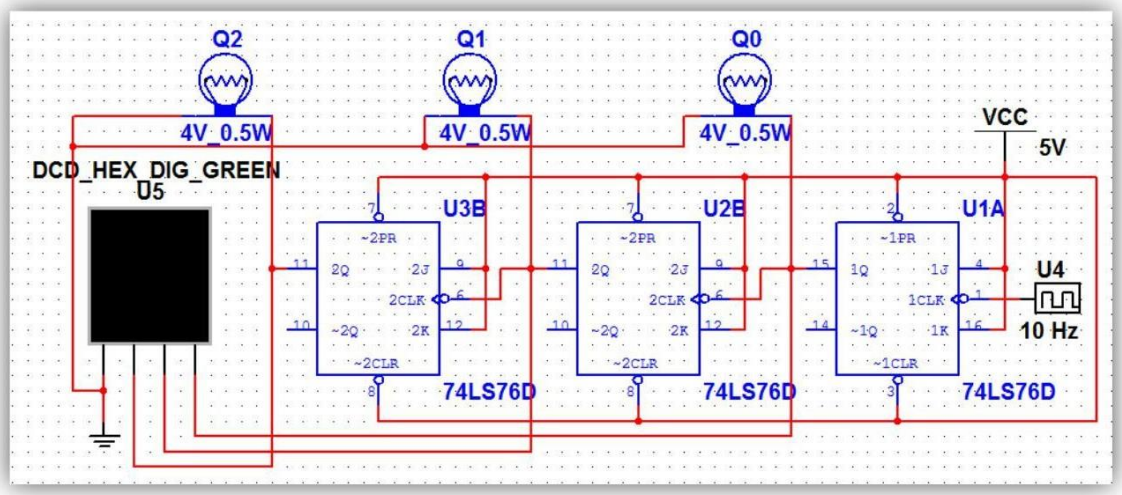

Fig 9.5: 3-bit Asynchronous Counter

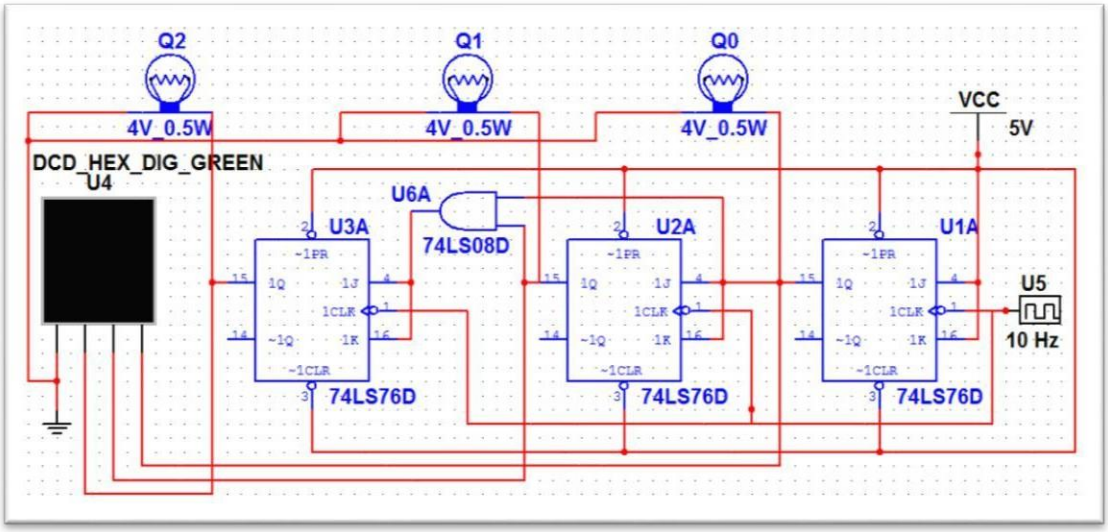

Fig 9.6: 3-bit Synchronous Counter

Pre-Lab Homework:

1. Write down in detail the operation of JK Flip Flops mentioning its circuit diagram, truth table and timing diagram (also mention about the asynchronous inputs).
2. Also write down in brief the operations of other different types of Flip Flops.

Apparatus:

- IC 74LS76 (JK Flip Flop)
- IC 7408 (AND Gate)
- LED Lamps or Display
- Trainer Board
- Oscilloscope
- Connecting Wires

Precautions:

- Before preparing the circuits, check all the ICs (74LS76 & 7408) to make sure they are all working properly.
- Careful about the biasing of JK Flip Flops.
- Make sure you connect the preset and clear pins with Vcc.
- Try to use as less wire as possible. Make sure there is no loose connection.
- If you use an LED display, then make sure you biased it properly.
- For Clock pulse, the trainer board's analog signal generator is a good choice. Use lower frequencies so that the change is slow enough to observe the outputs and take readings.

Experimental Procedure:

Part 1: 3-bit Asynchronous Counter:

1. Design the circuit on the bread board as shown in Figure 9.5.
2. Use the trainer board's signal generator for the clock pulse and power supply for biasing the Flip Flops.
3. The output can also be viewed in oscilloscope, just connect the outputs to the different channels of the oscilloscope.
4. Observe the output results, record them, and take some pictures for your lab report.

3-bit Synchronous Counter:

1. Design the circuit on the bread board as shown in Figure 9.6.
2. Use the trainer board's signal generator for the clock pulse and power supply for biasing the Flip Flops.
3. The output can also be viewed in oscilloscope, just connect the outputs to the different channels of the oscilloscope.
4. Observe the output results and take some pictures for your lab report.

Simulation and Measurement:

3-bit Asynchronous Up Counter:

Truth Table:

CLK	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

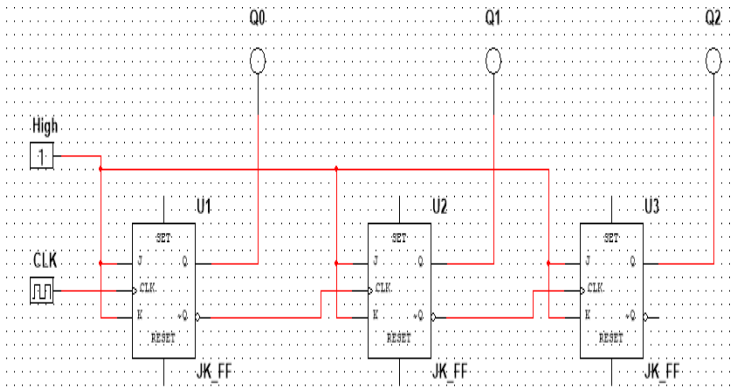

Figure: 3-bit Asynchronous up counter

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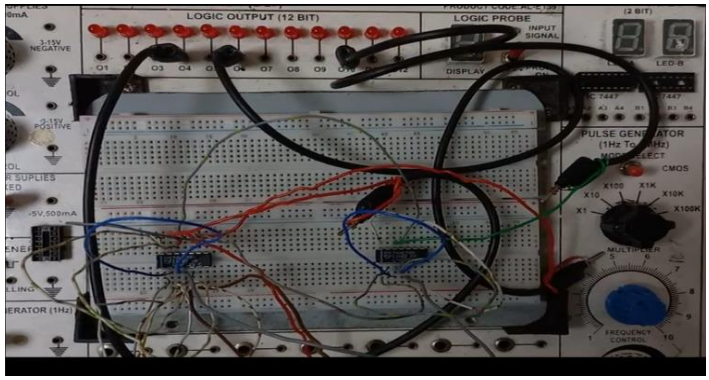	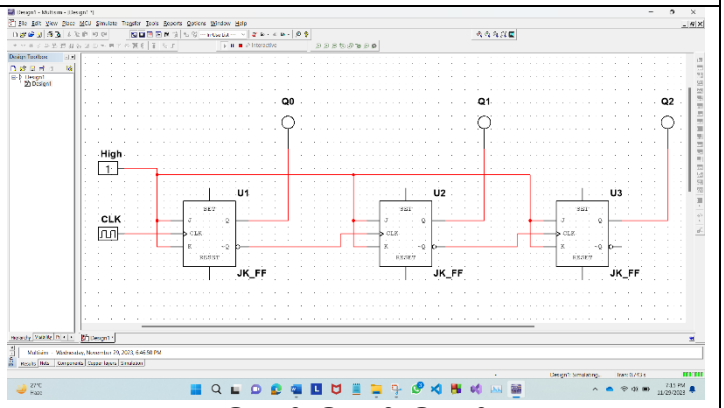
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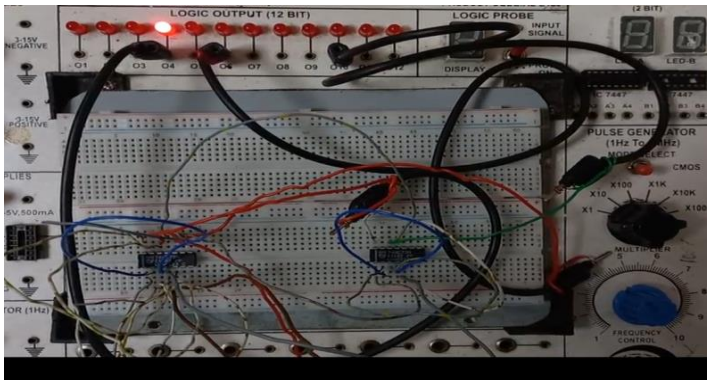	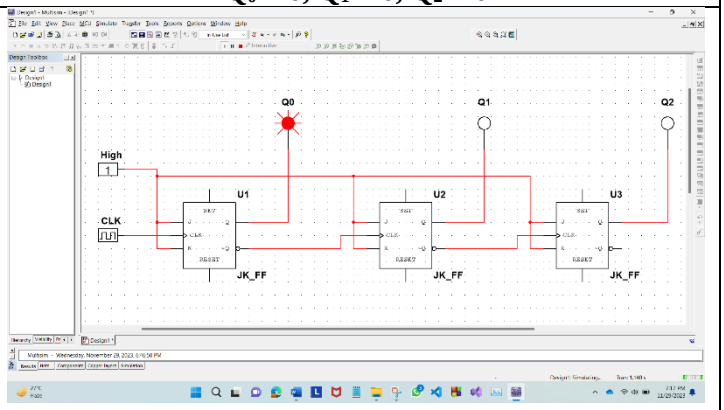
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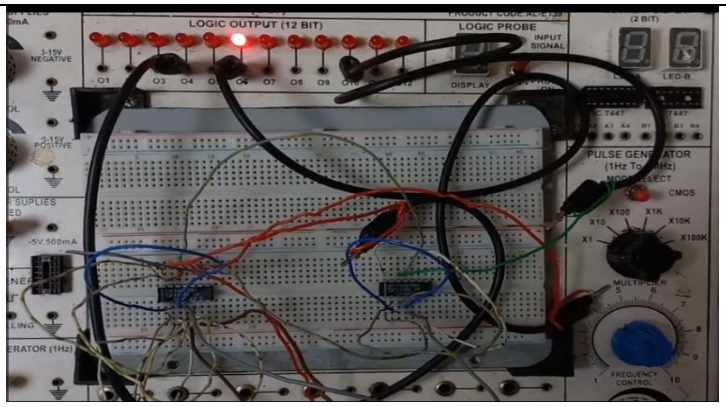	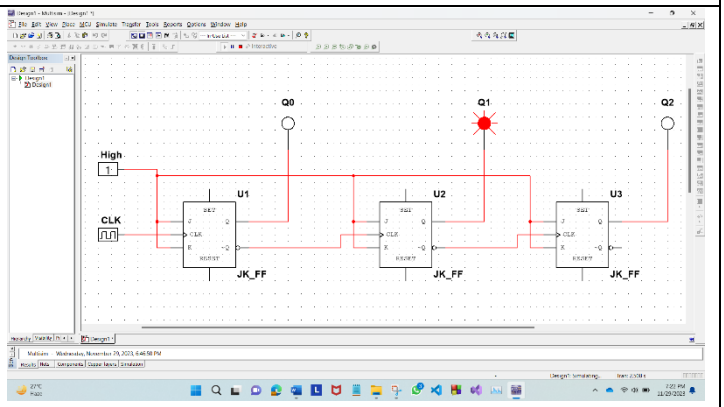
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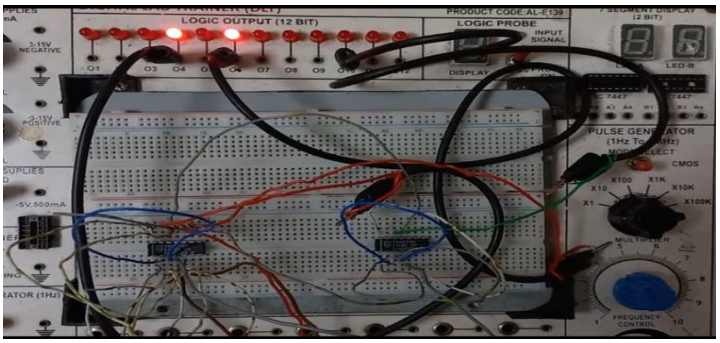	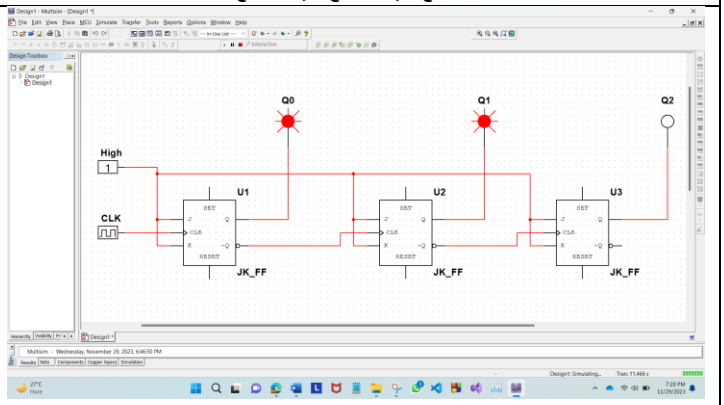
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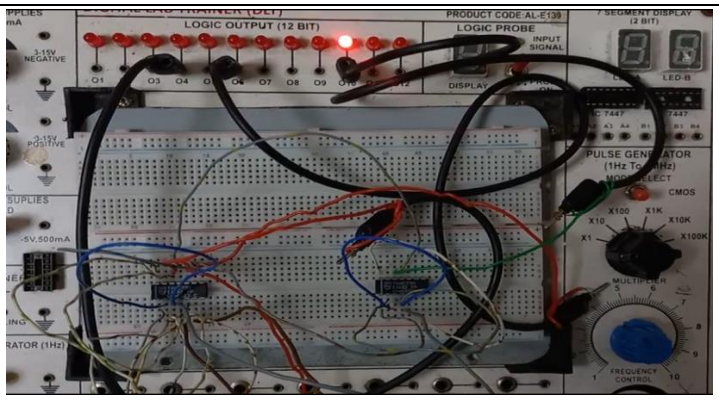	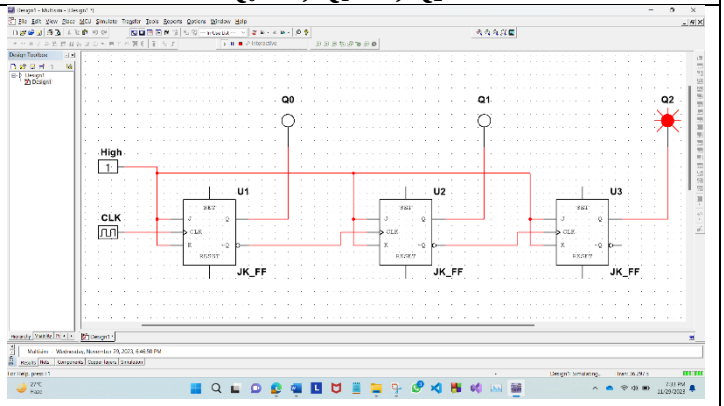
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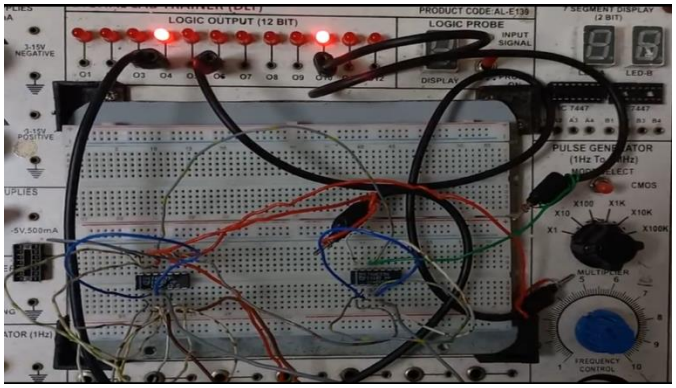	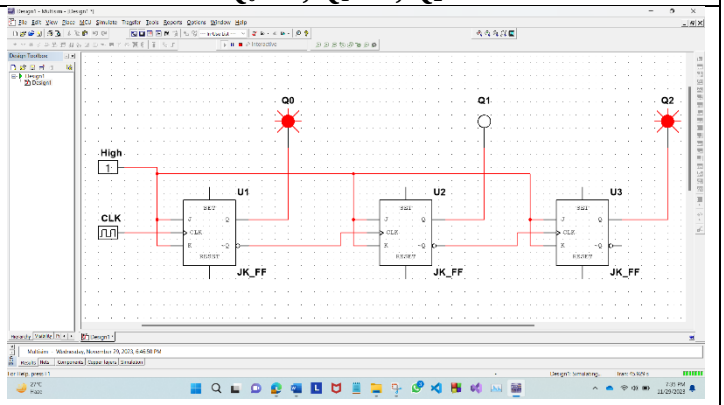
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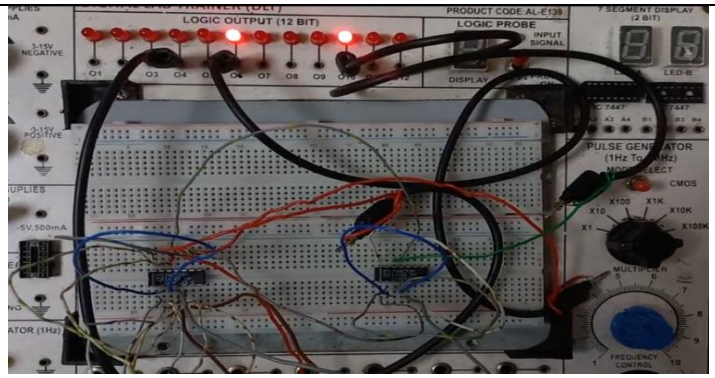	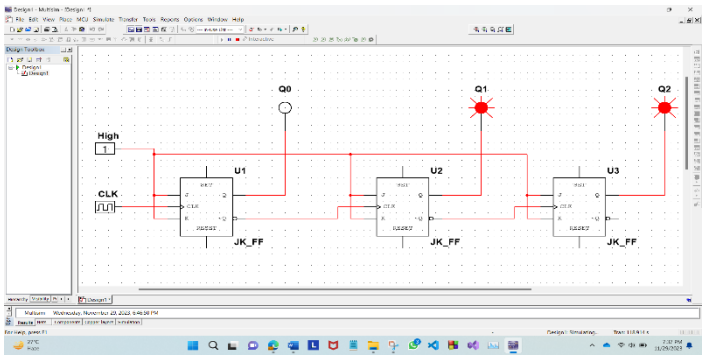
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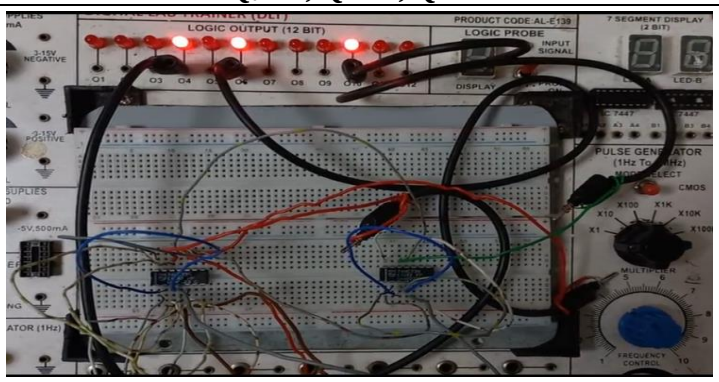	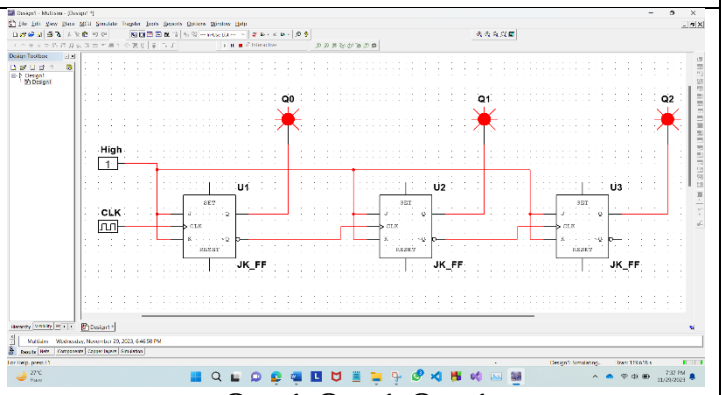
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3-bit Synchronous Up Counter:

Truth Table:

CLK	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

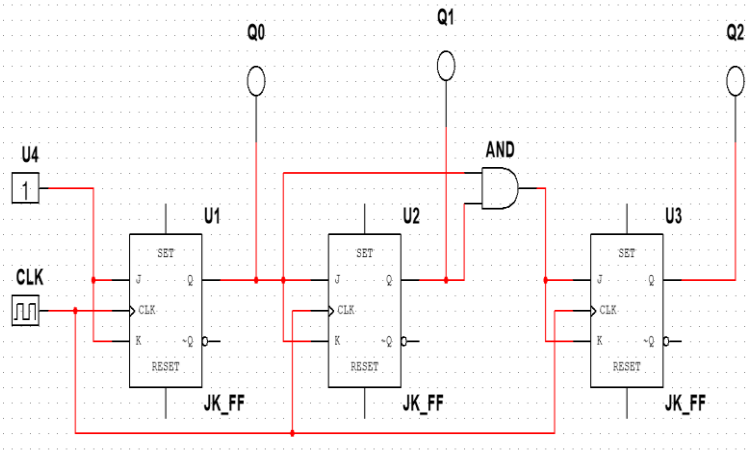
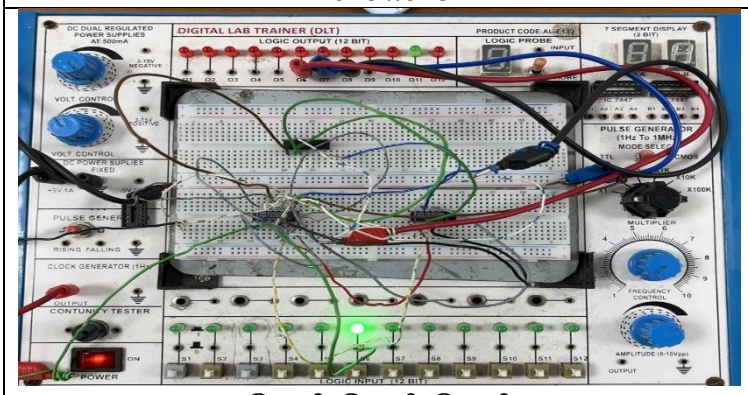
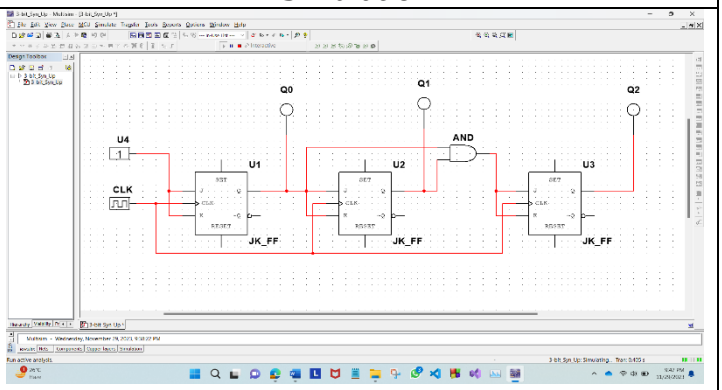


Figure: 3-bit Asynchronous up counter

Hardware	Simulation
	
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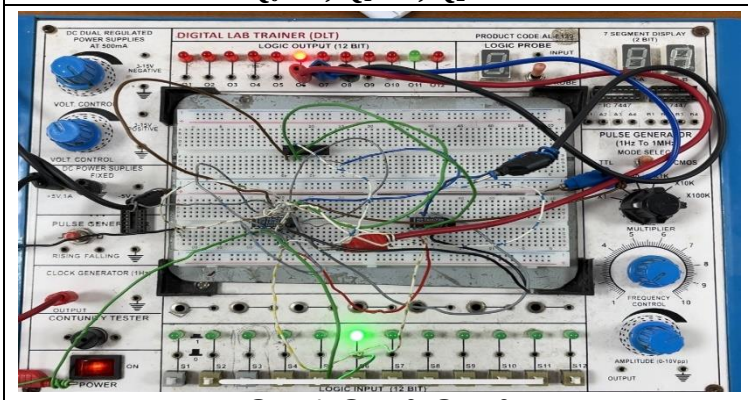	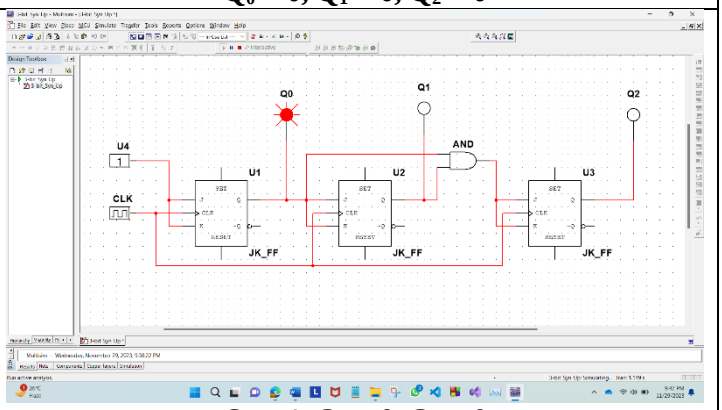
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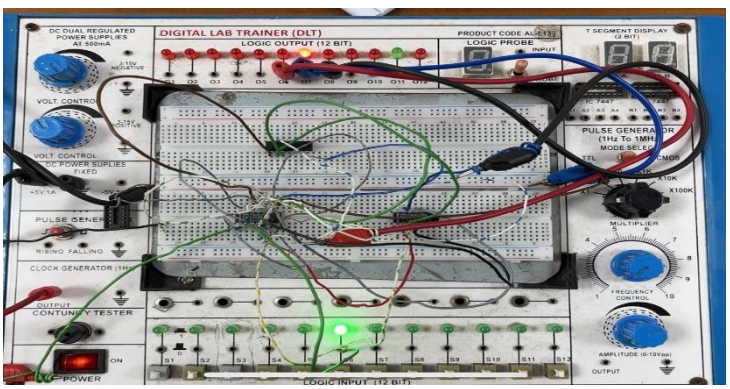	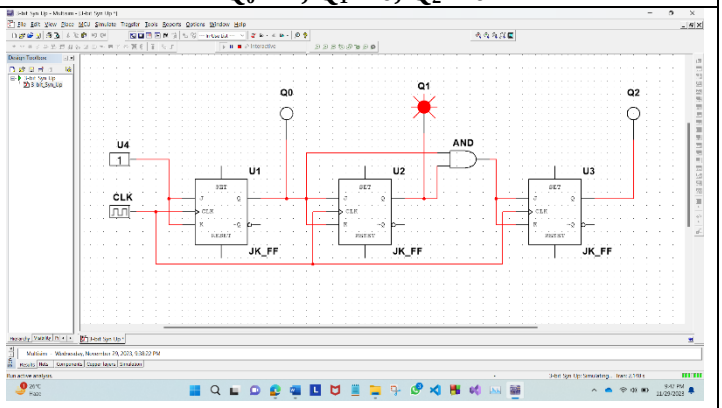
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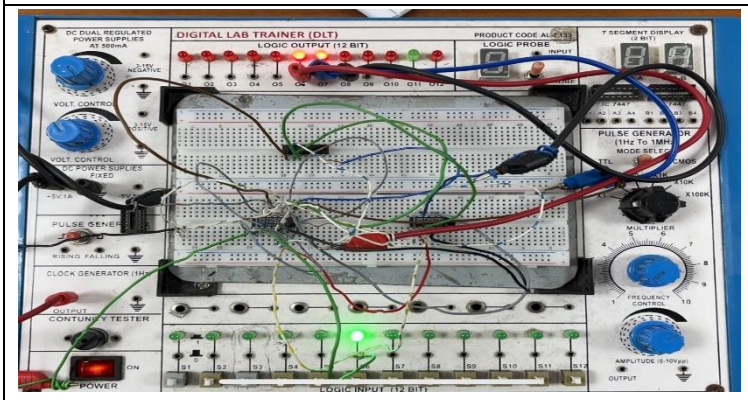	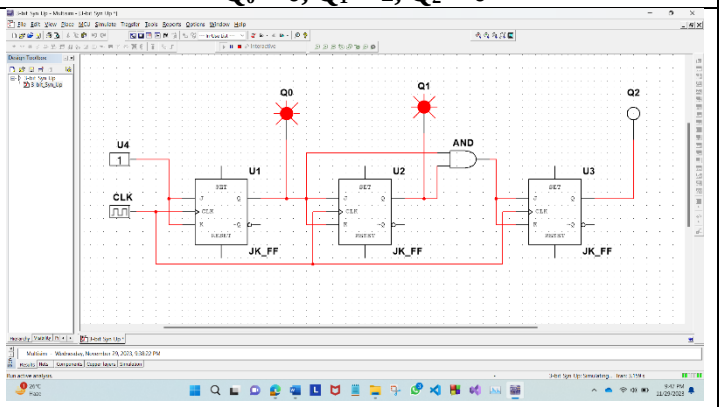
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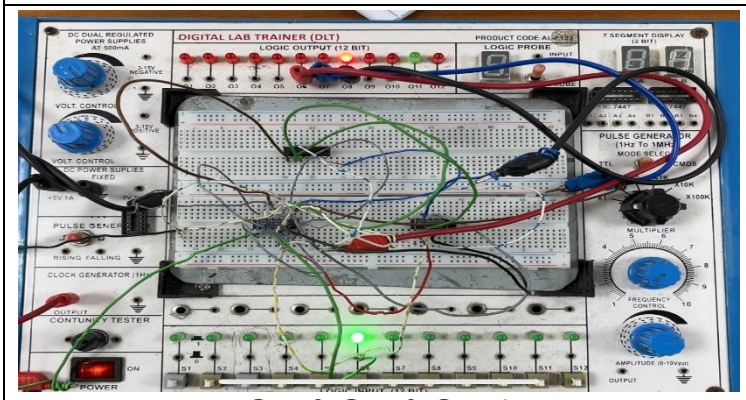
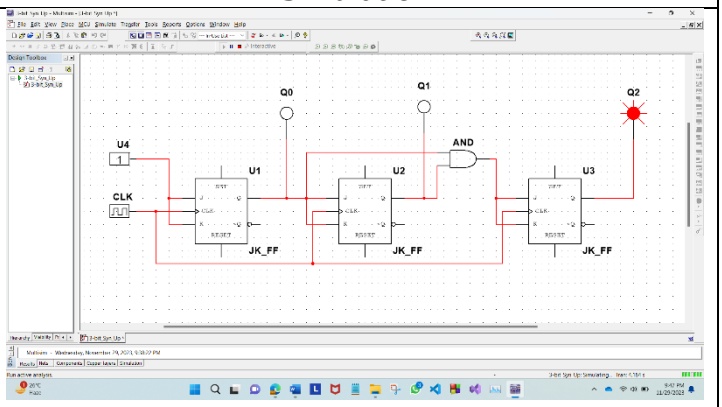
Hardware	Simulation
	
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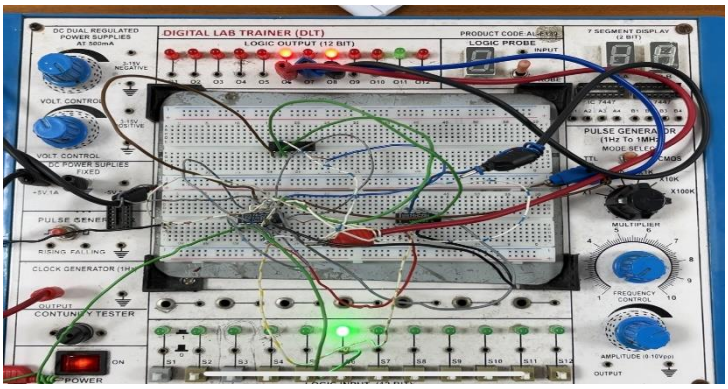
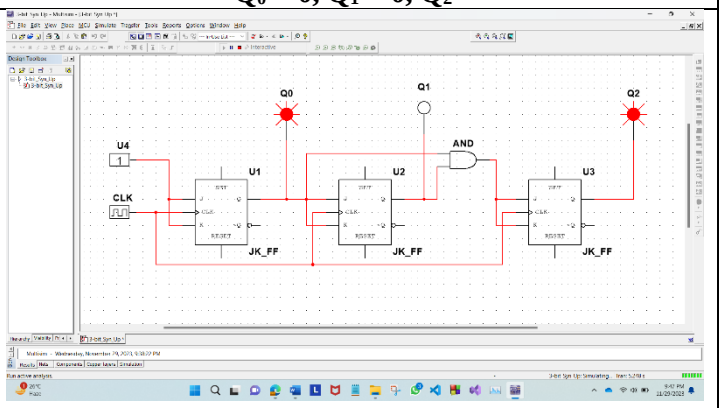
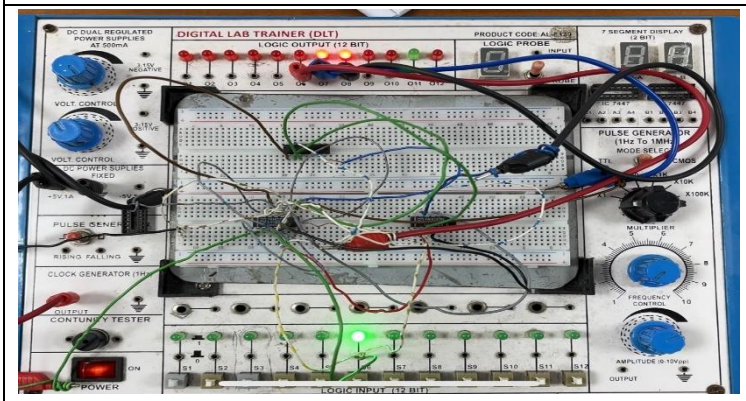
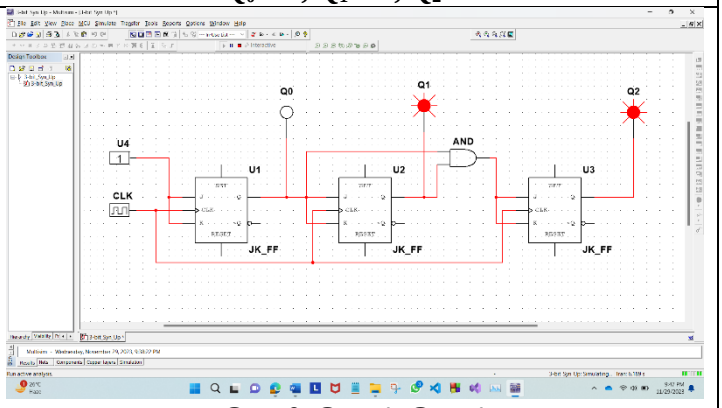
	
$Q_0 = 1, Q_1 = 0, Q_2 = 1$	$Q_0 = 1, Q_1 = 0, Q_2 = 1$
	
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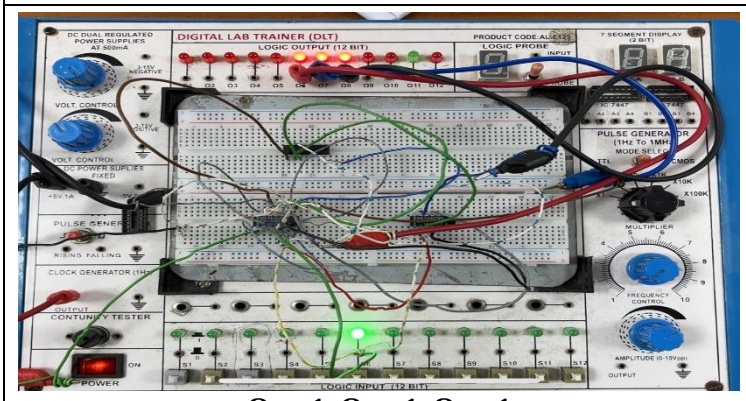	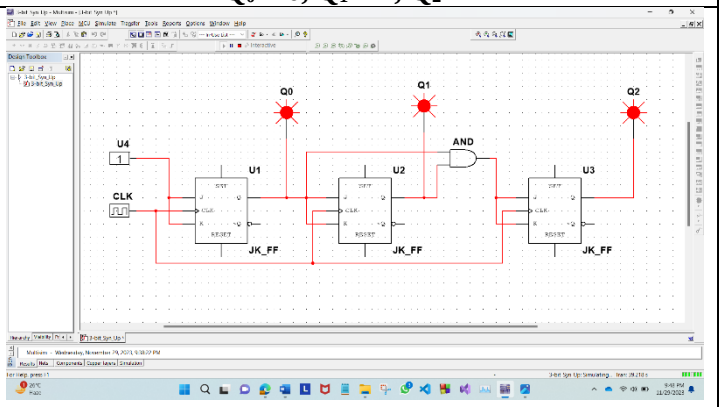
$Q_0 = 1, Q_1 = 1, Q_2 = 1$	$Q_0 = 1, Q_1 = 1, Q_2 = 1$

Questions with answers for report writing:

1. Design a 4 bit Asynchronous Up- Counter.
   Ans:

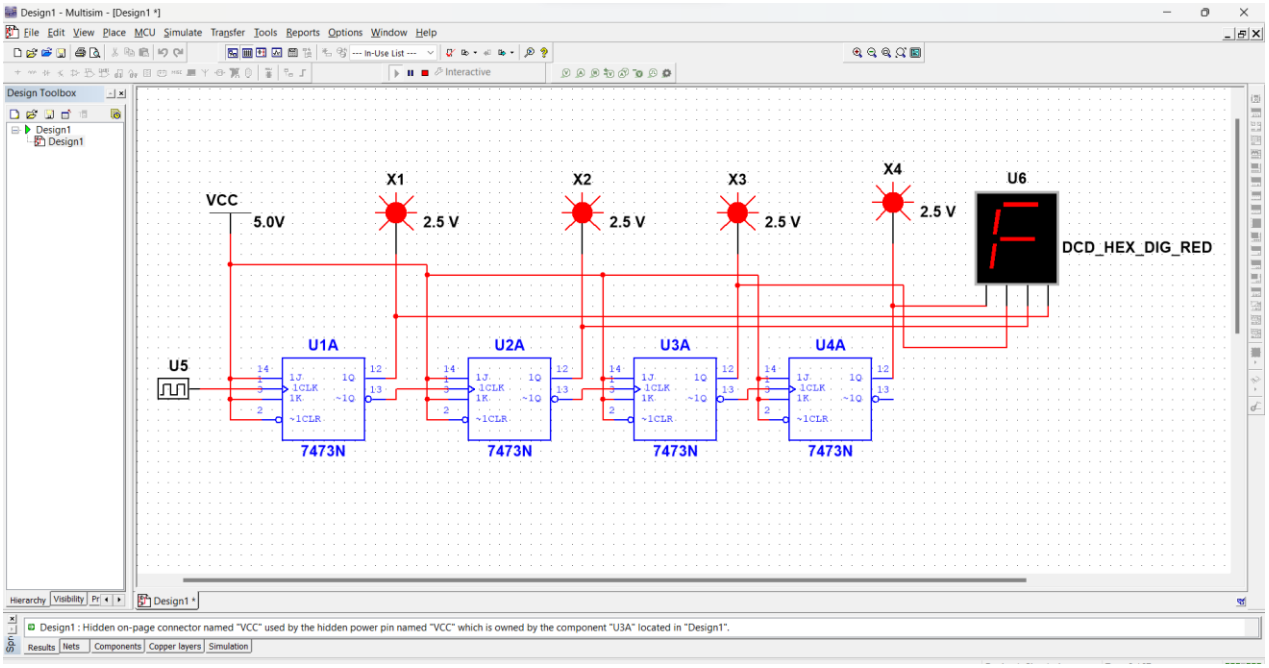

Fig: 4-bit Asynchronous Up counter.

2. Design a 4 bit Synchronous Up- Counter.
   Ans:

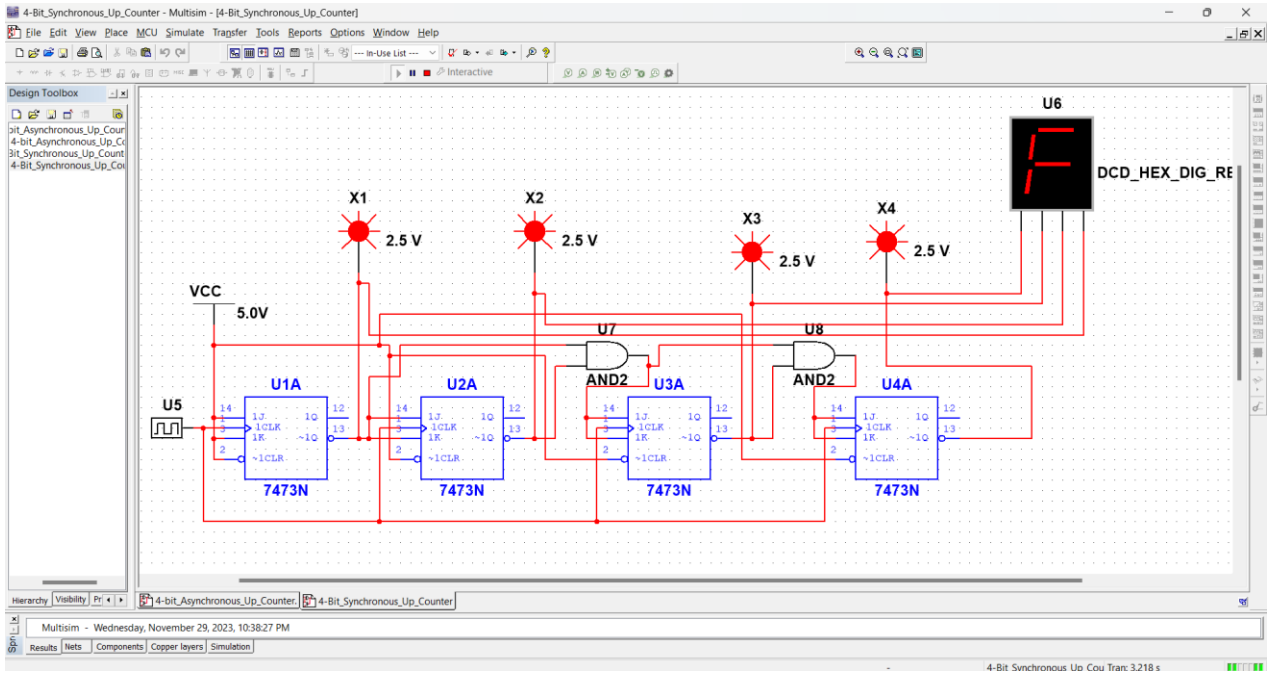

Fig: 4-bit Synchronous Up counter.

3. Design a 3 -bit Asynchronous down counter.
   Ans:

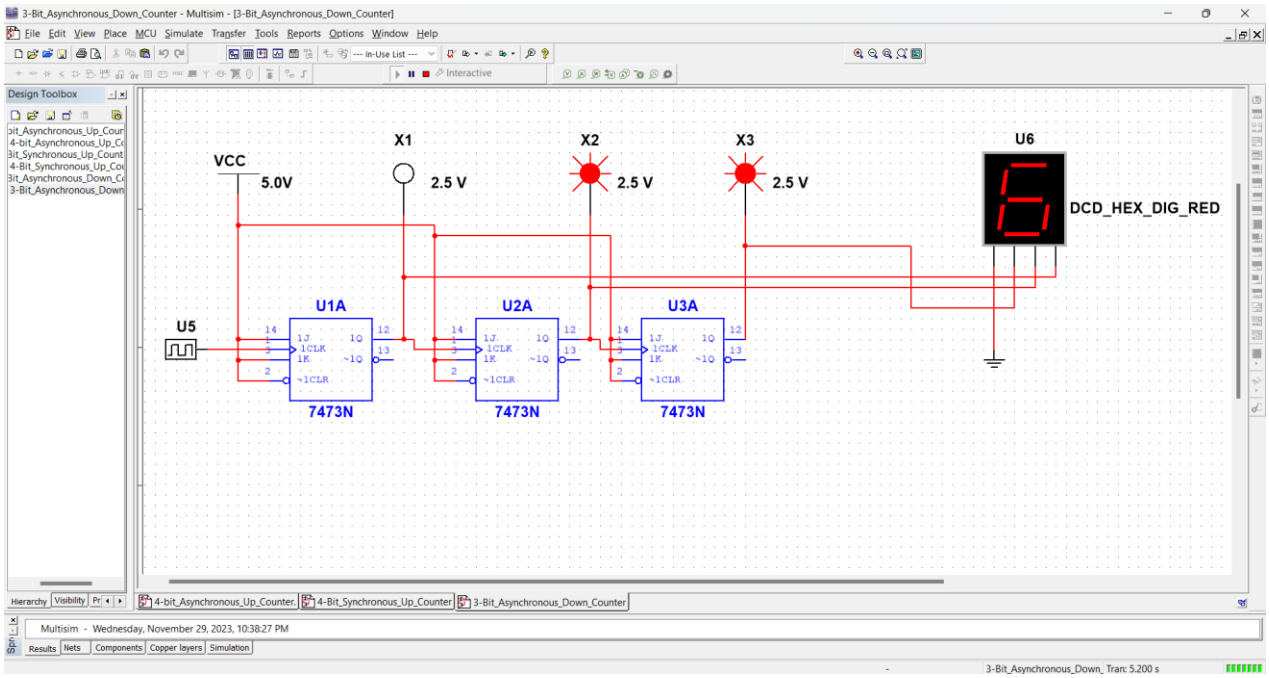

Fig: 3-bit Asynchronous Down counter

4. Design a Mod-10 Synchronous UP counter.
   Ans:

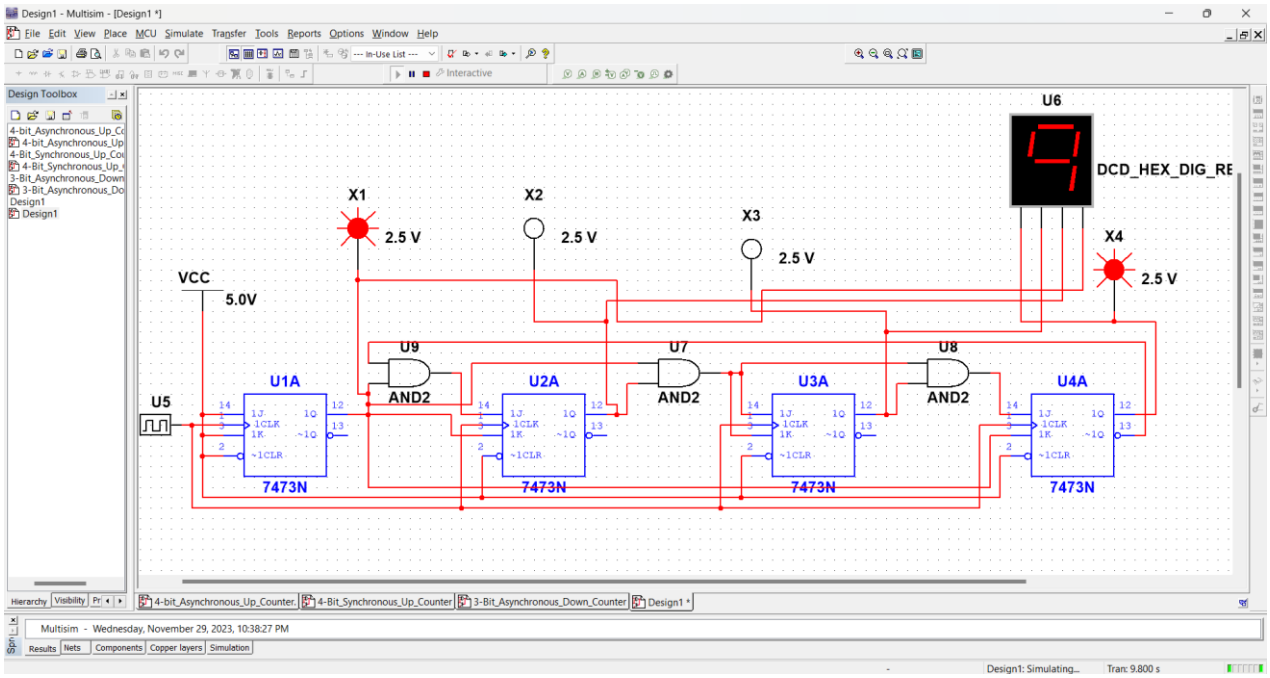

Fig: Mod-10 Synchronous UP counter

Discussion and conclusion:

In this experiment, both a 3-bit asynchronous and synchronous counter were designed, constructed, and simulated using the IC 7403, which incorporates four J-K flip-flops. The primary goal was to observe and analyze the functionality of these counters.

The 3-bit asynchronous counter operated as intended, seamlessly counting from 0 to 7 in the correct sequence and cycling without any deviations. The simulated circuit for the asynchronous counter also produced expected results, demonstrating the accurate functioning of the designed counter.

However, the 3-bit synchronous counter initially encountered issues as it failed to sequentially count and became stuck at the count of 7. To address this, a systematic approach was taken to identify and rectify the errors. Testing and building the counter in steps allowed for pinpointing the specific problem areas. After resolving the issues, the synchronous counter operated flawlessly. The simulation of the synchronous counter confirmed its proper functionality, displaying the expected values without any errors.

In the experimental setup, the IC 7403 served as the core component, with its CLR pin connected to a high voltage (5V), a clock provided, and J and K inputs configured according to the counter design. Upon powering the circuit, the outputs were observed and analyzed.

In conclusion, both the 3-bit asynchronous and synchronous counters were successfully designed, constructed, and simulated. The asynchronous counter consistently counted in the correct order, while the initial issues with the synchronous counter were identified and resolved, leading to its proper operation. This experiment not only provided hands-on experience in building digital counters but also highlighted the importance of systematic troubleshooting in addressing circuit malfunctions.

References:

[1] Thomas L. Floyd, “Digital Fundamentals”, Ninth Edition.