

# Electronic Devices

## Mid Term Lecture - 10

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Reference book:

**Electronic Devices and Circuit Theory (Chapter-4)**

Robert L. Boylestad and L. Nashelsky , (11<sup>th</sup> Edition)



**Faculty of Engineering**

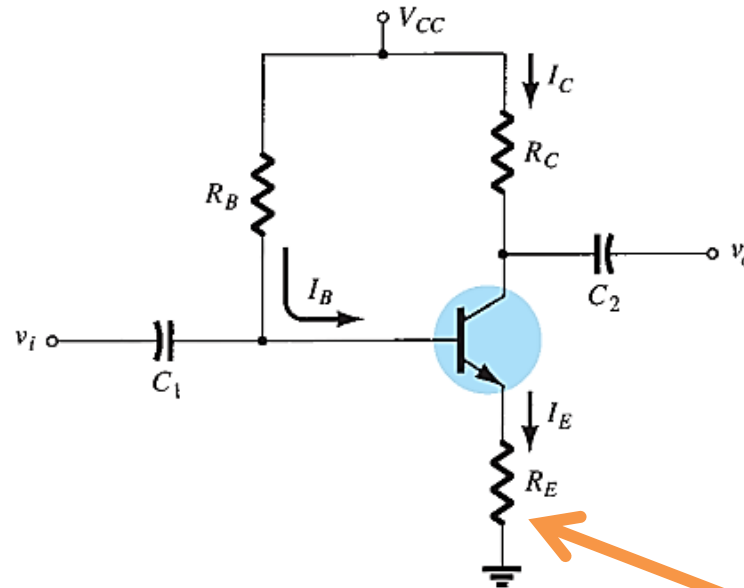
**American International University-Bangladesh**

# Objectives

- Be able to determine the dc levels for the variety of important BJT configurations.
- Understand how to measure the important voltage levels of a BJT transistor configuration and use them to determine whether the network is operating properly.
- Become aware of the saturation and cutoff conditions of a BJT network and the expected voltage and current levels established by each condition.
- Be able to perform a load-line analysis of the most common BJT configurations.
- Become acquainted with the design process for BJT amplifiers.
- Understand the basic operation of transistor switching networks.
- Begin to understand the troubleshooting process as applied to BJT configurations.
- Develop a sense for the stability factors of a BJT configuration and how they affect its operation due to changes in specific characteristics and environmental changes.



# EMITTER-BIAS CONFIGURATION



**FIG. 4.17**

*BJT bias circuit with emitter resistor.*

Adding a resistor in the Emitter circuit stabilizes the bias circuit.

# BIAS STABILITY

- If  $V_{BE}$  is held constant and the temperature rises, the current through the base-emitter diode  $I_B$  will increase, and thus the collector  $I_C$  will also increase. The power dissipated in the transistor may also increase, which will further increase its temperature and exacerbate the problem. This deleterious positive feedback results in thermal runaway.
- Adding  $R_E$  to the Emitter improves the stability of a transistor.
- Stability refers to a bias circuit in which the currents and voltages will remain fairly constant for a while range of temperatures and transistor Beta's ( $\beta$ ).
- $$V_{RB} = V_{CC} - I_E R_E - V_{BE}$$

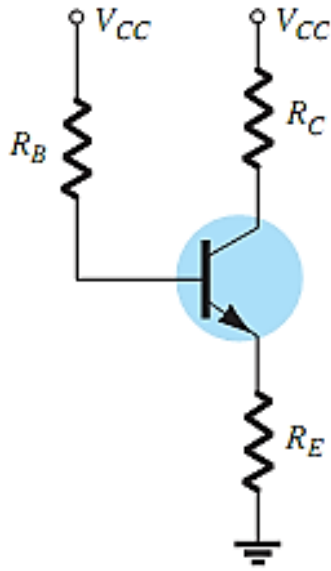


# BIAS STABILITY

- If temperature increases, emitter current increases.
- However, a larger  $I_E$  increases the emitter voltage  $V_E = I_E R_E$ , which in turn reduces the voltage  $V_{RB}$  across the base resistor.
- A lower base-resistor voltage drop reduces the base current, which results in less collector current because  $I_C = \beta I_B$ .

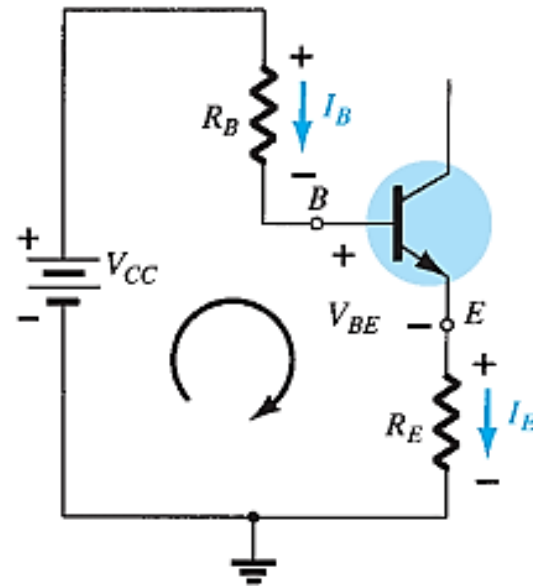


## BASE-EMITTER LOOP



**FIG. 4.18**

*DC equivalent of Fig. 4.17.*



**FIG. 4.19**

*Base-emitter loop.*

## BASE-EMITTER LOOP

$$+V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta + 1)I_B$$

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1)I_B R_E = 0$$

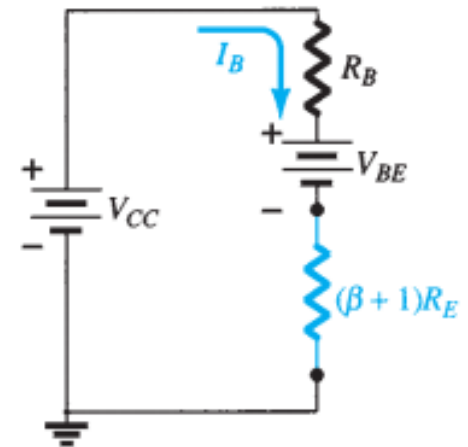
$$-I_B(R_B + (\beta + 1)R_E) + V_{CC} - V_{BE} = 0$$

$$I_B(R_B + (\beta + 1)R_E) - V_{CC} + V_{BE} = 0$$

$$I_B(R_B + (\beta + 1)R_E) = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$R_i = (\beta + 1)R_E$$



**FIG. 4.20**

*Network derived from Eq. (4.17).*

## COLLECTOR-EMITTER LOOP

$$+I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

Substituting  $I_E \cong I_C$  and grouping terms gives

$$V_{CE} - V_{CC} + I_C(R_C + R_E) = 0$$

and

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

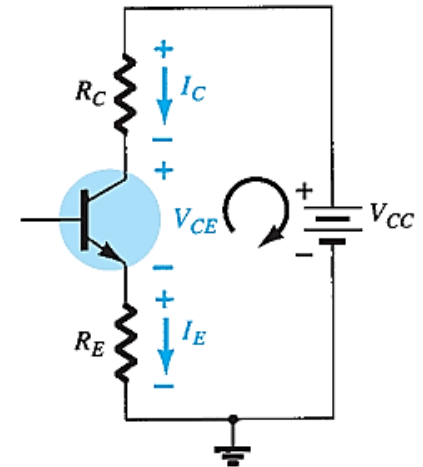
$$V_E = I_E R_E$$

$$V_{CE} = V_C - V_E$$

$$V_C = V_{CC} - I_C R_C$$

$$V_B = V_{CC} - I_B R_B$$

$$V_B = V_{BE} + V_E$$



**FIG. 4.22**

Collector-emitter loop.



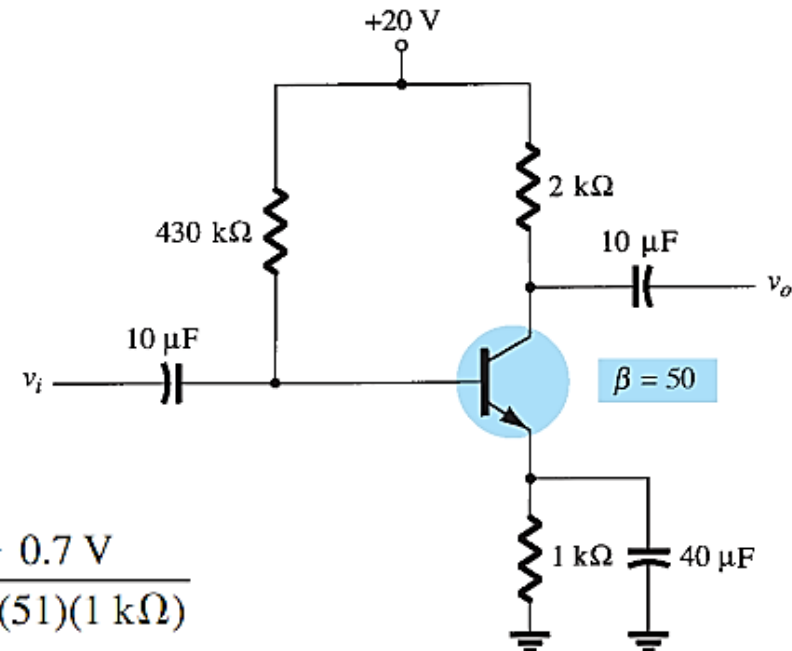
## EXAMPLE

**EXAMPLE 4.4** For the emitter-bias network of Fig. 4.23, determine:

- $I_B$ .
- $I_C$ .
- $V_{CE}$ .
- $V_C$ .
- $V_E$ .
- $V_B$ .
- $V_{BC}$ .

$$\begin{aligned} \text{a. Eq. (4.17): } I_B &= \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 \text{ V} - 0.7 \text{ V}}{430 \text{ k}\Omega + (51)(1 \text{ k}\Omega)} \\ &= \frac{19.3 \text{ V}}{481 \text{ k}\Omega} = 40.1 \mu\text{A} \end{aligned}$$

$$\begin{aligned} \text{b. } I_C &= \beta I_B \\ &= (50)(40.1 \mu\text{A}) \\ &\cong 2.01 \text{ mA} \end{aligned}$$



**FIG. 4.23**

*stabilized bias circuit for Example 4.4.*

# EXAMPLE

c. Eq. (4.19):  $V_{CE} = V_{CC} - I_C(R_C + R_E)$   
 $= 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega + 1 \text{ k}\Omega) = 20 \text{ V} - 6.03 \text{ V}$   
 $= 13.97 \text{ V}$

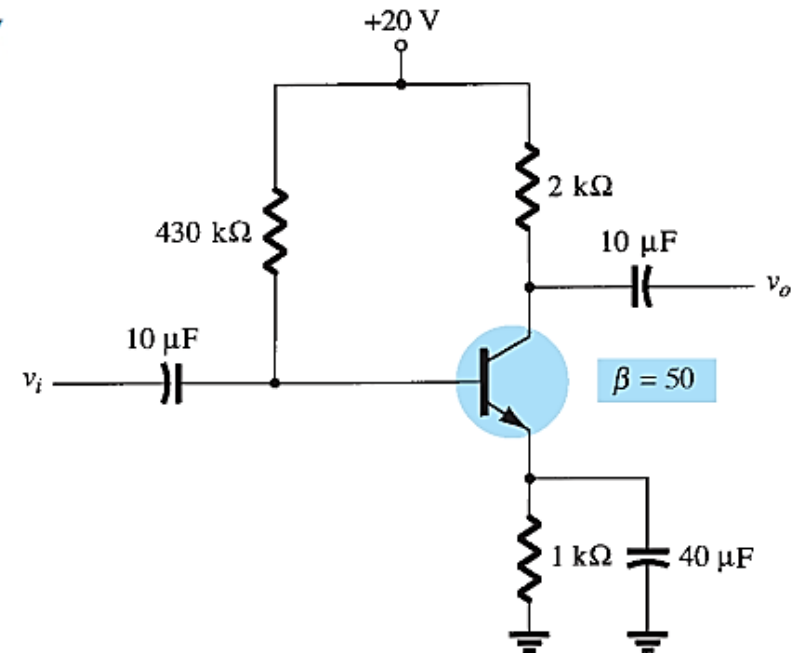
d.  $V_C = V_{CC} - I_C R_C$   
 $= 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega) = 20 \text{ V} - 4.02 \text{ V}$   
 $= 15.98 \text{ V}$

e.  $V_E = V_C - V_{CE}$   
 $= 15.98 \text{ V} - 13.97 \text{ V}$   
 $= 2.01 \text{ V}$

or  $V_E = I_E R_E \cong I_C R_E$   
 $= (2.01 \text{ mA})(1 \text{ k}\Omega)$   
 $= 2.01 \text{ V}$

f.  $V_B = V_{BE} + V_E$   
 $= 0.7 \text{ V} + 2.01 \text{ V}$   
 $= 2.71 \text{ V}$

g.  $V_{BC} = V_B - V_C$   
 $= 2.71 \text{ V} - 15.98 \text{ V}$   
 $= -13.27 \text{ V}$  (reverse-biased as required)



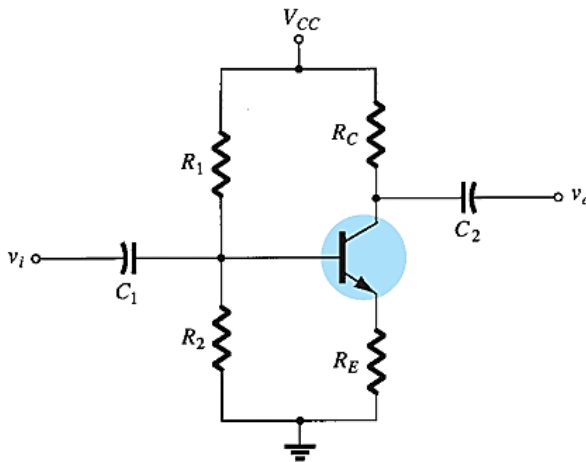
**FIG. 4.23**

*Emitter-stabilized bias circuit for Example 4.4.*

# VOLTAGE-DIVIDER BIAS CONFIGURATION

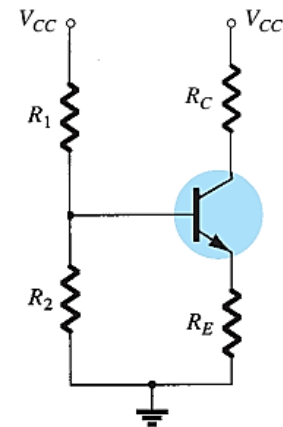
- The bias current  $I_{CQ}$  and voltage  $V_{CEQ}$  is a function of the current gain  $\beta$  of the transistor
- Since  $\beta$  is temperature sensitive, especially for silicon transistors, it would be desirable to develop a bias circuit that is independent of the transistor  $\beta$ .

The voltage-divider bias configuration is such a network.



**FIG. 4.28**

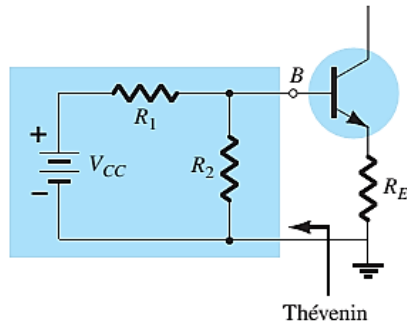
*Voltage-divider bias configuration.*



**FIG. 4.30**

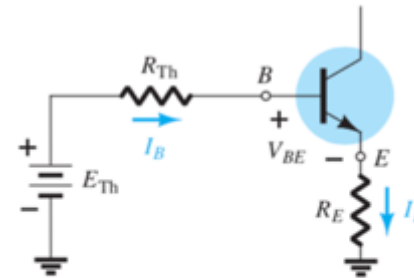
*DC components of the voltage-divider configuration.*

# EXACT ANALYSIS



**FIG. 4.31**

Redrawing the input side of the network of Fig. 4.28.



**FIG. 4.34**

Inserting the Thévenin equivalent circuit.

$$R_{Th} = R_1 \parallel R_2$$

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

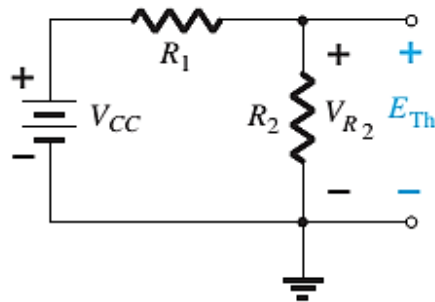
$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

# EXAMPLE

**EXAMPLE 4.8** Determine the dc bias voltage  $V_{CE}$  and the current  $I_C$  for the voltage-divider configuration of Fig. 4.35.

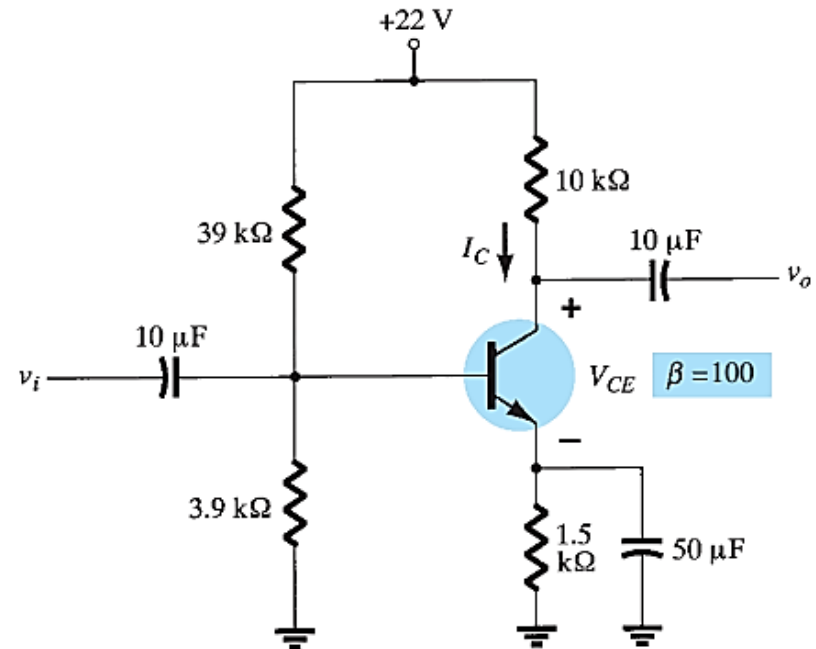


**FIG. 4.33**

*Determining  $E_{Th}$ .*

$$R_{Th} = R_1 \parallel R_2$$

$$= \frac{(39 \text{ k}\Omega)(3.9 \text{ k}\Omega)}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} = 3.55 \text{ k}\Omega$$



**FIG. 4.35**

*Beta-stabilized circuit for Example 4.8.*

## EXAMPLE CONTD.

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$= \frac{(3.9 \text{ k}\Omega)(22 \text{ V})}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} = 2 \text{ V}$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{2 \text{ V} - 0.7 \text{ V}}{3.55 \text{ k}\Omega + (101)(1.5 \text{ k}\Omega)} = \frac{1.3 \text{ V}}{3.55 \text{ k}\Omega + 151.5 \text{ k}\Omega}$$

$$= 8.38 \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (100)(8.38 \mu\text{A})$$

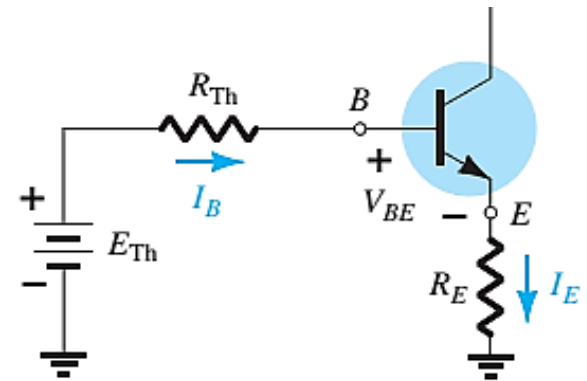
$$= \mathbf{0.84 \text{ mA}}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 22 \text{ V} - (0.84 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega)$$

$$= 22 \text{ V} - 9.66 \text{ V}$$

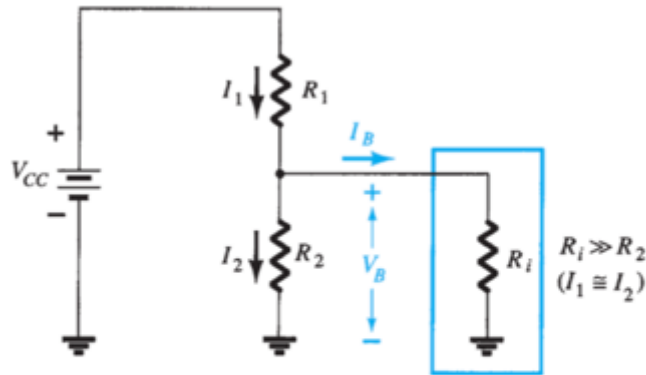
$$= \mathbf{12.34 \text{ V}}$$



**FIG. 4.34**

*Inserting the Thévenin equivalent circuit.*

# Approximate Analysis



**FIG. 4.36**

Partial-bias circuit for calculating the approximate base voltage  $V_B$ .

$$\beta R_E \geq 10R_2$$

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$R_i = (\beta + 1) R_E \cong \beta R_E$$

Once  $V_B$  is determined, the level of  $V_E$  can be calculated from

$$V_E = V_B - V_{BE}$$

and the emitter current can be determined from

$$I_E = \frac{V_E}{R_E}$$

and

$$I_{CQ} \cong I_E$$

The collector-to-emitter voltage is determined by

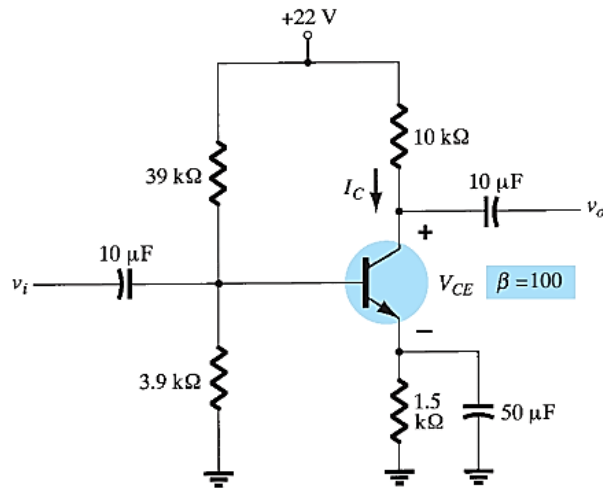
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

but because  $I_E \cong I_C$ ,

$$V_{CEQ} = V_{CC} - I_C (R_C + R_E)$$

# EXAMPLE

**EXAMPLE 4.9** Repeat the analysis of Fig. 4.35 using the approximate technique, and compare solutions for  $I_{CQ}$  and  $V_{CEQ}$ .



**FIG. 4.35**

Beta-stabilized circuit for Example 4.8.

$$\begin{aligned} \text{Eq. (4.32): } V_B &= \frac{R_2 V_{CC}}{R_1 + R_2} \\ &= \frac{(3.9 \text{ k}\Omega)(22 \text{ V})}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} \\ &= 2 \text{ V} \end{aligned}$$

Testing:

$$\begin{aligned} \beta R_E &\geq 10 R_2 \\ (100)(1.5 \text{ k}\Omega) &\geq 10(3.9 \text{ k}\Omega) \\ 150 \text{ k}\Omega &\geq 39 \text{ k}\Omega \text{ (satisfied)} \end{aligned}$$

$$\begin{aligned} \text{Eq. (4.34): } V_E &= V_B - V_{BE} \\ &= 2 \text{ V} - 0.7 \text{ V} \\ &= 1.3 \text{ V} \end{aligned}$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3 \text{ V}}{1.5 \text{ k}\Omega} = 0.867 \text{ mA}$$

compared to 0.84 mA with the exact analysis. Finally,

$$\begin{aligned} V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\ &= 22 \text{ V} - (0.867 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega) \\ &= 22 \text{ V} - 9.97 \text{ V} \\ &= 12.03 \text{ V} \end{aligned}$$

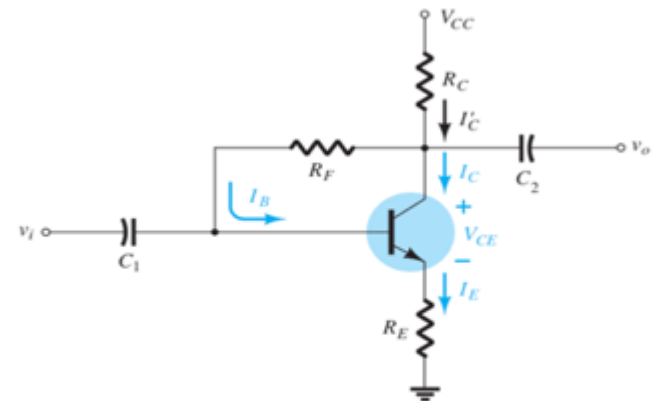
versus 12.34 V obtained in Example 4.8.





# COLLECTOR FEEDBACK CONFIGURATION

- An improved level of stability can also be obtained by introducing a feedback path from collector to base
- Although the  $Q$ -point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations.
- The analysis will again be performed by first analyzing the base–emitter loop, with the results then applied to the collector–emitter loop



**FIG. 4.38**

*DC bias circuit with voltage feedback.*

# BASE-EMITTER LOOP

$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

$$V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0$$

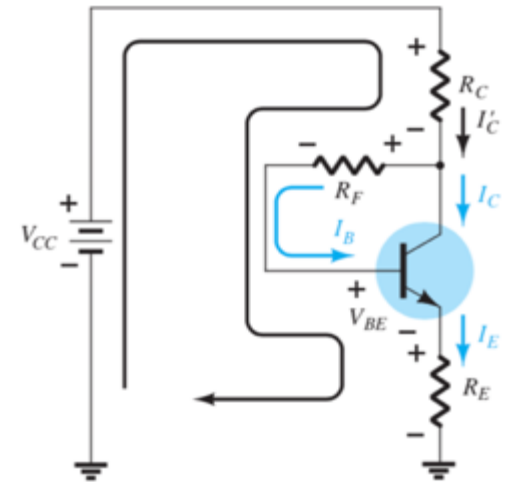
$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_F = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$$

$$I_B = \frac{V'}{R_F + \beta R'}$$

$$I_{CQ} = \frac{\beta V'}{R_F + \beta R'} = \frac{V'}{\frac{R_F}{\beta} + R'}$$

$$I_{CQ} \cong \frac{V'}{R'}$$



**FIG. 4.39**

Base-emitter loop for the network of Fig. 4.38.

## COLLECTOR-EMITTER LOOP

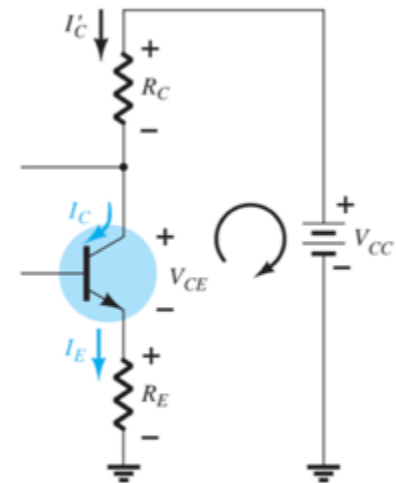
$$I_E R_E + V_{CE} + I'_C R_C - V_{CC} = 0$$

Because  $I'_C \cong I_C$  and  $I_E \cong I_C$ , we have

$$I_C(R_C + R_E) + V_{CE} - V_{CC} = 0$$

and

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$



**FIG. 4.40**

Collector-emitter loop for the network of Fig. 4.38.

### EXAMPLE 4.12



# Thank You

