

# Electronic Devices

## Mid Term Lecture - 09

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Reference book:

**Electronic Devices and Circuit Theory (Chapter-4)**

Robert L. Boylestad and L. Nashelsky , (11<sup>th</sup> Edition)



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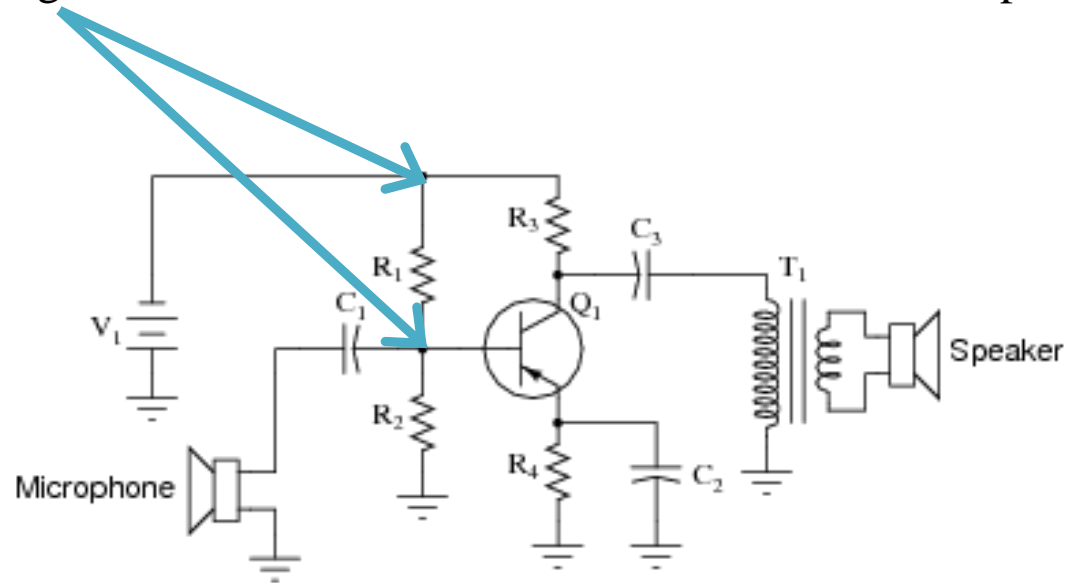
# Objectives

- Be able to determine the dc levels for the variety of important BJT configurations.
- Understand how to measure the important voltage levels of a BJT transistor configuration and use them to determine whether the network is operating properly.
- Become aware of the saturation and cutoff conditions of a BJT network and the expected voltage and current levels established by each condition.
- Be able to perform a load-line analysis of the most common BJT configurations.
- Become acquainted with the design process for BJT amplifiers.
- Understand the basic operation of transistor switching networks.
- Begin to understand the troubleshooting process as applied to BJT configurations.
- Develop a sense for the stability factors of a BJT configuration and how they affect its operation due to changes in specific characteristics and environmental changes.



# BIASING

- Applying DC voltages to the transistor to turn it on so that it can amplify AC signal.



- Once the desired DC current and voltage levels have been defined, a network must be constructed that will establish the desired operating point.



# INTRODUCTION

- BJT amplifier design requires knowledge of both the DC and AC.
- BJT needs to be operated in active region used as amplifier.
- BJT operated in cut-off and saturation region is used as a switch.
- The following basic current relationships for a transistor are required for transistor network analysis:

$$V_{BE} = 0.7 \text{ V}$$

$$I_E = (\beta + 1) I_B \cong I_C$$

$$I_C = \beta I_B$$



# INTRODUCTION

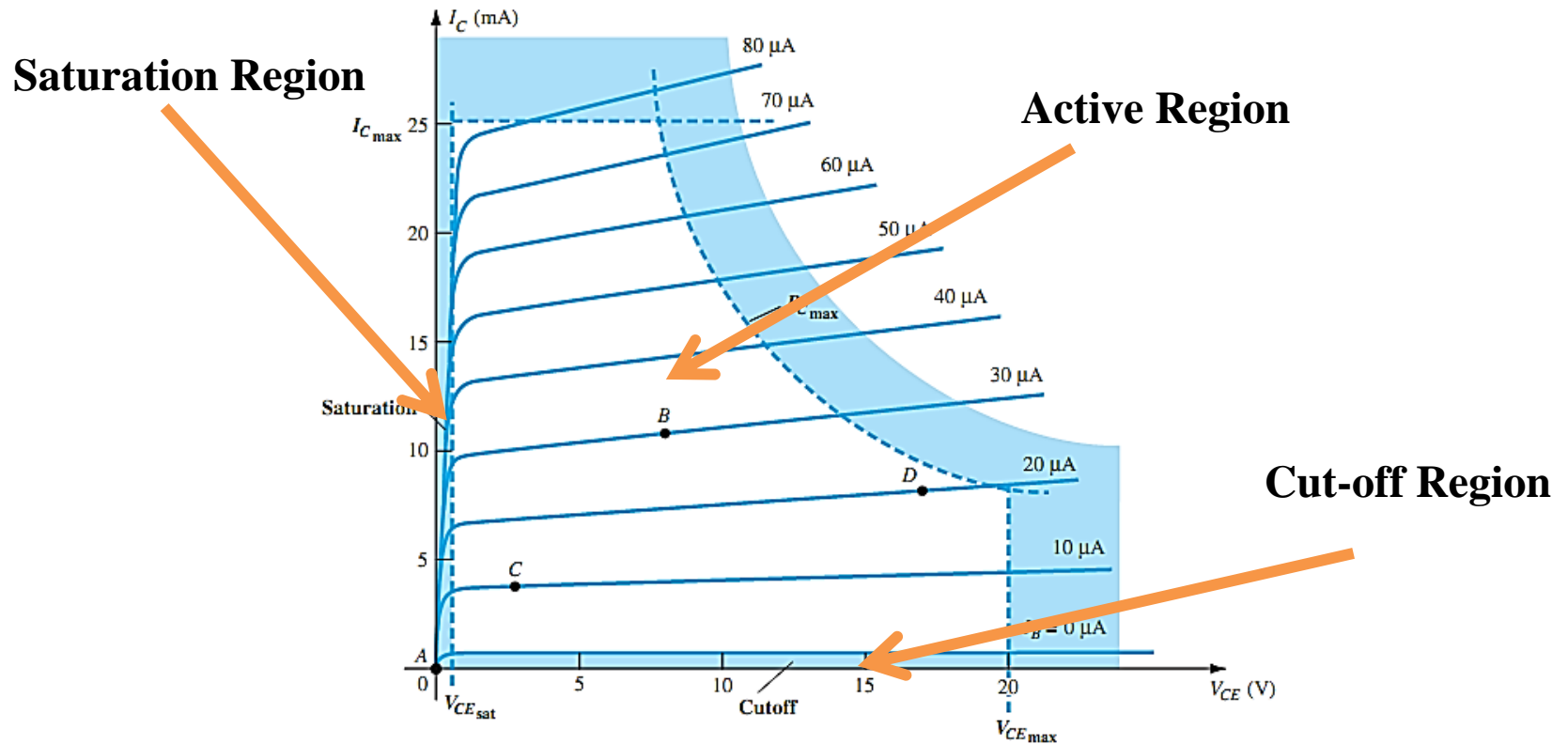
- Biasing:

Applying DC voltages to establish a fixed level of current and voltage.

- The applied DC establishes an operating point (Q-point) that define the region for the signal amplification.
- For a BJT to be biased in active operating region, the following must be true:
  - 1) BE junction = forward biased
  - 2) BC junction = reverse biased



# BIASING AND THE 3 STATES OF OPERATION



**FIG. 4.1**

*Various operating points within the limits of operation of a transistor.*

# OPERATING POINT (Q-POINT)

- Operating Point: Quiescent point or Q-point (static point)
- The biasing circuit can be designed to set the device operation at any of these points or others within the active region.
- The BJT device could be biased to operate outside the max limits, but the result of such operation would be shortening of the lifetime of the device or destruction of the device.
- The chosen Q-point often depends on the intended use of the circuit.



# VARIOUS Q-POINTS WITHIN THE LIMITS OF OPERATION

## Q-point B:

- The best operating point for linear gain & largest possible voltage & current.
- Desired condition for a small signal analysis.

## Q-point A:

- $I = 0A$ ,  $V = 0V$
- Not suitable for transistor to operate

## Q-point D:

- Near the maximum voltage & power level.

## Q-point C:

- Concern on nonlinearities due to  $I_B$  curves is rapidly changes in this region.

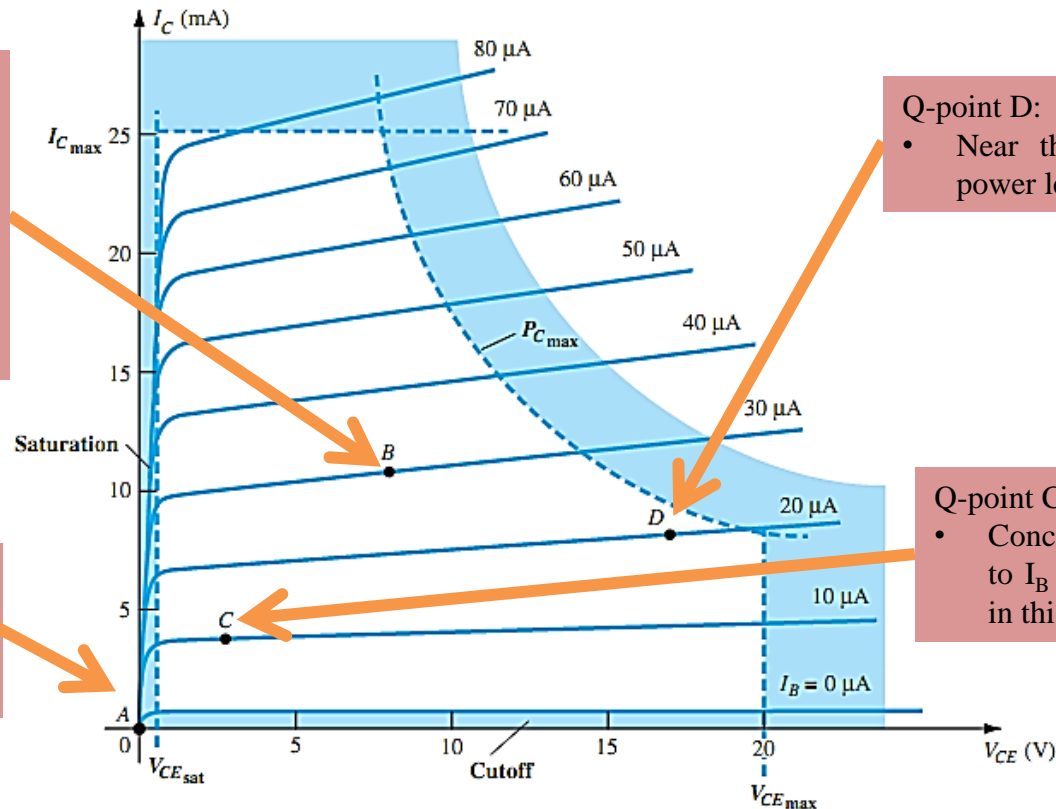


FIG. 4.1

Various operating points within the limits of operation of a transistor.

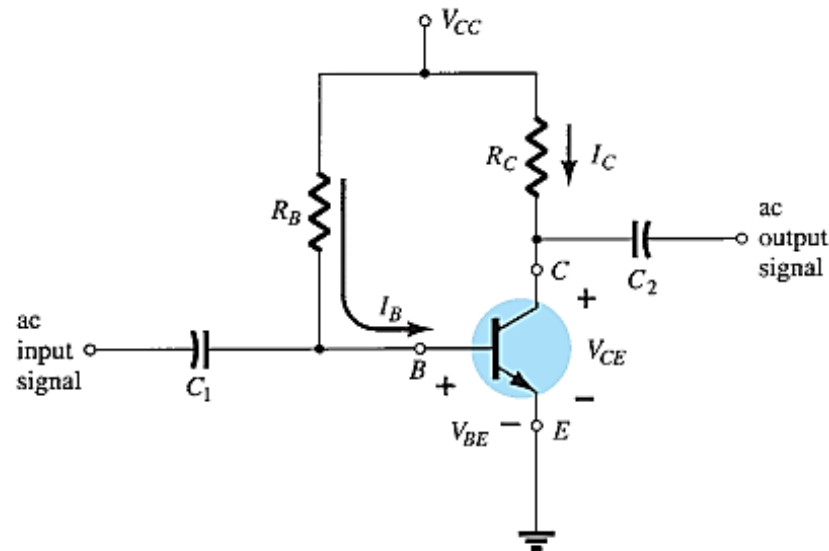


# BJT BIAS CONFIGURATIONS

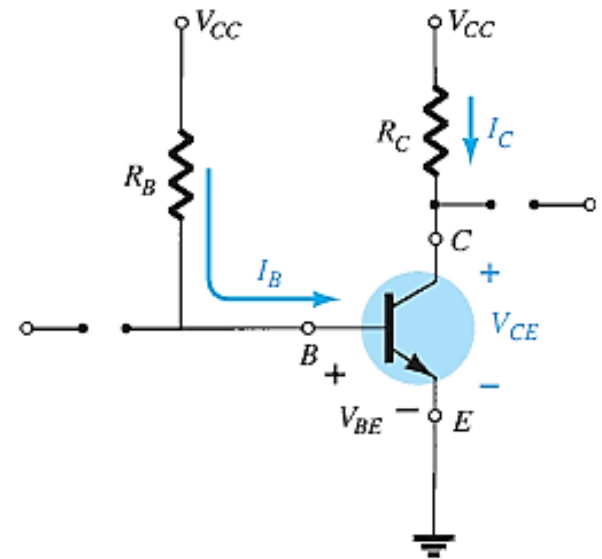
- 1. Fixed-Bias Configuration**
- 2. Emitter-Bias Configuration**
- 3. Voltage-Divider Bias Configuration**
- 4. Collector Feedback Configuration**



# FIXED-BIAS CONFIGURATION



**FIG. 4.2**  
*Fixed-bias circuit.*

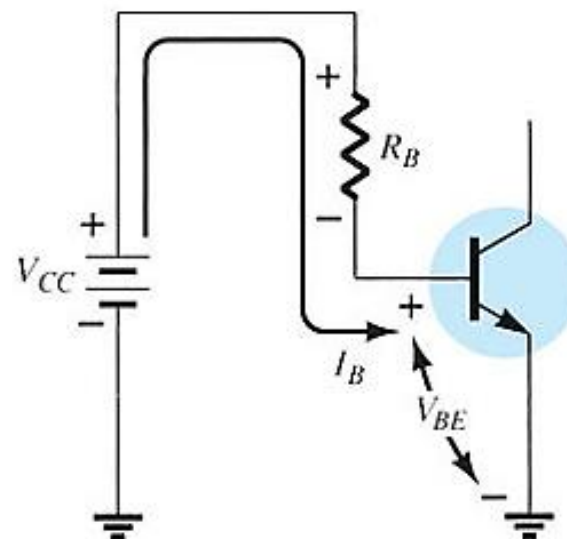


**FIG. 4.3**  
*DC equivalent of Fig. 4.2.*

# FORWARD BIAS OF BASE-EMITTER

$$+V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$



**FIG. 4.4**

*Base-emitter loop.*

## COLLECTOR-EMITTER LOOP

$$I_C = \beta I_B$$

$$V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

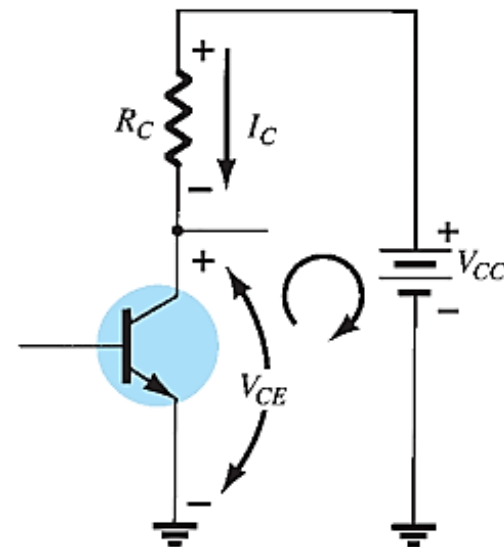
$$V_{CE} = V_C - V_E$$

In this case, since  $V_E = 0$  V, we have

$$V_{CE} = V_C$$

$$V_{BE} = V_B - V_E$$

$$V_{BE} = V_B$$



**FIG. 4.5**

*Collector-emitter loop.*

# FIXED-BIAS CONFIGURATION EXAMPLE

**EXAMPLE 4.1** Determine the following for the fixed-bias configuration of Fig. 4.7.

- $I_{BQ}$  and  $I_{CQ}$ .
- $V_{CEQ}$ .
- $V_B$  and  $V_C$ .
- $V_{BC}$ .

a. Eq. (4.4): 
$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = 47.08\text{ }\mu\text{A}$$

Eq. (4.5): 
$$I_{CQ} = \beta I_{BQ} = (50)(47.08\text{ }\mu\text{A}) = 2.35\text{ mA}$$

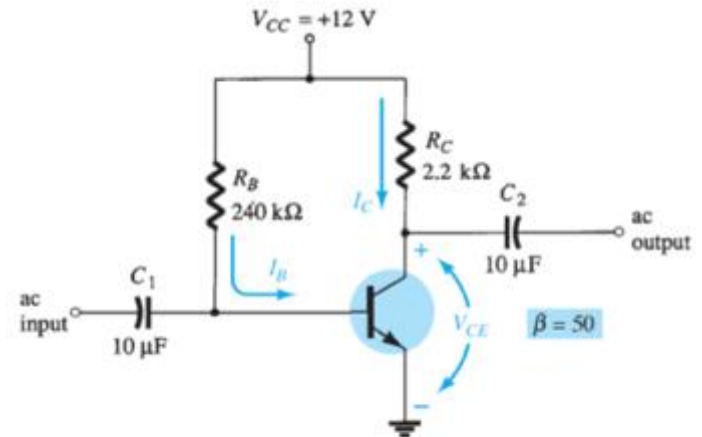
b. Eq. (4.6): 
$$\begin{aligned} V_{CEQ} &= V_{CC} - I_C R_C \\ &= 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega) \\ &= 6.83\text{ V} \end{aligned}$$

c.  $V_B = V_{BE} = 0.7\text{ V}$   
 $V_C = V_{CE} = 6.83\text{ V}$

d. Using double-subscript notation yields

$$\begin{aligned} V_{BC} &= V_B - V_C = 0.7\text{ V} - 6.83\text{ V} \\ &= -6.13\text{ V} \end{aligned}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.



**FIG. 4.7**

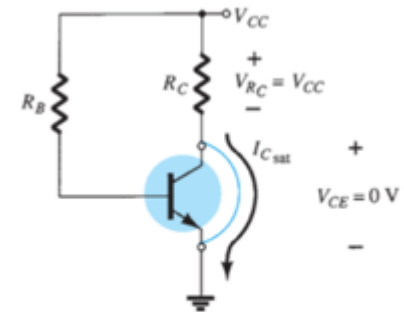
DC fixed-bias circuit for Example 4.1.

# Transistor Saturation

- For a transistor operating in the saturation region, the current is a maximum value *for the particular design*
- The highest saturation level is defined by the maximum collector current as provided by the specification sheet.
- Saturation conditions are normally avoided because the base–collector junction is no longer reverse-biased and the output amplified signal will be distorted.
- It is in a region where the characteristic curves join, and the collector-to-emitter voltage is at or below  $V_{CEsat}$ .

The resulting saturation current for the fixed-bias configuration is

$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$



**FIG. 4.10**

Determining  $I_{C_{sat}}$  for the fixed-bias configuration.

**See Example 4.2**

# Load-Line Analysis

- The characteristics of the BJT are superimposed on a plot of the network equation defined by the same axis parameters
- The load resistor  $R_C$  for the fixed-bias configuration will define the slope of the network equation and the resulting intersection between the two plots.

The network of Fig. 4.11(a) establishes an output equation that relates the variables  $I_C$  and  $V_{CE}$  in the following manner:

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_{CC} |_{I_C = 0 \text{ mA}}$$

$$I_C = \frac{V_{CC}}{R_C} |_{V_{CE} = 0 \text{ V}}$$

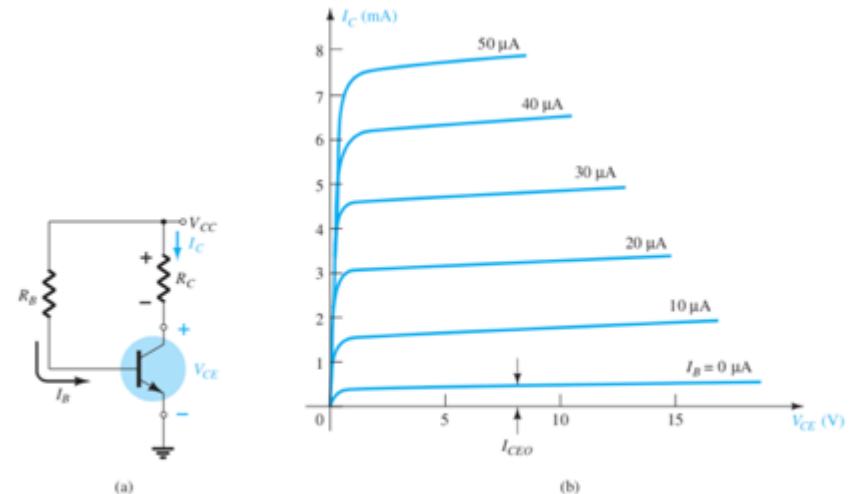
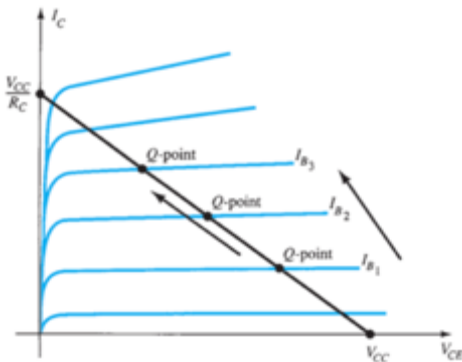


FIG. 4.11

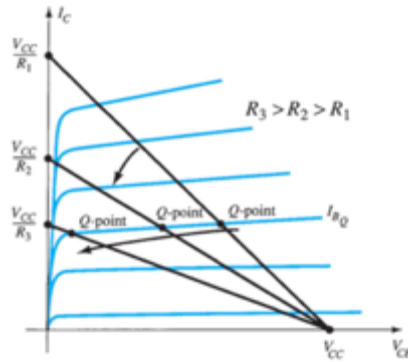
Load-line analysis: (a) the network; (b) the device characteristics.

# Load-Line Analysis



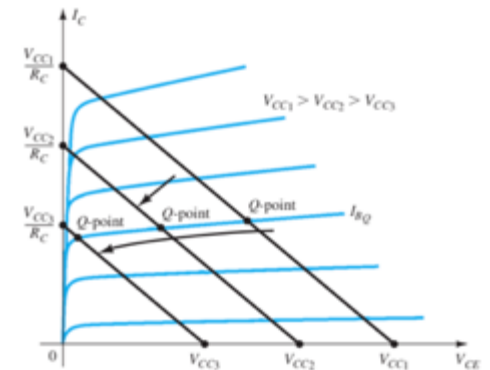
**FIG. 4.13**

Movement of the Q-point with increasing level of  $I_B$ .



**FIG. 4.14**

Effect of an increasing level of  $R_C$  on the load line and the Q-point.



**FIG. 4.15**

Effect of lower values of  $V_{CC}$  on the load line and the Q-point.



# EXAMPLE

**EXAMPLE 4.3** Given the load line of Fig. 4.16 and the defined  $Q$ -point, determine the required values of  $V_{CC}$ ,  $R_C$ , and  $R_B$  for a fixed-bias configuration.

**Solution:** From Fig. 4.16,

$$V_{CE} = V_{CC} = 20 \text{ V at } I_C = 0 \text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0 \text{ V}$$

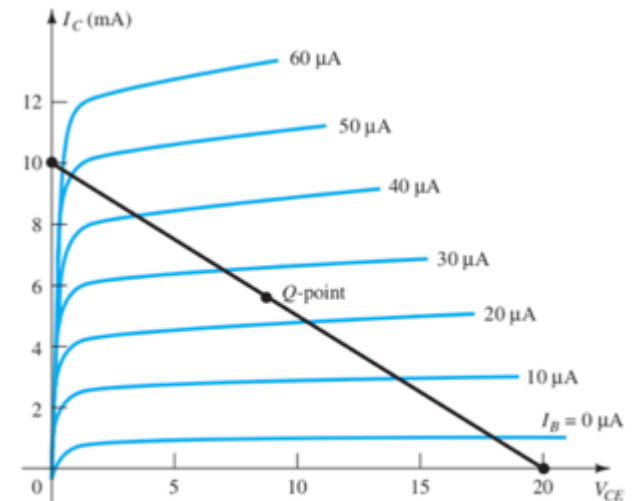
and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{10 \text{ mA}} = 2 \text{ k}\Omega$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V}}{25 \mu\text{A}} = 772 \text{ k}\Omega$$



**FIG. 4.16**  
Example 4.3.

# Thank You

