8 FET Amplifiers

CHAPTER OBJECTIVES

- Become acquainted with the small-signal ac model for a JFET and MOSFET.
- Be able to perform a small-signal ac analysis of a variety of JFET and MOSFET configurations.
- Begin to appreciate the design sequence applied to FET configurations.
- Understand the effects of a source resistor and load resistor on the input impedance, output impedance and overall gain.
- Be able to analyze cascaded configurations with FETs and/or BJT amplifiers.

8.1 INTRODUCTION

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance. They are also low-power-consumption configurations with good frequency range and minimal size and weight. JFETs, depletion MOSFETs, and MESFETs can be used to design amplifiers having similar voltage gains. The depletion MOSFET (MESFET) circuit, however, has a much higher input impedance than a similar JFET configuration.

Whereas a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a *current-controlled* device and the FET is a *voltage-controlled* device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. Whereas the BJT has an amplification factor, β (beta), the FET has a transconductance factor, g_m.

The FET can be used as a linear amplifier or as a digital device in logic circuits. In fact, the enhancement MOSFET is quite popular in digital circuitry, especially in CMOS circuits that require very low power consumption. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications. Table 8.1 in Section 8.13 provides a summary of FET small-signal amplifier circuits and related formulas.

Although the common-source configuration is the most popular one, providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally assumed to be 0 μA and the current gain is an undefined quantity.

Whereas the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides a much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuits.

FET ac amplifier networks can also be analyzed using computer software. Using PSpice or Multisim, one can perform a dc analysis to obtain the circuit bias conditions and an ac analysis to determine the small-signal voltage gain. Using PSpice transistor models, one can analyze the circuit using specific transistor models. On the other hand, one can develop a program using a language such as C++ that can perform both the dc and ac analyses and provide the results in a very special format.

8.2 JFET SMALL-SIGNAL MODEL

The ac analysis of a JFET configuration requires that a small-signal ac model for the JFET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.

The gate-to-source voltage controls the drain-to-source (channel) current of a JFET.

Recall from Chapter 7 that a dc gate-to-source voltage controls the level of dc drain current through a relationship known as Shockley's equation: $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$. The *change* in drain current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\Delta I_D = g_m \Delta V_{GS} \tag{8.1}$$

The prefix *trans-* in the terminology applied to g_m reveals that it establishes a relationship between an output and an input quantity. The root word *conductance* was chosen because g_m is determined by a current-to-voltage ratio similar to the ratio that defines the conductance of a resistor, $G = 1/R = I/V$.

Solving for g_m in Eq. (8.1), we have

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \tag{8.2}$$

Graphical Determination of g_m

If we now examine the transfer characteristics of Fig. 8.1, we find that g_m is actually the slope of the characteristics at the point of operation. That is,

$$g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}} \tag{8.3}$$

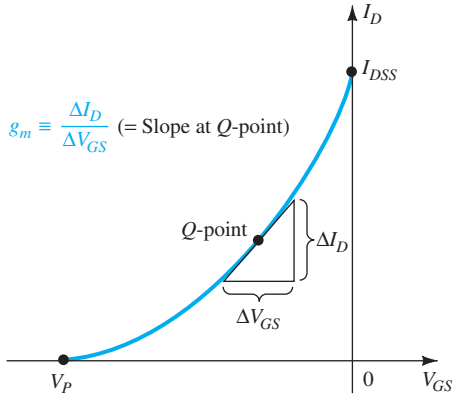


FIG. 8.1
Definition of g_m using transfer characteristic.

Following the curvature of the transfer characteristics, it is reasonably clear that the slope and, therefore, g_m increase as we progress from V_P to I_{DSS}. In other words, as V_{GS} approaches 0 V, the magnitude of g_m increases.

Equation (8.2) reveals that g_m can be determined at any Q-point on the transfer characteristics by simply choosing a finite increment in V_{GS} (or in I_D) about the Q-point and then finding the corresponding change in I_D (or V_{GS}, respectively). The resulting changes in each quantity are then substituted in Eq. (8.2) to determine g_m.

EXAMPLE 8.1 Determine the magnitude of g_m for a JFET with $I_{DSS} = 8$ mA and $V_P = -4$ Vat the following dc bias points:

a. $V_{GS} = -0.5$ V.
b. $V_{GS} = -1.5$ V.
c. $V_{GS} = -2.5$ V.

Solution: The transfer characteristics are generated as Fig. 8.2 using the procedure defined in Chapter 7. Each operating point is then identified and a tangent line is drawn at each point to best reflect the slope of the transfer curve in this region. An appropriate increment is then chosen for V_{GS} to reflect a variation to either side of each Q-point. Equation (8.2) is then applied to determine g_m.

a. $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} \cong \dfrac{2.1\text{ mA}}{0.6\text{ V}} = \mathbf{3.5\text{ mS}}$

b. $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} \cong \dfrac{1.8\text{ mA}}{0.7\text{ V}} \cong \mathbf{2.57\text{ mS}}$

c. $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{1.5\text{ mA}}{1.0\text{ V}} = \mathbf{1.5\text{ mS}}$

Note the decrease in g_m as V_{GS} approaches V_P.

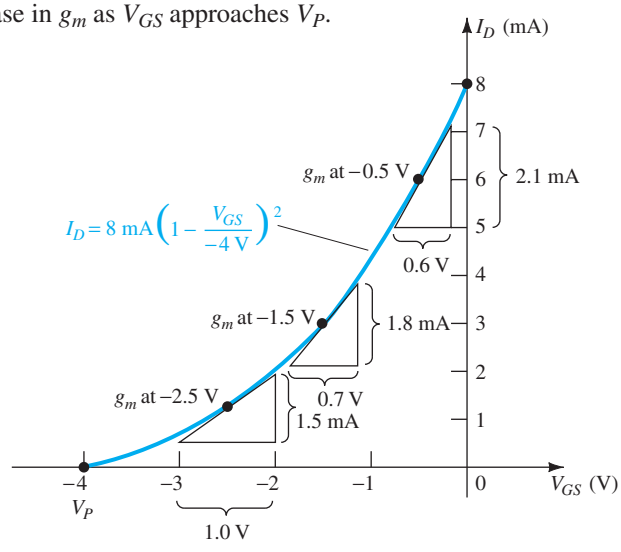


FIG. 8.2
Calculating g_m at various bias points.

Mathematical Definition of g_m

The graphical procedure just described is limited by the accuracy of the transfer plot and the care with which the changes in each quantity can be determined. Naturally, the larger the graph, the better is the accuracy, but this can then become a cumbersome problem. An alternative approach to determining g_m employs the approach used to find the ac resistance of a diode in Chapter 1, where it was stated that:

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

If we therefore take the derivative of I_D with respect to V_{GS} (differential calculus) using Shockley's equation, we can derive an equation for g_m as follows:

$$g_m = \left.\frac{dI_D}{dV_{GS}}\right|_{Q\text{-pt.}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right]$$

$$= I_{DSS}\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\frac{d}{dV_{GS}}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$= 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[\frac{d}{dV_{GS}}(1) - \frac{1}{V_P}\frac{dV_{GS}}{dV_{GS}}\right] = 2I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]\left[0 - \frac{1}{V_P}\right]$$

and

$$\boxed{g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]} \tag{8.4}$$

where $|V_P|$ denotes magnitude only, to ensure a positive value for g_m.

It was mentioned earlier that the slope of the transfer curve is a maximum at $V_{GS} = 0$ V. Plugging in $V_{GS} = 0$ V into Eq. (8.4) results in the following equation for the maximum value of g_m for a JFET in which I_{DSS} and V_P have been specified:

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

and

$$\boxed{g_{m0} = \frac{2I_{DSS}}{|V_P|}} \tag{8.5}$$

where the added subscript 0 reminds us that it is the value of g_m when $V_{GS} = 0$ V. Equation (8.4) then becomes

$$\boxed{g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]} \tag{8.6}$$

EXAMPLE 8.2 For the JFET having the transfer characteristics of Example 8.1:

a. Find the maximum value of g_m.
b. Find the value of g_m at each operating point of Example 8.1 using Eq. (8.6) and compare with the graphical results.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\text{ mA})}{4\text{ V}} = \mathbf{4\text{ mS}}$ (maximum possible value of g_m)

b. At $V_{GS} = -0.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-0.5\text{ V}}{-4\text{ V}}\right] = \mathbf{3.5\text{ mS}}$$ (vs. 3.5 mS graphically)

At $V_{GS} = -1.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-1.5\text{ V}}{-4\text{ V}}\right] = \mathbf{2.5\text{ mS}}$$ (vs. 2.57 mS graphically)

At $V_{GS} = -2.5$ V,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\text{ mS}\left[1 - \frac{-2.5\text{ V}}{-4\text{ V}}\right] = \mathbf{1.5\text{ mS}}$$ (vs. 1.5 mS graphically)

The results of Example 8.2 are certainly sufficiently close to validate Eq. (8.4) through (8.6) for future use when g_m is required.

On specification sheets, g_m is often provided as g_{fs} or y_{fs}, where y indicates it is part of an admittance equivalent circuit. The f signifies *f*orward transfer conductance, and the s indicates that it is connected to the *s*ource terminal.

In equation form,

$$g_m = g_{fs} = y_{fs} \tag{8.7}$$

For the JFET of Fig. 6.20, g_{fs} ranges from 1000 μS to 5000 μS, or 1 mS to 5 mS.

Plotting g_m versus V_{GS}

Since the factor $\left(1 - \frac{V_{GS}}{V_P}\right)$ of Eq. (8.6) is less than 1 for any value of V_{GS} other than 0 V, the magnitude of g_m will decrease as V_{GS} approaches V_P and the ratio $\frac{V_{GS}}{V_P}$ increases in magnitude. At $V_{GS} = V_P$, $g_m = g_{m0}(1 - 1) = 0$. Equation (8.6) defines a straight line with a minimum value of 0 and a maximum value of g_m, as shown by the plot of Fig. 8.3.

In general, therefore

the maximum value of g_m occurs where $V_{GS} = 0$ V and the minimum value at $V_{GS} = V_P$. The more negative the value of V_{GS} the less the value of g_m.

Figure 8.3 also shows that when V_{GS} is one-half the pinch-off value, g_m is one-half the maximum value.

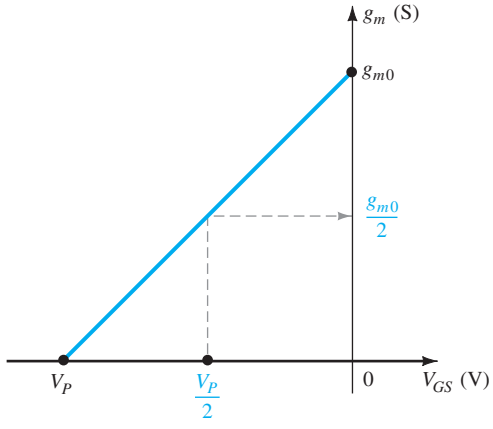


FIG. 8.3
Plot of g_m versus V_{GS}.

EXAMPLE 8.3 Plot g_m versus V_{GS} for the JFET of Examples 8.1 and 8.2.

Solution: Note Fig. 8.4.

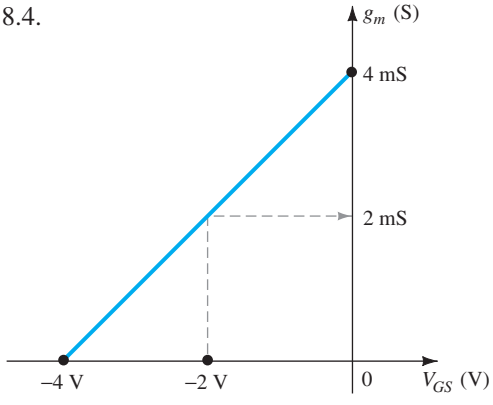


FIG. 8.4
Plot of g_m versus V_{GS} for a JFET with I_{DSS} = 8 mA and $V_P = -4$ V.

Effect of I_D on g_m

A mathematical relationship between g_m and the dc bias current I_D can be derived by noting that Shockley's equation can be written in the following form:

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}} \tag{8.8}$$

Substituting Eq. (8.8) into Eq. (8.6) results in

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}} \tag{8.9}$$

Using Eq. (8.9) to determine g_m for a few specific values of I_D, we obtain the following results:

a. If $I_D = I_{DSS}$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}}{I_{DSS}}} = \boldsymbol{g_{m0}}$$

b. If $I_D = I_{DSS}/2$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/2}{I_{DSS}}} = \mathbf{0.707}\boldsymbol{g_{m0}}$$

c. If $I_D = I_{DSS}/4$,

$$g_m = g_{m0}\sqrt{\frac{I_{DSS}/4}{I_{DSS}}} = \frac{g_{m0}}{2} = \mathbf{0.5}\boldsymbol{g_{m0}}$$

EXAMPLE 8.4 Plot g_m versus I_D for the JFET of Examples 8.1 through 8.3.

Solution: See Fig. 8.5.

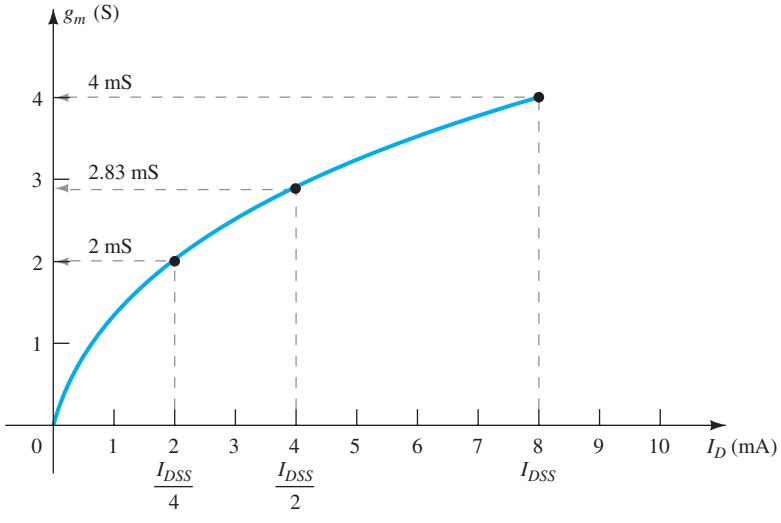


FIG. 8.5
Plot of g_m versus I_D for a JFET with $I_{DSS} = 8$ mA and $V_{GS} = -4$ V.

The plots of Examples 8.3 and 8.4 clearly reveal that

the highest values of g_m are obtained when V_{GS} approaches 0 V and I_D approaches its maximum value of I_{DSS}.

JFET Input Impedance Z_i

The input impedance of all commercially available JFETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i\,(\text{JFET}) = \infty\,\Omega \tag{8.10}$$

For a JFET a practical value of $10^9\ \Omega$ (1000 MΩ) is typical, whereas a value of $10^{12}\ \Omega$ to $10^{15}\ \Omega$ is typical for MOSFETs and MESFETs.

JFET Output Impedance Z_o

The output impedance of JFETs is similar in magnitude to that of conventional BJTs. On JFET specification sheets, the output impedance will typically appear as g_{os} or y_{os} with the units of μS. The parameter y_{os} is a component of an *admittance equivalent circuit*, with the subscript o signifying an *o*utput network parameter and s the terminal (*s*ource) to which it is attached in the model. For the JFET of Fig. 6.20, g_{os} has a range of 10 μS to 50 μS or 20 kΩ ($R = 1/G = 1/50\ \mu$S) to 100 kΩ ($R = 1/G = 1/10\ \mu$S).

In equation form,

$$Z_o\,(\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}} \tag{8.11}$$

The output impedance is defined on the characteristics of Fig. 8.6 as the slope of the horizontal characteristic curve at the point of operation. The more horizontal the curve, the greater is the output impedance. If it is perfectly horizontal, the ideal situation is on hand with the output impedance being infinite (an open circuit)—an often applied approximation.

In equation form,

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}} \tag{8.12}$$

Note the requirement when applying Eq. (8.12) that the voltage V_{GS} remain constant when r_d is determined. This is accomplished by drawing a straight line approximating the V_{GS} line at the point of operation. A ΔV_{DS} or ΔI_D is then chosen and the other quantity measured off for use in the equation.

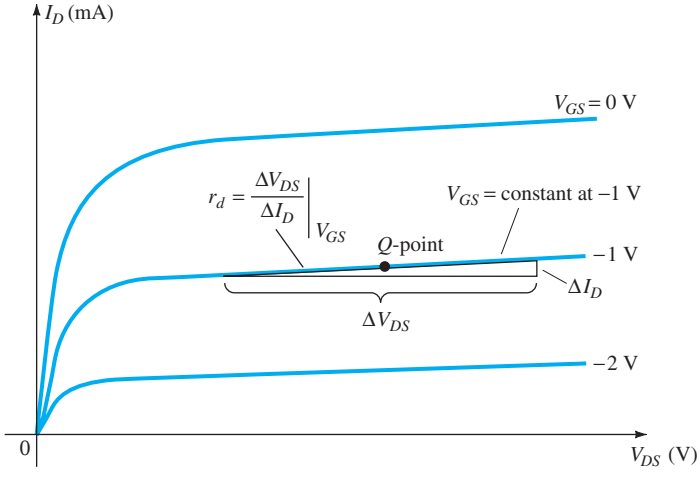


FIG. 8.6
Definition of r_d using JFET drain characteristics.

EXAMPLE 8.5 Determine the output impedance for the JFET of Fig. 8.7 for $V_{GS} = 0$ V and $V_{GS} = -2$ V at $V_{DS} = 8$ V.

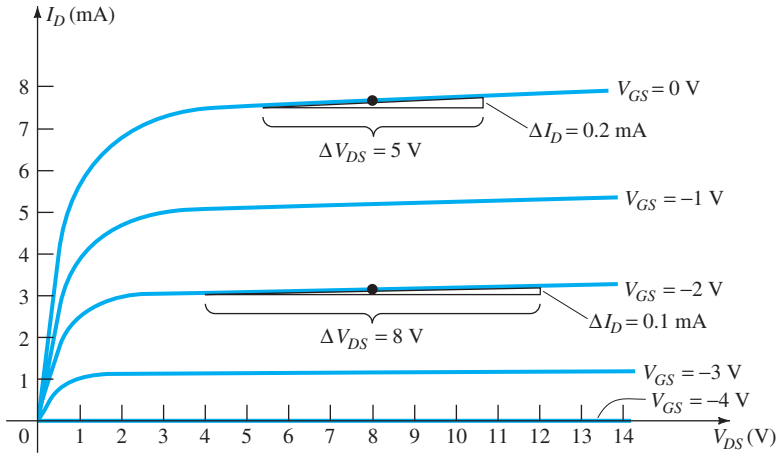


FIG. 8.7

Drain characteristics used to calculate r_d in Example 8.5.

Solution: For $V_{GS} = 0$ V, a tangent line is drawn and ΔV_{DS} is chosen as 5 V, resulting in a ΔI_D of 0.2 mA. Substituting into Eq. (8.12), we find

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=0\text{ V}} = \frac{5\text{ V}}{0.2\text{ mA}} = \mathbf{25\ k\Omega}$$

For $V_{GS} = -2$ V, a tangent line is drawn and ΔV_{DS} is chosen as 8 V, resulting in a ΔI_D of 0.1 mA. Substituting into Eq. (8.12), we find

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=-2\text{ V}} = \frac{8\text{ V}}{0.1\text{ mA}} = \mathbf{80\ k\Omega}$$

which shows that r_d does change from one operating region to another, with lower values typically occurring at lower levels of V_{GS} (closer to 0 V).

JFET AC Equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the JFET transistor in the ac domain can be constructed. The control of I_d by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source as shown in Fig. 8.8. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

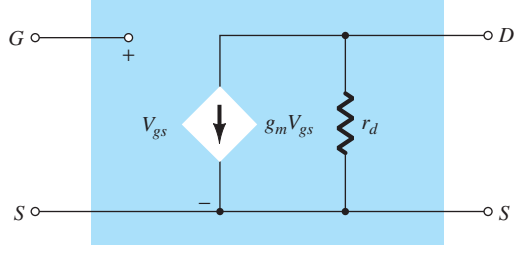


FIG. 8.8

JFET ac equivalent circuit.

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor r_d from drain to source. Note that the gate-to-source voltage is now represented by V_{gs} (lowercase subscripts) to distinguish it from dc levels. In addition, note that the source is common to both input and output circuits, whereas the gate and drain terminals are only in "touch" through the controlled current source $g_m V_{gs}$.

In situations where r_d is ignored (assumed sufficiently large in relation to other elements of the network to be approximated by an open circuit), the equivalent circuit is simply a current source whose magnitude is controlled by the signal V_{gs} and parameter g_m—clearly a voltage-controlled current source.

EXAMPLE 8.6 Given $g_{fs} = 3.8$ mS and $g_{os} = 20\ \mu$S, sketch the FET ac equivalent model.

Solution:

$$g_m = g_{fs} = 3.8 \text{ mS} \qquad \text{and} \qquad r_d = \frac{1}{g_{os}} = \frac{1}{20\ \mu\text{S}} = 50\ \text{k}\Omega$$

resulting in the ac equivalent model of Fig. 8.9.

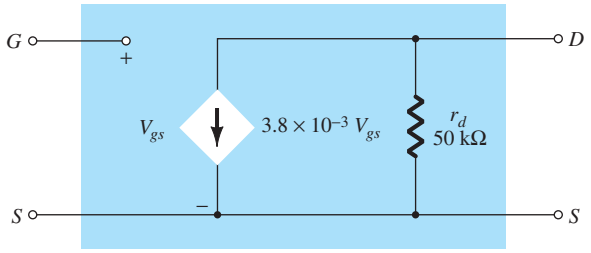


FIG. 8.9
JFET ac equivalent model for Example 8.6.

8.3 FIXED-BIAS CONFIGURATION

Now that the JFET equivalent circuit has been defined, a number of fundamental JFET small-signal configurations are investigated. The approach parallels the ac analysis of BJT amplifiers with a determination of the important parameters of Z_i, Z_o, and A_v for each configuration.

The *fixed-bias* configuration of Fig. 8.10 includes the coupling capacitors C_1 and C_2, which isolate the dc biasing arrangement from the applied signal and load; they act as short-circuit equivalents for the ac analysis.

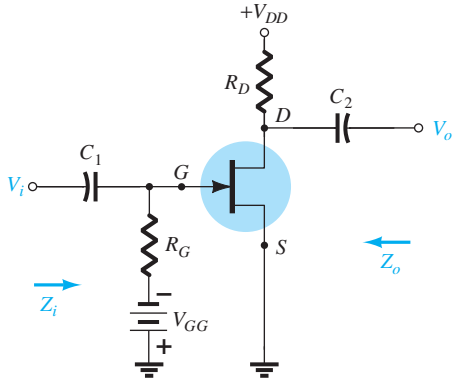


FIG. 8.10
JFET fixed-bias configuration.

Once the levels of g_m and r_d are determined from the dc biasing arrangement, specification sheet, or characteristics, the ac equivalent model can be substituted between the appropriate terminals as shown in Fig. 8.11. Note that both capacitors have the short-circuit equivalent because the reactance $X_C = 1/(2\pi fC)$ is sufficiently small compared to other impedance levels of the network, and the dc batteries V_{GG} and V_{DD} are set to 0 V by a short-circuit equivalent.

The network of Fig. 8.11 is then carefully redrawn as shown in Fig. 8.12. Note the defined polarity of V_{gs}, which defines the direction of $g_m V_{gs}$. If V_{gs} is negative, the direction of the current source reverses. The applied signal is represented by V_i and the output signal across $R_D \| r_d$ by V_o.

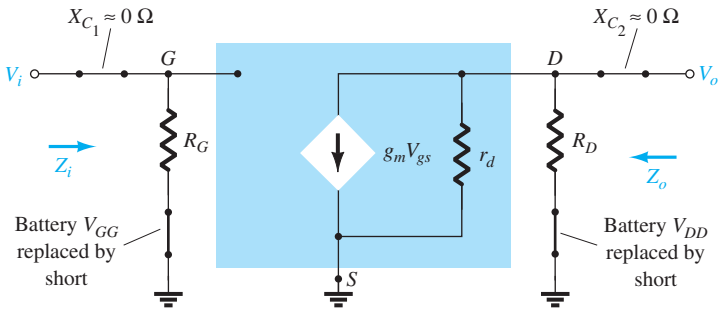


FIG. 8.11
Substituting the JFET ac equivalent circuit unit into the network of Fig. 8.10.

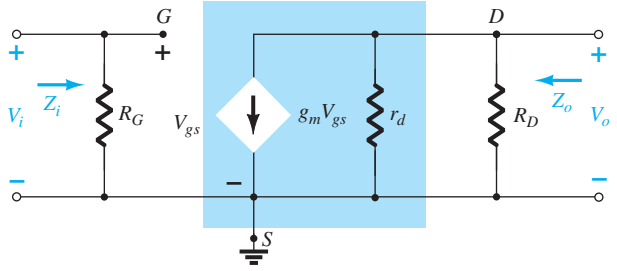


FIG. 8.12
Redrawn network of Fig. 8.11.

Z_i Figure 8.12 clearly reveals that

$$\boxed{Z_i = R_G} \tag{8.13}$$

because of the infinite input impedance at the input terminals of the JFET.

Z_o Setting $V_i = 0$ V as required by the definition of Z_o will establish V_{gs} as 0 V also. The result is $g_m V_{gs} = 0$ mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 8.13. The output impedance is

$$\boxed{Z_o = R_D \| r_d} \tag{8.14}$$

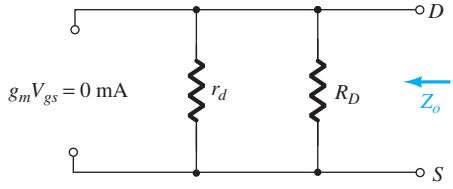


FIG. 8.13
Determining Z_o.

If the resistance r_d is sufficiently large (at least 10:1) compared to R_D, the approximation $r_d \| R_D \cong R_D$ can often be applied and

$$\boxed{Z_o \cong R_D}_{\ r_d \geq 10R_D} \tag{8.15}$$

A_v Solving for V_o in Fig. 8.12, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but
$$V_{gs} = V_i$$

and
$$V_o = -g_m V_i (r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D) \tag{8.16}$$

If $r_d \geq 10R_D$,

$$A_v = \frac{V_o}{V_i} = -g_m R_D \quad r_d \geq 10R_D \tag{8.17}$$

Phase Relationship The negative sign in the resulting equation for A_v clearly reveals a phase shift of 180° between input and output voltages.

EXAMPLE 8.7 The fixed-bias configuration of Example 7.1 had an operating point defined by $V_{GS_Q} = -2$ V and $I_{D_Q} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The network is redrawn as Fig. 8.14 with an applied signal V_i. The value of y_{os} is provided as 40 μS.

a. Determine g_m.
b. Find r_d.
c. Determine Z_i.
d. Calculate Z_o.
e. Determine the voltage gain A_v.
f. Determine A_v ignoring the effects of r_d.

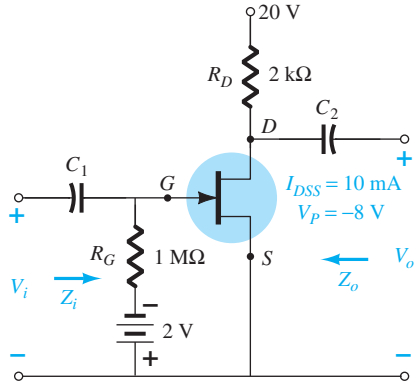


FIG. 8.14
JFET configuration for Example 8.7.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\text{ mS}}$$

b. $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{40\ \mu\text{S}} = \mathbf{25\ k\Omega}$

c. $Z_i = R_G = \mathbf{1\ M\Omega}$

d. $Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\ k\Omega}$

e. $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega)$
$= \mathbf{-3.48}$

f. $A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$

As demonstrated in part (f), a ratio of 25 kΩ:2 kΩ = 12.5:1 between r_d and R_D results in a difference of 8% in the solution.

8.4 SELF-BIAS CONFIGURATION

Bypassed R_S

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources. The *self-bias* configuration of Fig. 8.15 requires only one dc supply to establish the desired operating point.

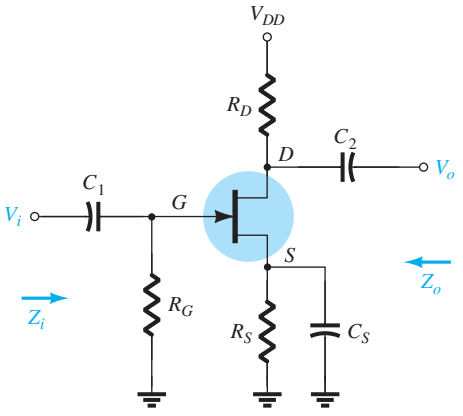


FIG. 8.15
Self-bias JFET configuration.

The capacitor C_S across the source resistance assumes its open-circuit equivalence for dc, allowing R_S to define the operating point. Under ac conditions, the capacitor assumes the short-circuit state and "short circuits" the effects of R_S. If left in the ac, gain will be reduced, as will be shown in the paragraphs to follow.

The JFET equivalent circuit is established in Fig. 8.16 and carefully redrawn in Fig. 8.17.

Since the resulting configuration is the same as appearing in Fig. 8.12, the resulting equations for Z_i, Z_o, and A_v will be the same.

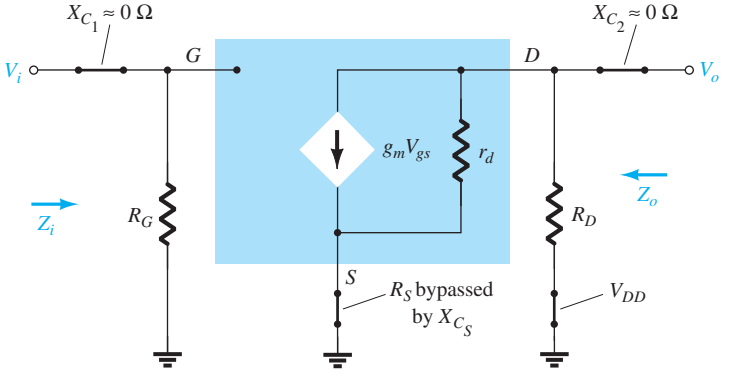


FIG. 8.16
Network of Fig. 8.15 following the substitution of the JFET ac equivalent circuit.

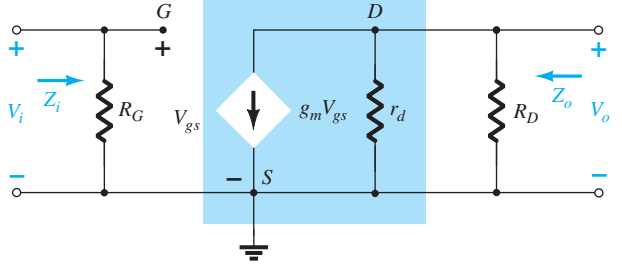


FIG. 8.17
Redrawn network of Fig. 8.16.

Z_i

$$Z_i = R_G \tag{8.18}$$

Z_o

$$Z_o = r_d \| R_D \tag{8.19}$$

If $r_d \geq 10R_D$,

$$Z_o \cong R_D \quad r_d \geq 10R_D \tag{8.20}$$

A_v

$$A_v = -g_m(r_d \| R_D) \tag{8.21}$$

If $r_d \geq 10R_D$,

$$A_v = -g_m R_D \quad r_d \geq 10R_D \tag{8.22}$$

Phase Relationship The negative sign in the solutions for A_v again indicates a phase shift of 180° between V_i and V_o.

Unbypassed R_S

If C_S is removed from Fig 8.15, the resistor R_S will be part of the ac equivalent circuit as shown in Fig. 8.18. In this case, there is no obvious way to reduce the network to lower its level of complexity. In determining the levels of Z_i, Z_o, and A_v, one must be very careful with notation and defined polarities and direction. Initially, the resistance r_d will be left out of the analysis to form a basis for comparison.

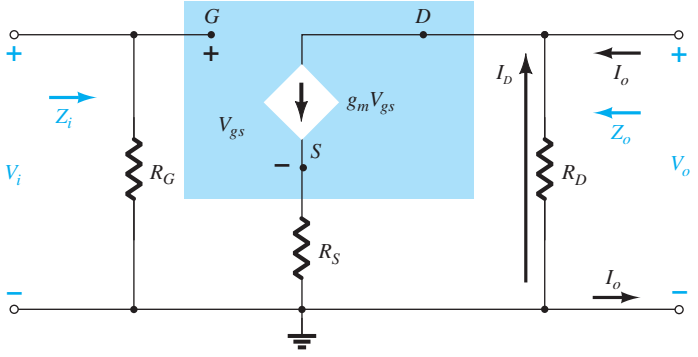


FIG. 8.18
Self-bias JFET configuration including the effects of R_S with $r_d = \infty\Omega$.

Z_i Due to the open-circuit condition between the gate and the output network, the input remains the following:

$$Z_i = R_G \tag{8.23}$$

Z_o The output impedance is defined by

$$Z_o = \left.\frac{V_o}{I_o}\right|_{V_i=0}$$

Setting $V_i = 0$ V in Fig. 8.18 results in the gate terminal being at ground potential (0 V). The voltage across R_G is then 0 V, and R_G has been effectively "shorted out" of the picture.

Applying Kirchhoff's current law results in

$$I_o + I_D = g_m V_{gs}$$

with

$$V_{gs} = -(I_o + I_D)R_S$$

so that $$I_o + I_D = -g_m(I_o + I_D)R_S = -g_m I_o R_S - g_m I_D R_S$$

or $$I_o[1 + g_m R_S] = -I_D[1 + g_m R_S]$$

and $$I_o = -I_D$$ (the controlled current source $g_m V_{gs} = 0$ A for the applied conditions)

Since $$V_o = -I_D R_D$$

then $$V_o = -(-I_o)R_D = I_o R_D$$

and $$\boxed{Z_o = \frac{V_o}{I_o} = R_D}\Big|_{r_d = \infty\,\Omega} \qquad \textbf{(8.24)}$$

If r_d is included in the network, the equivalent will appear as shown in Fig. 8.19.

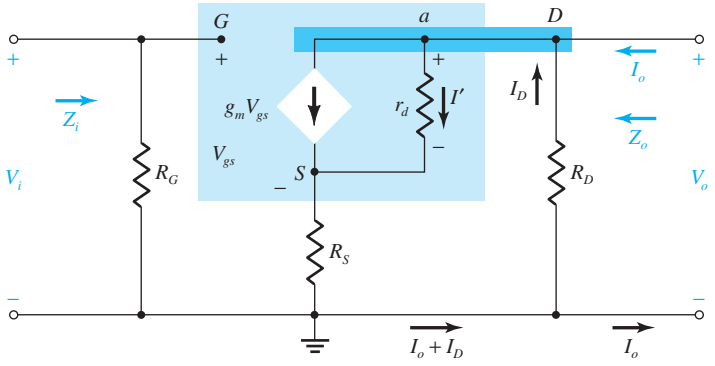


FIG. 8.19
Including the effects of r_d in the self-bias JFET configuration.

Since $$Z_o = \frac{V_o}{I_o}\bigg|_{V_i = 0\text{ V}} = -\frac{I_D R_D}{I_o}$$

we should try to find an expression for I_o in terms of I_D.

Applying Kirchhoff's current law, we have

$$I_o = g_m V_{gs} + I_{r_d} - I_D$$

but $$V_{r_d} = V_o + V_{gs}$$

and $$I_o = g_m V_{gs} + \frac{V_o + V_{gs}}{r_d} - I_D$$

or $$I_o = \left(g_m + \frac{1}{r_d}\right)V_{gs} - \frac{I_D R_D}{r_d} - I_D \text{ using } V_o = -I_D R_D$$

Now, $$V_{gs} = -(I_D + I_o)R_S$$

so that $$I_o = -\left(g_m + \frac{1}{r_d}\right)(I_D + I_o)R_S - \frac{I_D R_D}{r_d} - I_D$$

with the result that $$I_o\left[1 + g_m R_S + \frac{R_S}{r_d}\right] = -I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]$$

or $$I_o = \frac{-I_D\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]}{1 + g_m R_S + \frac{R_S}{r_d}}$$

and $$Z_o = \frac{V_o}{I_o} = \frac{-I_D R_D}{\frac{-I_D\left(1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right)}{1 + g_m R_S + \frac{R_S}{r_d}}}$$

and finally,

$$\boxed{Z_o = \frac{\left[1 + g_m R_S + \dfrac{R_S}{r_d}\right]}{\left[1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]} R_D} \qquad \textbf{(8.25a)}$$

For $r_d \geq 10R_D$,

$$\left(1 + g_m R_S + \frac{R_S}{r_d}\right) \gg \frac{R_D}{r_d}$$

and

$$1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d} \cong 1 + g_m R_S + \frac{R_S}{r_d}$$

resulting in

$$\boxed{Z_o \cong R_D}_{\,r_d \geq 10R_D} \qquad \textbf{(8.25b)}$$

A_v For the network of Fig. 8.19, application of Kirchhoff's voltage law to the input circuit results in

$$V_i - V_{gs} - V_{R_S} = 0$$
$$V_{gs} = V_i - I_D R_S$$

The voltage across r_d using Kirchhoff's voltage law is

$$V_{r_d} = V_o - V_{R_S}$$

and

$$I' = \frac{V_{r_d}}{r_d} = \frac{V_o - V_{R_S}}{r_d}$$

so that application of Kirchhoff's current law results in

$$I_D = g_m V_{gs} + \frac{V_o - V_{R_S}}{r_d}$$

Substituting for V_{gs} from above and substituting for V_o and V_{R_S}, we have

$$I_D = g_m[V_i - I_D R_S] + \frac{(-I_D R_D) - (I_D R_S)}{r_d}$$

so that

$$I_D\left[1 + g_m R_S + \frac{R_D + R_S}{r_d}\right] = g_m V_i$$

or

$$I_D = \frac{g_m V_i}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

The output voltage is then

$$V_o = -I_D R_D = -\frac{g_m R_D V_i}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}} \qquad \textbf{(8.26)}$$

Again, if $r_d \geq 10(R_D + R_S)$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{g_m R_D}{1 + g_m R_S}}_{\,r_d \geq 10(R_D + R_S)} \qquad \textbf{(8.27)}$$

Phase Relationship The negative sign in Eq. (8.26) again reveals that a 180° phase shift will exist between V_i and V_o.

EXAMPLE 8.8 The self-bias configuration of Example 7.2 has an operating point defined by $V_{GS_Q} = -2.6$ V and $I_{D_Q} = 2.6$ mA, with $I_{DSS} = 8$ mA and $V_P = -6$ V. The network is redrawn as Fig. 8.20 with an applied signal V_i. The value of g_{os} is given as 20 μS.

a. Determine g_m.
b. Find r_d.
c. Find Z_i.
d. Calculate Z_o with and without the effects of r_d. Compare the results.
e. Calculate A_v with and without the effects of r_d. Compare the results.

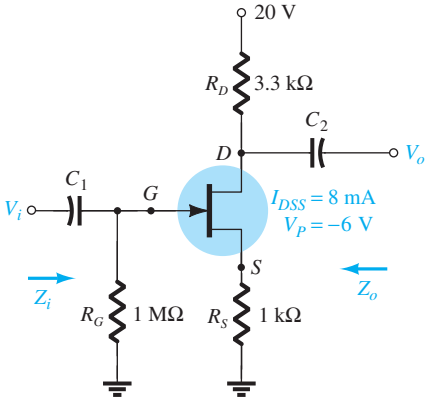


FIG. 8.20
Network for Example 8.8.

Solution:

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\text{ mA})}{6\text{ V}} = 2.67\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.67\text{ mS}\left(1 - \frac{(-2.6\text{ V})}{(-6\text{ V})}\right) = \mathbf{1.51\text{ mS}}$$

b. $$r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$$

c. $Z_i = R_G = \mathbf{1\ M\Omega}$

d. With r_d,

$$r_d = 50\text{ k}\Omega > 10R_D = 33\text{ k}\Omega$$

Therefore,

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

If $r_d = \infty\,\Omega$,

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

e. With r_d,

$$A_v = \frac{-g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega) + \dfrac{3.3\text{ k}\Omega + 1\text{ k}\Omega}{50\text{ k}\Omega}}$$

$$= \mathbf{-1.92}$$

With $r_d = \infty\,\Omega$ (open-circuit equivalence),

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega)} = \mathbf{-1.98}$$

As above, the effect of r_d is minimal because the condition $r_d \geq 10(R_D + R_S)$ is satisfied.

Note also that the typical gain of a JFET amplifier is less than that generally encountered for BJTs of similar configurations. Keep in mind, however, that Z_i is magnitudes greater than the typical Z_i of a BJT, which will have a very positive effect on the overall gain of a system.

The popular voltage-divider configuration for BJTs can also be applied to JFETs as demonstrated in Fig. 8.21.

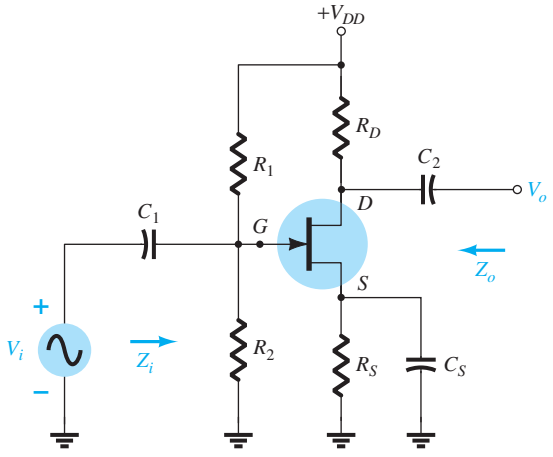


FIG. 8.21
JFET voltage-divider configuration.

Substituting the ac equivalent model for the JFET results in the configuration of Fig. 8.22. Replacing the dc supply V_{DD} by a short-circuit equivalent has grounded one end of R_1 and R_D. Since each network has a common ground, R_1 can be brought down in parallel with R_2 as shown in Fig. 8.23. R_D can also be brought down to ground, but in the output circuit across r_d. The resulting ac equivalent network now has the basic format of some of the networks already analyzed.

Z_i R_1 and R_2 are in parallel with the open-circuit equivalence of the JFET, resulting in

$$Z_i = R_1 \| R_2 \tag{8.28}$$

Z_o Setting $V_i = 0$ V sets V_{gs} and $g_m V_{gs}$ to zero, and

$$Z_o = r_d \| R_D \tag{8.29}$$

For $r_d \geq 10R_D$,

$$Z_o \cong R_D \qquad r_d \geq 10R_D \tag{8.30}$$

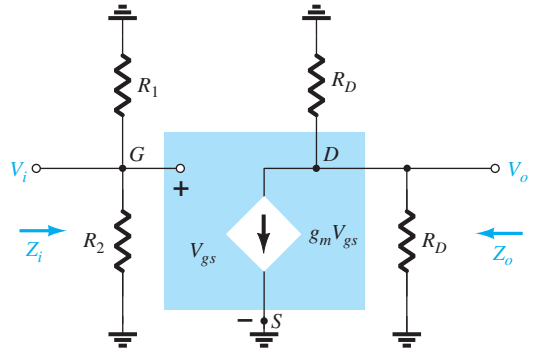


FIG. 8.22
Network of Fig. 8.21 under ac conditions.

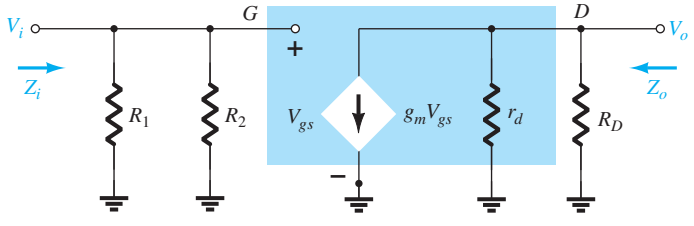


FIG. 8.23
Redrawn network of Fig. 8.22.

A_v

$$V_{gs} = V_i$$

and

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

so that

$$A_v = \frac{V_o}{V_i} = \frac{-g_m V_{gs}(r_d \| R_D)}{V_{gs}}$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)} \tag{8.31}$$

If $r_d \geq 10R_D$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -g_m R_D}_{r_d \geq 10R_D} \tag{8.32}$$

Note that the equations for Z_o and A_v are the same as obtained for the fixed-bias and self-bias (with bypassed R_S) configurations. The only difference is the equation for Z_i, which is now sensitive to the parallel combination of R_1 and R_2.

8.6 COMMON-GATE CONFIGURATION

The last JFET configuration to be analyzed in detail is the common-gate configuration of Fig. 8.24, which parallels the common-base configuration employed with BJT transistors.

Substituting the JFET equivalent circuit results in Fig. 8.25. Note the continuing requirement that the controlled source $g_m V_{gs}$ be connected from drain to source with r_d in parallel. The isolation between input and output circuits has obviously been lost since the gate terminal is now connected to the common ground of the network and the controlled current source is connected directly from drain to source. In addition, the resistor connected between input terminals is no longer R_G, but the resistor R_S connected from source to ground. Note also the location of the controlling voltage V_{gs} and the fact that it appears directly across the resistor R_S.

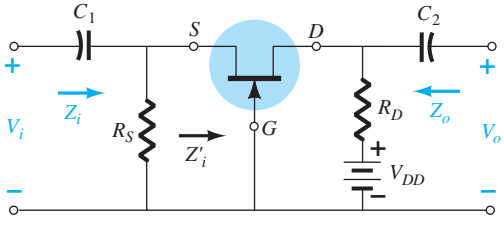


FIG. 8.24
JFET common-gate configuration.

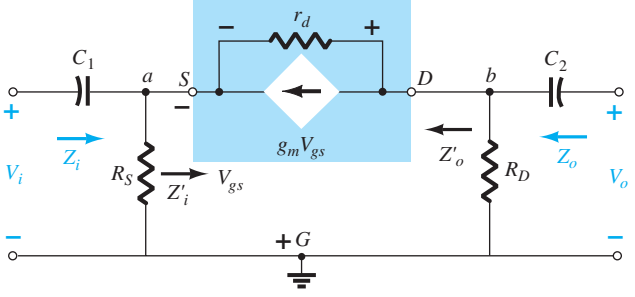


FIG. 8.25
Network of Fig. 8.24 following substitution of JFET ac equivalent model.

Z_i The resistor R_S is directly across the terminals defining Z_i. Let us therefore find the impedance Z_i' of Fig. 8.24, which will simply be in parallel with R_S when Z_i is defined.

The network of interest is redrawn as Fig. 8.26. The voltage $V' = -V_{gs}$. Applying Kirchhoff's voltage law around the output perimeter of the network results in

$$V' - V_{r_d} - V_{R_D} = 0$$

and

$$V_{r_d} = V' - V_{R_D} = V' - I'R_D$$

Applying Kirchhoff's current law at node a results in

$$I' + g_m V_{gs} = I_{r_d}$$

and

$$I' = I_{r_d} - g_m V_{gs} = \frac{(V' - I'R_D)}{r_d} - g_m V_{gs}$$

or

$$I' = \frac{V'}{r_d} - \frac{I'R_D}{r_d} - g_m[-V']$$

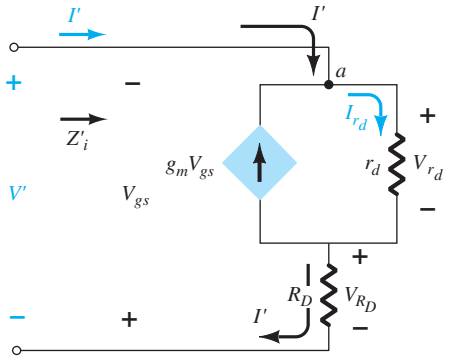


FIG. 8.26
Determining Z_i' for the network of Fig. 8.24.

so that
$$I'\left[1 + \frac{R_D}{r_d}\right] = V'\left[\frac{1}{r_d} + g_m\right]$$

and
$$\boxed{Z_i' = \frac{V'}{I'} = \frac{\left[1 + \dfrac{R_D}{r_d}\right]}{\left[g_m + \dfrac{1}{r_d}\right]}} \qquad \textbf{(8.33)}$$

or
$$Z_i' = \frac{V'}{I'} = \frac{r_d + R_D}{1 + g_m r_d}$$

and
$$Z_i = R_S \| Z_i'$$

which results in
$$\boxed{Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right]} \qquad \textbf{(8.34)}$$

If $r_d \geq 10R_D$, Eq. (8.33) permits the following approximation since $R_D/r_d \ll 1$ and $1/r_d \ll g_m$:

$$Z_i' = \frac{\left[1 + \dfrac{R_D}{r_d}\right]}{\left[g_m + \dfrac{1}{r_d}\right]} \cong \frac{1}{g_m}$$

and
$$\boxed{Z_i \cong R_S \| 1/g_m}_{\,r_d \geq 10R_D} \qquad \textbf{(8.35)}$$

Z_o Substituting $V_i = 0$ V in Fig. 8.25 will "short-out" the effects of R_S and set V_{gs} to 0 V. The result is $g_m V_{gs} = 0$, and r_d will be in parallel with R_D. Therefore,

$$\boxed{Z_o = R_D \| r_d} \qquad \textbf{(8.36)}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{\,r_d \geq 10R_D} \qquad \textbf{(8.37)}$$

A_v Figure 8.25 reveals that

$$V_i = -V_{gs}$$

and
$$V_o = I_D R_D$$

The voltage across r_d is

$$V_{r_d} = V_o - V_i$$

and
$$I_{r_d} = \frac{V_o - V_i}{r_d}$$

Applying Kirchhoff's current law at node b in Fig. 8.25 results in
$$I_{r_d} + I_D + g_m V_{gs} = 0$$

and
$$I_D = -I_{r_d} - g_m V_{gs}$$
$$= -\left[\frac{V_o - V_i}{r_d}\right] - g_m[-V_i]$$
$$I_D = \frac{V_i - V_o}{r_d} + g_m V_i$$

so that
$$V_o = I_D R_D = \left[\frac{V_i - V_o}{r_d} + g_m V_i\right] R_D$$
$$= \frac{V_i R_D}{r_d} - \frac{V_o R_D}{r_d} + g_m$$

and
$$V_o\left[1 + \frac{R_D}{r_d}\right] = V_i\left[\frac{R_D}{r_d} + g_m R_D\right]$$

with
$$\boxed{A_v = \frac{V_o}{V_i} = \frac{\left[g_m R_D + \dfrac{R_D}{r_d}\right]}{\left[1 + \dfrac{R_D}{r_d}\right]}} \qquad \textbf{(8.38)}$$

For $r_d \geq 10R_D$, the factor R_D/r_d of Eq. (8.38) can be dropped as a good approximation, and

$$\boxed{A_v \cong g_m R_D}_{\,r_d \geq 10R_D} \qquad \textbf{(8.39)}$$

Phase Relationship The fact that A_v is a positive number will result in an *in-phase* relationship between V_o and V_i for the common-gate configuration.

EXAMPLE 8.9 Although the network of Fig. 8.27 may not initially appear to be of the common-gate variety, a close examination will reveal that it has all the characteristics of Fig. 8.24. If $V_{GS_Q} = -2.2$ V and $I_{D_Q} = 2.03$ mA:

a. Determine g_m.
b. Find r_d.
c. Calculate Z_i with and without r_d. Compare results.
d. Find Z_o with and without r_d. Compare results.
e. Determine V_o with and without r_d. Compare results.

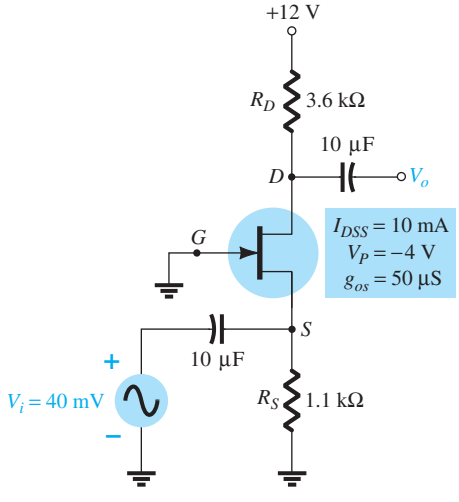


FIG. 8.27
Network for Example 8.9.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{4\text{ V}} = 5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 5\text{ mS}\left(1 - \frac{(-2.2\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.25\ mS}$$

b. $r_d = \dfrac{1}{g_{os}} = \dfrac{1}{50\ \mu\text{S}} = \mathbf{20\ k\Omega}$

c. With r_d,

$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right] = 1.1\text{ k}\Omega \| \left[\frac{20\text{ k}\Omega + 3.6\text{ k}\Omega}{1 + (2.25\text{ mS})(20\text{ k}\Omega)}\right]$$
$$= 1.1\text{ k}\Omega \| 0.51\text{ k}\Omega = \mathbf{0.35\ k\Omega}$$

Without r_d,

$$Z_i = R_S \| 1/g_m = 1.1\text{ k}\Omega \| 1/2.25\text{ ms} = 1.1\text{ k}\Omega \| 0.44\text{ k}\Omega$$
$$= \mathbf{0.31\ k\Omega}$$

Even though the condition $r_d \geq 10R_D$ is not satisfied with $r_d = 20\text{ k}\Omega$ and $10R_D = 36\text{ k}\Omega$, both equations result in essentially the same level of impedance. In this case, $1/g_m$ was the predominant factor.

d. With r_d,

$$Z_o = R_D \| r_d = 3.6\text{ k}\Omega \| 20\text{ k}\Omega = \mathbf{3.05\ k\Omega}$$

Without r_d,

$$Z_o = R_D = \mathbf{3.6\ k\Omega}$$

Again the condition $r_d \geq 10R_D$ is *not* satisfied, but both results are reasonably close. R_D is certainly the predominant factor in this example.

e. With r_d,

$$A_v = \frac{\left[g_m R_D + \dfrac{R_D}{r_d}\right]}{\left[1 + \dfrac{R_D}{r_d}\right]} = \frac{\left[(2.25\text{ mS})(3.6\text{ k}\Omega) + \dfrac{3.6\text{ k}\Omega}{20\text{ k}\Omega}\right]}{\left[1 + \dfrac{3.6\text{ k}\Omega}{20\text{ k}\Omega}\right]}$$
$$= \frac{8.1 + 0.18}{1 + 0.18} = \mathbf{7.02}$$

and $A_v = \dfrac{V_o}{V_i} \Rightarrow V_o = A_v V_i = (7.02)(40\text{ mV}) = \mathbf{280.8\ mV}$

Without r_d,

$$A_v = g_m R_D = (2.25\text{ mS})(3.6\text{ k}\Omega) = \mathbf{8.1}$$

with $V_o = A_v V_i = (8.1)(40\text{ mV}) = \mathbf{324\ mV}$

In this case, the difference is a little more noticeable, but not dramatically so.

Example 8.9 demonstrates that even though the condition $r_d \geq 10R_D$ was not satisfied, the results for the parameters given were not significantly different using the exact and approximate equations. In fact, in most cases, the approximate equations can be used to find a reasonable idea of particular levels with a reduced amount of effort.

8.7 SOURCE-FOLLOWER (COMMON-DRAIN) CONFIGURATION

The JFET equivalent of the BJT emitter-follower configuration is the source-follower configuration of Fig. 8.28. Note that the output is taken off the source terminal and, when the dc supply is replaced by its short-circuit equivalent, the drain is grounded (hence, the terminology *common-drain*).

Substituting the JFET equivalent circuit results in the configuration of Fig. 8.29. The controlled source and the internal output impedance of the JFET are tied to ground at one end and R_S on the other, with V_o across R_S. Since $g_m V_{gs}$, r_d, and R_S are connected to

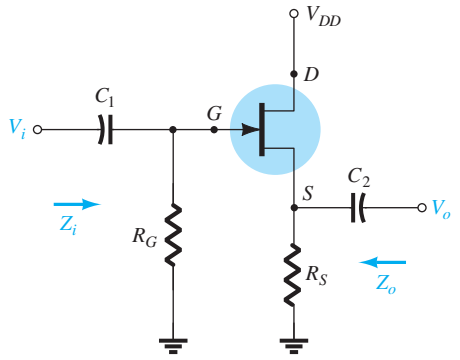


FIG. 8.28
JFET source-follower configuration.

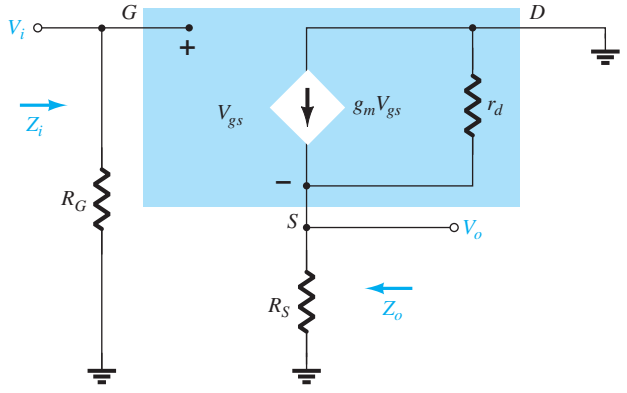


FIG. 8.29
Network of Fig. 8.28 following the substitution of the JFET ac equivalent model.

the same terminal and ground, they can all be placed in parallel as shown in Fig. 8.30. The current source reversed direction, but V_{gs} is still defined between the gate and source terminals.

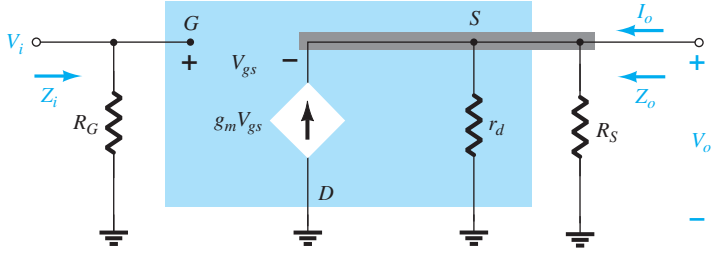


FIG. 8.30
Network of Fig. 8.29 redrawn.

Z_i Figure 8.30 clearly reveals that Z_i is defined by

$$\boxed{Z_i = R_G} \tag{8.40}$$

Z_o Setting $V_i = 0$ V results in the gate terminal being connected directly to the ground as shown in Fig. 8.31.

The fact that V_{gs} and V_o are across the same parallel network results in $V_o = -V_{gs}$.

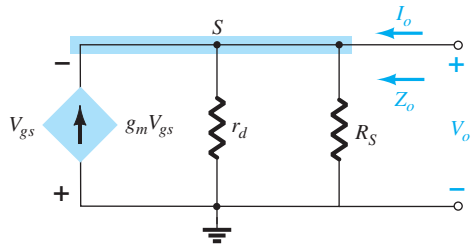


FIG. 8.31
Determining Z_o for the network of Fig. 8.30.

Applying Kirchhoff's current law at node S, we obtain

$$I_o + g_m V_{gs} = I_{r_d} + I_{R_s} = \frac{V_o}{r_d} + \frac{V_o}{R_S}$$

The result is

$$I_o = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m V_{gs} = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m[-V_o] = V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]$$

and

$$Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + g_m} = \frac{1}{\frac{1}{r_d} + \frac{1}{R_S} + \frac{1}{1/g_m}}$$

which has the same format as the total resistance of three parallel resistors. Therefore,

$$\boxed{Z_o = r_d \| R_S \| 1/g_m} \tag{8.41}$$

For $r_d \geq 10\,R_S$,

$$\boxed{Z_o \cong R_S \| 1/g_m}_{\,r_d \geq 10R_S} \tag{8.42}$$

A_v The output voltage V_o is determined by

$$V_o = g_m V_{gs}(r_d \| R_S)$$

and applying Kirchhoff's voltage law around the perimeter of the network of Fig. 8.30 results in

$$V_i = V_{gs} + V_o$$

and

$$V_{gs} = V_i - V_o$$

so that

$$V_o = g_m(V_i - V_o)(r_d \| R_S)$$

or

$$V_o = g_m V_i(r_d \| R_S) - g_m V_o(r_d \| R_S)$$

and

$$V_o[1 + g_m(r_d \| R_S)] = g_m V_i(r_d \| R_S)$$

so that

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}} \tag{8.43}$$

In the absence of r_d or if $r_d \geq 10\,R_S$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong \frac{g_m R_S}{1 + g_m R_S}}_{\,r_d \geq 10R_S} \tag{8.44}$$

Since the denominator of Eq. (8.43) is larger than the numerator by a factor of one, the gain can never be equal to or greater than one (as encountered for the emitter-follower BJT network).

Phase Relationship Since A_v of Eq. (8.43) is a positive quantity, V_o and V_i are in phase for the JFET source-follower configuration.

EXAMPLE 8.10 A dc analysis of the source-follower network of Fig. 8.32 results in $V_{GS_Q} = -2.86$ V and $I_{D_Q} = 4.56$ mA.

a. Determine g_m.
b. Find r_d.
c. Determine Z_i.
d. Calculate Z_o with and without r_d. Compare results.
e. Determine A_v with and without r_d. Compare results.

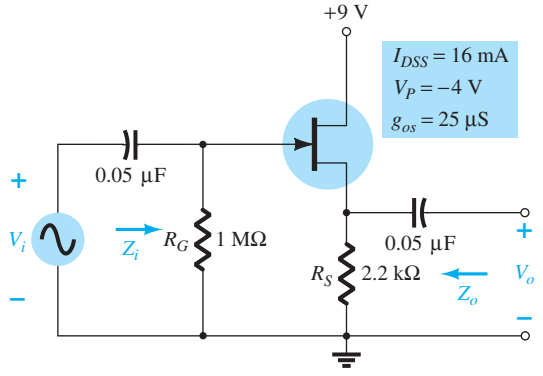


FIG. 8.32
Network to be analyzed in Example 8.10.

Solution:

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(16\text{ mA})}{4\text{ V}} = 8\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 8\text{ mS}\left(1 - \frac{(-2.86\text{ V})}{(-4\text{ V})}\right) = \mathbf{2.28\ mS}$$

b. $$r_d = \frac{1}{g_{os}} = \frac{1}{25\ \mu\text{S}} = \mathbf{40\ k\Omega}$$

c. $Z_i = R_G = \mathbf{1\ M\Omega}$

d. With r_d,

$$Z_o = r_d \| R_S \| 1/g_m = 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 1/2.28\text{ mS}$$
$$= 40\text{ k}\Omega \| 2.2\text{ k}\Omega \| 438.6\ \Omega$$
$$= \mathbf{362.52\ \Omega}$$

which shows that Z_o is often relatively small and determined primarily by $1/g_m$.
Without r_d,

$$Z_o = R_S \| 1/g_m = 2.2\text{ k}\Omega \| 438.6\ \Omega = \mathbf{365.69\ \Omega}$$

which shows that r_d typically has little effect on Z_o.

e. With r_d,

$$A_v = \frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)} = \frac{(2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}{1 + (2.28\text{ mS})(40\text{ k}\Omega \| 2.2\text{ k}\Omega)}$$
$$= \frac{(2.28\text{ mS})(2.09\text{ k}\Omega)}{1 + (2.28\text{ mS})(2.09\text{ k}\Omega)} = \frac{4.77}{1 + 4.77} = \mathbf{0.83}$$

which is less than 1, as predicted above.

Without r_d,

$$A_v = \frac{g_m R_S}{1 + g_m R_S} = \frac{(2.28\ \text{mS})(2.2\ \text{k}\Omega)}{1 + (2.28\ \text{mS})(2.2\ \text{k}\Omega)}$$
$$= \frac{5.02}{1 + 5.02} = \mathbf{0.83}$$

which shows that r_d usually has little effect on the gain of the configuration.

8.8 DEPLETION-TYPE MOSFETs

The fact that Shockley's equation is also applicable to depletion-type MOSFETs (D-MOSFETs) results in the same equation for g_m. In fact, the ac equivalent model for D-MOSFETs shown in Fig. 8.33 is exactly the same as that employed for JFETs, as shown in Fig. 8.8.

The only difference offered by D-MOSFETs is that V_{GS_Q} can be positive for n-channel devices and negative for p-channel units. The result is that g_m can be greater than g_{m0}, as demonstrated by the example to follow. The range of r_d is very similar to that encountered for JFETs.

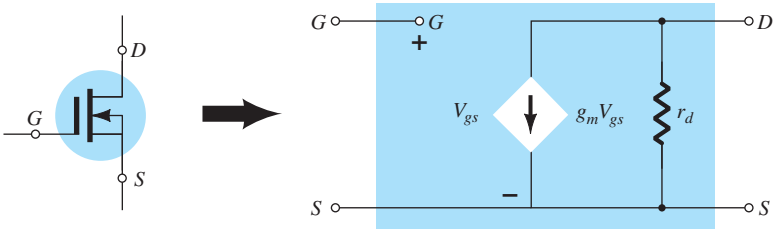


FIG. 8.33
D-MOSFET ac equivalent model.

EXAMPLE 8.11 The network of Fig. 8.34 was analyzed as Example 7.7, resulting in $V_{GS_Q} = 0.35$ V and $I_{D_Q} = 7.6$ mA.

a. Determine g_m and compare to g_{m0}.
b. Find r_d.
c. Sketch the ac equivalent network for Fig. 8.34.
d. Find Z_i.
e. Calculate Z_o.
f. Find A_v.

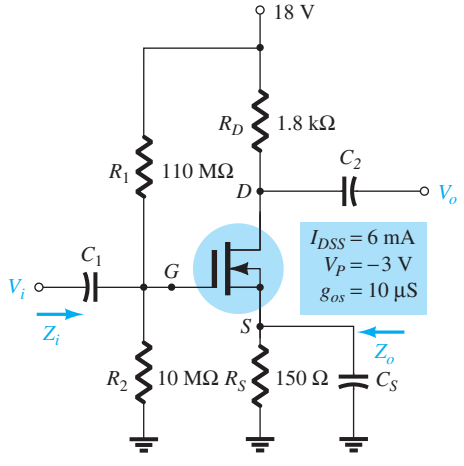


FIG. 8.34
Network for Example 8.11.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(6\text{ mA})}{3\text{ V}} = 4\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 4\text{ mS}\left(1 - \frac{(+0.35\text{ V})}{(-3\text{ V})}\right) = 4\text{ mS}(1 + 0.117) = \mathbf{4.47\text{ mS}}$$

b. $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{10\ \mu\text{S}} = \mathbf{100\text{ k}\Omega}$

c. See Fig. 8.35. Note the similarities with the network of Fig. 8.23. Equations (8.28) through (8.32) are therefore applicable.

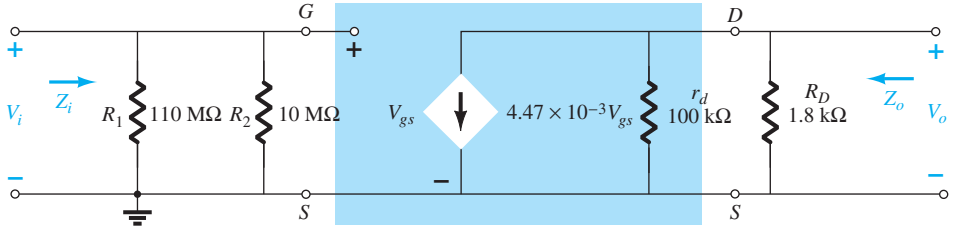


FIG. 8.35
AC equivalent circuit for Fig. 8.34.

d. Eq. (8.28): $Z_i = R_1 \| R_2 = 10\text{ M}\Omega \| 110\text{ M}\Omega = \mathbf{9.17\text{ M}\Omega}$

e. Eq. (8.29): $Z_o = r_d \| R_D = 100\text{ k}\Omega \| 1.8\text{ k}\Omega = \mathbf{1.77\text{ k}\Omega} \cong R_D = \mathbf{1.8\text{ k}\Omega}$

f. $r_d \geq 10R_D \rightarrow 100\text{ k}\Omega \geq 18\text{ k}\Omega$

Eq. (8.32): $A_v = -g_m R_D = -(4.47\text{ mS})(1.8\text{ k}\Omega) = \mathbf{8.05}$

8.9 ENHANCEMENT-TYPE MOSFETs

The enhancement-type MOSFET (E-MOSFET) can be either an *n*-channel (*n*MOS) or *p*-channel (*p*MOS) device, as shown in Fig. 8.36. The ac small-signal equivalent circuit of either device is shown in Fig. 8.36, revealing an open-circuit between gate and drain–source channel and a current source from drain to source having a magnitude dependent on the gate-to-source voltage. There is an output impedance from drain to source r_d, which is usually provided on specification sheets as a conductance g_{os} or admittance y_{os}. The device transconductance g_m is provided on specification sheets as the forward transfer admittance y_{fs}.

In our analysis of JFETs, an equation for g_m was derived from Shockley's equation. For E-MOSFETs, the relationship between output current and controlling voltage is defined by

$$I_D = k(V_{GS} - V_{GS(\text{Th})})^2$$

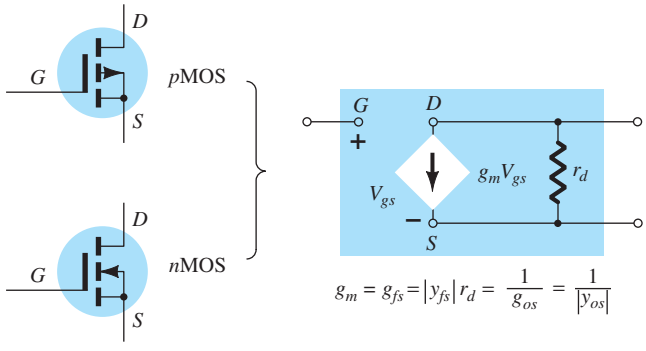


FIG. 8.36
Enhancement MOSFET ac small-signal model.

Since g_m is still defined by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

we can take the derivative of the transfer equation to determine g_m as an operating point. That is,

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\text{Th})})^2 = k\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})})^2$$

$$= 2k(V_{GS} - V_{GS(\text{Th})})\frac{d}{dV_{GS}}(V_{GS} - V_{GS(\text{Th})}) = 2k(V_{GS} - V_{GS(\text{Th})})(1 - 0)$$

and

$$\boxed{g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})})} \tag{8.45}$$

Recall that the constant k can be determined from a given typical operating point on a specification sheet. In every other respect, the ac analysis is the same as that employed for JFETs or D-MOSFETs. Be aware, however, that the characteristics of an E-MOSFET are such that the biasing arrangements are somewhat limited.

8.10 E-MOSFET DRAIN-FEEDBACK CONFIGURATION

The E-MOSFET drain-feedback configuration appears in Fig. 8.37. Recall from dc calculations that R_G could be replaced by a short-circuit equivalent since $I_G = 0$ A and therefore $V_{R_G} = 0$ V. However, for ac situations it provides an important high impedance between V_o and V_i. Otherwise, the input and output terminals would be connected directly and $V_o = V_i$.

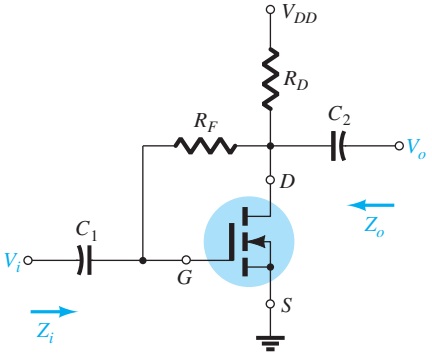


FIG. 8.37
E-MOSFET drain-feedback configuration.

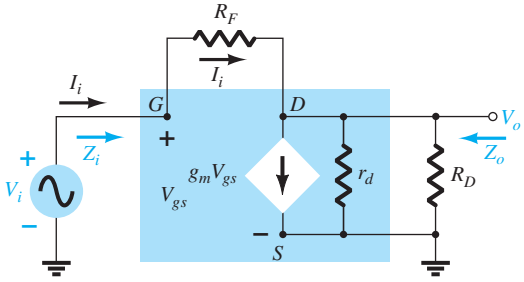


FIG. 8.38
AC equivalent of the network of Fig. 8.37.

Substituting the ac equivalent model for the device results in the network of Fig. 8.38. Note that R_F is not within the shaded area defining the equivalent model of the device, but does provide a direct connection between input and output circuits.

Z_i Applying Kirchhoff's current law to the output circuit (at node D in Fig. 8.38) results in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

and

$$V_{gs} = V_i$$

so that

$$I_i = g_m V_i + \frac{V_o}{r_d \| R_D}$$

or

$$I_i - g_m V_i = \frac{V_o}{r_d \| R_D}$$

Therefore,

$$V_o = (r_d \| R_D)(I_i - g_m V_i)$$

with

$$I_i = \frac{V_i - V_o}{R_F} = \frac{V_i - (r_d \| R_D)(I_i - g_m V_i)}{R_F}$$

and $$I_i R_F = V_i - (r_d \| R_D) I_i + (r_d \| R_D) g_m V_i$$

so that $$V_i[1 + g_m(r_d \| R_D)] = I_i[R_F + r_d \| R_D]$$

and finally,
$$\boxed{Z_i = \frac{V_i}{I_i} = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}} \tag{8.46}$$

Typically, $R_F \gg r_d \| R_D$, so that

$$Z_i \cong \frac{R_F}{1 + g_m(r_d \| R_D)}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_i \cong \frac{R_F}{1 + g_m R_D}} \quad {}_{R_F \gg r_d \| R_D,\ r_d \geq 10R_D} \tag{8.47}$$

Z_o Substituting $V_i = 0$ V results in $V_{gs} = 0$ V and $g_m V_{gs} = 0$, with a short-circuit path from gate to ground as shown in Fig. 8.39. R_F, r_d, and R_D are then in parallel and

$$\boxed{Z_o = R_F \| r_d \| R_D} \tag{8.48}$$

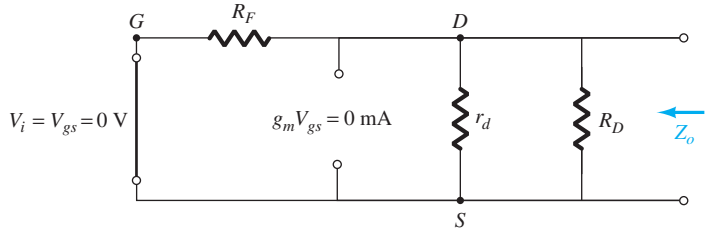


FIG. 8.39
Determining Z_o for the network of Fig. 8.37.

Normally, R_F is so much larger than $r_d \| R_D$ that

$$Z_o \cong r_d \| R_D$$

and with $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D} \quad {}_{R_F \gg r_d \| R_D,\ r_d \geq 10R_D} \tag{8.49}$$

A_v Applying Kirchhoff's current law at node D of Fig. 8.38 results in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

but $$V_{gs} = V_i \quad \text{and} \quad I_i = \frac{V_i - V_o}{R_F}$$

so that $$\frac{V_i - V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \| R_D}$$

and $$\frac{V_i}{R_F} - \frac{V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \| R_D}$$

so that $$V_o\left[\frac{1}{r_d \| R_D} + \frac{1}{R_F}\right] = V_i\left[\frac{1}{R_F} - g_m\right]$$

and $$A_v = \frac{V_o}{V_i} = \frac{\left[\frac{1}{R_F} - g_m\right]}{\left[\frac{1}{r_d \| R_D} + \frac{1}{R_F}\right]}$$

but $$\frac{1}{r_d \| R_D} + \frac{1}{R_F} = \frac{1}{R_F \| r_d \| R_D}$$

and $$g_m \gg \frac{1}{R_F}$$

so that $$\boxed{A_v = -g_m(R_F \| r_d \| R_D)} \quad \textbf{(8.50)}$$

Since R_F is usually $\gg r_d \| R_D$ and if $r_d \geq 10R_D$,

$$\boxed{A_v \cong -g_m R_D}_{R_F \gg r_d \| R_D,\ r_d \geq 10R_D} \quad \textbf{(8.51)}$$

Phase Relationship The negative sign for A_v reveals that V_o and V_i are out of phase by 180°.

EXAMPLE 8.12 The E-MOSFET of Fig. 8.40 was analyzed in Example 7.10, with the result that $k = 0.24 \times 10^{-3}\ \text{A/V}^2$, $V_{GS_Q} = 6.4\ \text{V}$, and $I_{D_Q} = 2.75\ \text{mA}$.

a. Determine g_m.
b. Find r_d.
c. Calculate Z_i with and without r_d. Compare results.
d. Find Z_o with and without r_d. Compare results.
e. Find A_v with and without r_d. Compare results.

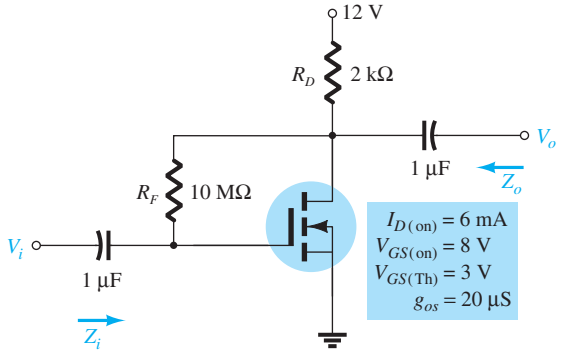


FIG. 8.40
Drain-feedback amplifier from Example 8.11.

Solution:

a. $g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})}) = 2(0.24 \times 10^{-3}\ \text{A/V}^2)(6.4\ \text{V} - 3\ \text{V})$
$= \mathbf{1.63\ mS}$

b. $r_d = \dfrac{1}{g_{os}} = \dfrac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$

c. With r_d,

$$Z_i = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)} = \frac{10\ \text{M}\Omega + 50\ \text{k}\Omega \| 2\ \text{k}\Omega}{1 + (1.63\ \text{mS})(50\ \text{k}\Omega \| 2\ \text{k}\Omega)}$$
$$= \frac{10\ \text{M}\Omega + 1.92\ \text{k}\Omega}{1 + 3.13} = \mathbf{2.42\ M\Omega}$$

Without r_d,

$$Z_i \cong \frac{R_F}{1 + g_m R_D} = \frac{10\ \text{M}\Omega}{1 + (1.63\ \text{mS})(2\ \text{k}\Omega)} = \mathbf{2.53\ M\Omega}$$

which shows that since the condition $r_d \geq 10R_D = 50\ \text{k}\Omega \geq 40\ \text{k}\Omega$ is satisfied, the results for Z_o with or without r_d will be quite close.

d. With r_d,

$$Z_o = R_F \| r_d \| R_D = 10\ \text{M}\Omega \| 50\ \text{k}\Omega \| 2\ \text{k}\Omega = 49.75\ \text{k}\Omega \| 2\ \text{k}\Omega$$
$$= \mathbf{1.92\ k\Omega}$$

Without r_d,

$$Z_o \cong R_D = \mathbf{2\,k\Omega}$$

again providing very close results.

e. With r_d,

$$\begin{aligned} A_v &= -g_m(R_F \| r_d \| R_D) \\ &= -(1.63\text{ mS})(10\text{ M}\Omega \| 50\text{ k}\Omega \| 2\text{ k}\Omega) \\ &= -(1.63\text{ mS})(1.92\text{ k}\Omega) \\ &= \mathbf{-3.21} \end{aligned}$$

Without r_d,

$$\begin{aligned} A_v &= -g_m R_D = -(1.63\text{ mS})(2\text{ k}\Omega) \\ &= \mathbf{-3.26} \end{aligned}$$

which is very close to the above result.

8.11 E-MOSFET VOLTAGE-DIVIDER CONFIGURATION

The last E-MOSFET configuration to be examined in detail is the voltage-divider network of Fig. 8.41. The format is exactly the same as appearing in a number of earlier discussions.

Substituting the ac equivalent network for the E-MOSFET results in the configuration of Fig. 8.42, which is exactly the same as Fig. 8.23. The result is that Eqs. (8.28) through (8.32) are applicable, as listed below for the E-MOSFET.

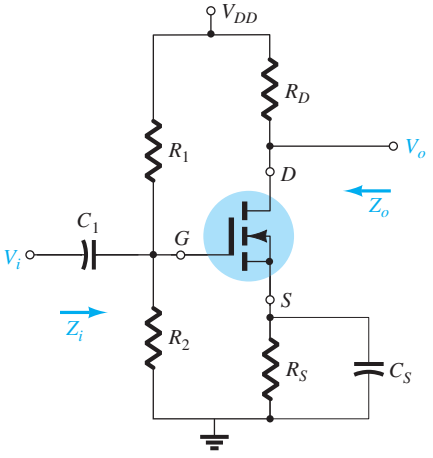


FIG. 8.41
E-MOSFET voltage-divider configuration.

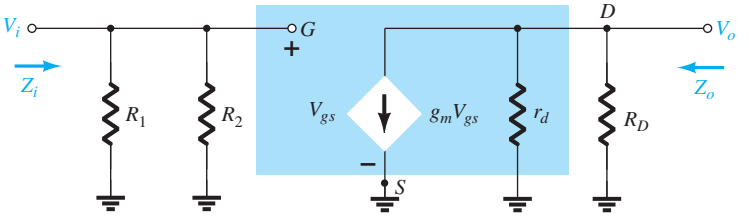


FIG. 8.42
AC equivalent network for the configuration of Fig. 8.41.

Z_i

$$\boxed{Z_i = R_1 \| R_2} \tag{8.52}$$

Z_o

$$\boxed{Z_o = r_d \| R_D} \tag{8.53}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_d}_{r_d \geq 10R_D} \tag{8.54}$$

A_v

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D)} \tag{8.55}$$

and if $r_d \geq 10R_D$,

$$A_v = \frac{V_o}{V_i} \cong -g_m R_D \tag{8.56}$$

8.12 DESIGNING FET AMPLIFIER NETWORKS

Design problems at this stage are limited to obtaining a desired dc bias condition or ac voltage gain. In most cases, the various equations developed are used "in reverse" to define the parameters necessary to obtain the desired gain, input impedance, or output impedance. To avoid unnecessary complexity during the initial stages of the design, the approximate equations are often employed because some variation will occur when calculated resistors are replaced by standard values. Once the initial design is completed, the results can be tested and refinements made using the complete equations.

Throughout the design procedure be aware that although superposition permits a separate analysis and design of the network from a dc and an ac viewpoint, a parameter chosen in the dc environment will often play an important role in the ac response. In particular, recall that the resistance R_G could be replaced by a short-circuit equivalent in the feedback configuration because $I_G \cong 0$ A for dc conditions, but for the ac analysis, it presents an important high-impedance path between V_o and V_i. In addition, recall that g_m is larger for operating points closer to the I_D axis ($V_{GS} = 0$ V), requiring that R_S be relatively small. In the unbypassed R_S network, a small R_S will also contribute to a higher gain, but for the source-follower, the gain is reduced from its maximum value of 1. In total, simply keep in mind that network parameters can affect the dc and ac levels in different ways. Often a balance must be made between a particular operating point and its effect on the ac response.

In most situations, the available dc supply voltage is known, the FET to be employed has been determined, and the capacitors to be employed at the chosen frequency are defined. It is then necessary to determine the resistive elements necessary to establish the desired gain or impedance level. The next three examples determine the required parameters for a specific gain.

EXAMPLE 8.13 Design the fixed-bias network of Fig. 8.43 to have an ac gain of 10. That is, determine the value of R_D.

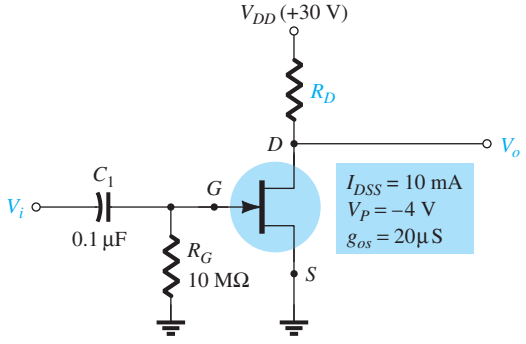


FIG. 8.43
Circuit for desired voltage gain in Example 8.13.

Solution: Since $V_{GS_Q} = 0$ V, the level of g_m is g_{m0}. The gain is therefore determined by

$$A_v = -g_m(R_D \| r_d) = -g_{m0}(R_D \| r_d)$$

with

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{4\text{ V}} = 5\text{ mS}$$

The result is

$$-10 = -5\text{ mS}(R_D \| r_d)$$

and

$$R_D \| r_d = \frac{10}{5\text{ mS}} = 2\text{ k}\Omega$$

From the device specifications,

$$r_d = \frac{1}{g_{os}} = \frac{1}{20 \times 10^{-6}\ \text{S}} = 50\ \text{k}\Omega$$

Substituting, we find

$$R_D \| r_d = R_D \| 50\ \text{k}\Omega = 2\ \text{k}\Omega$$

and

$$\frac{R_D(50\ \text{k}\Omega)}{R_D + 50\ \text{k}\Omega} = 2\ \text{k}\Omega$$

or

$$50R_D = 2(R_D + 50\ \text{k}\Omega) = 2R_D + 100\ \text{k}\Omega$$

with

$$48R_D = 100\ \text{k}\Omega$$

and

$$R_D = \frac{100\ \text{k}\Omega}{48} \cong 2.08\ \text{k}\Omega$$

The closest standard value is **2 kΩ** (Appendix D), which would be employed for this design.

The resulting level of V_{DS_Q} is then determined as follows:

$$V_{DS_Q} = V_{DD} - I_{D_Q}R_D = 30\ \text{V} - (10\ \text{mA})(2\ \text{k}\Omega) = \mathbf{10\ V}$$

The levels of Z_i and Z_o are set by the levels of R_G and R_D, respectively. That is,

$$Z_i = R_G = \mathbf{10\ M\Omega}$$

$$Z_o = R_D \| r_d = 2\ \text{k}\Omega \| 50\ \text{k}\Omega = \mathbf{1.92\ k\Omega} \cong R_D = 2\ \text{k}\Omega$$

EXAMPLE 8.14 Choose the values of R_D and R_S for the network of Fig. 8.44 that will result in a gain of 8 using a relatively high level of g_m for this device defined at $V_{GS_Q} = \frac{1}{4}V_P$.

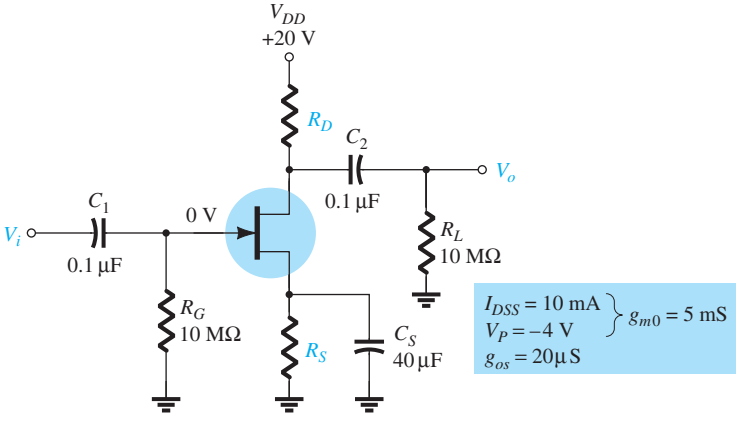


FIG. 8.44
Network for desired voltage gain in Example 8.14.

Solution: The operating point is defined by

$$V_{GS_Q} = \frac{1}{4}V_P = \frac{1}{4}(-4\ \text{V}) = -1\ \text{V}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2 = 10\ \text{mA}\left(1 - \frac{(-1\ \text{V})}{(-4\ \text{V})}\right)^2 = 5.625\ \text{mA}$$

Determining g_m, we obtain

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$

$$= 5\ \text{mS}\left(1 - \frac{(-1\ \text{V})}{(-4\ \text{V})}\right) = 3.75\ \text{mS}$$

The magnitude of the ac voltage gain is determined by

$$|A_v| = g_m(R_D \| r_d)$$

Substituting known values results in

$$8 = (3.75\ \text{mS})(R_D \| r_d)$$

so that

$$R_D \| r_d = \frac{8}{3.75\ \text{mS}} = 2.13\ \text{k}\Omega$$

The level of r_d is defined by

$$r_d = \frac{1}{g_{os}} = \frac{1}{20\ \mu\text{S}} = 50\ \text{k}\Omega$$

and

$$R_D \| 50\ \text{k}\Omega = 2.13\ \text{k}\Omega$$

with the result that

$$R_D = \mathbf{2.2\ k\Omega}$$

which is a standard value.

The level of R_S is determined by the dc operating conditions as follows:

$$V_{GS_Q} = -I_D R_S$$

$$-1\ \text{V} = -(5.625\ \text{mA})R_S$$

and

$$R_S = \frac{1\ \text{V}}{5.625\ \text{mA}} = 177.8\ \Omega$$

The closest standard value is **180 Ω**. In this example, R_S does not appear in the ac design because of the shorting effect of C_S.

In the next example, R_S is unbypassed and the design becomes a bit more complicated.

EXAMPLE 8.15 Determine R_D and R_S for the network of Fig. 8.44 to establish a gain of 8 if the bypass capacitor C_S is removed.

Solution: V_{GS_Q} and I_{D_Q} are still -1 V and 5.625 mA, respectively, and since the equation $V_{GS} = -I_D R_S$ has not changed, R_S continues to equal the standard value of **180 Ω** obtained in Example 8.14.

The gain of an unbypassed self-bias configuration is

$$A_v = -\frac{g_m R_D}{1 + g_m R_S}$$

For the moment it is assumed that $r_d \geq 10(R_D + R_S)$. Using the full equation for A_v at this stage of the design would simply complicate the process unnecessarily.

Substituting (for the specified magnitude of 8 for the gain), we obtain

$$|8| = \left| \frac{-(3.75\ \text{mS})R_D}{1 + (3.75\ \text{mS})(180\ \Omega)} \right| = \frac{(3.75\ \text{mS})R_D}{1 + 0.675}$$

and

$$8(1 + 0.675) = (3.75\ \text{mS})R_D$$

so that

$$R_D = \frac{13.4}{3.75\ \text{mS}} = 3.573\ \text{k}\Omega$$

with the closest standard value at **3.6 kΩ**.

We can now test the condition

$$r_d \geq 10(R_D + R_S)$$

We have

$$50\ \text{k}\Omega \geq 10(3.6\ \text{k}\Omega + 0.18\ \text{k}\Omega) = 10(3.78\ \text{k}\Omega)$$

and

$$50\ \text{k}\Omega \geq 37.8\ \text{k}\Omega$$

which is satisfied—the solution stands!

8.13 SUMMARY TABLE

To provide a quick comparison between configurations and offer a listing that can be helpful for a variety of reasons, Table 8.1 was developed. The exact and approximate equations for each important parameter are provided with a typical range of values for each. Although

TABLE 8.1

Z_i, Z_o, and A_v for various FET configurations

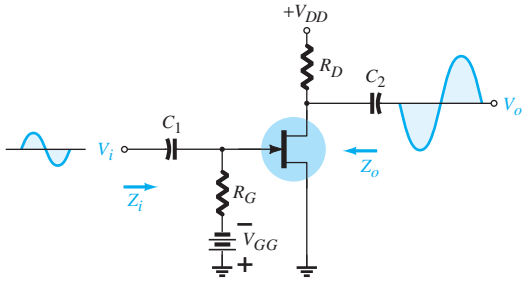
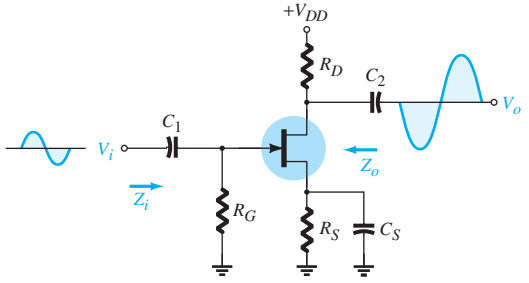
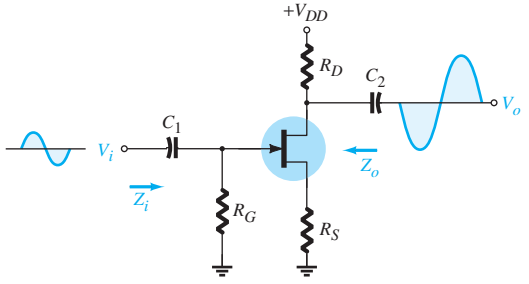
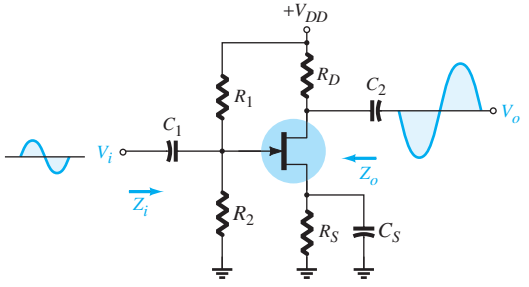
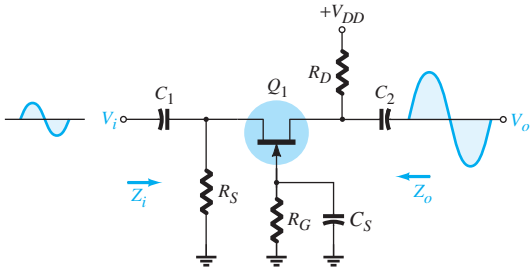
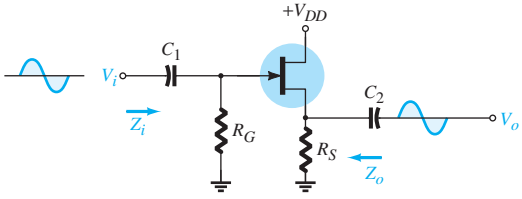
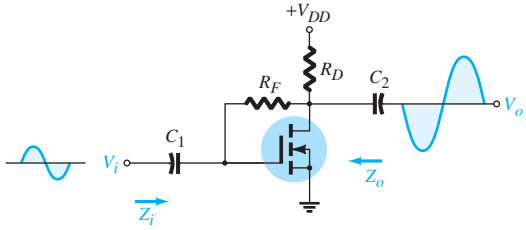
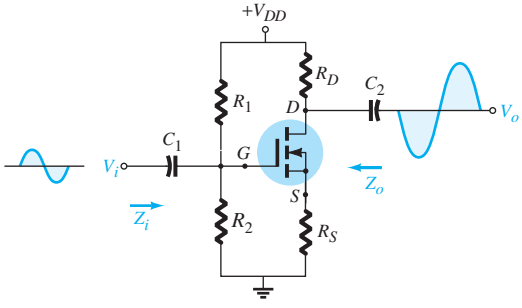
Configuration	Z_i	Z_o	$A_v = \dfrac{V_o}{V_i}$
Fixed-bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$
Self-bias bypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$
Self-bias unbypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	$= \dfrac{\left[1 + g_m R_S + \dfrac{R_S}{r_d}\right] R_D}{\left[1 + g_m R_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]}$ $= R_D$ $r_d \geq 10\,R_D$ or $r_d = \infty\,\Omega$	Low (−2) $= \dfrac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$ $\cong -\dfrac{g_m R_D}{1 + g_m R_S}$ $[r_d \geq 10\,(R_D + R_S)]$
Voltage-divider bias [JFET or D-MOSFET] 	High (10 MΩ) $= R_1 \| R_2$	Medium (2 kΩ) $= R_D \| r_d$ $\cong R_D$ $(r_d \geq 10\,R_D)$	Medium (−10) $= -g_m(r_d \| R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\,R_D)$

TABLE 8.1
(Continued)

Configuration	Z_i	Z_o	$A_v = \dfrac{V_o}{V_i}$
Common-gate [JFET or D-MOSFET] 	Low (1 kΩ) $= R_S \Vert \left[\dfrac{r_d + R_D}{1 + g_m r_d} \right]$ $\cong R_S \Vert \dfrac{1}{g_m}$ $(r_d \geq 10\, R_D)$	Medium (2 kΩ) $= R_D \Vert r_d$ $\cong R_D$ $(R_d \geq 10\, R_D)$	Medium (+10) $= \dfrac{g_m R_D + \dfrac{R_D}{r_d}}{1 + \dfrac{R_D}{r_d}}$ $\cong g_m R_D$ $(r_d \geq 10\, RD)$
Source-follower [JFET or D-MOSFET] 	High (10 MΩ) $= R_G$	Low (100 kΩ) $= r_d \Vert R_S \Vert 1/g_m$ $\cong R_S \Vert 1/g_m$ $(r_d \geq 10\, R_S)$	Low (<1) $= \dfrac{g_m(r_d \Vert R_S)}{1 + g_m(r_d \Vert R_S)}$ $\cong \dfrac{g_m R_S}{1 + g_m R_S}$ $(r_d \geq 10\, R_S)$
Drain-feedback bias E-MOSFET 	Medium (1 MΩ) $= \dfrac{R_F + r_d \Vert R_D}{1 + g_m(r_d \Vert R_D)}$ $\cong \dfrac{R_F}{1 + g_m R_D}$ $(r_d \geq 10\, R_D)$	Medium (2 kΩ) $= R_F \Vert r_d \Vert R_D$ $\cong R_D$ $(R_F, r_d \geq 10 R_D)$	Medium (−10) $= -g_m(R_F \Vert r_d \Vert R_D)$ $\cong -g_m R_D$ $(R_F, r_d \geq 10 R_D)$
Voltage-divider bias E-MOSFET 	Medium (1 MΩ) $= R_1 \Vert R_2$	Medium (2 kΩ) $= R_D \Vert r_d$ $\cong R_D$ $(r_d \geq 10\, R_D)$	Medium (−10) $= -g_m(r_d \Vert R_D)$ $\cong -g_m R_D$ $(r_d \geq 10\, R_D)$

all the possible configurations are not present, the majority of the most frequently encountered are included. In fact, any configuration not listed will probably be some variation of those appearing in the table, so at the very least, the listing will provide some insight as to what expected levels should be and which path will probably generate the desired equations. The format chosen was designed to permit a duplication of the entire table on the front and back of one $8\frac{1}{2}$ by 11 inch page.

8.14 EFFECT OF R_L AND R_{sig}

This section will parallel Sections 5.16 and 5.17 of the BJT small-signal ac analysis chapter dealing with the effect of the source resistance and load resistance on the ac gain of an amplifier. There are again two approaches to the analysis. One can simply substitute the ac model for the FET of interest and perform a detailed analysis similar to the unloaded situation, or apply the two-port equations introduced in Section 5.17.

All of the two-port equations developed for the BJT transistor apply to FET networks also because the quantities of interest are defined at the input and output terminals and not the components of the system.

A few of the most important equations are repeated below to provide an easy reference for the analysis of this chapter and to refresh your memory about the conclusions:

$$A_{v_L} = \frac{R_L}{R_L + R_o} A_{v_{NL}} \tag{8.57}$$

$$A_i = -A_{v_L} \frac{Z_i}{R_L} \tag{8.58}$$

$$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s} \cdot \frac{V_o}{V_i} = \left(\frac{R_i}{R_i + R_{sig}}\right)\left(\frac{R_L}{R_L + R_o}\right) A_{v_{NL}} \tag{8.59}$$

Some of the important conclusions about the gain of BJT transistor configurations are also applicable to FET networks. They include the following facts:

The greatest gain of an amplifier is the no-load gain.

The loaded gain is always less than the no-load gain.

A source impedance will always reduce the overall gain below the no-load or loaded level.

In general, therefore,

$$A_{v_{NL}} > A_{v_L} > A_{v_S} \tag{8.60}$$

Recall from Chapter 5 that some BJT configurations are such that the output impedance is sensitive to the source impedance or the input impedance is sensitive to the applied load. For FET networks, however:

Due to the high impedance between the gate terminal and the channel, one can generally assume that the input impedance is unaffected by the load resistor and the output impedance is unaffected by the source resistance.

One must always be aware, however, that there are special situations where the above may not be totally true. Take, for instance, the feedback configuration that results in a direct connection between input and output networks. Although the feedback resistor is usually many times that of the source resistance, permitting the approximation that the source resistance is essentially 0 Ω, it does present a situation where the source resistance could possibly affect the output resistance or the load resistance could affect the input impedance. In general, however, due to the high isolation provided between the gate and the drain or source terminals, the general equations for the loaded gain are less complex than those encountered for BJT transistors. Recall that the base current provided a direct link between input and output circuits of any BJT transistor configuration.

To demonstrate each approach, let us examine the self-bias configuration of Fig. 8.45 with a bypassed source resistance. Substituting the ac equivalent model for the JFET results in the configuration of Fig. 8.46.

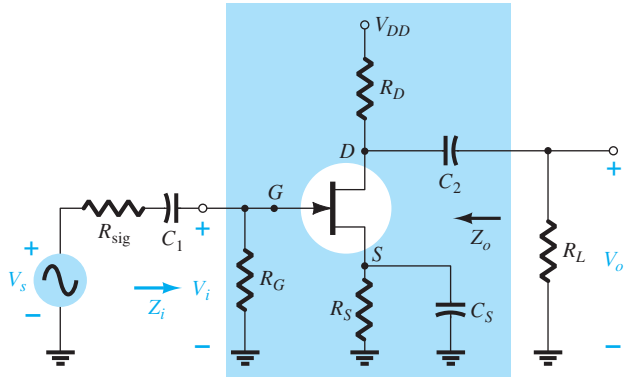


FIG. 8.45
JFET amplifier with R_{sig} and R_L.

Note that the load resistance appears in parallel with the drain resistance and the source resistance R_{sig} appears in series with the gate resistance R. For the overall voltage gain the result is a modified form of Eq. (8.21):

$$A_{v_L} = \frac{V_o}{V_i} = -g_m(r_d \| R_D \| R_L) \tag{8.61}$$

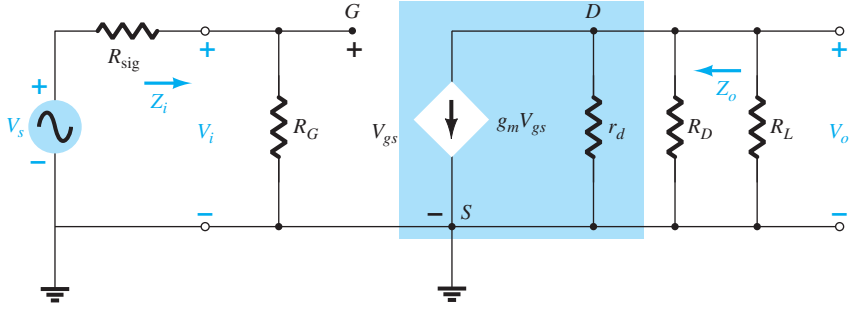


FIG. 8.46
Network of Fig. 8.45 following the substitution of the ac equivalent circuit for the JFET.

The output impedance is the same as obtained for the unloaded situation without a source resistance:

$$Z_o = r_d \| R_D \tag{8.62}$$

The input impedance remains as

$$Z_i = R_G \tag{8.63}$$

For the overall gain A_{v_S},

$$V_i = \frac{R_G V_S}{R_G + R_{sig}}$$

and

$$A_{v_S} = \frac{V_o}{V_s} = \frac{V_i}{V_s}\cdot\frac{V_o}{V_i} = \left[\frac{R_G}{R_G + R_{\text{sig}}}\right][-g_m(r_d \| R_D \| R_L)] \tag{8.64}$$

which for most applications where $R_G \gg R_{\text{sig}}$ and $R_D \| R_L \ll r_d$ results in

$$A_{v_S} \cong -g_m(R_D \| R_L) \tag{8.65}$$

If we now turn to the two-port approach for the same network, the equation for the overall gain becomes

$$A_{v_L} = \frac{R_L}{R_L + R_o}A_{v_{\text{NL}}} = \frac{R_L}{R_L + R_o}[-g_m(r_d \| R_D)]$$

but

$$R_o = R_D \| r_d,$$

so that

$$A_{v_L} = \frac{R_L}{R_L + R_D \| r_d}[-g_m(r_d \| R_D] = -g_m\frac{(r_d \| R_D)(R_L)}{(r_d + R_D) + R_L}$$

and

$$A_{v_L} = -g_m(r_d \| R_D \| R_L)$$

matching the previous result.

The above derivation was included to demonstrate that the same result will be obtained using either approach. If numerical values for R_i, R_o, and $A_{v_{\text{NL}}}$ were available, it would simply be a matter of substituting the values into Eq. (8.57).

Continuing in the same manner for the most common configurations results in the equations of Table 8.2.

8.15 CASCADE CONFIGURATION

The cascade configuration introduced in Chapter 5 for BJTs can also be used with JFETs or MOSFETs, as shown for JFETs in Fig. 8.47. Recall that the output of one stage appears as the input for the following stage. The input impedance for the second stage is the load impedance for the first stage.

The total gain is the product of the gain of each stage including the loading effects of the following stage.

Too often, the no-load gain is employed and the overall gain is an unrealistic result. For each stage the loading effect of the following stage must be included in the gain calculations. Using the results of the previous sections of this chapter results in the following equation for the overall gain of the configuration of Fig. 8.47:

$$A_v = A_{v_1}A_{v_2} = (-g_{m_1}R_{D_1})(-g_{m_2}R_{D_2}) = g_{m_1}g_{m_2}R_{D_1}R_{D_2} \tag{8.66}$$

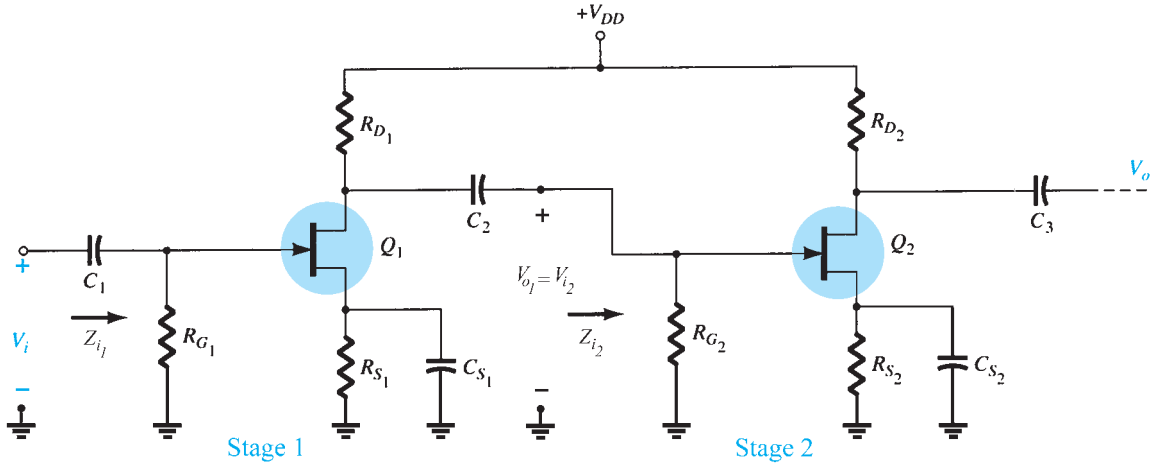
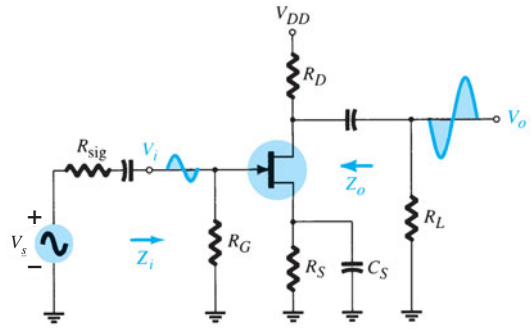
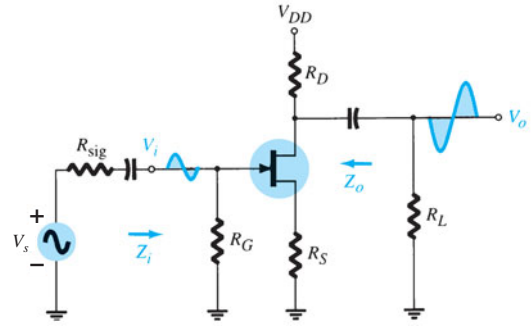
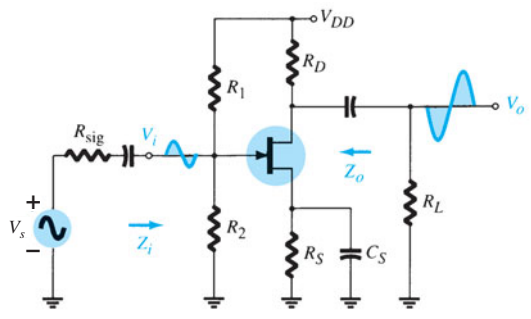
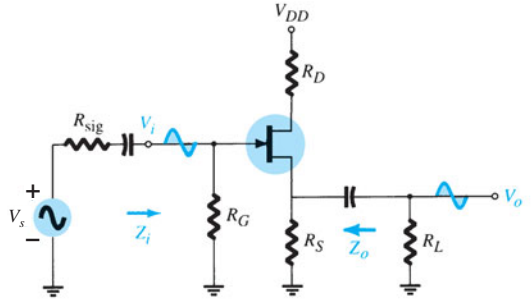
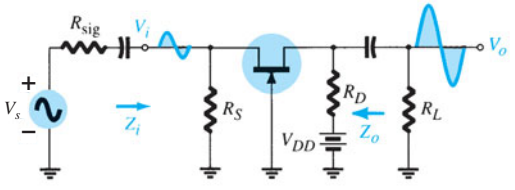


FIG. 8.47
Cascaded FET amplifier.

TABLE 8.2

Configuration	$A_{v_L} = V_o \| V_i$	Z_i	Z_o
	$-g_m(R_D \| R_L)$ Including r_d: $-g_m(R_D \| R_L \| r_d)$	R_G R_G	R_D $R_D \| r_d$
	$\dfrac{-g_m(R_D \| R_L)}{1 + g_m R_S}$ Including r_d: $\dfrac{-g_m(R_D \| R_L)}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$	R_G R_G	$\dfrac{R_D}{1 + g_m R_S}$ $\cong \dfrac{R_D}{1 + g_m R_S}$
	$-g_m(R_D \| R_L)$ Including r_d: $-g_m(R_D \| R_L \| r_d)$	$R_1 \| R_2$ $R_1 \| R_2$	R_D $R_D \| r_d$;
	$\dfrac{g_m(R_S \| R_L)}{1 + g_m(R_S \| R_L)}$ Including r_d: $= \dfrac{g_m r_d (R_S \| R_L)}{r_d + R_D + g_m r_d (R_S \| R_L)}$	R_G R_G	$R_S \| 1/g_m$ $\dfrac{R_S}{1 + \dfrac{g_m r_d R_S}{r_d + R_D}}$
	$g_m(R_D \| R_L)$ Including r_d: $\cong g_m(R_D \| R_L)$	$\dfrac{R_S}{1 + g_m R_S}$ $Z_i = \dfrac{R_S}{1 + \dfrac{g_m r_d R_S}{r_d + R_D \| R_L}}$	R_D $R_D \| r_d$

The input impedance of the cascade amplifier is that of stage 1,

$$\boxed{Z_i = R_{G_1}} \tag{8.67}$$

and the output impedance is that of stage 2,

$$\boxed{Z_o = R_{D_2}} \tag{8.68}$$

The main function of cascading stages is the larger overall gain achieved. Since dc bias and ac calculations for a cascade amplifier follow those derived for the individual stages, an example will demonstrate the various calculations to determine dc bias and ac operation.

EXAMPLE 8.16 Calculate the dc bias, voltage gain, input impedance, output impedance, and resulting output voltage for the cascade amplifier shown in Fig. 8.48.

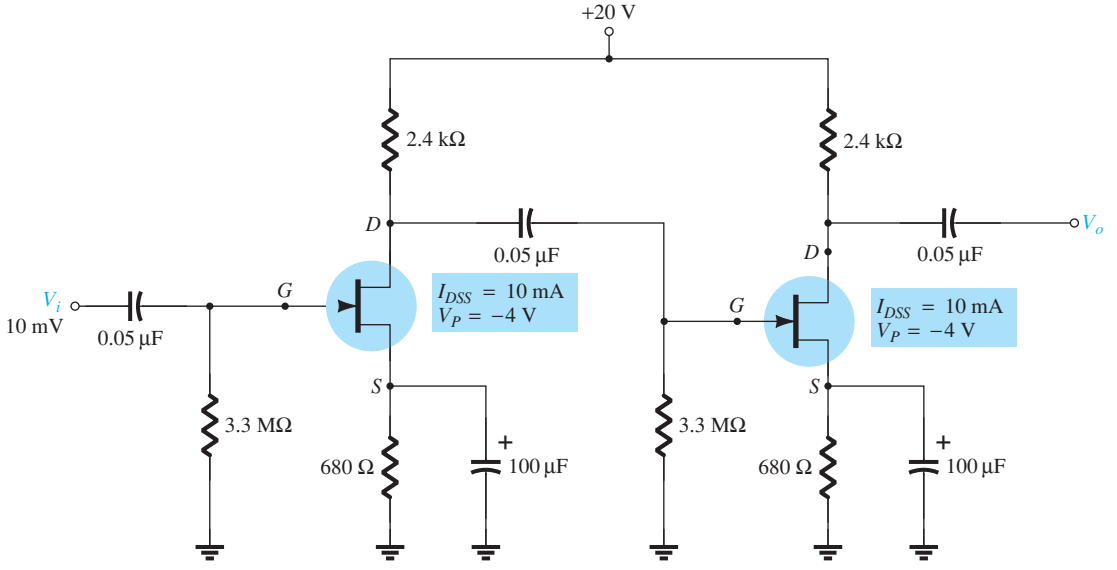


FIG. 8.48
Cascade amplifier circuit for Example 8.16.

Solution: Both amplifier stages have the same dc bias. Using dc bias techniques from Chapter 7 results in

$$V_{GS_Q} = -1.9\text{ V}, \qquad I_{D_Q} = 2.8\text{ mA} \qquad g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{|-4\text{ V}|} = \mathbf{5\text{ mS}}$$

and at the dc bias point,

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = (5\text{ mS})\left(1 - \frac{-1.9\text{ V}}{-4\text{ V}}\right) = \mathbf{2.6\text{ mS}}$$

Since the second stage is unloaded

$$A_{v_2} = -g_m R_D = -(2.6\text{ mS})(2.4\text{ k}\Omega) = \mathbf{-6.24}$$

For the first stage $2.4\text{ k}\Omega \| 3.3\text{ M}\Omega \cong 2.4\text{ k}\Omega$ resulting in the same gain.
The cascade amplifier voltage gain is

$$\text{Eq. (8.66):} \quad A_v = A_{v_1}A_{v_2} = (-6.2)(-6.2) = \mathbf{38.4}$$

Take special note of the fact that the total gain is positive.
The output voltage is then

$$V_o = A_v V_i = (38.4)(10\text{ mV}) = \mathbf{384\text{ mV}}$$

The cascade amplifier input impedance is

$$Z_i = R_G = \mathbf{3.3\ M\Omega}$$

The cascade amplifier output impedance (assuming that $r_d = \infty\Omega$) is

$$Z_o = R_D = \mathbf{2.4\ k\Omega}$$

A combination of FET and BJT stages can also be used to provide high voltage gain and high input impedance, as demonstrated by the next example.

EXAMPLE 8.17 For the cascade amplifier of Fig. 8.49, use the dc bias calculated in Examples 5.15 and 8.16 to calculate input impedance, output impedance, voltage gain, and resulting output voltage.

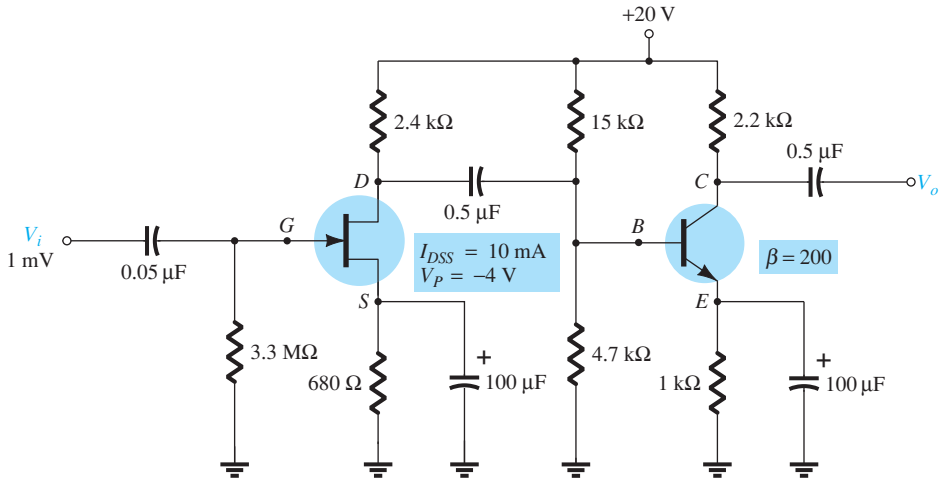


FIG. 8.49
Cascaded JFET-BJT amplifier for Example 8.17.

Solution: Since R_i (stage 2) $= 15\ \text{k}\Omega \| 4.7\ \text{k}\Omega \| 200(6.5\ \Omega) = 953.6\ \Omega$, the gain of stage 1 (when loaded by stage 2) is

$$\begin{aligned} A_{v_1} &= -g_m[R_D \| R_i \text{ (stage 2)}] \\ &= -2.6\ \text{mS}(2.4\ \text{k}\Omega \| 953.6\ \Omega) = -1.77 \end{aligned}$$

From Example 5.18, the voltage gain of stage 2 is $A_{v_2} = -338.46$. The overall voltage gain is then

$$A_v = A_{v_1}A_{v_2} = (-1.77)(-338.46) = \mathbf{599.1}$$

The output voltage is then

$$V_o = A_vV_i = (599.1)(1\ \text{mV}) \approx \mathbf{0.6\ V}$$

The input impedance of the amplifier is that of stage 1,

$$Z_i = \mathbf{3.3\ M\Omega}$$

and the output impedance is that of stage 2,

$$Z_o = R_D = \mathbf{2.2\ k\Omega}$$

8.16 TROUBLESHOOTING

As mentioned before, troubleshooting a circuit is a combination of knowing the theory and having experience using meters and an oscilloscope to check the operation of the circuit. A good troubleshooter has a sense for what to check based on the behavior of the networks. This ability is developed through building, testing, and repairing a wide

variety of configurations. For any small-signal amplifier one might consider the following steps:

1. Look at the circuit board to see if any obvious problems can be seen: an area charred by excess heating of a component; a component that feels or seems too hot to touch; what appears to be a poor solder joint; any connection that appears to have come loose.
2. Use a dc meter: make some measurements as marked in a repair manual containing the circuit schematic diagram and a listing of test dc voltages.
3. Apply a test ac signal: measure the ac voltages starting at the input and work along toward the output.
4. If the problem is identified at a particular stage, the ac signal at various points should be checked using an oscilloscope to see the waveform, its polarity, amplitude, and frequency, as well as any unusual waveform "glitches" that may be present. In particular, observe that the signal is present for the full signal cycle.

Possible Symptoms and Actions

In the absence of an output ac voltage:

1. Check whether the supply voltage is properly connected.
2. Check whether the output voltage at V_D is in the midrange between 0 V and V_{DD}.
3. Check whether there is any input ac signal at the gate terminal.
4. Check the ac voltage at each side of the coupling capacitor terminals.

When building and testing an FET amplifier circuit in the laboratory:

1. Check the color code of resistor values to be sure that they are correct. Even better, measure the resistor values because components used repeatedly may get overheated when used incorrectly, causing the nominal value to change.
2. Check that all dc voltages are present at the component terminals. Be sure that all ground connections are made common.
3. Measure the ac input signal to be sure the expected value is provided to the circuit.

8.17 PRACTICAL APPLICATIONS

Three-Channel Audio Mixer

The basic components of a three-channel JFET audio mixer are shown in Fig. 8.50. The three input signals can come from different sources such as a microphone, a musical instrument, background sound generators, and so on. All signals can be applied to the same gate terminal because the input impedance of the JFET is so high that it can be approximated by

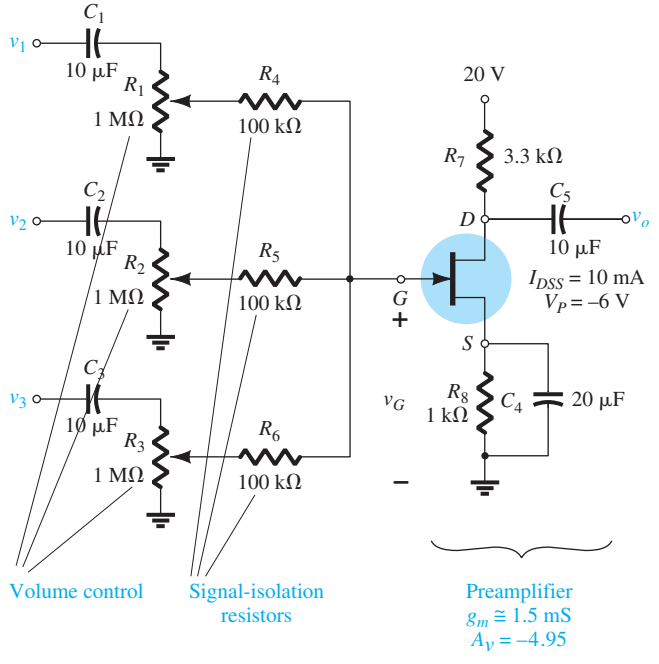


FIG. 8.50
Basic components of a three-channel JFET audio mixer.

an open circuit. **In general, the input impedance is 1000 MΩ (10^9 Ω) or better for JFETs and 100 million MΩ (10^{14} Ω) or better for MOSFETs**. If BJTs were employed instead of JFETs, the lower input impedance would require a transistor amplifier for each channel or at least an emitter-follower as the first stage to provide a higher input impedance.

The 10-μF capacitors are there to prevent any dc biasing levels on the input signal from appearing at the gate of the JFET, and the 1-MΩ potentiometers are the volume controls for each channel. The need for the 100-kΩ resistors for each channel is less obvious. Their purpose is to ensure that one channel does not load down the other channels and severely reduce or distort the signal at the gate. For instance, in Fig. 8.51a, one channel has a high-impedance (10-kΩ) microphone, whereas another channel has a low-impedance (0.5-kΩ) guitar amplifier. Channel 3 is left open, and the 100-kΩ isolation resistors have been removed for the moment. Replacing the capacitors by their short-circuit equivalent for the frequency range of interest and ignoring the effects of the parallel 1-MΩ potentiometers (set at their maximum value) result in the equivalent circuit of Fig. 8.51b at the gate of the JFET amplifier. Using the superposition theorem, we determine the voltage at the gate of the JFET by

$$v_G = \frac{0.5\ \text{k}\Omega(v_{\text{mic}})}{10.5\ \text{k}\Omega} + \frac{10\ \text{k}\Omega(v_{\text{guitar}})}{10.5\ \text{k}\Omega}$$
$$= 0.047v_{\text{mic}} + 0.95v_{\text{guitar}} \cong v_{\text{guitar}}$$

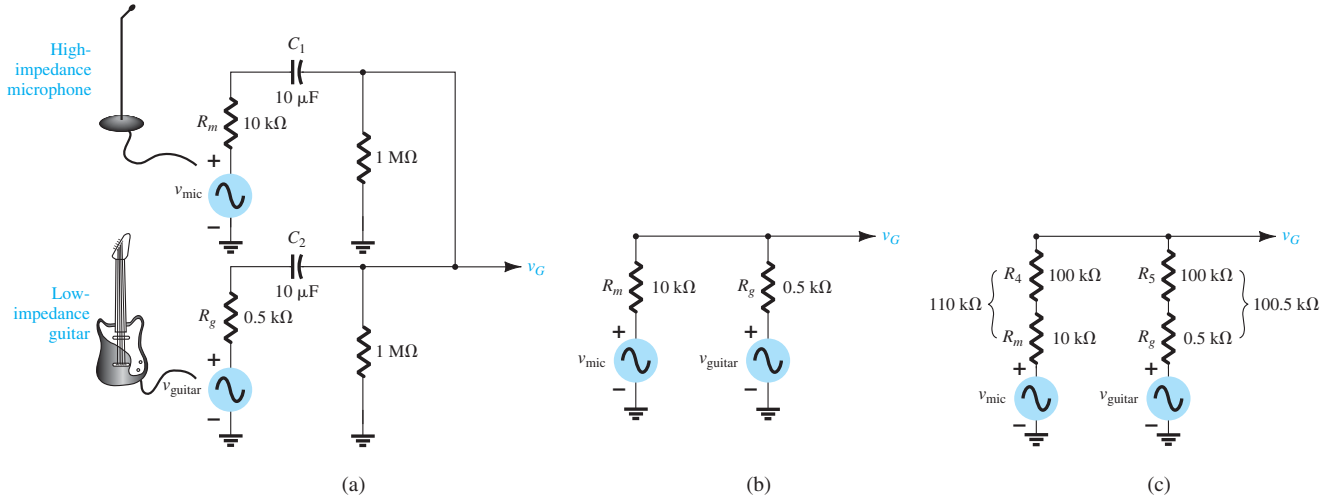


FIG. 8.51

(a) Application of a high- and a low-impedance source to the mixer of Fig. 8.50; (b) reduced equivalent without the 100-kΩ isolation resistors; (c) reduced equivalent with the 100-kΩ resistors.

clearly showing that the guitar has swamped the signal of the microphone. The only response of the amplifier of Fig. 8.51 will be to the guitar. Now, with the 100-kΩ resistors in place, the situation of Fig. 8.51c results. Using the superposition theorem again, we obtain the following equation for the voltage at the gate:

$$v_G = \frac{101\ \text{k}\Omega(v_{\text{mic}})}{211\ \text{k}\Omega} + \frac{110\ \text{k}\Omega(v_{\text{guitar}})}{211\ \text{k}\Omega}$$
$$\cong 0.48v_{\text{mic}} + 0.52v_{\text{guitar}}$$

showing an even balance in the signals at the gate of the JFET. **In general, therefore, the 100-kΩ resistors compensate for any difference in signal impedance to ensure that one does not load down the other and develop a mixed level of signals at the amplifier. Technically, they are often called "signal isolation resistors."**

An interesting consequence of a situation such as described in Fig. 8.51b is depicted in Fig. 8.52, where a guitar of low impedance has a signal level of about 150 mV, whereas the microphone, having a larger internal impedance, has a signal strength of only 50 mV. As pointed out above, the major part of the signal at the "feed" point (v_G) is that of the guitar. The resulting direction of current and power flow is unquestionably from the guitar to the microphone. **Furthermore, since the basic construction of a microphone and a speaker is quite similar, the microphone may be forced to act like a speaker and broadcast the guitar signal**. New acoustic bands often face this problem as they learn the rudiments of

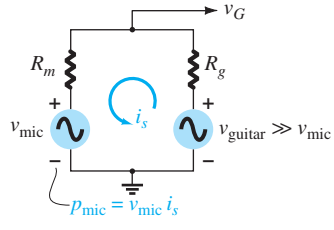


FIG. 8.52

Demonstrating that for parallel signals, the channel with the least internal impedance and most power controls the situation.

good amplifier basics. **In general, for parallel signals, the channel with the least internal impedance controls the situation**.

In Fig. 8.50, the gain of the self-biased JFET is determined by $-g_m R_D$, which for this situation is

$$-g_m R_D = (-1.5\ \text{mS})(3.3\ \text{k}\Omega) = \mathbf{-4.95}$$

For some it may come as quite a surprise that a microphone can actually behave like a speaker. However, the classical example of the use of one voice cone to act as a microphone and a speaker is in the typical intercom system such as appearing in Fig. 8.53a. The 8 Ω, 0.2 W speaker of Fig. 8.53b can be used as a microphone or a speaker, depending on the position of the activation switch. It is important to note, however, as in the microphone–guitar example above, that most speakers are designed to handle reasonable power levels, but most microphones are designed to simply accept the voice-activated input, and they cannot handle the power levels normally associated with speakers. Just compare the size of each in any audio system. In general, a situation such as described above, where the guitar signal is heard over the microphone, will ultimately damage the microphone. For an intercom system the speaker is designed to handle both types of excitation without difficulty.

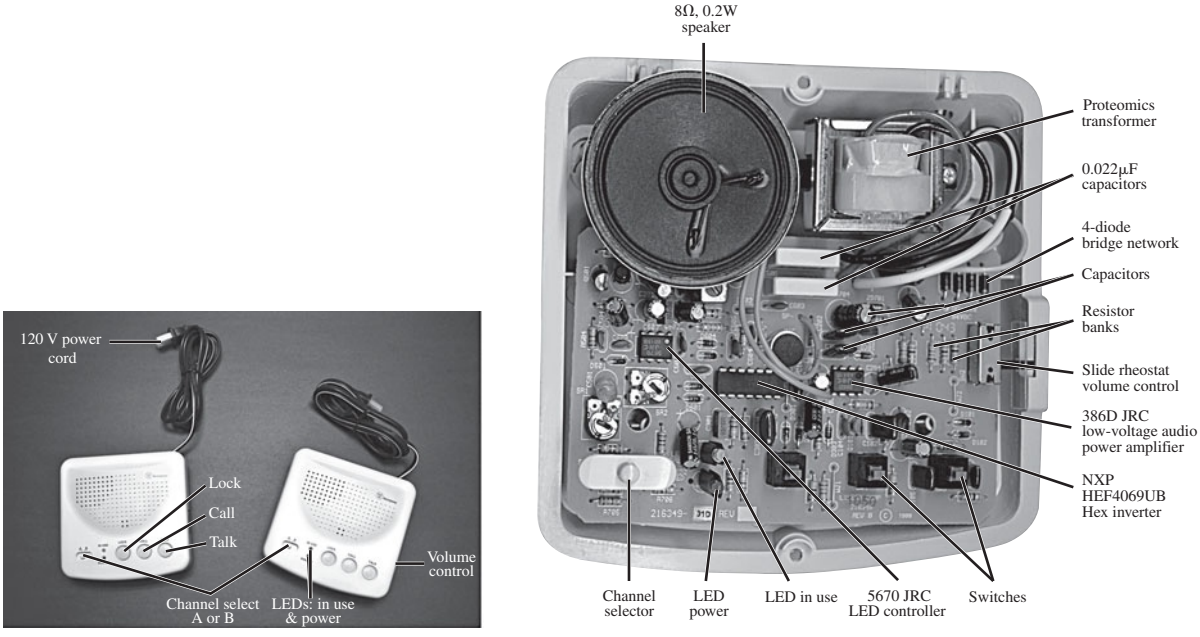


FIG. 8.53

Two-station, two channel intercom: (a) external appearance; (b) internal construction.
(Photos by Dan Trudden/Pearson).

Silent Switching

Any electronic system that incorporates mechanical switching such as shown in Fig. 8.54 is prone to developing noise on the line that will reduce the signal-to-noise ratio. When the switch of Fig. 8.54 is opened and closed, one often gets an annoying "pfft, pfft" sound as part of the output signal. In addition, the longer wires normally associated with

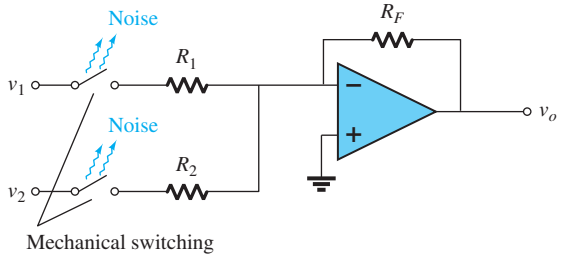
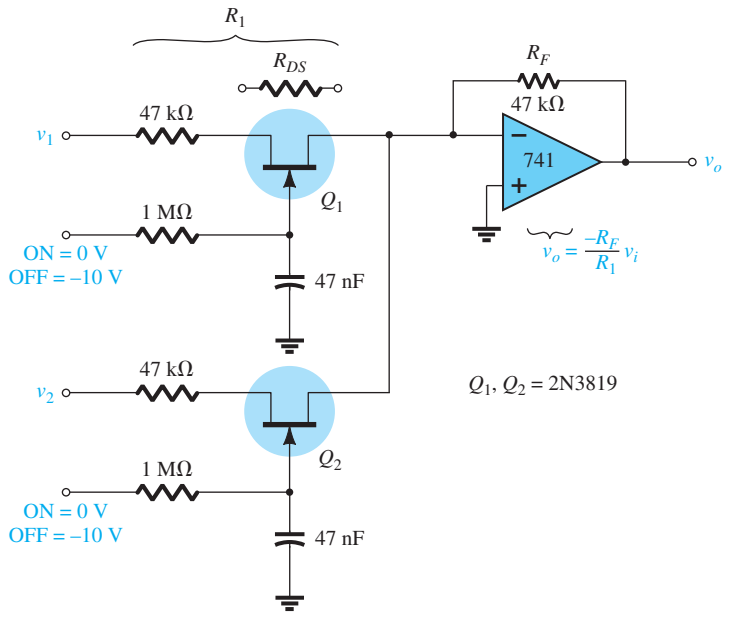


FIG. 8.54

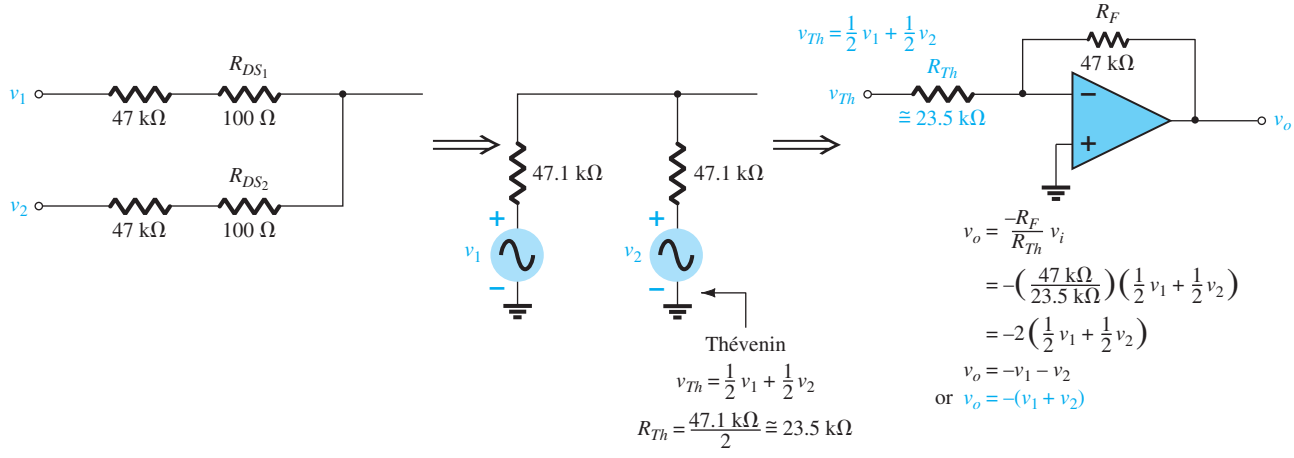
Noise development due to mechanical switching.

mechanical switches will require that the switch be as close to the amplifier as possible to reduce the noise pickup on the line.

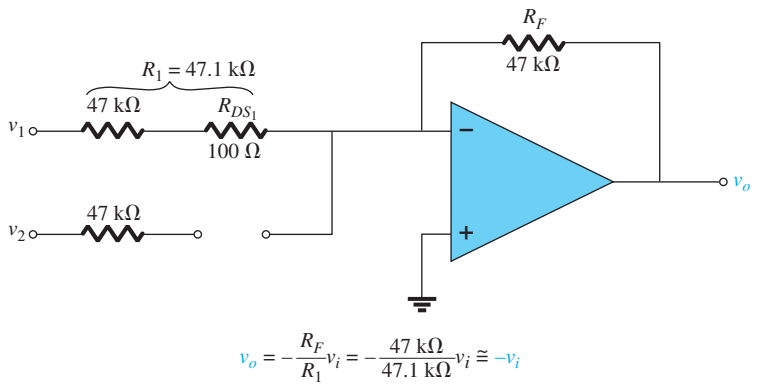
One effective method to essentially eliminate this source of noise is to use electronic switching such as shown in Fig. 8.55a for a two-channel mixing network. Recall from Chapter 7 that the drain to source of a JFET for low values of V_{DS} can be looked on as a



(a)



(b)



(c)

FIG. 8.55

Silent switching audio network: (a) JFET configuration; (b) with both signals present; (c) with one signal on.

resistance whose value is determined by the applied gate-to-source voltage as described in detail in Section 7.13. In addition, recall that the resistance is the least at $V_{GS} = 0$ V and the highest near pinch-off. In Fig. 8.55a, the signals to be mixed are applied to the drain side of each JFET, and the dc control is connected directly to the gate terminal of each JFET. With 0 V at each control terminal, both JFETs are heavily "on," and the resistance from D_1 to S_1 and from D_2 to S_2 is relatively small, say, 100 Ω for this discussion. Although 100 Ω is not the 0 Ω assumed with an ideal switch, it is so small compared to the series 47-kΩ resistor that it can often be ignored. Both switches are therefore in the "on" position, and both input signals can make their way to the input of the inverting amplifier (to be introduced in Chapter 10) as shown in Fig. 8.55b. In particular, note that the chosen resistor values result in an output signal that is simply an inversion of the sum of the two signals. The amplifier stage to follow will then raise the summation to audio levels.

Both electronic switches can be put in the "off" state by applying a voltage that is more negative than the pinch-off level as indicated by the 10 V in Fig. 8.55a. The level of "off" resistance can approach 10,000 MΩ, which certainly can be approximated by an open circuit for most applications. Since both channels are isolated, one can be "on" while the other is "off." The speed of operation of a JFET switch is controlled by the substrate (those due to the device construction) and stray capacitance levels and the low "on" resistance of the JFET. **Maximum speeds for JFETs are about 100 MHz, with 10 MHz being more typical**. However, this speed is critically reduced by the input resistance and capacitance of the design. In Fig. 8.55a, the 1-MΩ resistor and the 47-nF capacitors have a time constant of $\tau = RC = 47 \text{ ms} = 0.047$ s for the dc charging network that is controlling the voltage at the gate. If we assume two time constants to charge to the pinch-off level, the total time is 0.094 s, or a switching speed of $1/0.094 \text{ s} \cong 10.6$ per second. Compared to the typical switching speed of the JFET at 10 million times in 1 s, this number is extremely small. Keep in mind, however, that the application is the important consideration, and for a typical mixer, switching is not going to occur at speeds greater than 10.6 per second unless we have some radical input signals. One might ask why it is necessary to have the *RC* time constant at the gate at all. Why not let the applied dc level at the gate simply control the state of the JFET? In general, the *RC* time constant ensures that the control signal is not a spurious one generated by noise or "ringing" due to the sharply rising and falling applied pulses at the gate. By using a charging network, we ensure that the dc level must be present for a period of time before the pinch-off level is reached. Any spike on the line will not be present long enough to charge the capacitor and switch the state of the JFET.

It is important to realize **that the JFET switch is a bilateral switch**. That is, signals in the "on" state can pass through the drain–source region in either direction. This, of course, is the way ordinary mechanical switches work, which makes it that much easier to replace mechanical switch designs with electronic switches. Remember that the diode is not a bilateral switch because it can conduct current at low voltages in only one direction.

It should be noted that **because the state of the JFETs can be controlled by a dc level, the design of Fig. 8.55a lends itself to remote and computer control** for the same reasons described in Chapter 7 when dc control was discussed.

The data sheet for a low-cost JFET analog switch is provided in Fig. 8.56. Note under the heading Drain Cutoff Current that the pinch-off voltage $V_{GS} = V_P$ is typically about −10 V at a drain-to-source voltage of 12 V. In addition, a current level of 10 nA is used to define the pinch-off level. The level of I_{DSS} is 15 mA, whereas the drain-to-source resistance is quite low at 150 Ω with $V_{GS} = 0$ V. The turn-on time is quite small at 10 ns ($t_d + t_r$), whereas the turn-off time is 25 ns.

Phase-Shift Networks

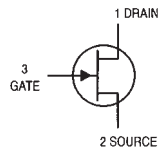
Using the voltage-controlled drain-to-source resistance characteristic of a JFET, we can control the phase angle of a signal using the configurations of Fig. 8.57. The network of Fig. 8.57a is a phase-advance network, which adds an angle to the applied signal, whereas the network of Fig. 8.57b is a phase-retard configuration, which creates a negative phase shift.

JFET Switching

N–Channel — Depletion

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Drain–Gate Voltage	V_{DG}	25	Vdc
Gate–Source Voltage	V_{GS}	25	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Junction Temperature Range	T_J	–65 to +150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C



2 SOURCE

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Gate–Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	25	—	Vdc
Gate Reverse Current (V_{GS} = 15 Vdc, V_{DS} = 0)	I_{GSS}	—	1.0	nAdc
Drain Cutoff Current (V_{DS} = 12 Vdc, V_{GS} = –10 V) (V_{DS} = 12 Vdc, V_{GS} = –10 V, T_A = 100°C)	$I_{D(off)}$	— —	10 2.0	nAdc μAdc
ON CHARACTERISTICS				
Zero–Gate–Voltage Drain Current(1) (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	15	—	mAdc
Gate–Source Forward Voltage ($I_{G(f)}$ = 1.0 mAdc, V_{DS} = 0)	$V_{GS(f)}$	—	1.0	Vdc
Drain–Source On–Voltage (I_D = 7.0 mAdc, V_{GS} = 0)	$V_{DS(on)}$	—	1.5	Vdc
Static Drain–Source On Resistance (I_D = 0.1 mAdc, V_{GS} = 0)	$r_{DS(on)}$	—	150	Ohms

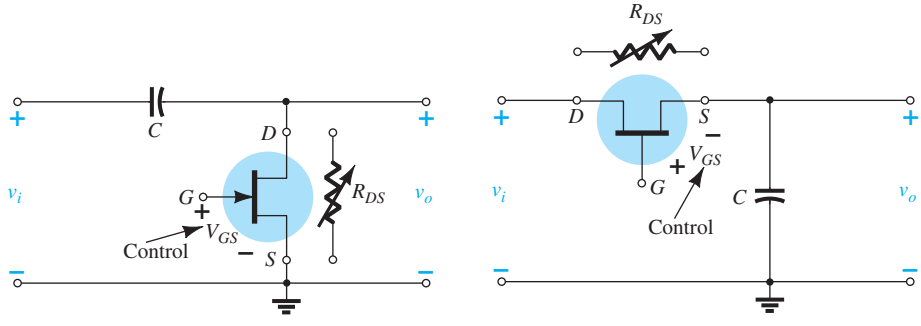
1. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 3.0%.

Characteristic		Symbol	Min	Max	Unit
SMALL–SIGNAL CHARACTERISTICS					
Small–Signal Drain–Source "ON" Resistance (V_{GS} = 0, I_D = 0, f = 1.0 kHz)		$r_{ds(on)}$	—	150	Ohms
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)		C_{iss}	—	5.0	pF
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 10 Vdc, f = 1.0 MHz)		C_{rss}	—	1.2	pF
SWITCHING CHARACTERISTICS					
Turn–On Delay Time	(V_{DD} = 10 Vdc, $I_{D(on)}$ = 7.0 mAdc, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = –10 Vdc)	$t_{d(on)}$	—	5.0	ns
Rise Time		t_r	—	5.0	ns
Turn–Off Delay Time	(V_{DD} = 10 Vdc, $I_{D(on)}$ = 7.0 mAdc, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = –10 Vdc)	$t_{d(off)}$	—	15	ns
Fall Time		t_f	—	10	ns

FIG. 8.56

Specification sheet for a low-cost analog JFET current switch.

(Copyright of Semiconductor Components Industries, LLC. Used by permission.)



(a) (b)

FIG. 8.57

Phase-shift networks: (a) advance; (b) retard.

For example, let us consider the effect of R_{DS} on an input signal having a frequency such as 10 kHz if we apply it to the network of Fig. 8.57a. For discussion, let us assume that the drain-to-source resistance is 2 kΩ due to an applied gate-to-source voltage of −3 V. Drawing the equivalent network results in the general configuration of Fig. 8.58. Solving for the output voltage results in

$$\mathbf{V_o} = \frac{R_{DS}\angle 0^\circ \, V_i\angle 0^\circ}{R_{DS} - jX_C} = \frac{R_{DS}V_i\angle 0^\circ}{\sqrt{R_{DS}^2 + X_C^2}\angle -\tan^{-1}\frac{X_C}{R_{DS}}}$$

$$= \frac{R_{DS}V_i}{\sqrt{R_{DS}^2 + X_C^2}}\angle \tan^{-1}\frac{X_C}{R_{DS}} = \left(\frac{R_{DS}}{\sqrt{R_{DS}^2 + X_C^2}}\right)V_i \angle \tan^{-1}\frac{X_C}{R_{DS}}$$

so that

$$\mathbf{V_o} = k_1 V_i \angle \theta_1$$

where

$$\boxed{k_1 = \frac{R_{DS}}{\sqrt{R_{DS}^2 + X_C^2}} \quad \text{and} \quad \theta_1 = \tan^{-1}\frac{X_C}{R_{DS}}} \tag{8.69}$$

Substituting the numerical values from above results in

$$X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi(10\text{ kHz})(0.01\ \mu\text{F})} = 1.592\text{ k}\Omega$$

and

$$k_1 = \frac{R_{DS}}{\sqrt{R_{DS}^2 + X_C^2}} = \frac{2\text{ k}\Omega}{\sqrt{(2\text{ k}\Omega)^2 + (1.592\text{ k}\Omega)^2}} = 0.782$$

with

$$\theta_1 = \tan^{-1}\frac{X_C}{R_{DS}} = \tan^{-1}\frac{1.592\text{ k}\Omega}{2\text{ k}\Omega} = \tan^{-1} 0.796 = 38.52^\circ$$

so that

$$\mathbf{V_o} = 0.782V_i \angle 38.52^\circ$$

and an output signal that is 78.2% of its applied signal but with a phase shift of 38.52°.

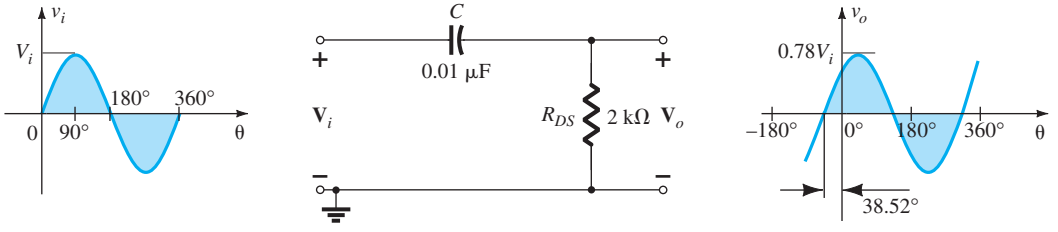


FIG. 8.58
RC phase-advance network.

In general, therefore, the network of Fig. 8.57a can introduce a positive phase shift extending from a few degrees (with X_C relatively small compared to R_{DS}) to almost 90° (with X_C relatively large compared to R_{DS}). Keep in mind, however, that for fixed values of R_{DS}, as the frequency increases, X_C will decrease and the phase shift will approach 0°. For decreasing frequencies and a fixed R_{DS}, the phase shift will approach 90°. It is also important to realize that for a fixed R_{DS}, an increasing level of X_C results in diminishing magnitude for V_o. For such a network, a balance between gain and desired phase shift will have to be made.

For the network of Fig. 8.57b, the resulting equation is

$$\boxed{\mathbf{V_o} = k_2 V_i \angle \theta_2} \tag{8.70}$$

where

$$k_2 = \frac{X_C}{\sqrt{R_{DS}^2 + X_C^2}} \quad \text{and} \quad \theta_2 = -\tan^{-1}\frac{R_{DS}}{X_C}$$

Motion-Detection System

The basic components of a passive infrared (PIR) motion-detection system are shown in Fig. 8.59. The heart of the system is **the pyroelectric detector, which generates a voltage that varies with the amount of incident heat**. It filters out all but the infrared radiation from a particular area and focuses the energy onto a temperature-sensing element. Recall from Chapter 7, Section 7.13, that the infrared band is a nonvisible band just below the visible light spectrum. **Passive detectors do not emit a signal of any kind but simply respond to the energy flow of the environment**.

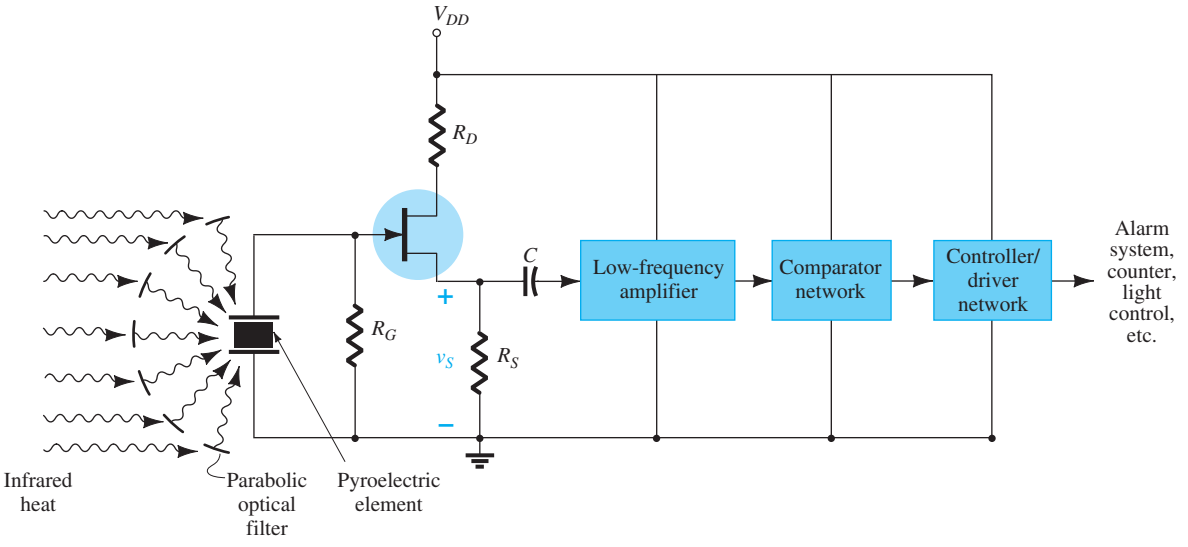
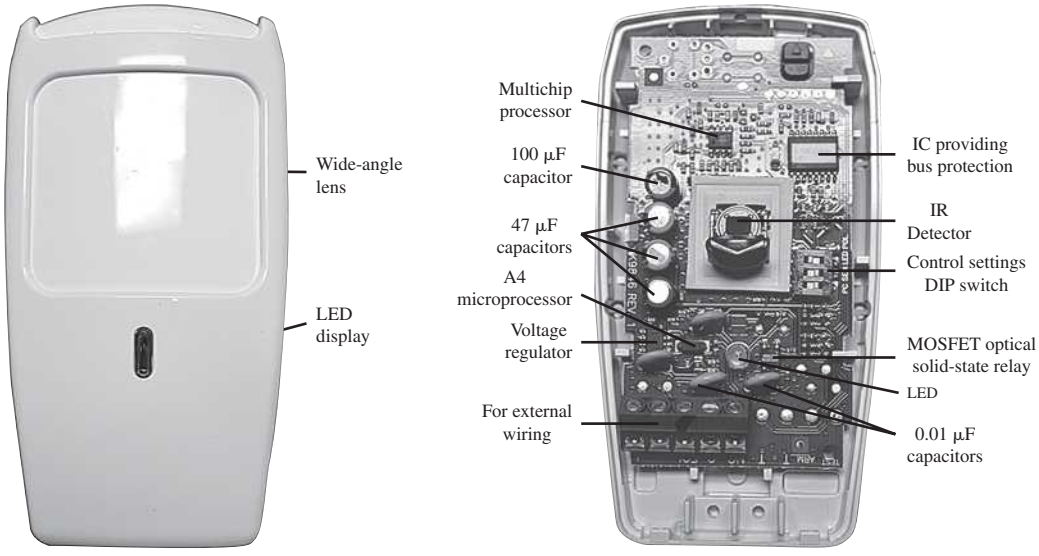


FIG. 8.59
Passive infrared (PIR) motion-detection system.

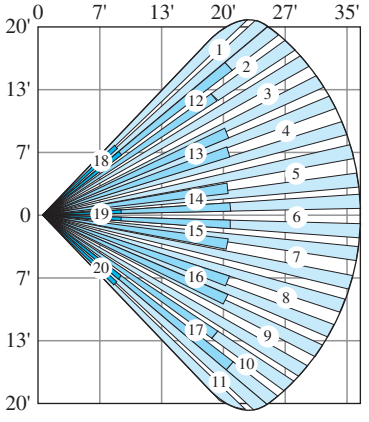
An external and an internal view of a commercially available unit are provided in Fig. 8.60a and b, respectively. Four interchangeable lens are provided for different coverage areas. For our purposes the "pet" option was selected with the coverage indicated in Fig. 8.60c. The unit is mounted at a height of 7′6″ and operates at a dc voltage of 8.5 V to 15.4 V, drawing a current of 17 mA at 12 V dc. The range of coverage is 35′ perpendicular to the sensor and 20′ to each side. In the lowest sensitivity setting the combined weight of the animals cannot exceed 80 lbs.

To focus the incident ambient heat on the pyroelectric detector, the unit of Fig. 8.60 uses a parabolic deflector. As a person walks past a sensor, he or she will cut the various fields appearing in Fig. 8.60c, and the detector will sense the **rapid changes** in heat level. **The result is a changing dc level akin to a low-frequency ac signal of relatively high internal impedance appearing at the gate of the JFET**. One might then ask why turning a heating system on or turning on a lamp doesn't generate an alarm signal since heat will be generated. The answer is that both will generate a voltage at the detector that grows steadily with increasing heat level from the heating system or the burning bulb. Remember that for the lamp, the detector is heat sensitive and not light sensitive. The resulting voltage is not oscillating between levels, but simply climbing in level and will not set off the alarm—a varying ac voltage will not be generated by the pyroelectric detector!

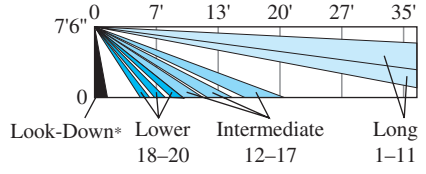
Note in Fig. 8.59 that a JFET source-follower configuration was employed to ensure a very high input impedance to capture most of the pyroelectric signal. It is then passed through a low-frequency amplifier, followed by a peak-detecting network and a comparator to determine whether the alarm should be set off. The dc voltage comparator is a network that "captures" the peak value of the generated ac voltage and compares it to a known dc voltage level. The output processor determines whether the difference between the two levels is sufficient to tell the driver to energize the alarm.



DETECTION PATTERNS
Top View
Wide Angle Pet Immune Lens



Side View
Pet Immune Lens



(c)

FIG. 8.60

Commercially available PIR motion-detection unit: (a) external appearance; (b) internal construction; (c) pet option coverage.
[Photos (a) and (b) by Dan Trudden/Pearson.]

8.18 SUMMARY

Important Conclusions and Concepts

1. **The transconductance parameter** g_m is determined by the **ratio of the change in drain current** associated with a particular **change in gate-to-source voltage** in the region of interest. The **steeper the slope** of the I_D-versus-V_{GS} curve, the **greater** is the level of g_m. In addition, the **closer the point or region of interest to the saturation current** I_{DSS}, the **greater** is the transconductance parameter.
2. On specification sheets, g_m is provided as y_{fs}.
3. When V_{GS} is **one-half the pinch-off value**, g_m is **one-half the maximum value**.
4. When I_D is **one-fourth the saturation level of** I_{DSS}, g_m **is one-half the value at saturation**.
5. The **output impedance** of FETs is **similar in magnitude** to that of **conventional BJTs**.
6. On specification sheets the **output impedance** r_d **is provided as** $1/y_{os}$. The **more horizontal** the characteristic curves on the drain characteristics, the **greater is the output impedance**.

7. The **voltage gain** for the fixed-bias and self-bias JFET configurations (with a bypassed source capacitance) **is the same**.
8. The **ac analysis** of JFETs and depletion-type MOSFETs **is the same**.
9. The **ac equivalent network** for an enhancement-type MOSFET **is the same** as that employed for JFETs and depletion-type MOSFETs. The only difference is the equation for g_m.
10. The **magnitude of the gain** of FET networks is typically **between 2 and 20**. The **self-bias configuration** (without a bypass source capacitance) and the **source-follower** are **low-gain configurations**.
11. There is **no phase shift** between input and output for the **source-follower** and **common-gate configurations**. Most others have a 180° phase shift.
12. The **output impedance** for most FET configurations is **determined primarily by R_D**. For the **source-follower** configuration it is determined by R_S and g_m.
13. The **input impedance** for most FET configurations is **quite high**. However, it is **quite low** for the **common-gate configuration**.
14. When **troubleshooting any electronic or mechanical system**, always check the **most obvious causes first**.

Equations

$$g_m = y_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

$$g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$$

$$r_d = \frac{1}{y_{os}} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}}$$

For JFET and depletion-type MOSFET configurations, see Tables 8.1 and 8.2.

8.19 COMPUTER ANALYSIS

PSpice Windows

JFET Fixed-Bias Configuration The first JFET configuration to be analyzed in the ac domain will be the fixed-bias configuration of Fig. 8.61, using a JFET with $V_P = -4$ V and $I_{DSS} = 10$ mA. The 10-MΩ resistor was added to act as a path to ground for the capacitor but is essentially an open circuit for the ac analysis. The **J2N3819** *n*-channel JFET from the **EVAL** library was used, and the ac voltage is to be determined at four different points for comparison and review.

The constant **Beta** is determined by

$$\text{Beta} = \frac{I_{DSS}}{|V_P|^2} = \frac{10\text{ mA}}{4^2\text{V}^2} = 0.625\text{ mA/V}^2$$

and is inserted in the **Edit Model** dialog box obtained by the sequence **EDIT-PROPERTIES**. **Vto** is also changed to -4 V. The remaining elements of the network are set as described for the transistor in Chapter 5.

An analysis of the network results in the printout of Fig. 8.62. The **CIRCUIT DESCRIPTION** includes all the elements of the network along with their assigned nodes. In particular, note that **Vi** is set at **10 mV** at a frequency of **10 kHz** and a phase angle of **0**

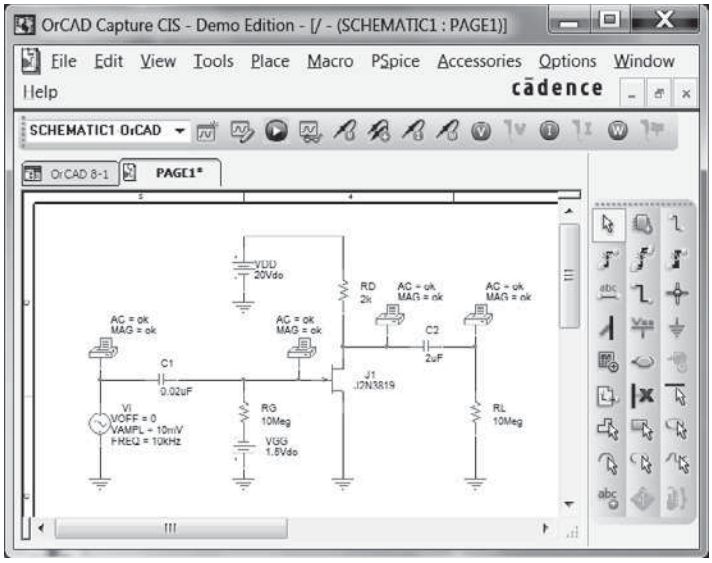


FIG. 8.61

Fixed-bias JFET configuration with an ac source.

```
****          CIRCUIT DESCRIPTION
******************************************************************************************************************
*Analysis directives:
.AC LIN 1 10kHz 10kHz
.OP
.PROBE V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))
.INC "..\SCHEMATIC1.net"
**** INCLUDING SCHEMATIC1.net ****
* source ORCAD 8-1
V_Vi          N00344 0  AC 10mV
+SIN 0 10mV 10kHz 0 0 0
C_C1          N00344 N00351  0.02uF  TC=0,0
C_C2          N00315 N00326  2uF  TC=0,0
R_RG          N00358 N00351  10Meg TC=0,0
R_RD          N00315 N00303  2k TC=0,0
R_RL          0 N00326  10Meg TC=0,0
V_VDD         N00303 0 20Vdc
V_VGG         0 N00358 1.5Vdc
J_J1          N00315 N00351 0 J2N3819
.PRINT        AC
+ VM([N00344])
.PRINT        AC
+ VM([N00351])
.PRINT        AC
+ VM([N00315])
.PRINT        AC
+ VM([N00326])
.END
****          Junction FET MODEL PARAMETERS
******************************************************************************************************************
                    J2N3819
                    NJF
               VTO    -4
              BETA    625.000000E-06
            LAMBDA    2.250000E-03
                IS    33.570000E-15
               ISR    322.400000E-15
             ALPHA    311.700000E-06
                VK    243.6
                RD    1
                RS    1
               CGD    1.600000E-12
               CGS    2.414000E-12
                M     .3622
             VTOTC    -2.500000E-03
           BETATCE    -.5
                KF    9.882000E-18

****          SMALL SIGNAL BIAS SOLUTION          TEMPERATURE  =     27.000 DEG C
******************************************************************************************************************
 NODE       VOLTAGE          NODE       VOLTAGE          NODE       VOLTAGE
(N00303)    20.0000          (N00315)   12.0020          (N00326)   0.0000
(N00344)    0.0000           (N00351)   -1.5000          (N00358)   -1.5000

   VOLTAGE SOURCE CURRENTS
   NAME       CURRENT
   V_Vi      0.000E+00
   V_VDD     -3.999E-03
   V_VGG     -1.366E-12

****          OPERATING POINT INFORMATION         TEMPERATURE  =     27.000 DEG C
******************************************************************************************************************
**** JFETS
NAME                J_J1
MODEL               J2N3819
ID                  4.00E-03
VGS                 -1.50E+00
VDS                 1.20E+01
GM                  3.20E-03
GDS                 8.76E-06
CGS                 1.73E-12
CGD                 6.07E-13

****          AC ANALYSIS                         TEMPERATURE  =     27.000 DEG C
******************************************************************************************************************
  FREQ        VM(N00344)
  1.000E+04   1.000E-02

  FREQ        VM(N00351)
  1.000E+04   9.997E-03

  FREQ        VM(N00315)
  1.000E+04   6.275E-02

  FREQ        VM(N00326)
  1.000E+04   6.275E-02
```

FIG. 8.62

Output file for the network of Fig. 8.61.

degrees. In the following list of **Junction FET MODEL PARAMETERS** note that **VTO** is -4 V and **BETA** is 625E-6 $A/V^2 = 0.625$ mA/V^2, as entered earlier. The **SMALL SIGNAL BIAS SOLUTION** reveals that the voltage at both ends of R_G is -1.5 V, resulting in $V_{GS} = -1.5$ V. The voltage levels of this section can be related to the original network by simply noting the assigned node list in the **CIRCUIT DESCRIPTION**. The voltage from drain to source (ground) is 12 V, leaving a drop of 8 V across R_D. The **AC ANALYSIS** listing reveals that the voltage at the source (N01707) is 10 mV as set, but the voltage at the other end of the capacitor is 3 μV less due to the impedance of the capacitor at 10 kHz—certainly a drop to be ignored. The choice of 0.02 μF for this frequency was obviously a good one. The voltages before and after the capacitor on the output side are exactly the same (to three places), revealing that the larger the capacitor, the closer are the characteristics to those of a short circuit. The output of 6.275E-2 = 62.75 mV reflects a gain of 6.275.

The **OPERATING POINT INFORMATION** reveals that I_D is 4 mA and g_m is 3.2 mS. We calculate the value of g_m from

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS_Q}}{V_P}\right)$$

$$g_m = \frac{2(10\text{ mA})}{4\text{ V}}\left[1 - \frac{(-1.5\text{ V})}{(-4\text{ V})}\right]$$

$$= 3.125\text{ mS}$$

which confirms our analysis.

JFET Voltage-Divider Configuration The next network to be analyzed in the ac domain is the voltage-divider bias configuration of Fig. 8.63. Note that the parameters chosen are different from those employed in earlier examples, with V_i at 24 mV and a frequency of 5 kHz. In addition, the dc levels are displayed, and a plot of the output and input voltages are displayed on the same screen.

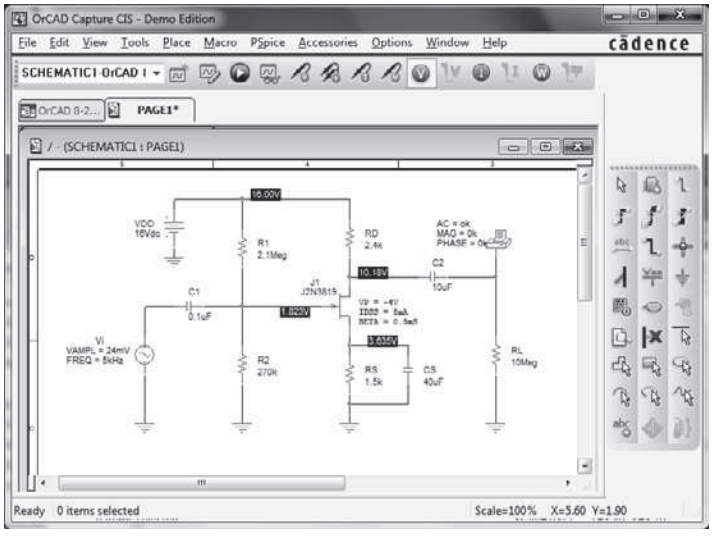


FIG. 8.63
JFET voltage-divider configuration with an ac source.

To run the analysis, select the **New Simulation Profile** key to obtain the **New Simulation** dialog box. After entering **Name** of **OrCAD 8-2**, select **Create**, and the **Simulation Settings** dialog box will appear. Under **Analysis type**, select **AC/Sweep/Noise**, and then under **AC Sweep** choose **Linear**. The **Start Frequency** is **5 kHz**, the **End Frequency** is **5 kHz** and the **Total Points** is **1**. An **OK**, and the simulation can be initiated by selecting the **Run PSpice** key. A schematic will appear, which can be exited to result in the display of Fig. 8.63 with all the voltage levels displayed as controlled by the **V** option. The resulting dc levels reveal that V_{GS} is 1.823 V − 3.635 V = −1.812 V, comparing very well with the −1.8 V calculated in Example 7.4. V_D is 10.18 V, compared to the calculated level of 10.24 V, and V_{DS} is 10.18 V −3.635 V = 6.545 V, compared to 6.64 V.

For the ac solution, we can select **View-Output File** and find under **OPERATING POINT INFORMATION** that g_m is 2.22 mS, comparing very well with the hand-calculated value of 2.2 mS, and under **AC ANALYSIS** that the output ac voltage is 125.8 mV, resulting in a gain of 125.8 mV/24 mV = 5.24. The hand-calculated level is $g_m R_D = (2.2\text{ mS})(2.4\text{ k}\Omega) = 5.28$.

The ac waveform for the output voltage can be obtained by returning to the **Simulation Settings** dialog box and under **Analysis type** choosing **Time Domain (Transient)**. Then, since the period of a 5-kHz signal is 200 μs, select a **Run to** time of 1 ms, so that five cycles of the waveform will appear. Leave the **Start saving data after** option at 0 s, and under **Transient options** enter a **Maximum step size** of 2 μs, so that we have at least 100 plot points for each cycle of the waveform. An **OK**, and the **SCHEMATIC** screen will appear. Select **Trace-Add Trace-V(J1:d)** and the waveform at the bottom of Fig 8.64 appears. If you then choose

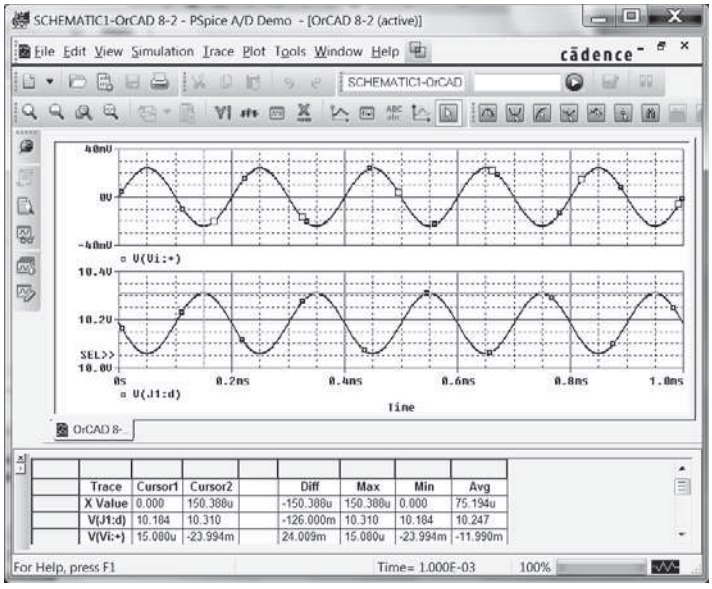


FIG. 8.64

The ac drain and gate voltage for the voltage-divider JFET configuration of Fig. 8.63.

Plot-Add Plot to Window-Trace-Add Trace-V(Vi:+), the waveform of the applied voltage appears at the top of Fig. 8.64. Now shift **SEL >>** to the bottom waveform by simply bringing the cursor down to the left of the other waveform and left clicking the mouse once. Now select **Trace-Cursor-Display**, and a horizontal line will appear at the dc level of the output voltage at 10.184 V (note the level of **V(J1:d)** in the **Probe Cursor** dialog box in the bottom right of the screen). A right click of the mouse, and a second set of intersecting lines will appear. Choose the **Cursor Peak** icon in the toolbar above the display, and the intersection will automatically go to the peak value of the waveform [**(V(Vi:+)** in the dialog box]. Note that **Cursor 2** indicates that the peak value occurs at about 150 μs and the instantaneous peak value is 10.31 V. The **Diff** is simply the difference between **Cursor 1** and **Cursor 2** intersections for time and amplitude.

Cascaded JFET Amplifier The extensive two-stage JFET amplifier of Fig. 8.65 can be created using the same procedures described in the previous examples using PSpice. For both JFETs, **Beta** was set at 0.625 mA/V^2 and **Vto** at -4 V as shown in Fig. 8.66. The applied frequency is 10 kHz to ensure that the capacitors take on a short-circuit approximation. The ac output at the output of each stage is requested.

After simulation, the output file of Fig. 8.67 results, revealing that the gain is 63.23 mV/10 mV = 6.3 after the first stage and 322.6 mV/10 mV = 32.3 after both stages. The gain

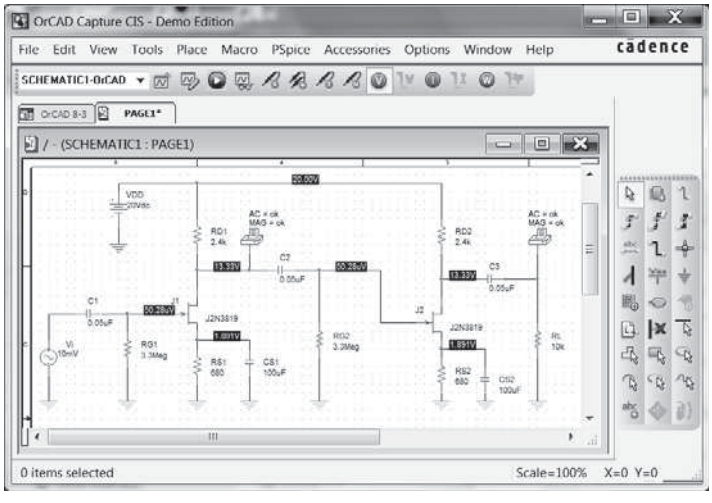


FIG. 8.65

Design Center network for analyzing cascaded JFET amplifiers.

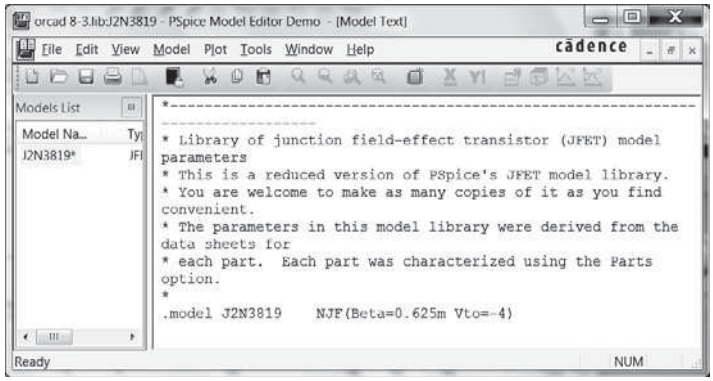


FIG. 8.66

Display of resulting JFET model definition.

```
****          CIRCUIT DESCRIPTION
*******************************************************************************
*Libraries:
* Profile Libraries :
* Local Libraries :
.LIB "../../../orcad 8-3-pspicefiles/orcad 8-3.lib"
* From [PSPICE NETLIST] section of C:\OrCAD\OrCAD_16.3_Demo\tools\PSpice\PSpice.ini file:
.lib "nomd.lib"
*Analysis directives:
.AC LIN 1 10kHz 10kHz
.OP
.PROBE V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))
.INC "..\SCHEMATIC1.net"

**** INCLUDING SCHEMATIC1.net ****
* source ORCAD 8-3
J_J1        N00328 N00336 N00332 J2N3819
J_J2        N00340 N00416 N00344 J2N3819
V_VDD       N00308 0 20Vdc
R_RD1       N00328 N00308  2.4k TC=0,0
R_RS1       0 N00332  680 TC=0,0
R_RG1       0 N00336  3.3Meg TC=0,0
R_RD2       N00340 N00308  2.4k TC=0,0
R_RS2       0 N00344  680 TC=0,0
R_RG2       0 N00416  3.3Meg TC=0,0
R_RL        0 N00361  10k TC=0,0
C_C1        N01393 N00336  0.05uF  TC=0,0
C_C2        N00328 N00416  0.05uF  TC=0,0
C_C3        N00340 N00361  0.05uF  TC=0,0
C_CS1       0 N00332  100uF  TC=0,0
C_CS2       0 N00344  100uF  TC=0,0

.PRINT      AC
+ VM([N00361])

.PRINT      AC
+ VM([N00328])
V_Vi        N01393 0 DC 0Vdc AC 10mV

**** RESUMING "OrCAD 8-3.cir" ****
.END

****          Junction FET MODEL PARAMETERS
*******************************************************************************

               J2N3819
               NJF
      VTO      -4
     BETA   625.000000E-06

****          SMALL SIGNAL BIAS SOLUTION          TEMPERATURE =    27.000  DEG C
*******************************************************************************
NODE       VOLTAGE     NODE       VOLTAGE     NODE       VOLTAGE     NODE       VOLTAGE
(N00308)   20.0000     (N00328)   13.3270     (N00332)   1.8908      N00336)    50.28E-06
(N00340)   13.3270     (N00344)    1.8908     (N00361)   0.0000      (N00416)   50.28E-06
(N01393)    0.0000

VOLTAGE SOURCE CURRENTS
NAME         CURRENT
V_VDD       -5.561E-03
V_Vi         0.000E+00

****          OPERATING POINT INFORMATION         TEMPERATURE =    27.000  DEG C
*******************************************************************************
**** JFETS
NAME         J_J1          J_J2
MODEL        J2N3819       J2N3819
ID           2.78E-03      2.78E-03
VGS         -1.89E+00     -1.89E+00
VDS          1.14E+01      1.14E+01
GM           2.64E-03      2.64E-03
GDS          0.00E+00      0.00E+00
CGS          0.00E+00      0.00E+00
CGD          0.00E+00      0.00E+00
****          AC ANALYSIS                         TEMPERATURE =    27.000  DEG C
*******************************************************************************
FREQ         VM(N00361)
1.000E+04    3.226E-01

****          AC ANALYSIS                         TEMPERATURE =    27.000  DEG C
*******************************************************************************
FREQ         VM(N00328)
1.000E+04    6.323E-02
```

FIG. 8.67

PSpice output for the network of Fig. 8.65.

for the second stage is 322.6 mV/63.23 mV = 5.1. The gains and output voltage are very close to the results obtained in Example 8.1.

In Fig. 8.67 the **V** option is selected to obtain the dc levels of the network. In particular, note how close the gate voltages are to 0 V, ensuring that the gate-to-source bias voltage is essentially the same as that across the source resistor. In fact, due to the isolation offered by the **C2** capacitor, the bias levels of each configuration are exactly the same.

Multisim

The ac gain for the JFET self-bias network of Fig. 8.68 will now be determined using Multisim. The entire procedure for setting up the network and obtaining the desired readings was described for BJT ac networks in Chapter 5. This particular network will appear again

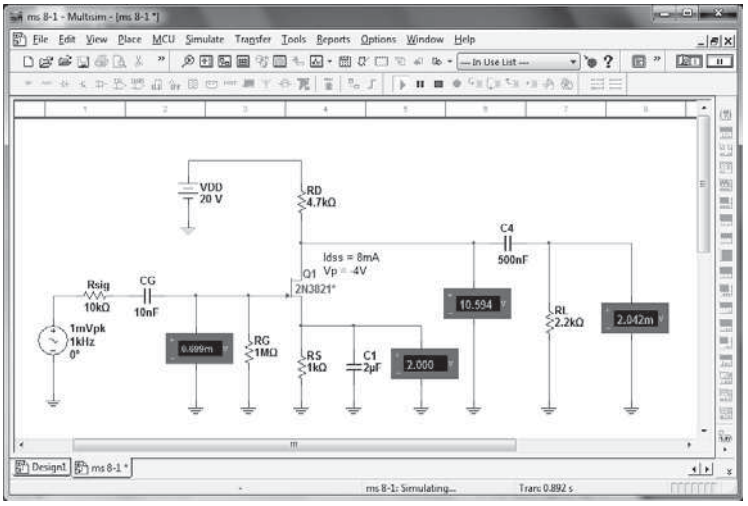


FIG. 8.68
Analysis of a JFET self-bias network using Multisim.

in Chapter 9 as Fig. 9.70 when we turn our attention to the frequency response of a loaded JFET amplifier. A detailed analysis is provided in Chapter 9, including determining the dc levels, the value of g_m, and the loaded gain. The drain current of Example 9.12 is 2 mA, resulting in a drain voltage of 10.6 V and a source voltage of 2 V, which compare very well with the 10.594 V and 2.0 V respectively, of Fig. 8.68. When a load such as R_L is added to the network, it will appear in parallel with R_D of the network, changing the gain equation to $-g_m R_D \| R_L$. For Example 9.12, g_m is 2 mS, resulting in a gain V_o/V_i of $(-2\text{ mS})(2.2\text{ k}\Omega \| 4.7\text{ k}\Omega) = -2.997$. The meters of Fig. 8.68 provide the effective values of the voltages at those points. Since we used a power source, the reading of the meter XMM1 is very close to that of the applied source. The difference is due solely to the ac drop of voltage across $\boldsymbol{R_{sig}}$ and **CG**. The magnitude of the ac gain (V_o/V_i) of the configuration is $2.042\text{ mV}/0.699\text{ mV} = 2.921$, which is very close to the hand-calculated solution.

PROBLEMS

Note: Asterisks indicate more difficult questions.

8.2 FET Small-Signal Model

1. Calculate g_{m0} for a JFET having device parameters $I_{DSS} = 12\text{ mA}$ and $V_P = -4\text{ V}$.
2. Determine the pinch-off voltage of a JFET with $g_{m0} = 10\text{ mS}$ and $I_{DSS} = 12\text{ mA}$.
3. For a JFET having device parameters $g_{m0} = 5\text{ mS}$ and $V_P = -4\text{ V}$, what is the device current at $V_{GS} = 0\text{ V}$?
4. Calculate the value of g_m for a JFET ($I_{DSS} = 12\text{ mA}$, $V_P = -3\text{ V}$) at a bias point of $V_{GS} = -0.5\text{ V}$.
5. For a JFET having $g_m = 6\text{ mS}$ at $V_{GS_Q} = -1\text{ V}$, what is the value of I_{DSS} if $V_P = -2.5\text{ V}$?
6. A JFET ($I_{DSS} = 10\text{ mA}$, $V_P = -5\text{ V}$) is biased at $I_D = I_{DSS}/4$. What is the value of g_m at that bias point?
7. Determine the value of g_m for a JFET ($I_{DSS} = 8\text{ mA}$, $V_P = -5\text{ V}$) when biased at $V_{GS_Q} = V_P/4$.
8. A specification sheet provides the following data (at a listed drain-source current):

   $$g_{fs} = 4.5\text{ mS}, \qquad g_{os} = 25\ \mu\text{S}$$

   At the listed drain–source current, determine:
   a. g_m.
   b. r_d.
9. For a JFET having specified values of $g_{fs} = 4.5\text{ mS}$ and $g_{os} = 25\ \mu\text{S}$, determine the device output impedance Z_o(FET) and device ideal voltage gain A_v(FET).
10. If a JFET having a specified value of $r_d = 100\text{ k}\Omega$ has an ideal voltage gain of A_v(FET) $= -200$, what is the value of g_m?

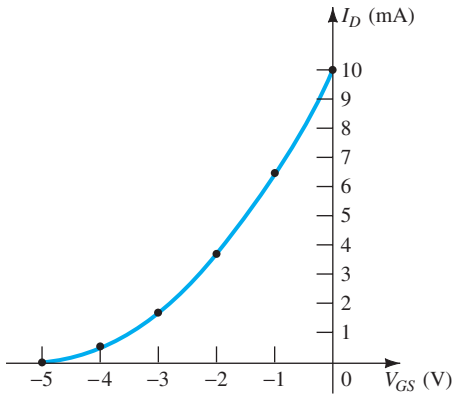


FIG. 8.69
JFET transfer characteristic for Problem 11.

11. Using the transfer characteristic of Fig. 8.69:
- **a.** What is the value of g_{m0}?
- **b.** Determine g_m at $V_{GS} = -0.5$ V graphically.
- **c.** What is the value of g_m at $V_{GS_Q} = -0.5$ V using Eq. (8.6)? Compare with the solution to part (b).
- **d.** Graphically determine g_m at $V_{GS} = -1$ V.
- **e.** What is the value of g_m at $V_{GS_Q} = -1$ V using Eq. (8.6)? Compare with the solution to part (d).

12. Using the drain characteristic of Fig. 8.70:
- **a.** What is the value of r_d for $V_{GS} = 0$ V?
- **b.** What is the value of g_{m0} at $V_{DS} = 10$ V?

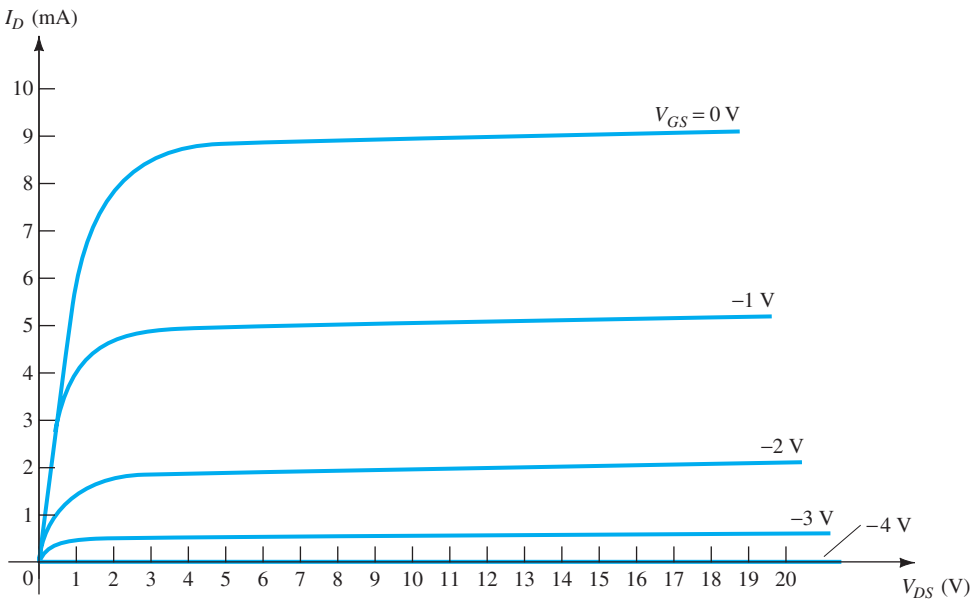


FIG. 8.70
JFET drain characteristic for Problem 12.

13. For a 2N4220 n-channel JFET [g_{fs}(minimum) $= 750\ \mu$S, g_{os}(maximum) $= 10\ \mu$S]:
- **a.** What is the value of g_m?
- **b.** What is the value of r_d?

14.
- **a.** Plot g_m versus V_{GS} for an n-channel JFET with $I_{DSS} = 12$ mA and $V_P = -6$ V.
- **b.** Plot g_m versus I_D for the same n-channel JFET as part (a).

15. Sketch the ac equivalent model for a JFET if $g_{fs} = 5.6$ mS and $g_{os} = 15\ \mu$S.

16. Sketch the ac equivalent model for a JFET if $I_{DSS} = 10$ mA, $V_P = -4$ V, $V_{GS_Q} = -2$ V, and $g_{os} = 25\ \mu$S.

8.3 Fixed-Bias Configuration

17. Determine Z_i, Z_o, and A_v for the network of Fig. 8.71 if $I_{DSS} = 10$ mA, $V_P = -6$ V, and $r_d = 40$ kΩ.

18. **a.** Determine Z_i, Z_o, and A_v for the network of Fig. 8.71 if I_{DSS} and V_P are one-half the values of Problems 17. This is $I_{DSS} = 5$ mA and $V_P = -3$ V.
b. Compare the solutions to that of Problem 17.

19. **a.** Determine Z_i, Z_o, and A_v for the network of Fig. 8.72 if $I_{DSS} = 10$ mA, $V_P = -4$ V, and $r_d = 20$ kΩ.
b. Repeat part (a) with $r_d = 40$ kΩ. What was the impact on the results?

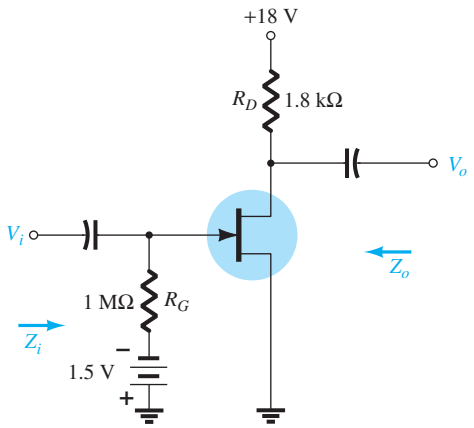


FIG. 8.71
Fixed-bias amplifier for Problems 17 and 18.

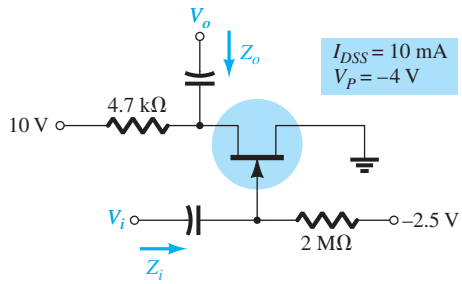


FIG. 8.72
Problem 19.

8.4 Self-Bias Configuration

20. Determine Z_i, Z_o, and A_v for the network of Fig. 8.73 if $g_{fs} = 3000$ μS and $g_{os} = 50$ μs.

21. Determine Z_i, Z_o, and A_v for the network of Fig. 8.73 if the 20-μF capacitor is removed and the parameters of the network are the same as in Problem 20. Compare results with those of Problem 20.

22. Repeat Problem 20 if g_{os} is 10 μS. Compare the results to those of Problem 20.

23. **a.** Find the value of R_S to obtain a voltage gain of 2 for the network of Fig. 8.74 using $r_d = \infty$ Ω.
b. Repeat part (a) with $r_d = 30$ kΩ. What was the impact of the change in r_d on the gain and the analysis?

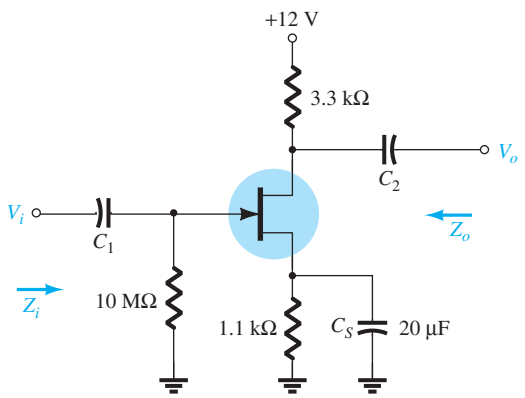


FIG. 8.73
Problems 20, 21, 22, and 59.

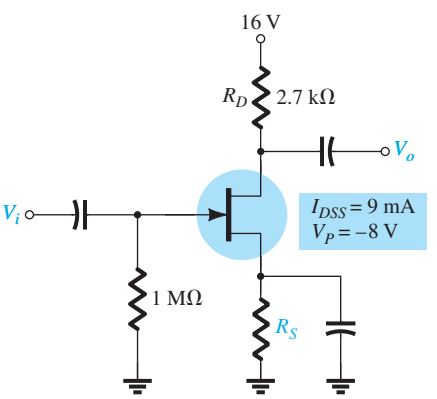


FIG. 8.74
Problem 23.

24. Determine Z_i, Z_o, and A_v for the network of Fig. 8.75 if $I_{DSS} = 6$ mA, $V_P = -6$ V, and $g_{os} = 40$ μS.

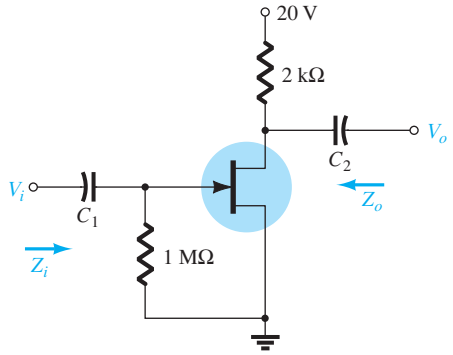


FIG. 8.75
Self-bias configuration for Problems 24 and 60.

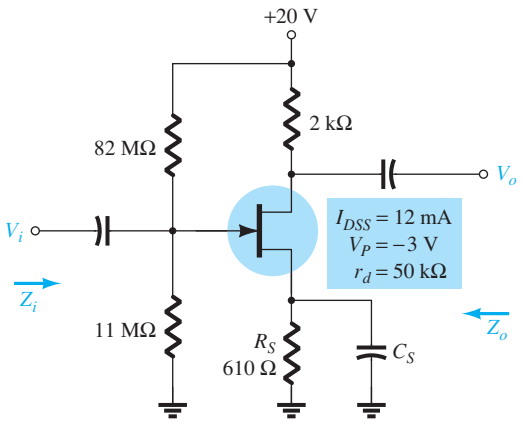


FIG. 8.76
Problems 25 to 28 and 61.

8.5 Voltage-Divider Configuration

25. Determine Z_i, Z_o, and V_o for the network of Fig. 8.76 if $V_i = 20$ mV.

26. Repeat Problem 25 with the capacitor C_S removed and compare results.

27. Repeat Problem 25 if $r_d = 20\ \text{k}\Omega$ and compare results.

28. Repeat Problem 26 if $r_d = 20\ \text{k}\Omega$ and compare results.

8.6 JFET Common-Gate Configuration

29. Determine Z_i, Z_o, and V_o for the network of Fig. 8.77 if $V_i = 4$ mV.

30. Repeat Problem 29 if $r_d = 20\ \text{k}\Omega$ and compare results.

31. Determine Z_i, Z_o, and A_v for the network of Fig. 8.78 if $r_d = 30\ \text{k}\Omega$.

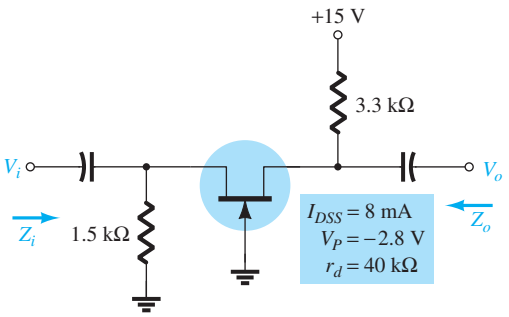


FIG. 8.77
Problems 29, 30, and 62.

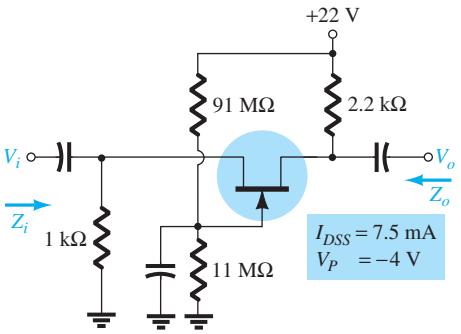


FIG. 8.78
Problem 31.

8.7 JFET Source-Follower Configuration

32. Determine Z_i, Z_o, and A_v for the network of Fig. 8.79.

33. Repeat Problem 32 if $r_d = 20\ \text{k}\Omega$ and compare results.

34. Determine Z_i, Z_o, and A_v for the network of Fig. 8.80.

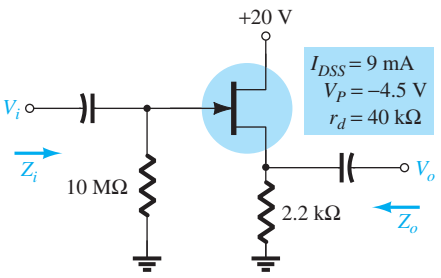


FIG. 8.79
Problems 32 and 33.

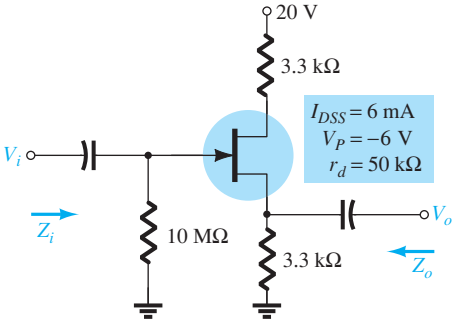


FIG. 8.80
Problem 34.

8.8 Depletion-Type MOSFETs

35. Determine V_o for the network of Fig. 8.81 if $g_{os} = 20\ \mu S$.

36. Determine Z_i, Z_o, and A_v for the network of Fig. 8.82 if $r_d = 60\ k\Omega$.

37. Repeat Problem 36 if $r_d = 25\ k\Omega$ and compare results.

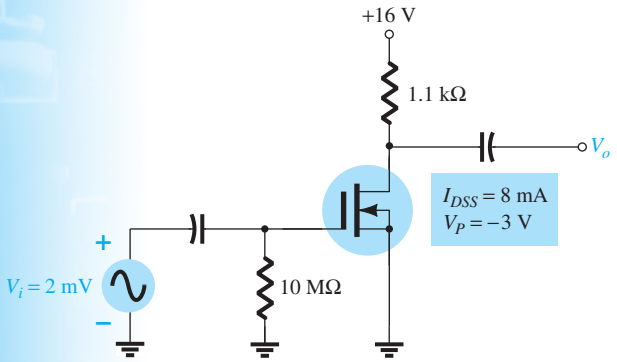


FIG. 8.81
Problem 35.

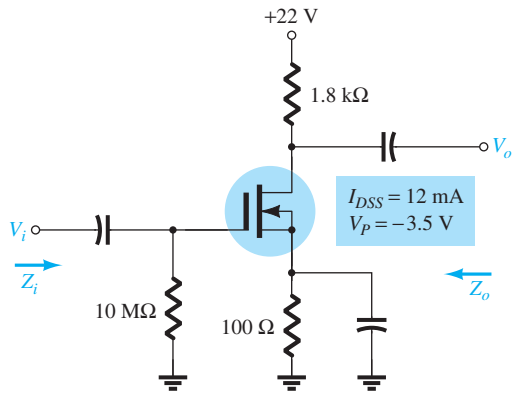


FIG. 8.82
Problems 36, 37, and 63.

38. Determine V_o for the network of Fig. 8.83 if $V_i = 1.8$ mV.

39. Determine Z_i, Z_o, and A_v for the network of Fig. 8.84.

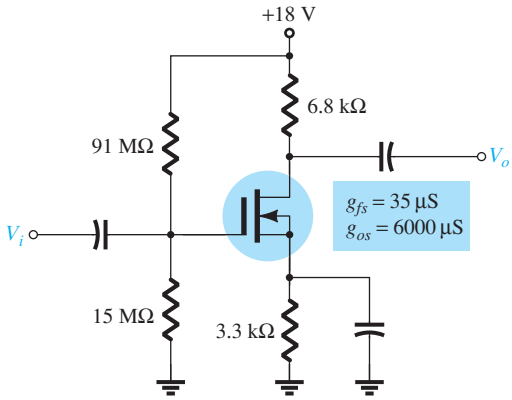


FIG. 8.83
Problem 38.

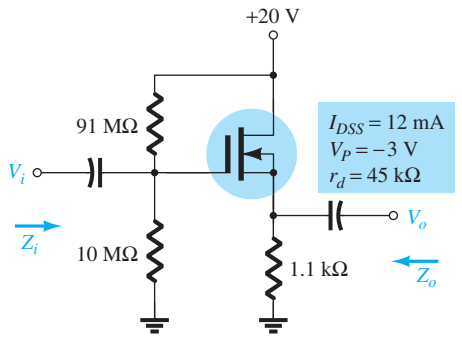


FIG. 8.84
Problem 39.

8.10 E-MOSFET Drain-Feedback Configuration

40. Determine g_m for a MOSFET if $V_{GS(Th)} = 3$ V and it is biased at $V_{GS_Q} = 8$ V. Assume $k = 0.3 \times 10^{-3}$.

41. Determine Z_i, Z_o, and A_v for the amplifier of Fig. 8.85 if $k = 0.3 \times 10^{-3}$.

42. Repeat Problem 41 if k drops to 0.2×10^{-3}. Compare results.

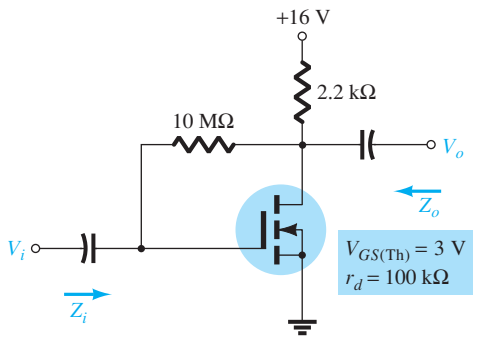


FIG. 8.85
Problems 41, 42, and 64.

43. Determine V_o for the network of Fig. 8.86 if $V_i = 20$ mV.

44. Determine V_o for the network of Fig. 8.86 if $V_i = 4$ mV, $V_{GS(\text{Th})} = 4$ V, and $I_{D(\text{on})} = 4$ mA, with $V_{GS(\text{on})} = 7$ V and $g_{os} = 20\ \mu$S.

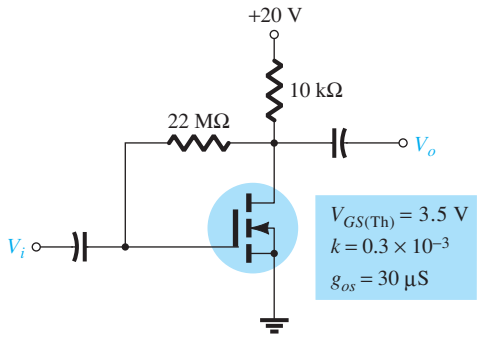


FIG. 8.86
Problems 43 and 44.

8.11 E-MOSFET Voltage-Divider Configuration

45. Determine the output voltage for the network of Fig. 8.87 if $V_i = 0.8$ mV and $r_d = 40$ kΩ.

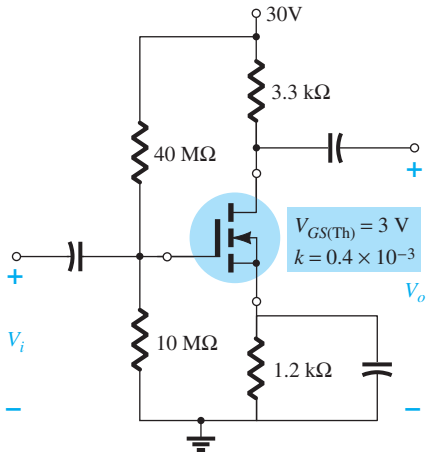


FIG. 8.87
Problem 45.

8.12 Designing FET Amplifier Networks

46. Design the fixed-bias network of Fig. 8.88 to have a gain of 8.

47. Design the self-bias network of Fig. 8.89 to have a gain of 10. The device should be biased at $V_{GS_Q} = \frac{1}{3}V_P$.

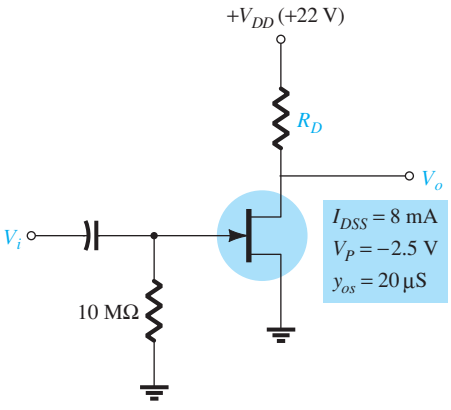


FIG. 8.88
Problem 46.

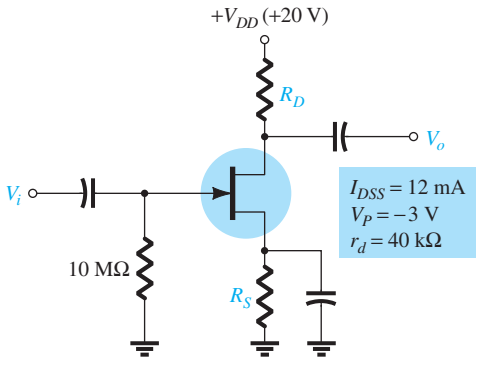


FIG. 8.89
Problem 47.

8.14 Effect of R_L and R_{sig}

48. For the self-bias JFET network of Fig. 8.90:

a. Determine $A_{v_{NL}}$, Z_i, and Z_o.

b. Sketch the two-port model of Fig. 5.75 with the parameters determined in part (a) in place.

c. Determine A_{v_L} and A_{v_s}.

d. Change R_{sig} to 10 kΩ and calculate the new levels of A_{v_L} and A_{v_s}. How is the voltage gain affected by an increase in R_s?

e. For the change of part (d), determine Z_i and Z_o. What was the effect on both impedances?

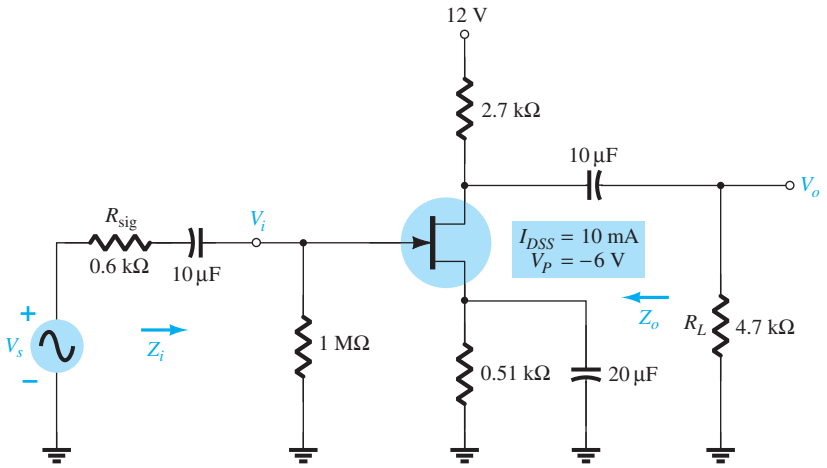


FIG. 8.90
Problem 48.

49. For the source-follower network of Fig. 8.91:

a. Determine $A_{v_{NL}}$, Z_i, and Z_o.

b. Sketch the two-port model of Fig. 5.75 with the parameters determined in part (a) in place.

c. Determine A_{v_L} and A_{v_s}.

d. Change R_L to 4.7 kΩ and calculate A_{v_L} and A_{v_s}. What was the effect of increasing levels of R_L on both voltage gains?

e. Change R_{sig} to 20 kΩ (with R_L at 2.2 kΩ) and calculate A_{v_L} and A_{v_s}. What was the effect of increasing levels of R_{sig} on both voltage gains?

f. Change R_L to 4.7 kΩ and R_{sig} to 20 kΩ and calculate Z_i and Z_o. What was the effect on both impedance parameters?

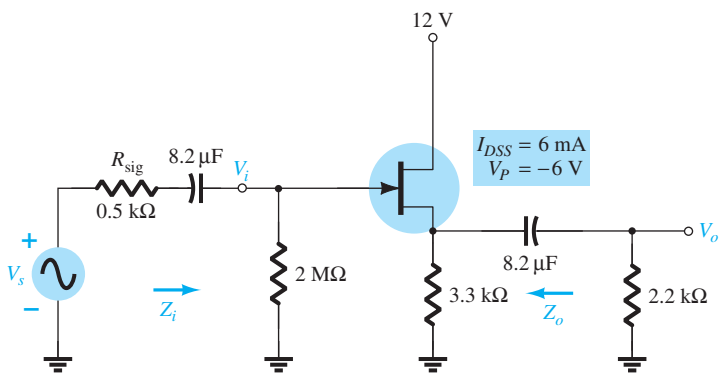


FIG. 8.91
Problem 49.

50. For the common-gate configuration of Fig. 8.92:

a. Determine $A_{v_{NL}}$, Z_i, and Z_o.

b. Sketch the two-port model of Fig. 5.75 with the parameters determined in part (a) in place.

c. Determine A_{v_L} and A_{v_s}.

d. Change R_L to 2.2 kΩ and calculate A_{v_L} and A_{v_s}. What was the effect of changing R_L on the voltage gains?

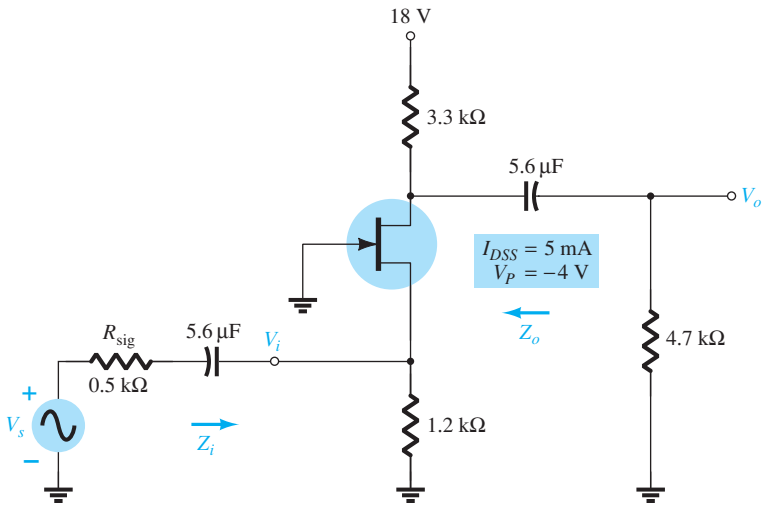


FIG. 8.92
Problem 50.

e. Change R_{sig} to 0.1 kΩ (with R_L at 4.7 kΩ) and calculate A_{v_L} and A_{v_s}. What was the effect of changing R_{sig} on the voltage gains?

f. Change R_L to 2.2 kΩ and R_{sig} to 0.1 kΩ and calculate Z_i and Z_o. What was the effect on both parameters?

g. What general conclusions can you draw from the above calculations?

8.15 Cascade Configuration

51. For the JFET cascade amplifier in Fig. 8.93, calculate the dc bias conditions for the two identical stages, using JFETs with $I_{DSS} = 8$ mA and $V_P = -4.5$ V.

52. For the JFET cascade amplifier of Fig. 8.93, using identical JFETs with $I_{DSS} = 8$ mA and $V_P = -4.5$ V, calculate the voltage gain of each stage, the overall gain of the amplifier, and the output voltage V_o.

53. If both JFETs in the cascade amplifier of Fig. 8.93 are changed to those having specifications $I_{DSS} = 12$ mA and $V_P = -3$ V, calculate the resulting dc bias of each stage.

54. If both JFETs in the cascade amplifier of Fig. 8.93 are changed to those having the specifications $I_{DSS} = 12$ mA, $V_P = -3$ V, and $g_{os} = 25\ \mu$S, calculate the resulting voltage gain for each stage, the overall voltage gain, and the output voltage, V_o.

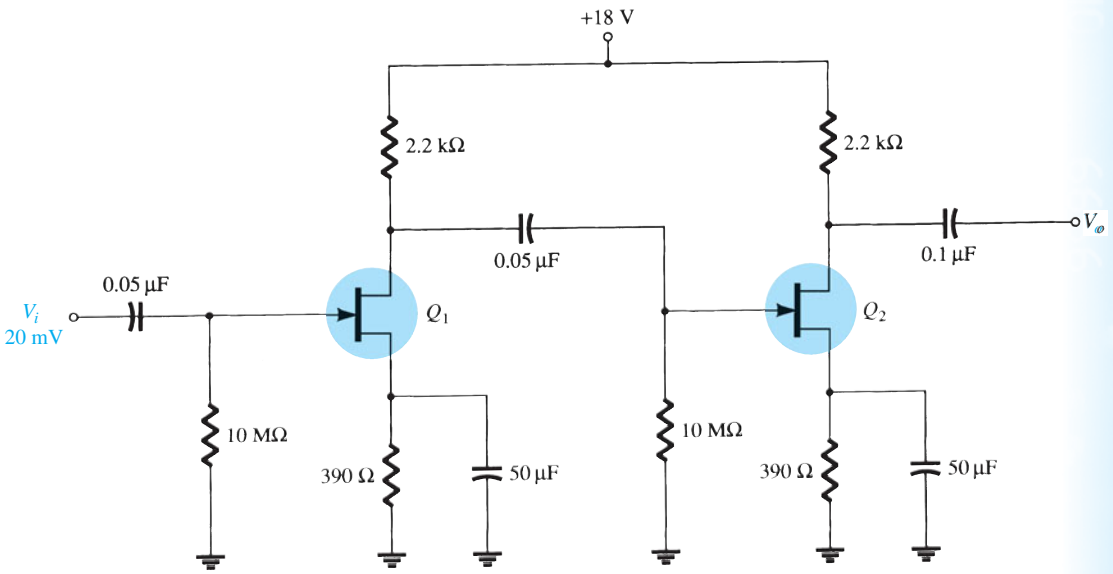


FIG. 8.93
Problems 51 to 55, 65, and 66.

55. For the cascade amplifier of Fig. 8.93, using JFETs with specifications $I_{DSS} = 12$ mA, $V_P = -3$ V, and $g_{os} = 25\ \mu$S, calculate the circuit input impedance (Z_i) and output impedance (Z_o).

56. For the cascade amplifier of Fig. 8.94, calculate the dc bias voltages currents of each stage.

57. For the amplifier circuit of Fig. 8.94, calculate the voltage gain of each stage and the overall amplifier voltage gain.

58. Calculate the input impedance (Z_i) and output impedance (Z_o) for the amplifier circuit of Fig. 8.94.

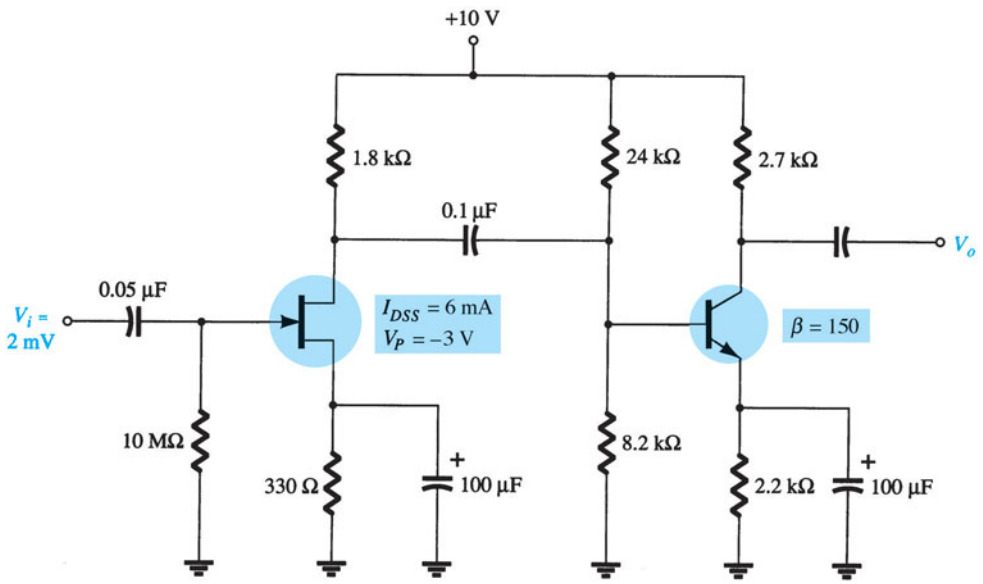


FIG. 8.94
Problems 56 to 58.

8.19 Computer Analysis

59. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.73.

60. Using Multisim, determine the voltage gain for the network of Fig. 8.75.

61. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.76.

62. Using Multisim, determine the voltage gain for the network of Fig. 8.77.

63. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.82.

64. Using PSpice Windows, determine the voltage gain for the network of Fig. 8.85.

***65.** Use the Design Center to draw a schematic circuit of the cascade JFET amplifier as in Fig. 8.93. Set the JFET parameters for $I_{DSS} = 12$ mA and $V_P = 3$ V, and have the analysis determine the dc bias.

***66.** Use the Design Center to draw a schematic circuit for a cascade JFET amplifier as shown in Fig. 8.93. Set the analysis to calculate the ac output voltage V_o for $I_{DSS} = 12$ mA and $V_P = -3$ V.