American International University-Bangladesh (AIUB)
Faculty of Engineering

DIGITAL LOGIC AND CIRCUITS
OBE Assignment [30 marks]
Fall Semester 2023-24
Submission Deadline:12/12/2023 (In Class)

CO2	**Develop** a system in context of Digital logic circuits with 555 timer and transistors for **conflicting requirements** of complex engineering problem.	P.a.3.C3

The ignition activation system of a car is attached to a digital system. The activation system turns on if the following conditions are met. The driver seat is occupied, and the driver seatbelt is fastened. The driver seat is occupied, and the driver seatbelt is fastened, and the passenger seat is occupied, and the passenger seatbelt is fastened. There are appropriate sensors present for detecting the above. Sensor for driver seat is A and sensor for driver seatbelt is B. The sensor for passenger seat is C and the sensor for the passenger seatbelt is D. **If those 2 conditions are not met, then an alarm goes off.**

Your task is to:

i. Outline the necessary steps in correct sequence of the standard procedure to design a digital system for **alarm circuit and design the system**. Also show the outlined steps, **which will trigger the alarm and implement the system with CMOS logic.**

ii. The human audible ranges from 20Hz – 20kHz. However, any sound below 250Hz is considered to be disturbingly low pitched and any sound above 4500Hz is considered to be disturbingly high pitched. Design the alarm timer circuit with a frequency of **P*20 Hz** and a duty cycle of **Q%** [where **P= N+O+I+S+E** and **Q = 100 – P]**. However, if P5 Hz is not within soothing hearing limits, take frequency, f =400Hz. Choose the capacitor value from the given list based on the suitability of your requirements. (C = 50uF/250uF/470uF)

iii. State the limitations of this developed system and explain the effect of increasing the frequency above 4500Hz.

Direction: The numbers NOISE are the middle five digits of your ID (XX-NOISE-SX
(In case the last two letters of your ID is 00, use 45 instead.)

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MARKING RUBRIC:

CP	Assessment Criteria	Evaluation Criteria				Marks
		Poor [1-2]	Average [3-4]	Good [5-6]	Excellent [7-7.5]	
P1	Outline of the standard procedure of digital system design	More than three steps are incorrect or missing and not in correct sequence	One or Two steps of the standard procedure is missing with a one or two steps not in sequence.	All the steps of the procedure have been identified with one or two steps not in correct sequence	All the steps of the procedure have been identified and in correct sequence	
	Digital Triggering Circuit Design.	Design flow has major errors and transistor level design has major flaws.	Design Flow has major error with error carried forward to transistor level design	Design Flow has minor error with error carried forward to transistor level design	Accurate Design Flow with transistor level design having no or minor errors	
P2, P6	Alarm/ Buzzer Design	Alarm design has major flaws which does not comply with the conflicting requirements with major calculation errors.	Alarm design has major flaws which does not comply with the conflicting requirements but with minor calculation errors.	Alarm design is correct and complies to the conflicting requirements but, with major calculation errors.	The alarm design is correct and comply to the requirements with no or minor calculation errors.	
	Limitation	Most of the limitations are irrelevant	Some of the limitations have been addressed	Addressed most of the major limitations	All are correct	
					Total Marks Obtained	