Due – Oct 9th 11:59:59 PM

Homework – III (40 Points)

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17. What is the theoretical speedup for a 4-stage pipeline with a 20ns clock cycle if it is processing 100 tasks?

$S = \frac{nK}{n+K-1} = \frac{100 \cdot 4}{4+100-1} = \frac{402}{103}$

8. Convert the following expressions from infix to reverse Polish (postfix) notation.

- **a)** $X \times Y + W \times Z + V \times U$ XY*WZ*+VU*+
- **b)** $W \times X + W \times (U \times V + Z)$ WX*W UV*Z+*+
- **c)** $(W \times (X + Y \times (U \times V)))/(U \times (X + Y))$

WXYUV**+*U*XY+*/

9. Convert the following expressions from reverse Polish notation to infix notation.

- **a)** W X Y Z − + × W*(X+(Y-Z))
- **b)** U V W X Y Z + * + × + U+(V*(W+(X*(Y+Z))))
- **c)** X Y Z + V W − × Z + +

X+(Y+Z)*(V-W)+Z

11. a) In a computer instruction format, the instruction length is 11 bits and the size of an address field is 4 bits. Is it possible to have

5 2-address instructions

45 1-address instructions

32 0-address instructions

using the format? Justify your answer.

4 bit address 11 bit instructions

5 2 address $2^4 = 16$ $16 \cdot 16 \cdot 5 = 1280$

45 1 $45 \cdot 16 = 720$

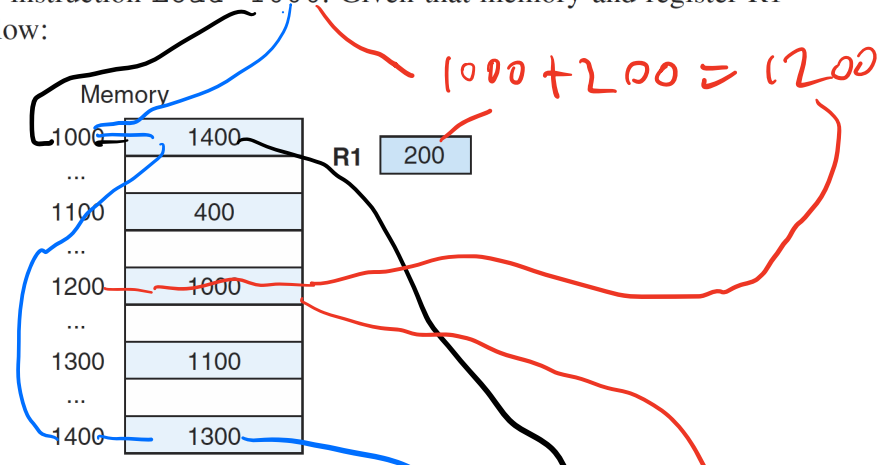
32 0 $+ 32$

2032

$2^{11} = 2048$ instructions

$2032 < 2048$ yes

13. Suppose we have the instruction `Load 1000`. Given that memory and register R1 contain the values below:



Assuming R1 is implied in the indexed addressing mode, determine the actual value loaded into the accumulator and fill in the table below:

Mode	Value Loaded into AC
Immediate	1000
Direct	1400
Indirect	1300
Indexed	1000

17. Write code to implement the expression A = (B + C) × (D + E) on 3-, 2-, 1-, and 0-address machines. In accordance with programming language practice, computing the expression should not change the values of its operands.

load B
Add C
Store temp
load d
add U
Mult temp
store A

load R1, B
Add R1, C
load R2, D
add R2, E
Mult R1, R2
Store A, R1

(2)

Add R1, B, C
Add R2, D, E
Mult A, R1, R2

A = (B+C)×(D+E)

16. A nonpipeline system takes 100ns to process a task. The same task can be processed in a 5-stage pipeline with a clock cycle of 20ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the theoretical speedup that could be achieved with the pipeline system over a nonpipelined system?

Nonpipeline = 100 ns | 5-Stage = 20 ns

speedup 100 tasks

$$S = \frac{nt_n}{(k+n-1)t_p} = \frac{100 \cdot 100}{(5+100-1)20} = \frac{10000}{2080} = 4.8$$

(5)

$X \times Y + W \times Z + V \times U$

$W \times X + W \times (U \times V + Z)$

$(W \times (X + Y \times (U \times V)))/(U \times (X + Y))$