Deniser board

Features

- MachXO3D FPGA
- 48-pin DIP connector
- 46 × 5 V compatible I/O
- On-board voltage regulation
- Powered from 5 V source
- User connector with 3.3 V I/O

General Description

The Deniser board is a 48-pin DIP form factor board designed around a Lattice Semiconductor MachXO3D FPGA. It was designed for use in Amiga computers, while it can also function as a general small-footprint FPGA breakout board.

Hardware Overview

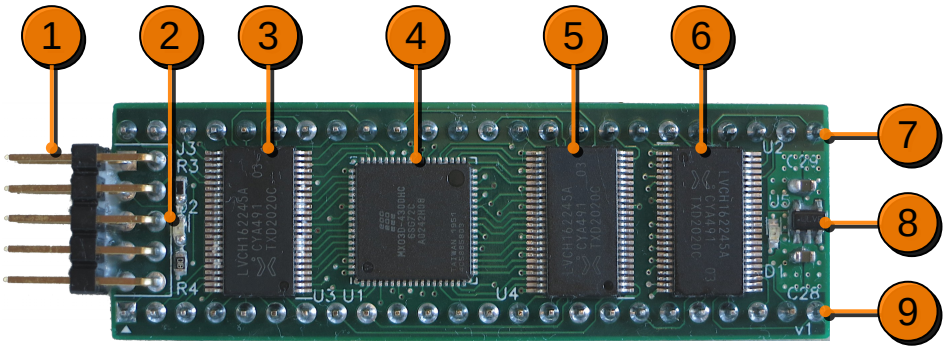


Figure 1: Deniser board with callouts

Callout	Description	Callout	Description
1	JTAG header	4	MachXO3D FPGA
2	User LED	7, 9	DIP connector
3, 5, 6	Bus transceiver 5 V ↔ 3.3 V	8	Voltage regulator

Board Power

The Deniser board is powered with 4.75 V to 5.25 V DC from the DIP connector. Input power is routed to a Texas Instruments LP5907 linear voltage regulator. This voltage regulator is rated for 250mA and produces the main 3.3 V supply for the board.

A LED (`D1`) indicates that the board is receiving power on the 5 V power rail.

Table 1: Voltage regulator circuit information

Supply	Circuits	Device	Max. Current
3.3 V	All	U5: Texas Instruments LP507	250 mA

FPGA Configuration

After power-on, the MachXO3D FPGA must be configured before it can perform any function. The FPGA is normally configured from the on-chip non-volatile configuration memory. The JTAG interface allows configuring the FPGA at any time aswell as programming the on-chip non-volatile configuration memory. JTAG signals are available on the user expansion header J3.

FPGA variants

The Deniser board is compatible with MachXO3D devices specified for 3.3 V supply voltage, such as the ZC and HC device variants. These devices have an internal linear voltage regulator, which is powered by the Deniser board 3.3 V power rail.

MachXO3D HE devices can not be used with the Deniser board.

Block diagram

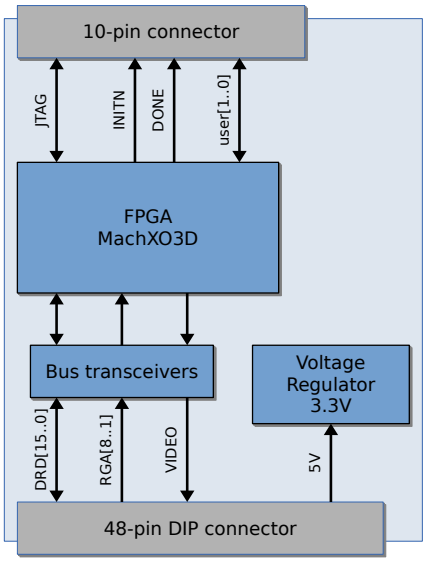


Figure 2: Hardware block diagram

DIP connector

Table 2: DIP connector pinout

Pin	Designation	Function	Direction	Board connection
01-07	D6-D0	Data bus lines 6 to 0	I/O	`U3`
08	M1H	Mouse 1 horizontal	I	`U4`
09	M0H	Mouse 0 horizontal	I	`U4`
10-17	RGA8-RGA1	Register address bus 8-1	I	`U4`
18	/BURST	Color burst	O	`U2`
19	VCC	+5 V	I	LDO input
20-23	R0-R3	Video red bits 0-3	O	`U2`
24-27	B0-B3	Video blue bits 0-3	O	`U2`
28-31	G0-G3	Video green bits 0-3	O	`U2`
32	/CSYNC	Composite sync	I	`U4`
33	/ZD	Background indicator	O	`U2`
34	CDAC[1]	CDAC clock	I (ECS Denise)	`U4`
35	7M	7.159 09 MHz	I	`U4`
36	CCK	Color clock	I	`U4`
37	VSS	Ground	I	Ground
38	M0V	Mouse 0 vertical	I	`U4`
39	M1V	Mouse 1 vertical	I	`U4`
40-48	D15-D7	Data bus lines 15 to 7	I/O	`U3`

[1] *"Not connected"* in OCS Denise

The transceivers `U2`, `U3` and `U4` are located between the DIP connector 5 V logic signals and the FPGA 3.3 V I/O.

- `U2` drives signals FPGA→DIP.
- `U4` drives signals FPGA←DIP.
- `U3` drives signals FPGA←DIP when the signal `drd_rl_to_fpga` is high, and FPGA→DIP when low. The board signal `drd_noe` is connected to the `U3` active low input `nOE`. `drd_rl_to_fpga` and `drd_noe` can be controlled by the FPGA.

User Expansion

The header `J3` provides connections for JTAG and user I/O.

Table 3: `J3` pinout

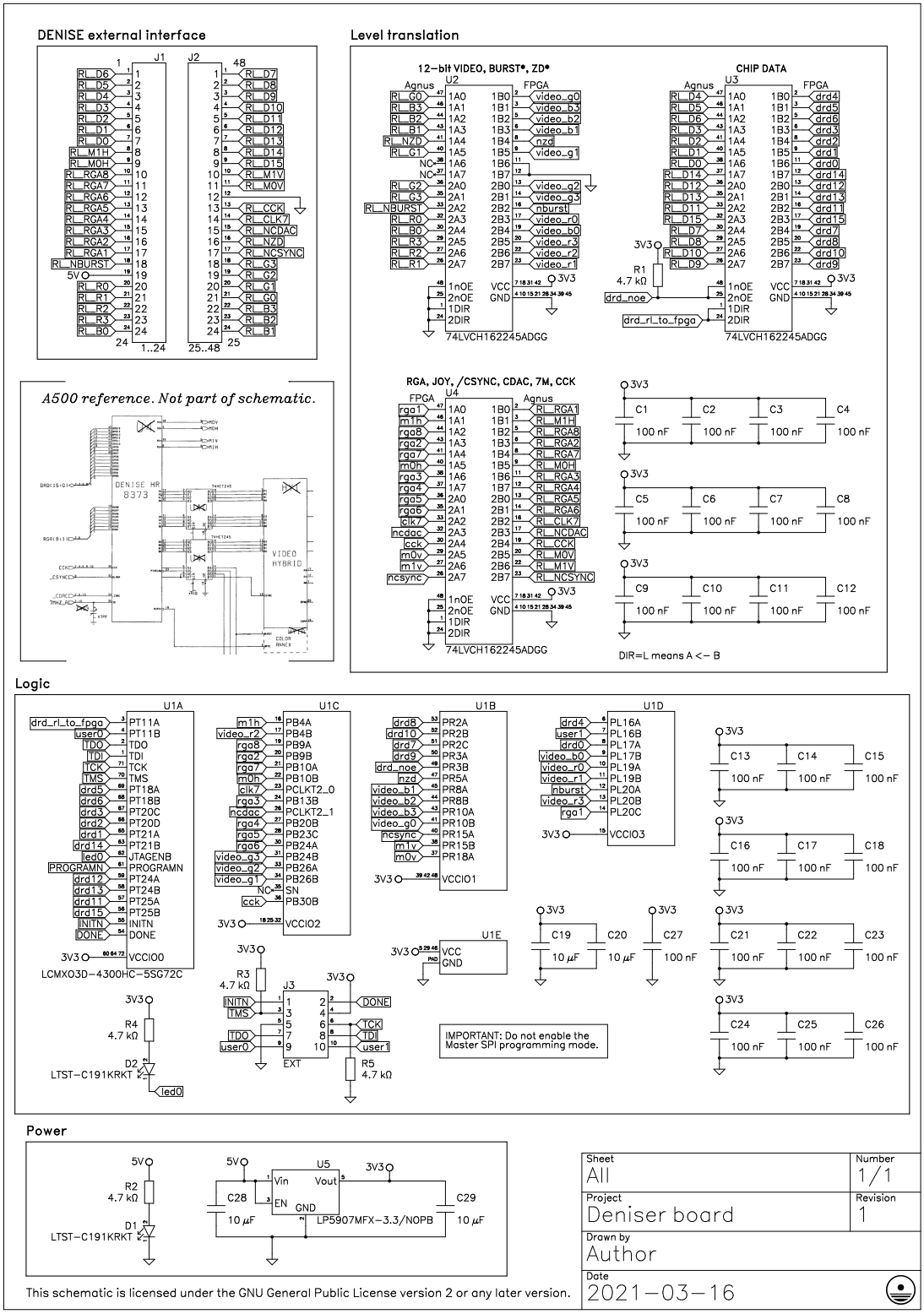
Pin	Signal	MachXO3D pin
1	INITN	55
2	DONE	54
3	TMS	70
4	3V3	*many*
5	GND	PAD
6	TCK	71
7	TDO	2
8	TDI	1
9	user0	4
10	user1	7

A convenient way to access the FPGA JTAG port is to connect with the FTDI FT2232H Mini Module (Table 4).

Table 4: Connection reference for the FT2232H Mini Module

Signal	Deniser board `J3`	FT2232H Mini Module	FT2232H
TCK	6	CN2-7	ADBUS0
TDI	8	CN2-10	ADBUS1
TDO	7	CN2-9	ADBUS2
TMS	3	CN2-12	ADBUS3
GND	5	CN2-2, CN2-4, CN2-6	GND

Electronic Schematics



Bill of materials

Table 5: Bill of materials

Item	#	Designator	MPN	Description
1	25	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C21, C22, C23, C24, C25, C26, C27	GRM155R71C104KA88	100 nF
2	4	C19, C20, C28, C29	LMK107BJ106MALTD	10 μF
3	5	R1, R2, R3, R4, R5	ERJ-3EKF4701	4.7 kΩ
4	2	D1, D2	LTST-C191KRKT	Red LED
5	1	U1	LCMXO3D-4300HC-5SG72C	FPGA
6	3	U2, U3, U4	74LVCH162245ADGG	16-bit transceiver
7	1	U5	LP5907MFX-3.3/NOPB	LDO 3.3 V 250 mA
8	2	J1, J2	M20-9992445	Header 1 $\times$ 24
9	1	J3	10129381-910001BLF	Header 2 $\times$ 5