

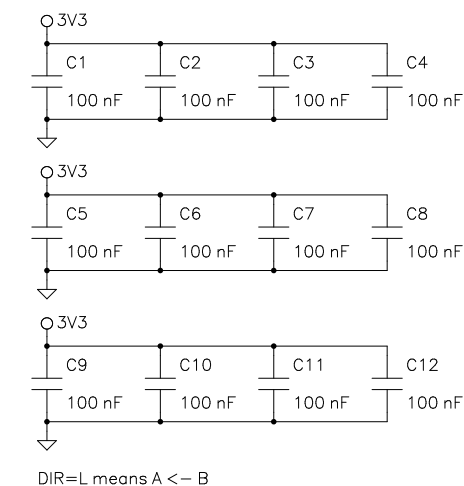
A500 reference. Not part of schematic.

U4

FPGA	Pin	Agustus	Pin
rga1	47	2	RL RGA1
m1h	46	1	RL M1H
rga8	44	5	RL RGA8
rga2	43	6	RL RGA2
rga7	41	8	RL RGA7
m0h	40	9	RL M0H
rga3	38	11	RL RGA3
rga4	37	12	RL RGA4
rga5	36	13	RL RGA5
rga6	35	14	RL RGA6
clk7	33	16	RL CLK7
ncdac	32	17	RL NCDAC
clk	30	19	RL CLK
m0v	28	20	RL M0V
m1v	27	22	RL M1V
ncsync	26	23	RL M1VSYNC
		27	

1nOE VCC 7 18 31 42
2nOE GND 4 10 15 21 28 34 39 45
1DIR
2DIR

74LVCH162245ADGG



Sheet All	Number 1/1
Project Deniser board	Revision 1
Drawn by Author	
Date 2021-03-16	

