HEAVY METAL KATA

BRIEF INTRODUCTION TO 8086 ASSEMBLER

Main Registers

- Accumulator (A)
 - Arithmetic
- Counter (C)

Used in loops and shift rotate operations

- Data (D)
 - I/O operations
- **Base** (B)

Pointer to data

16 bit: AX, BX, CX, DX, 8 bit: parts L,H

INDEX REGISTERS

- Source Index (SI)
 Used as a source pointer in string operations (in DS)
- Destination Index (DI)
 Used as a destination pointer in string operations (in ES)
- Base Pointer (BP)
 Points base of the stack
- Stack Pointer (SP)
 Points the top of the stack

All are 16 bit

SEGMENT REGISTERS

- Data Segment (DS)
- Extra Segment (ES)
- Stack Segment (SS)
- Code Segment (CS)

All are 16 bit

PROGRAM COUNTER

• Instruction Pointer (IP)

STATUS REGISTER

- Carry (C) Set when carry (borrow) was generated in last arithmetic operation
- Zero (Z) Set when last arithmetic operation result was zero
- Sign (S) Set when most significant bit is 1 (number is negative in two's complement form)
- Overflow (O) Set when 127 + 127 = -2 (in two's complement form)
- Parity (P) parity of the result of last operation
- Adjust (A) half carry (carry on lower 4 bits)
- Interrupt (I) if 0 maskable interrupts will be ignored
- Direction (D) 0 mean string is processing from lowest to highest address

DATA TRANSFER INSTRUCTIONS

- MOV move data between:
 - Register: MOV AX, BC
 - Immediate: MOV AX, 0x10
 - Memory: MOV AX, ES:[BX] (MOV AX, ES:[BX+5],MOV AX, ES:[BX][SI]+5)
- PUSH/POP stack operations
 - Register: PUSH AX
 - Memory: POP ES:[BX]

ARITMETIC

- ADD/SUB adding subtracting: (ADC/SBB carry/borrow version)
 - ADD destination, source (destination = destination + source)
 - o **ADD** ax, 10
 - o ADD ax, bx
 - ADD ax, es:[bx]
 - ADD es:[bx], ax
- INC/DEC increasing/decreasing register or memory
- MUL/DIV multiply/divide source by accumulator
- AND/OR/XOR/NOT/TEST binary operations
- SHR/SHL/ROL/ROR shift/rotate

CONTROL

- CALL/RET push/pop ip to stack
- JMP Unconditional jump
- **J*** paired with **CMP** or after arithmetic operations conditional jump
- LOOP decrease CX, and JNZ

8086 AND 8088 CENTRAL PROCESSING UNITS

Table 2-15. Interpretation of Conditional Transfers

MNEMONIC	CONDITION TESTED	"JUMP IF"
JA/JNBE JAE/JNB JB/JNAE JBE/JNA JC JE/JZ JG/JNLE JGE/JNL JL/JNGE JLE/JNG JNC JNE/JNZ JNO JNP/JPO JNS JO JP/JPE JS	(CF OR ZF)=0 CF=0 CF=1 (CF OR ZF)=1 CF=1 ZF=1 ((SF XOR OF) OR ZF)=0 (SF XOR OF)=0 (SF XOR OF)=1 ((SF XOR OF) OR ZF)=1 CF=0 ZF=0 OF=0 PF=0 SF=0 OF=1 PF=1 SF=1	above/not below nor equal above or equal/not below below/not above nor equal below or equal/not above carry equal/zero greater/not less nor equal greater or equal/not less less/not greater nor equal less or equal/not greater not carry not equal/not zero not overflow not parity/parity odd not sign overflow parity/parity equal sign

THE INT INSTRUCTION

Activate the interrupt procedure (I/O, BIOS, OS)

- INT 21h dos interrupt
- INT 10h bios interrupt

http://stanislavs.org/helppc/int_21.html

MOV AH, 0x02 MOV DL 'x' INT 0x21

MOV AX, 0x4c00 INT 0x21