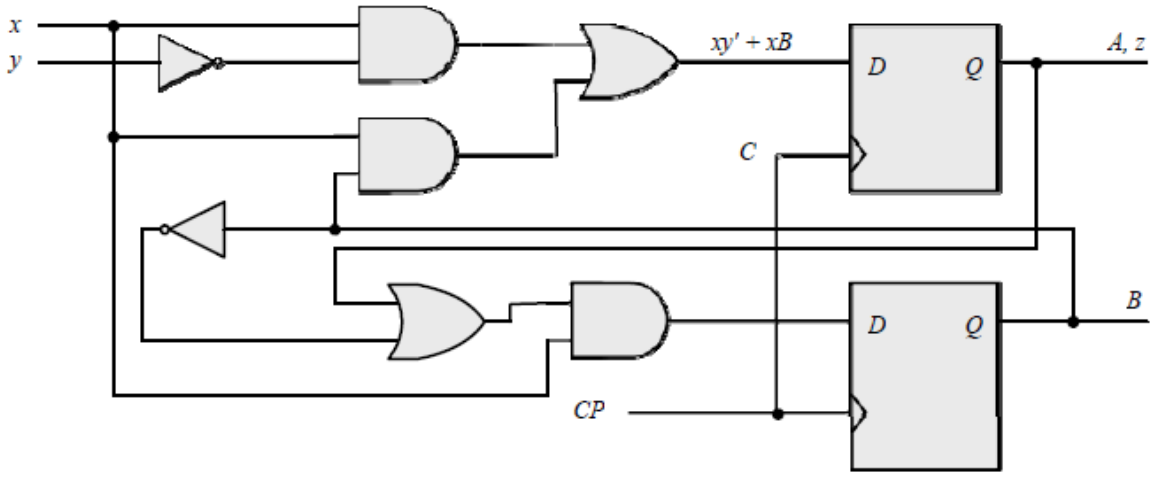
**5.6** A sequential circuit with two $D$ flip-flops $A$ and $B$, two inputs, $x$ and $y$; and one output $z$ is specified by the following next-state and output equations (HDL—see Problem 5.35):

$$A(t+1) = xy' + xB$$
$$B(t+1) = xA + xB'$$
$$z = A$$

(a) Draw the logic diagram of the circuit.
(b) List the state table for the sequential circuit.
(c) Draw the corresponding state diagram.

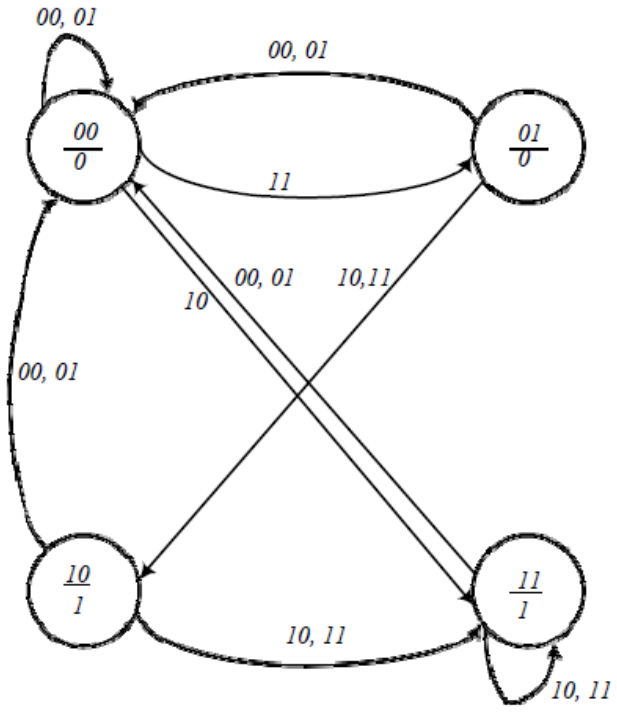



**(b)**

$A(t+1) = xy' + xB$
$B(t+1) = xA + xB'$
$z = A$

| Present state | | Inputs | | Next state | | Output |
|---|---|---|---|---|---|---|
| A | B | x | y | A | B | z |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**(c)**



**5.7*** A sequential circuit has one flip-flop $Q$, two inputs $x$ and $y$, and one output $S$. It consists of a full-adder circuit connected to a $D$ flip-flop, as shown in Fig. P5.7. Derive the state table and state diagram of the sequential circuit.

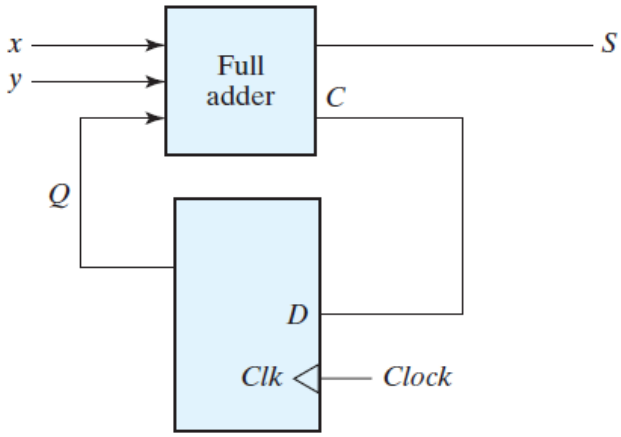
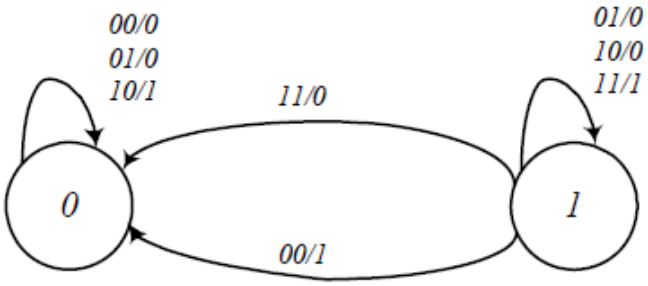



**FIGURE P5.7**

| Present state | Inputs | | Next state | Output |
|---|---|---|---|---|
| $Q$ | $x$ | $y$ | $Q$ | $S$ |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |




$$S = x \oplus y \oplus Q$$

$$Q(t+1) = xy + xQ + yQ$$

**5.8*** Derive the state table and the state diagram of the sequential circuit shown in Fig. P5.8. Explain the function that the circuit performs. (HDL—see Problem 5.36.)

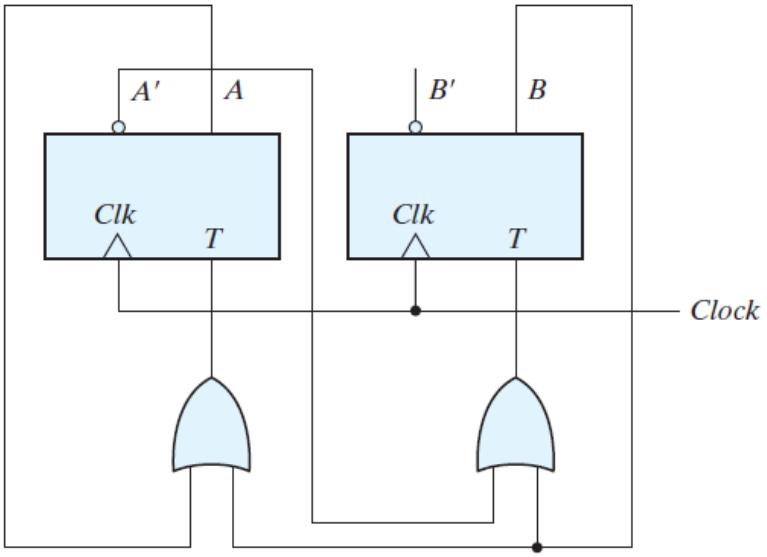



**FIGURE P5.8**

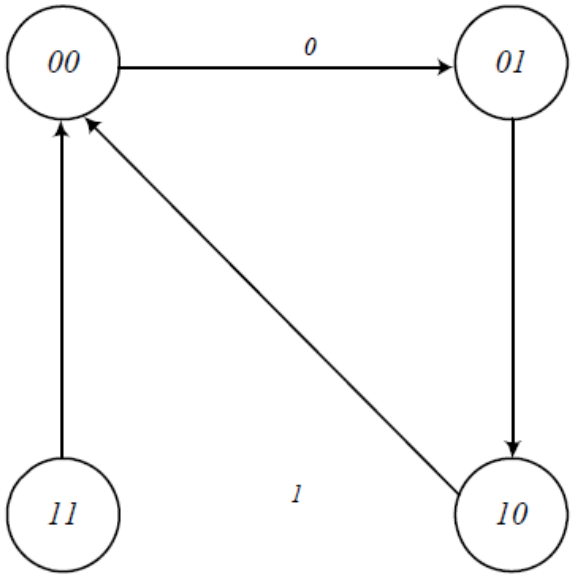
A counter with a repeated sequence of 00, 01, 10.

| Present State | | Next State | | FF Inputs | |
|---|---|---|---|---|---|
| A | B | A | B | $T_A$ | $T_B$ |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 1 |

$T_A = A + B$

$T_B = A' + B$

Repeated sequence: 00 → 01 → 10



**5.9** A sequential circuit has two *JK* flip-flops *A* and *B* and one input *x*. The circuit is described by the following flip-flop input equations:

$$J_A = x',\ K_A = B'$$
$$J_B = A,\ K_B = x$$

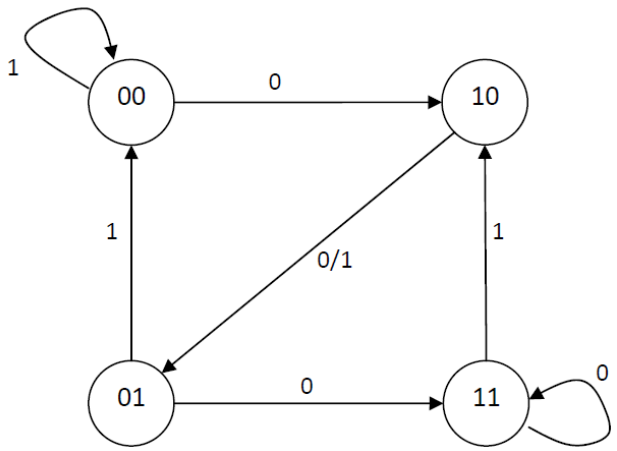
(a) Derive the state equations $A(t+1)$ and $B(t+1)$ by substituting the input equations for the *J* and *K* variables.
(b) Draw the state diagram of the circuit.

**(a)**

$$J_A = x',\ K_A = B';\ A(t+1) = JA' + K'A = x'A' + BA$$
$$J_B = A,\ K_B = x;\ B(t+1) = JB' + K'B = AB' + x'B$$

**(b)**

| Present State | | Input | Next state | |
|---|---|---|---|---|
| *A(t)* | *B(t)* | *x* | *A(t+1)* | *B(t+1)* |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 |



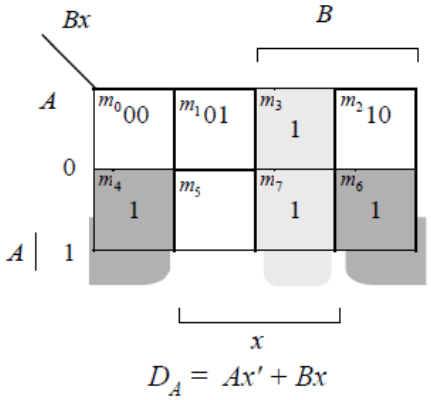
**5.16** Design a sequential circuit with two *D* flip-flops *A* and *B*, and one input *x_in*.

(a)* When *x_in* = 0, the state of the circuit remains the same. When *x_in* = 1, the circuit goes through the state transitions from 00 to 01, to 11, to 10, back to 00, and repeats.

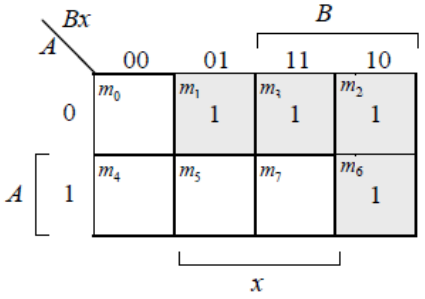
(b) When *x_in* = 0, the state of the circuit remains the same. When *x_in* =1, the circuit goes through the state transitions from 00 to 11, to 01, to 10, back to 00, and repeats. (HDL—see Problem 5.38.)

a)

| Present state | | Input | Next state | |
|---|---|---|---|---|
| A | B | x | A | B |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 |



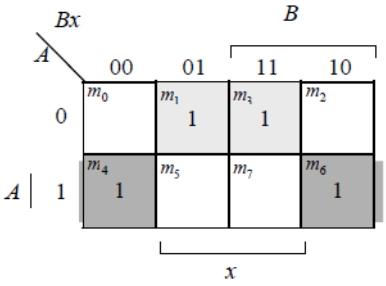

$D_A = Ax' + Bx$



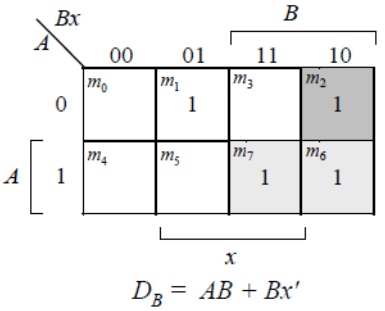

$D_B = A'x + Bx'$

b)

| *Present state* | | *Input* | *Next state* | |
|---|---|---|---|---|
| A | B | x | A | B |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |



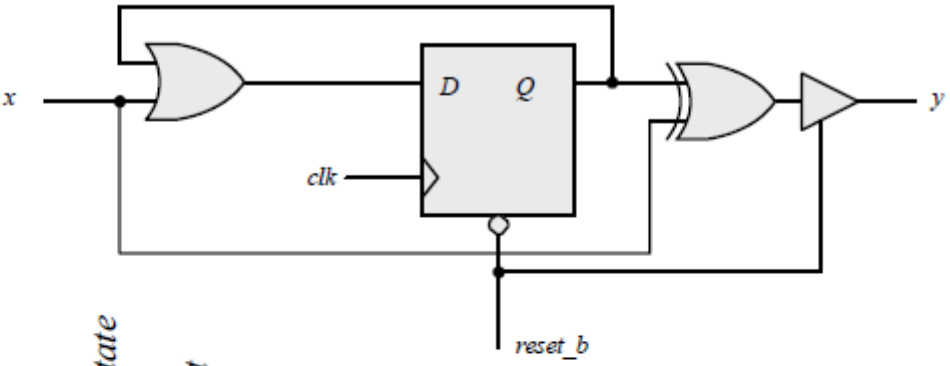

$D_A = A'x + Ax'$



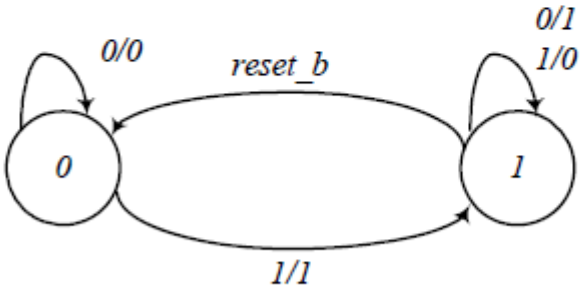

$D_B = AB + Bx'$

**5.17** Design a one-input, one-output serial 2's complementer. The circuit accepts a string of bits from the input and generates the 2's complement at the output. The circuit can be reset asynchronously to start and end the operation. (HDL—see Problem 5.39.)

The output is 0 for all 0 inputs until the first 1 occurs, at which time the output is 1. Thereafter, the output is the complement of the input. The state diagram has two states. In state 0: output = input; in state 1: output = input'.




| Present state | Input | Next state | Output |
|---|---|---|---|
| A | x | A | y |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 |

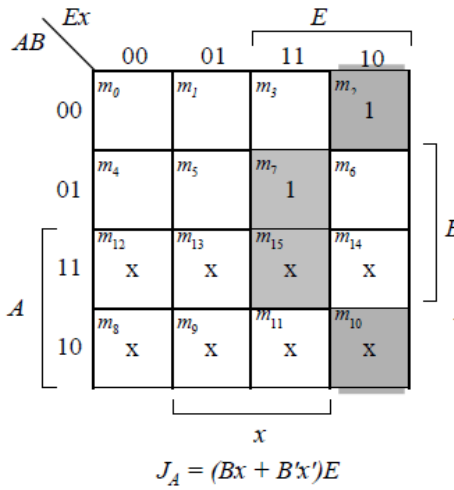



$$D_A = A + x$$
$$y = Ax' + A'x$$

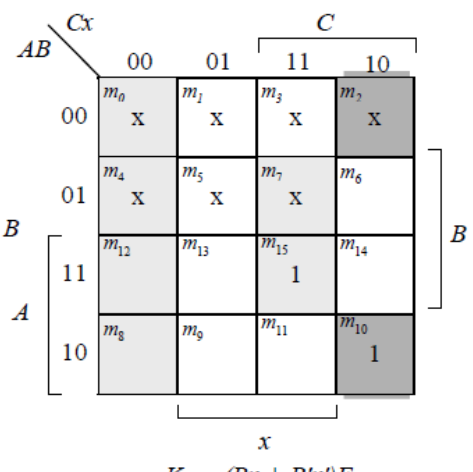
**5.18*** Design a sequential circuit with two *JK* flip-flops *A* and *B* and two inputs *E* and *F*. If $E = 0$, the circuit remains in the same state regardless of the value of *F*. When $E = 1$ and $F = 1$, the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats. When $E = 1$ and $F = 0$, the circuit goes through the state transitions from 00 to 11, to 10, to 01, back to 00, and repeats. (HDL—see Problem 5.40.)

## Binary up-down counter with enable *E*.

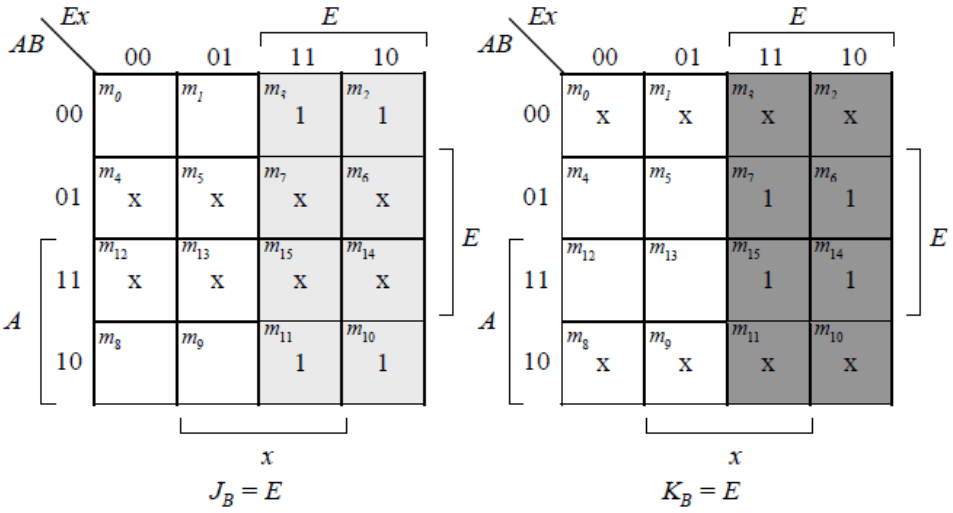
| *Present state* A B | *Input* x | *Next state* A B | *Flip-flop inputs* $J_A$ $K_A$ | $J_B$ $K_B$ |
|---|---|---|---|---|
| 0 0 | 0 1 | 0 0 | 0 x | 0 x |
| 0 0 | 0 1 | 0 0 | 0 x | 0 x |
| 0 0 | 1 0 | 1 1 | 1 x | 1 x |
| 0 0 | 1 1 | 0 1 | 0 x | 1 x |
| 0 1 | 0 0 | 0 1 | 0 x | x 0 |
| 0 1 | 0 1 | 0 1 | 0 x | x 0 |
| 0 1 | 1 0 | 0 1 | 0 x | x 1 |
| 0 1 | 1 1 | 1 0 | 1 x | x 1 |
| 1 0 | 0 0 | 1 0 | x 0 | 1 0 |
| 1 0 | 0 1 | 1 0 | x 0 | 1 0 |
| 1 0 | 1 0 | 0 1 | x 1 | x 1 |
| 1 0 | 1 1 | 1 1 | x 0 | x 1 |
| 1 1 | 0 0 | 1 1 | x 0 | x 0 |
| 1 1 | 0 1 | 1 1 | x 0 | x 0 |
| 1 1 | 1 0 | 1 1 | 1 0 | x 1 |
| 1 1 | 1 1 | 1 1 | x 1 | x 1 |




$J_A = (Bx + B'x')E$




$K_A = (Bx + B'x')E$




**5.19** A sequential circuit has three flip-flops *A*, *B*, *C*; one input *x_in*; and one output *y_out*. The state diagram is shown in Fig. P5.19. The circuit is to be designed by treating the unused states as don't-care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states. (HDL—see Problem 5.41.)

(a)* Use *D* flip-flops in the design.

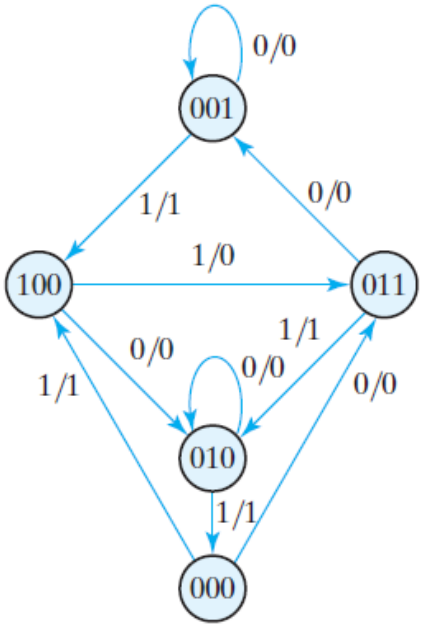
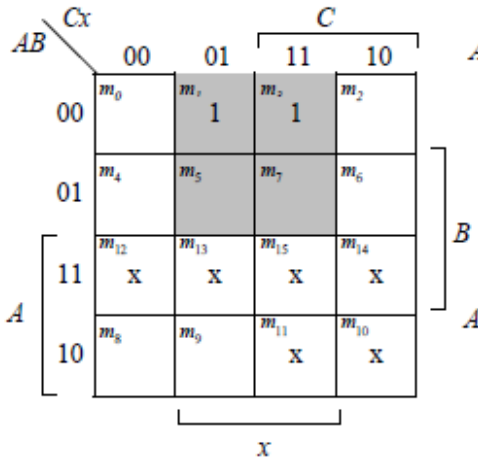



**FIGURE P5.19**

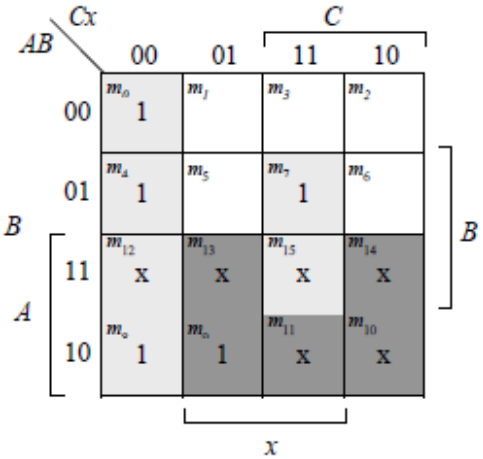
Unused states (see Fig. P5.19): 101, 110, 111.

| *Present state ABC* | *Input x* | *Next state ABC* | *Output y* |
|---|---|---|---|
| 000 | 0 | 011 | 0 |
| 000 | 1 | 100 | 1 |
| 001 | 0 | 001 | 0 |
| 001 | 1 | 100 | 1 |
| 010 | 0 | 010 | 0 |
| 010 | 1 | 000 | 1 |
| 011 | 0 | 001 | 0 |
| 011 | 1 | 010 | 1 |
| 100 | 0 | 010 | 0 |
| 100 | 1 | 011 | 1 |

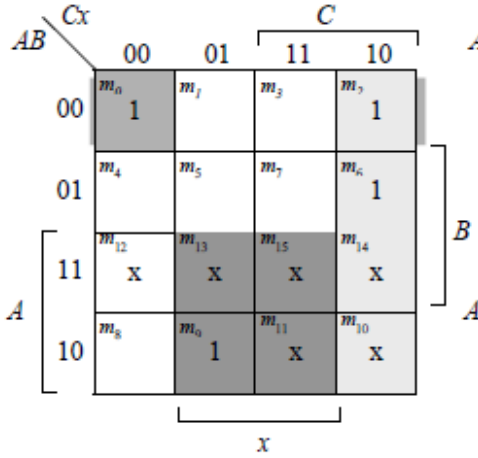
$d(A, B, C, x) = \Sigma\,(10, 11, 12, 13, 14, 15)$



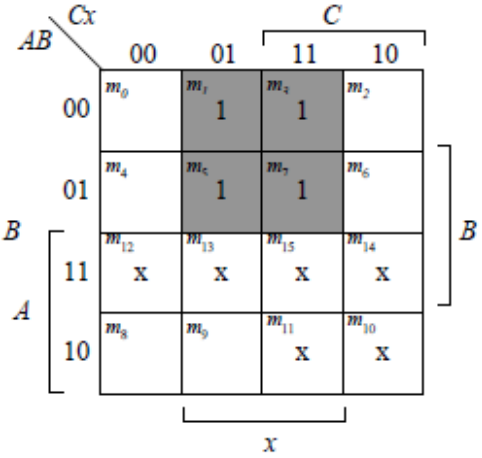

$D_A = A'B'x$




$D_B = A + C'x' + BCx$

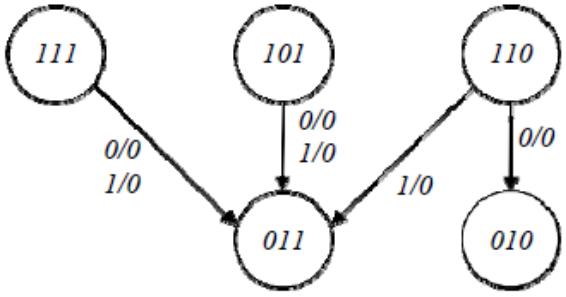



$D_C = Cx' + Ax + A'B'x'$




$y = A'x$

*The machine is self-correcting, i.e., the unused states transition to known states.*




**6.19** The flip-flop input equations for a BCD counter using *T* flip-flops are given in Section 6.4. Obtain the input equations for a BCD counter that uses

(b)* *D* flip- flops.

## BCD Counter

A BCD counter counts in binary-coded decimal from 0000 to 1001 and back to 0000. Because of the return to 0 after a count of 9, a BCD counter does not have a regular pattern, unlike a straight binary count. To derive the circuit of a BCD synchronous counter, it is necessary to go through a sequential circuit design procedure.

The state table of a BCD counter is listed in Table 6.5. The input conditions for the *T* flip-flops are obtained from the present- and next-state conditions. Also shown in the table is an output $y$, which is equal to 1 when the present state is 1001. In this way, $y$ can enable the count of the next-higher significant decade while the same pulse switches the present decade from 1001 to 0000.

The flip-flop input equations can be simplified by means of maps. The unused states for minterms 10 to 15 are taken as don't-care terms. The simplified functions are

$$\begin{aligned} T_{Q1} &= 1 \\ T_{Q2} &= Q'_8 Q_1 \\ T_{Q4} &= Q_2 Q_1 \\ T_{Q8} &= Q_8 Q_1 + Q_4 Q_2 Q_1 \\ y &= Q_8 Q_1 \end{aligned}$$

The circuit can easily be drawn with four *T* flip-flops, five AND gates, and one OR gate. Synchronous BCD counters can be cascaded to form a counter for decimal numbers of any length. The cascading is done as in Fig. 6.11, except that output $y$ must be connected to the count input of the next-higher significant decade.

**Table 6.5**
*State Table for BCD Counter*

| Present State | | | | Next State | | | | Output | Flip-Flop Inputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $Q_8$ | $Q_4$ | $Q_2$ | $Q_1$ | $Q_8$ | $Q_4$ | $Q_2$ | $Q_1$ | $y$ | $TQ_8$ | $TQ_4$ | $TQ_2$ | $TQ_1$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

From the state table in Table 6.5:

$D_{Q1} = Q'_1$
$D_{Q2} = \sum (1, 2, 5, 6)$
$D_{Q4} = \sum (3, 4, 5, 6)$
$D_{Q8} = \sum (7, 8)$
Don't care: $d = \sum (10, 11, 12, 13, 14, 15)$

Simplifying with maps:
$D_{Q2} = Q_2Q'_1 + Q'_8Q'_2Q_1$

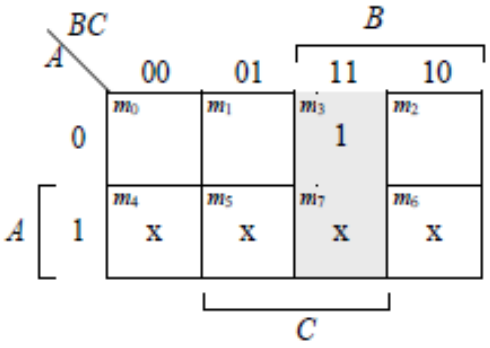
$D_{Q4} = Q_4Q'_1 + Q4Q'2 + Q'_4Q_2Q_1$
$D_{Q8} = Q_8Q'_1 + Q_4Q_2Q_1$

**6.27** Using *JK* flip-flops,

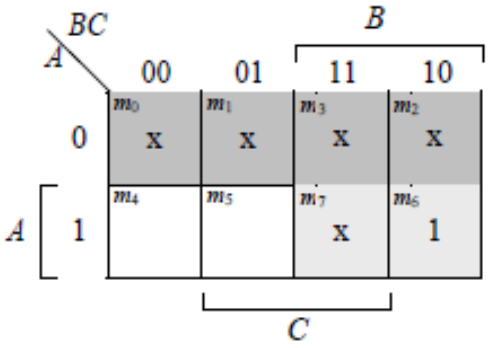
(a) Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6. (HDL—see Problem 6.50(a), 6.51.).

(b) Draw the logic diagram of the counter.

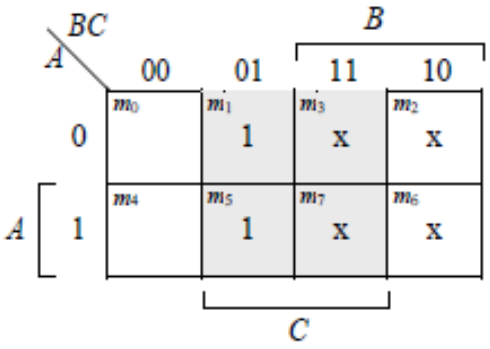
| *Present state* *ABC* | *Next state* *ABC* | *Flip-flop inputs* $J_A$ | $K_A$ | $J_B$ | $K_B$ | $J_C$ | $K_C$ |
|---|---|---|---|---|---|---|---|
| 000 | 001 | 0 | x | 0 | x | 1 | x |
| 001 | 010 | 0 | x | 1 | x | x | 1 |
| 010 | 011 | 0 | x | x | 0 | 1 | x |
| 011 | 100 | 1 | x | x | 1 | x | 1 |
| 100 | 101 | x | x | 0 | 0 | 1 | x |
| 101 | 110 | x | 0 | 1 | x | x | 1 |
| 110 | 000 | x | 1 | x | 1 | 0 | x |
| 111 | xxx | x | x | x | x | x | x |



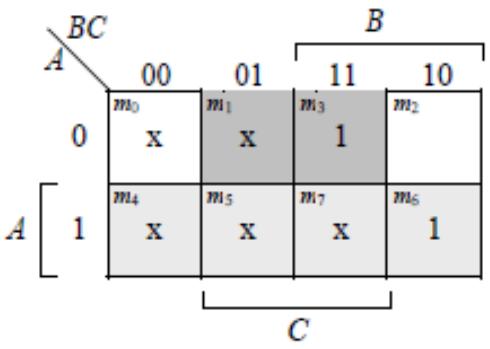

$J_A = BC$



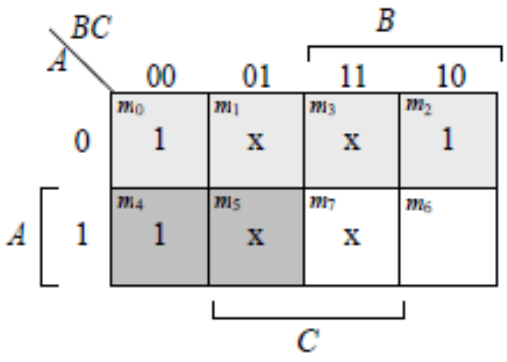

$K_A = A' + B$



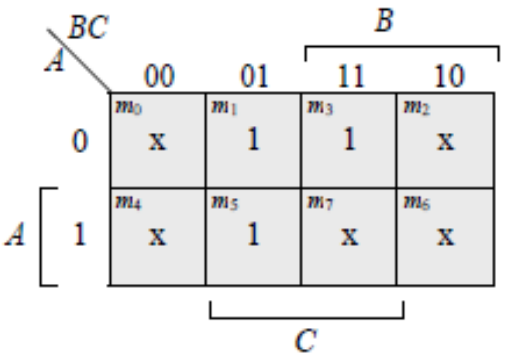

$J_B = C$



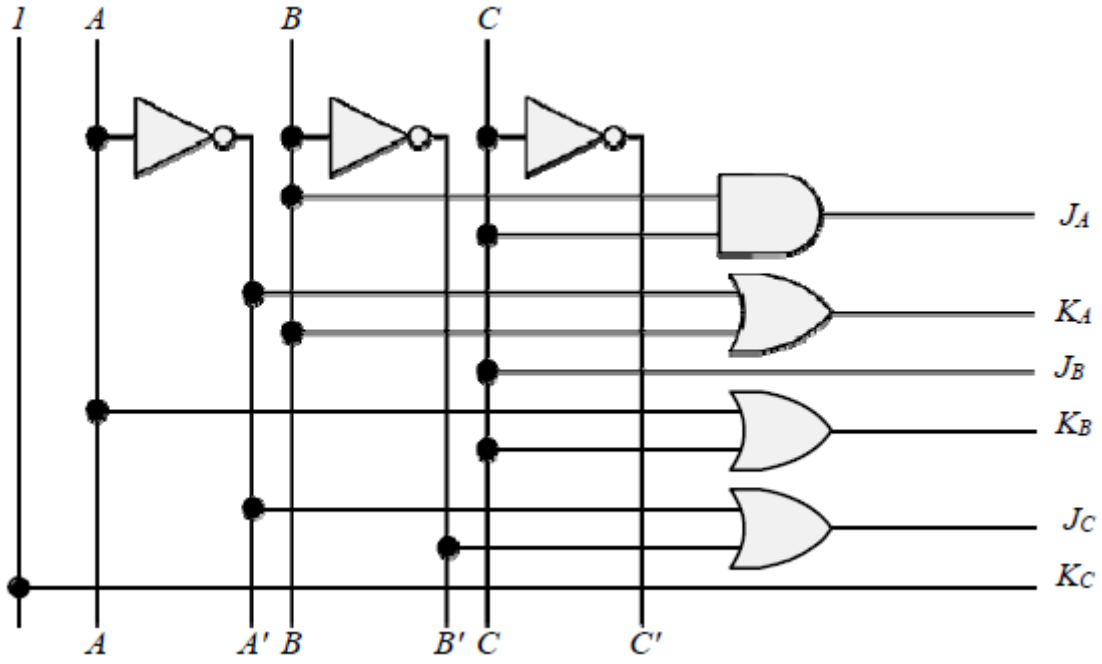

$K_B = A + C$


BC
A
B
00
01
11
10
0
1
A
$m_0$ 1
$m_1$ x
$m_3$ x
$m_2$ 1
$m_4$ 1
$m_5$ x
$m_7$ x
$m_6$
C

$J_C = A' + B'$


BC
A
B
00
01
11
10
0
1
A
$m_0$ x
$m_1$ 1
$m_3$ 1
$m_2$ x
$m_4$ x
$m_5$ 1
$m_7$ x
$m_6$ x
C

$K_C = 1$


1
A
B
C
$J_A$
$K_A$
$J_B$
$K_B$
$J_C$
$K_C$
A
A'
B
B'
C
C'