**Muhammed Enes İnanç**

**22001799**

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**Purpose:**

The purpose of lab3 is to physically use the logic gates we learned in the lesson and schematized through Vhdl and to make them understand their importance. The practical use of gates underlying electrical and electronic engineering on a breadboard is shown. In this lab, it is also aimed to reinforce the use of oscilloscope, signal generator and power supply.

**Logic of This Design:**

In Lab2, I determined 4 basic factors in order to be able to run a desktop computer in a healthy way and to take an image. These factors are computer(in1), monitor(in2), electricity(in3) and electricity generator(in4). Below is the truth table on which several of these factors must come together to fully run a computer. The parts where the result is 1 are the situations where the computer is working properly and the image can be taken.

| In1(computer) | In2 (monitor) | In3 (electricity) | In4 (generator) | Out1 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

In the 3rd lab, I physically built this circuit on the breadboard and observed the results both with an oscilloscope and by eye.

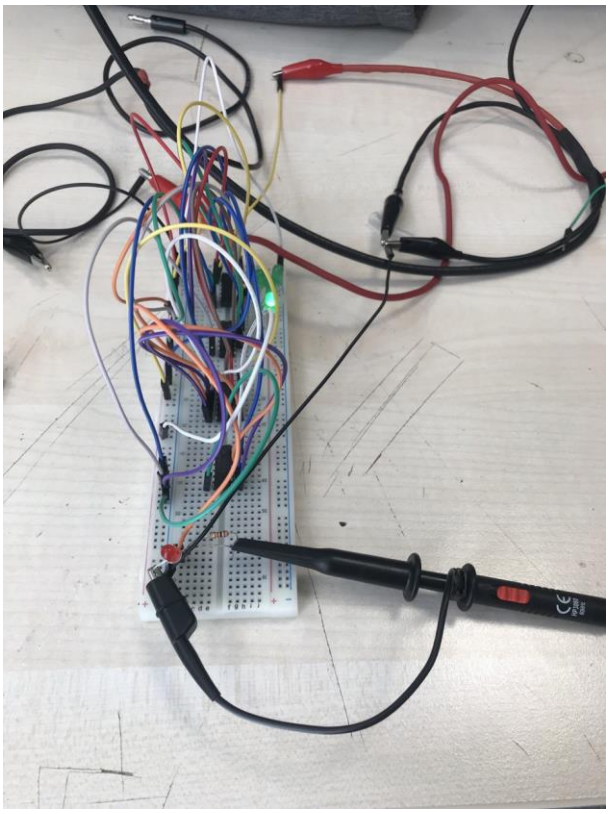

Figure 1

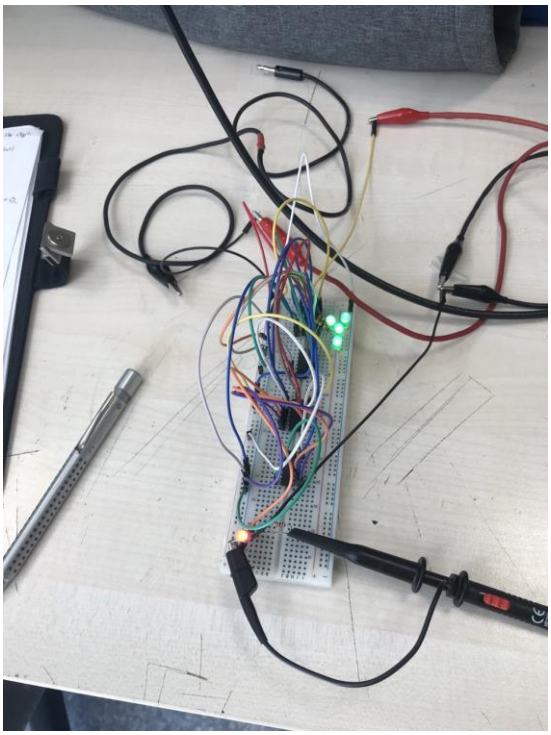

Figure 2

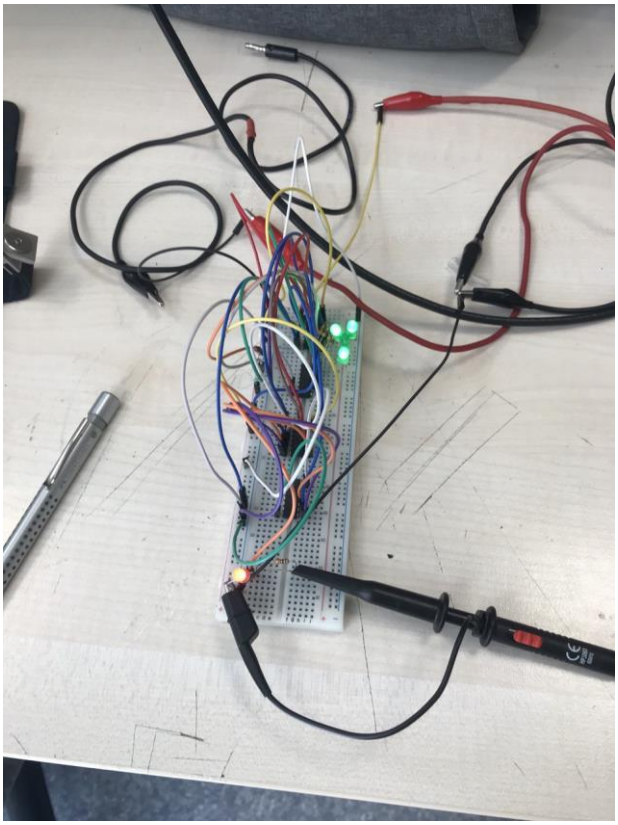

Figure 3

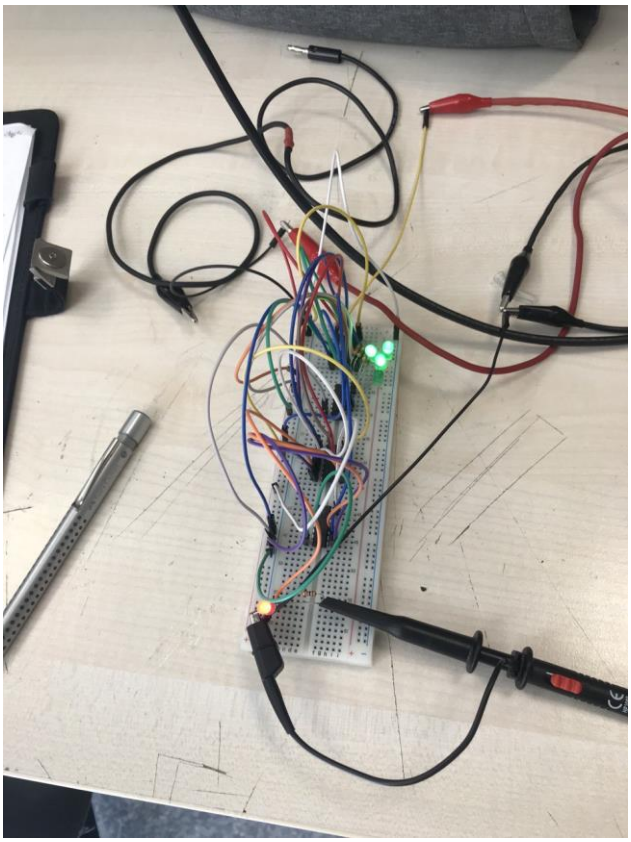

Figure 4

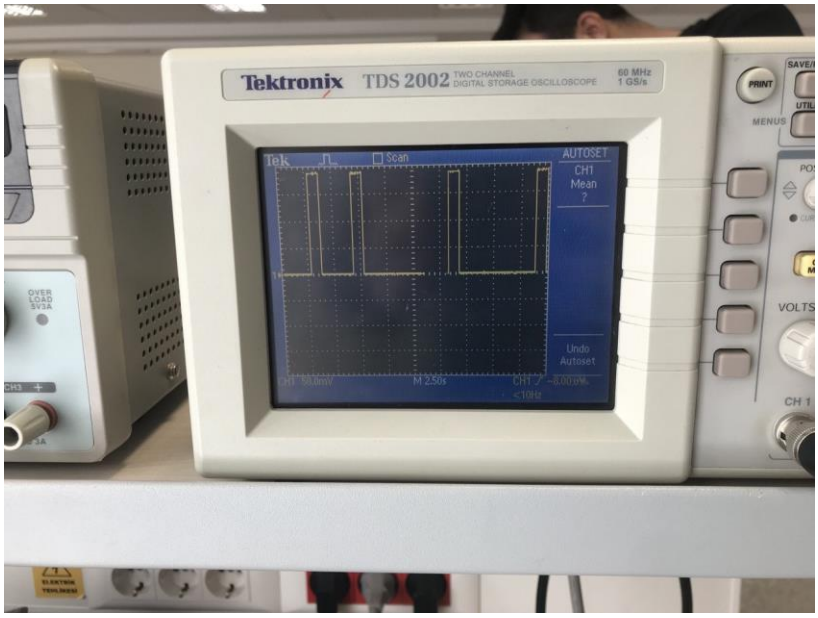


Figure 5

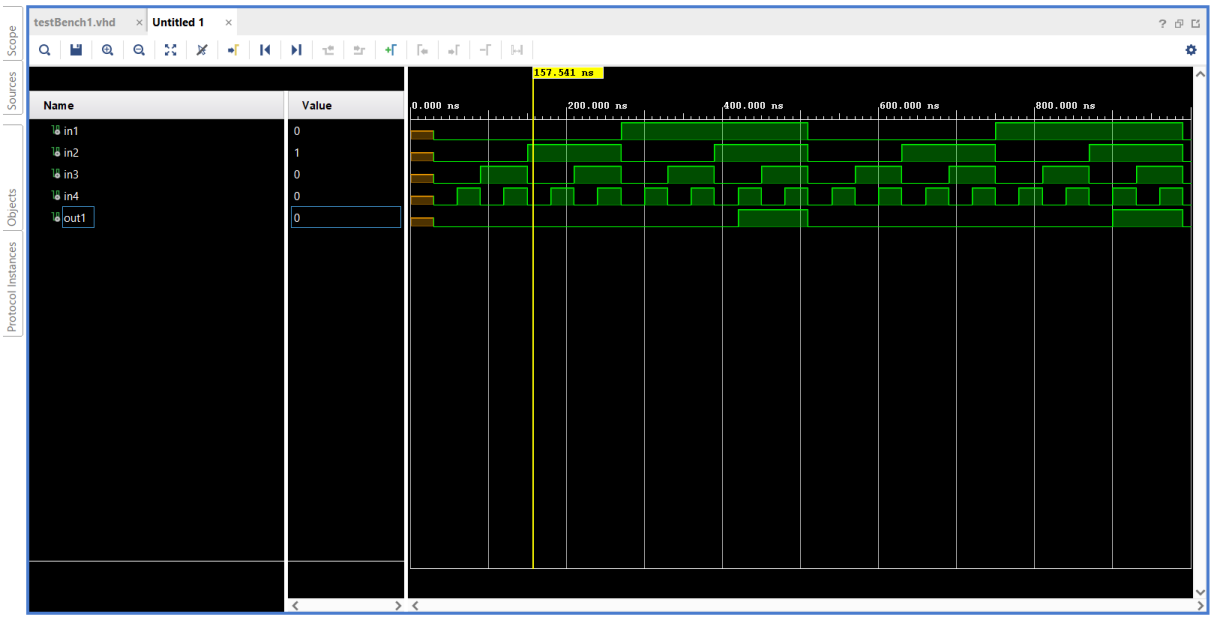


Figure 6 ( waves form generated by VHDL)

**How does the counter work? :**

To create a logic function, the circuit must have inputs. In fact, the counter takes over this task. However, some connections must be made on the breadboard as in figure 1 and figure 2 to enable the count mode. MR, CEP, CET, PE are connected to 5V DC voltage source. But CP is connected to AC source to make different inputs at the same time. As a result, 4 inputs are produced as Q0, Q1, Q2, Q3.

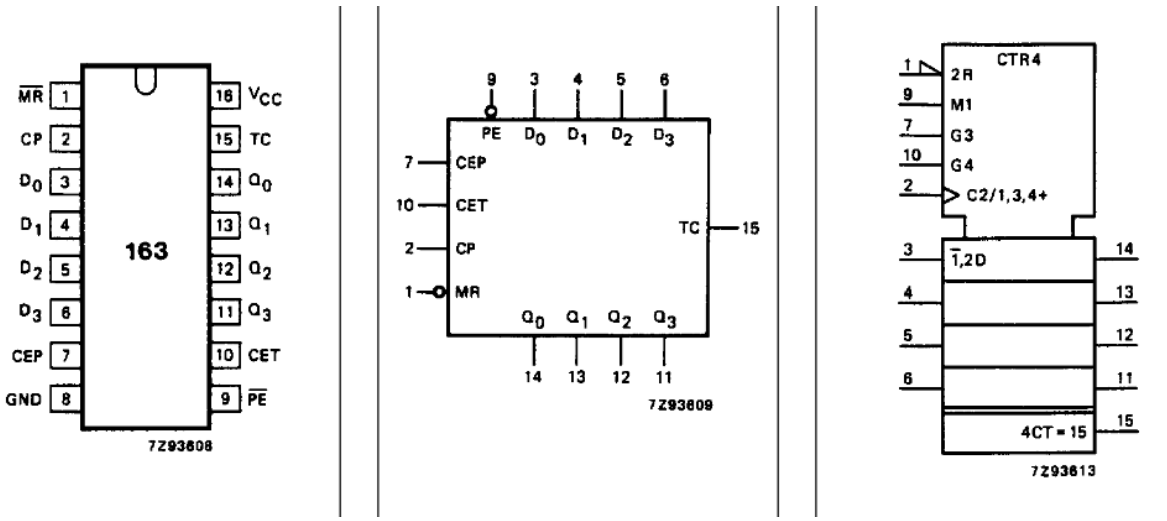


Figure 1

**FUNCTION TABLE**

| OPERATING MODE | INPUTS | | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|---|
| | $\overline{MR}$ | CP | CEP | CET | $\overline{PE}$ | $D_n$ | $Q_n$ | TC |
| reset (clear) | l | ↑ | X | X | X | X | L | L |
| parallel load | h<br>h | ↑<br>↑ | X<br>X | X<br>X | l<br>l | l<br>h | L<br>H | L<br>(1) |
| count | h | ↑ | h | h | h | X | count | (1) |
| hold<br>(do nothing) | h<br>h | X<br>X | l<br>X | X<br>l | h<br>h | X<br>X | $q_n$<br>$q_n$ | (1)<br>L |

**Notes**

1. The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).
   H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
   q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
   X = don't care
   ↑ = LOW-to-HIGH CP transition

Figure 2

## Conclusion:

In this lab, 2-input AND gate, 2-input OR gate, NOT gate and counter were used. The third of the inputs produced by the counter was reversed at the NOT gate and sent to the AND gate with the 4th input. Then the result of this operation was sent to the OR gate with the third input. Finally, the result of this operation is re-entered into the AND gate with the result of the first and second inputs sent to the AND gate. The result produced here represented the result of the function by connecting to the red led light. In addition, the inputs were represented by first connecting a 1 kΩ resistor to the end of each input on the counter and then connecting the green LEDs. The purpose of putting these resistors is to prevent the leds from overheating and exploding. Finally, the result function can be displayed on the oscilloscope by connecting the oscilloscope probe to the red LED. It has been a lab where logic gates are used physically, the separation of AC and DC sources is noticed and used effectively, and the Oscilloscope is used effectively.

F = (in1*in2) * ((not in3* in4)+ in3)