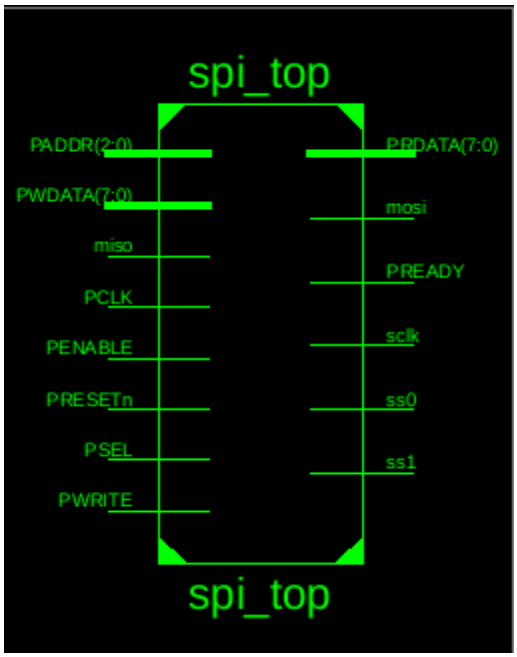
# APB BRIDGE TO SPI

## Features

1. support 32-bit wide data width,
2. full duplex transmission,
3. simple control ,
4. two slave select pins are available,

## Pin description




## Inputpin’s

- PRESETn- Active Low RESET
- PCLK-Peripheral Clock
- PENABLE- Data Transmission ENABLE
- PSEL-Select Spi
- PADDR-Configuration Bits(3-bit wide)
- PWRITE-Enable Read Write Operation
- PWDATA-Data Input,Apb Slave To SpiMosi(32-bit wide)
- Miso-Data Input,Spi Master To Apb Slave

## Output pin’s

- PREADY-Apb Slave Output
- PRDATA-Apb Slave Output, FromSpi Miso(32-bit wide)
- ss0-Slave 0
- ss1-Slave 1
- sclk-Slave Clk
- mosi-Output Of Spi Master

Note: by default remaining pins are 1-bit wide,

## Description

Thespi is a protocol which helps to communicate the external word sensors, data storage device,

So the spi protocol provide high speed data transmission, it also provides reliable data transfer with

Full duplex transmission.

**Register Description**

**SPI Control Register**

**MSTR->** 1 -SPI operates in master mode, 0-SPI operates in slave mode.

**CPHA->** 1-Output sampled on even clock edge, 0-Output sampled on odd clock edge.

**CPOL->** 1- n idle state, SClk is high , 0-In idle state, SClk is low .

**spe->** 1-SPI master enabled, 0-SPI master disabled (low power mode).

**SPISWAI->** 1-Txc interrupt from SPICR is enabled , 0-Txc interrupt from SPICR is disabled.

**SPTIE->** 1-SPTEF interrupt from SPICR is enabled , 0-SPTEF interrupt from SPICR is disabled.

**SPI Status Register**

**SPE->** 1-SPI controller enabled, 0- SPI controller disabled.

**Txc->** 1-Data transmission from master to slave completed , 0-Send not completed yet.

**SPTEF->** 1-Data register is empty, 0-Data register is not empty.

## Protocol operation

The pin configuration as follows  to perform read write operation,

Step1: For setup state

Psel=1'b1;

Pwrite=1'b1;

Penable=1'b0;

Step2: For write data state

Psel=1'b1;

Pwrite=1'b1;

Penable=1'b1;

Note: if pwrite pin is zero there is no transaction take place , so fsm changes it state to complete state,

For stimulus block first use step1 configuration with some delay provide step2 configuration,

**Pin Description**

| NET | Type | Port Number |
|---|---|---|
| PCLK | Input | E3(CLK100MHZ) |
| PRESETn | Input | N17(IO_41) |
| PSEL | Input | M16(IO_9) |
| PWRITE | Input | V17(IO_10) |
| PENABLE | Input | U18(IO_11) |
| PADDR[2] | Input | C10(sw[2]) |
| PADDR[1] | Input | C11(sw[1]) |
| PADDR[0] | Input | A8(sw[0]) |
| PWDATA[7] | Input | T16(IO_7) |
| PWDATA[6] | Input | T15(IO_6) |
| PWDATA[5] | Input | T14(IO_5) |
| PWDATA[4] | Input | R12(IO_4) |
| PWDATA[3] | Input | T11(IO_3) |
| PWDATA[2] | Input | P14(IO_2) |
| PWDATA[1] | Input | U16(IO_1) |
| PWDATA[0] | Input | V15(IO_0) |
| miso | Input | N15(IO_8) |
| PRDATA[7] | Output | G6(led0_r) |
| PRDATA[6] | Output | F6(led0_g) |
| PRDATA[5] | Output | E1(led0_b) |
| PRDATA[4] | Output | G3(led1_r) |
| PRDATA[3] | Output | J4(led1_g) |
| PRDATA[2] | Output | G4(led1_b) |
| PRDATA[1] | Output | J3(led2_r) |
| PRDATA[0] | Output | J2(led2_g) |
| ss1 | Output | J5(led2_b) |
| ss2 | Output | T18(IO_38) |
| mosi | Output | R18(IO_39) |
| Sclk | Output | P18(IO_14) |
| pready | Output | T9(led[2]) |

## Protocol power analysis

Spi protocol is analyzed using Xilinx ise 14.7,

| Supply Power (W) | Total | Dynamic | Quiescent |
|---|---|---|---|
| | 0.092 | 0.004 | 0.088 |

| Thermal Properties | Effective TJA (C/W) | Max Ambient (C) | Junction Temp (C) |
|---|---|---|---|
| | 4.6 | 84.6 | 25.4 |

| Supply Summary | | Total | Dynamic | Quiescent |
|---|---|---|---|---|
| Source | Voltage | Current (A) | Current (A) | Current (A) |
| Vccint | 1.000 | 0.018 | 0.001 | 0.017 |
| Vccaux | 1.800 | 0.013 | 0.000 | 0.013 |
| Vcco33 | 3.300 | 0.005 | 0.001 | 0.004 |
| Vccbram | 1.000 | 0.000 | 0.000 | 0.000 |
| Vccadc | 1.710 | 0.020 | 0.000 | 0.020 |

| On-Chip | Power (W) | Used | Available | Utilization (%) |
|---|---|---|---|---|
| Clocks | 0.001 | 2 | --- | --- |
| Logic | 0.000 | 110 | 63400 | 0 |
| Signals | 0.000 | 167 | --- | --- |
| IOs | 0.003 | 30 | 210 | 14 |
| Leakage | 0.088 | | | |
| Total | 0.092 | | | |

| Environment | |
|---|---|
| Ambient Temp (C) | 25.0 |
| Use custom TJA? | No |
| Custom TJA (C/W) | NA |
| Airflow (LFM) | 250 |
| Heat Sink | Medium Profile |
| Custom TSA (C/W) | NA |
| Board Selection | Medium (10"x10") |
| # of Board Layers | 12 to 15 |
| Custom TJB (C/W) | NA |
| Board Temperature (C) | NA |

## Resource utilization

| Slice Logic Utilization | Used | Available | Utilization | Note(s) |
|---|---|---|---|---|
| Number of Slice Registers | 101 | 126,800 | 1% | |
| Number used as Flip Flops | 101 | | | |
| Number used as Latches | 0 | | | |
| Number used as Latch-thrus | 0 | | | |
| Number used as AND/OR logics | 0 | | | |
| Number of Slice LUTs | 110 | 63,400 | 1% | |
| Number used as logic | 105 | 63,400 | 1% | |
| Number using O6 output only | 89 | | | |
| Number using O5 output only | 0 | | | |
| Number using O5 and O6 | 16 | | | |
| Number used as ROM | 0 | | | |
| Number used as Memory | 0 | 19,000 | 0% | |
| Number used exclusively as route-thrus | 5 | | | |
| Number with same-slice register load | 5 | | | |
| Number with same-slice carry load | 0 | | | |
| Number with other load | 0 | | | |
| Number of occupied Slices | 51 | 15,850 | 1% | |
| Number of LUT Flip Flop pairs used | 130 | | | |
| Number with an unused Flip Flop | 43 | 130 | 33% | |
| Number with an unused LUT | 20 | 130 | 15% | |
| Number of fully used LUT-FF pairs | 67 | 130 | 51% | |
| Number of unique control sets | 14 | | | |
| Number of slice register sites lost to control set restrictions | 51 | 126,800 | 1% | |
| Number of bonded IOBs | 30 | 210 | 14% | |
| Number of LOCed IOBs | 30 | 30 | 100% | |
| Number of RAMB36E1/FIFO36E1s | 0 | 135 | 0% | |
| Number of RAMB18E1/FIFO18E1s | 0 | 270 | 0% | |
| Number of BUFG/BUFGCTRLs | 2 | 32 | 6% | |
| Number used as BUFGs | 2 | | | |
| Number used as BUFGCTRLs | 0 | | | |
| Number of IDELAYE2/IDELAYE2_FINEDELAYs | 0 | 300 | 0% | |
| Number of ILOGICE2/ILOGICE3/ISERDESE2s | 0 | 300 | 0% | |

## Time constraint

Here the 30mhz PCLK clock are provided, and clock divider is frequency 0.5(1/2) of PCLk ,

| | Constraint | Paths | Failing Paths | Endpoints | Setup Errors | Hold Errors |
|---|---|---|---|---|---|---|
| 1 | TS_clkdivider_clk = PERIOD TIMEGRP "clkdivider/clk" 15 MHz HIGH 50%; | 595 | 0 | 269 | 0 | 0 |
| 2 | TS_PCLK = PERIOD TIMEGRP "PCLK" 30 MHz HIGH 50%; | 88 | 0 | 74 | 0 | 0 |

## Tested board

Spi protocol tested using artix-7 board with following chip device

| Device | |
|---|---|
| Family | Artix7 |
| Part | xc7a100t |
| Package | csg324 |
| Temp Grade | Commercial |
| Process | Typical |
| Speed Grade | -3 |

## Output