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High-Speed IO Buffer Modeling with IBIS-AMI

FTF-NET-F0097

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Overview

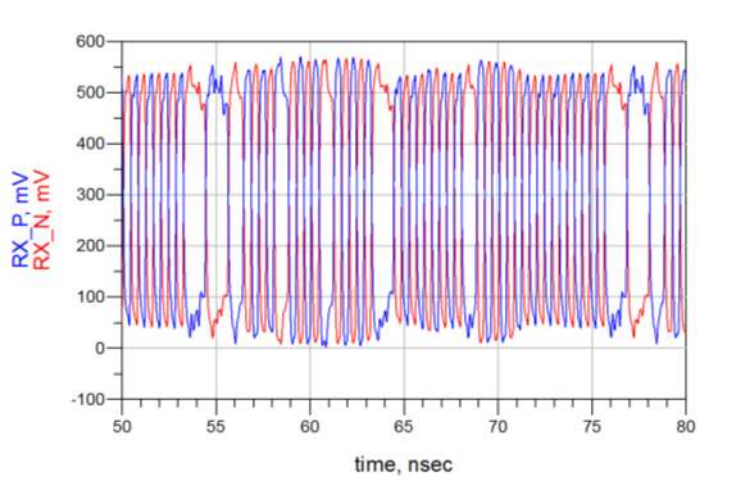
- High-speed SERDES devices operate at bus speeds and edge rates in which discontinuities and interconnect materials can greatly affect their signals.
- Multiple SERDES protocols have developed means to overcome or diminish the adverse effects of the interconnect on their signals.
- The transmitter (TX) and receiver (RX) designs have included circuitry to offset the degradation seen in the interconnect path for the signal, which is also known as the SERDES channel.
- This presentation will review the first generation IBIS-AMI model (TX and RX) and the second generation IBIS-AMI model (TX only for today).

Agenda

- IBIS-AMI Overview
- Freescale IBIS-AMI Model Overview
- Printed Circuit Board (PCB) and System Level Interconnect Attributes
- IBIS-AMI Model Simulation Results
- Summary

High-Speed Serial Channel Analysis

- Bit Period is small
  - 2.5 Gbps = 400 ps
  - 5 Gbps = 200 ps
  - 6.25 Gbps = 160 ps
  - 8 Gbps = 125 ps
  - 10 Gbps = 100 ps
  - 10.3125 Gbps = 96.9 ps
    - (DDR signal edge rate 100 ps; TDR 20 ps)



- Simulate with many bits into the channel
  - Long random data patterns needed to predict channel behavior
    - Need simulation speed

- Higher speed Serializer/Deserializer (SERDES) Devices
  - Use techniques to improve signaling through channel
  - Transmitter (TX) uses equalization, de-emphasis
  - Receiver (RX) uses equalization, like FFE, DFE, CTLE
    - Often proprietary designs

High-Speed SERDES Simulation Challenges

- TX and RX often use proprietary designs
  - Not open source
  - May require multiple tool flows, even for internal solutions
  - RX EQ not easily modeled in standard IBIS
  - RX EQ possibly not easily modeled in SPICE
  - Need to protect Intellectual Property (IP)

- SPICE solutions
  - May not work with other vendors' SPICE solutions
  - May take a long time to simulate many bits

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IBIS AMI Background

IBIS 5.0 – IBIS-AMI Introduced

- IBIS
  - IO Buffer Interface Specification (IBIS)
  - IBIS Specification 1.0: April 1993
    - Used extensively for PCI bus modeling
  - Subsequent key versions:
    - 2.1: December 1995
    - 3.2: September 1999
    - 5.0: August 2008
    - 5.1 Being reviewed now; substantial addition of resolution documents

- IBIS-AMI
  - IBIS 5.0 Release in 2008 added IBIS-AMI
  - IBIS Algorithmic Modeling Interface (AMI)
  - Expands IBIS Standard to include methods to model the algorithmic content in the SERDES TX and RX circuits
    - Used especially for RX EQ

IBIS vs. IBIS-AMI topology

IO Buffer (IBIS)

IO Buffer (IBIS)

Standard IBIS for two tap TX EQ or IBIS-AMI or misc models

IBIS-AMI or misc models

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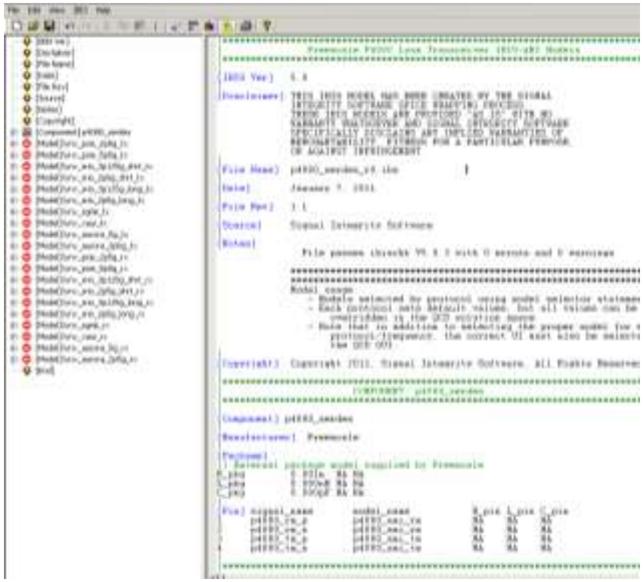
IBIS-AMI Model Sections

- IBIS-AMI model
  - Top Level is ".ibs" file, like standard IBIS
    - Has pin listing, signal to model name mapping, diff pair listing, etc.
    - Uses standard analog modeling for driver impedance, capacitive loading, edge rates, etc.
  - Parameter file – ".ami" file
    - Text file that is readable by user
    - Sets values to be used in DLL model file
  - DLL
    - Where algorithms are modeled in AMI language
    - Compiled to protect the proprietary TX and RX model information
    - IBIS 5.0 compliant allows it to run in multiple tools

IBIS-AMI Example Data

- View of ".ibs", ".ami" and DLL/SO file listing



.ibs file header

.ami file listing

Name	Size	Type
Freescale_Lynx_Rx.dll	144 KB	Application Extension
Freescale_Lynx_Rx.linux.so	66 KB	SO File
Freescale_Lynx_Tx.dll	112 KB	Application Extension
Freescale_Lynx_Tx.linux.so	44 KB	SO File

DLL/SO files

IBIS AMI Background

IBIS AMI EDA:

www.eda.org/pub/ibis/macromodel_wip/

Sigrity:

www.sigrity.com/products/systemsi/systemsi.htm

Mentor:

http://www.mentor.com/products/pcb-system-design/

Agilent: (see ADS, EEsof)

www.home.agilent.com/agilent/

Cadence: (see PCB, Signal/Power Integrity)

www.cadence.com/products/pcb/Pages/default.aspx

Ansoft/Ansys:

http://www.ansoft.com/products/si/designersi/

Synopsys HSPICE:

http://www.synopsys.com/Tools/Verification/AMSVerification/CircuitSimulation/HSPICE/Pages/HSPICE-ds.aspx

SiSoft IBIS AMI:

www.sisoft.com/services/ibis-model-generation.html

WHAT ARE IBIS-AMI MODELS?

IBIS-AMI models are behavioral models that support "plug and play" simulation of SerDes behavior using commercial EDA tools. They run much faster than traditional SPICE models (up to 1 million bits/minute), allowing designers to explore a much wider range of design variables. IBIS-AMI models provide speed and accuracy comparable to semiconductor in-house simulators and provide the ability to run simulations with devices from different vendors that proprietary simulators lack.

The IBIS-AMI specification enables standardized, high-performance SerDes models that meet the following goals:

- Interoperability: different vendor models work together
- Portability: one model runs in multiple simulators
- Flexibility: support Statistical / Time-Domain simulation
- High Performance: 1 million bits per CPU per minute
- Accurate: excellent correlation to measured data

Properly written IBIS-AMI models allow users to trade off speed vs. accuracy and expose controls to users that configure FFE, CTLE and DFE settings for simulation.

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IBIS Data within IBIS-AMI Models

IBIS-AMI Models Use IBIS Data

- IBIS AMI models include electrical data from standard IBIS Data
  - DC Data (IV Curves)
  - Transient Data (Voltage vs. Time)
  - IO Buffer Loading (C_Comp)

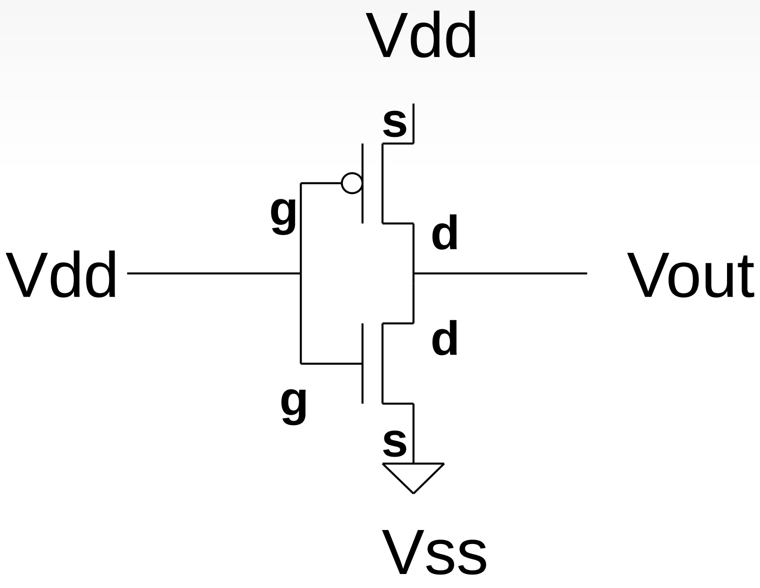
Elements of IBIS: Electrical Data to re-create IO buffer behaviorally

- DC IV data
  - Pulldown
  - Pullup
  - Ground clamp
  - Power clamp

- Transient (Voltage vs. Time) data
  - Ramp or dv/dt ratio
  - VT: rising, pulled low
  - VT: rising, pulled high
  - VT: falling, pulled low
  - VT: falling, pulled high

- Data is simulated or measured across process, voltage, temperature
  - IBIS min: worst-case drive (slow process, low voltage, high temperature)
  - IBIS typ: typical-case drive (typ process, typ voltage, typ temperature)
  - IBIS max: best-case drive (fast process, high voltage, low temperature)

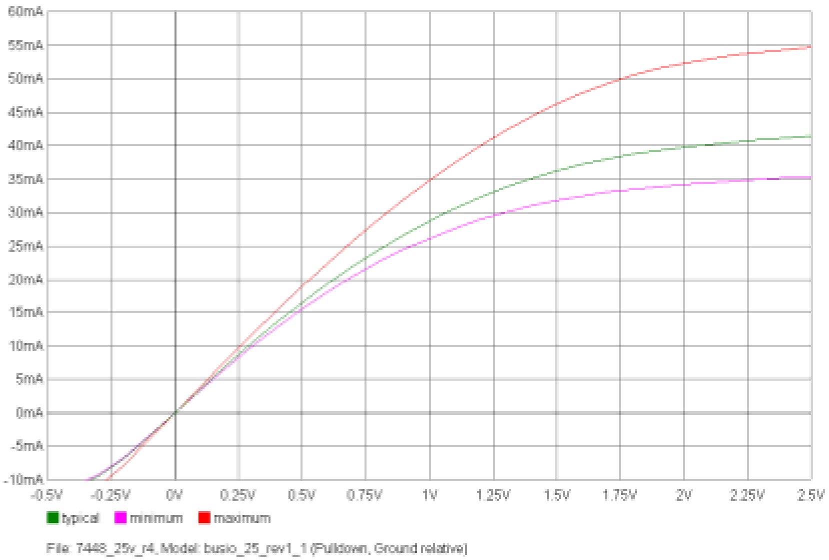
DC IV Data: Pulldown



Pulldown Extraction:

Excite Pulldown (e.g. NMOS)

Sweep I vs. –Vdd to 2Vdd



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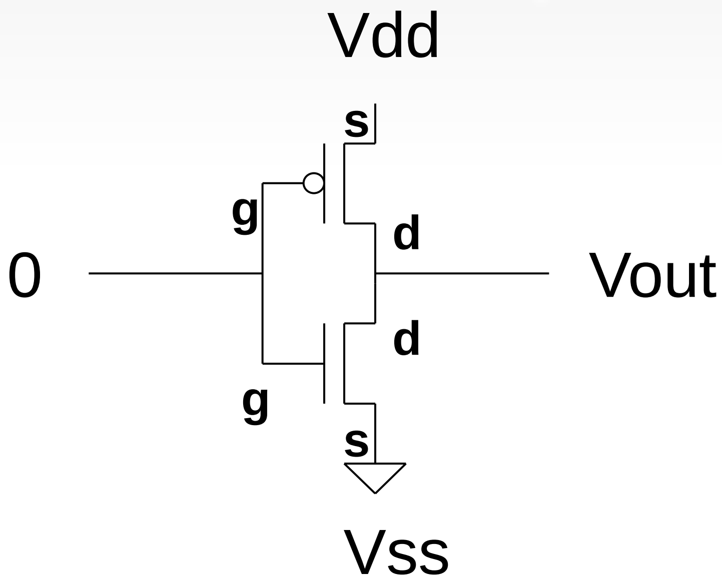
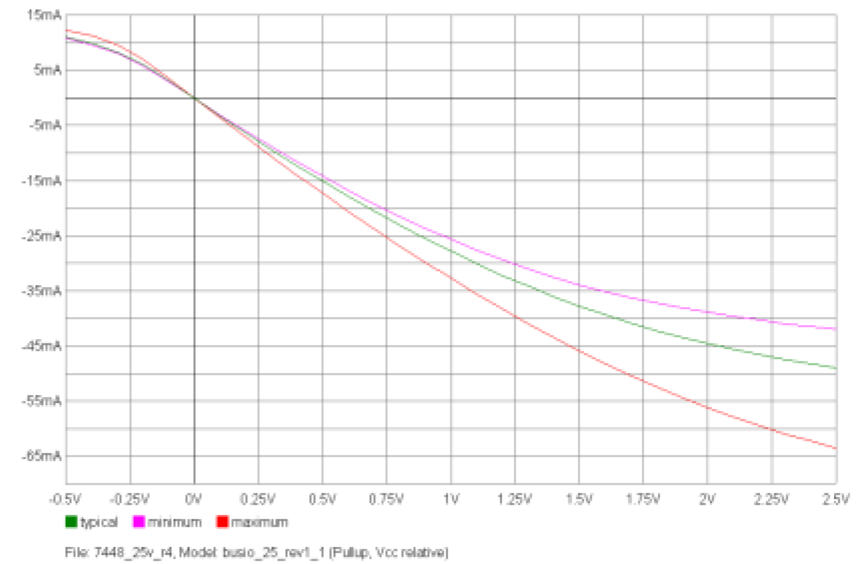
DC IV Data: Pullup



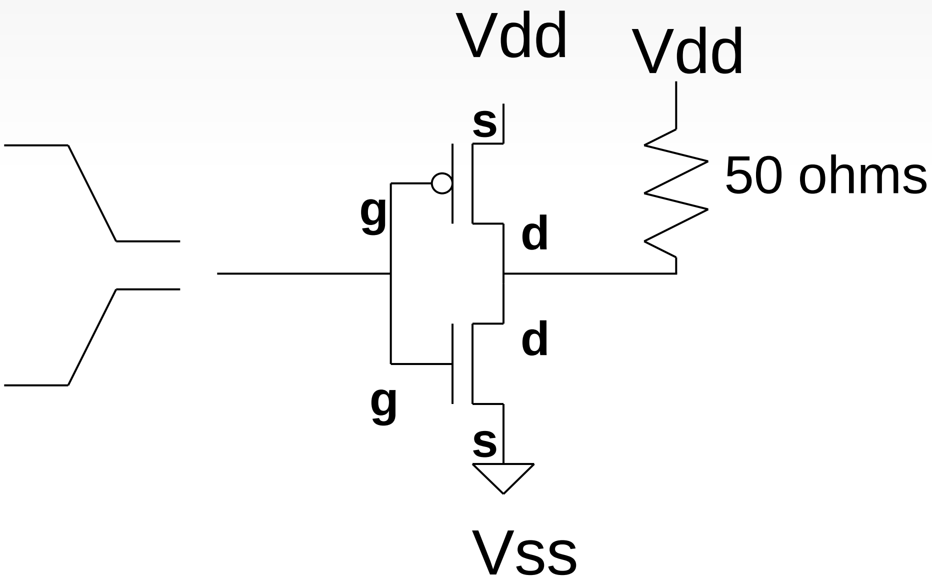
Pullup Extraction:

Excite Pullup (e.g. PMOS)

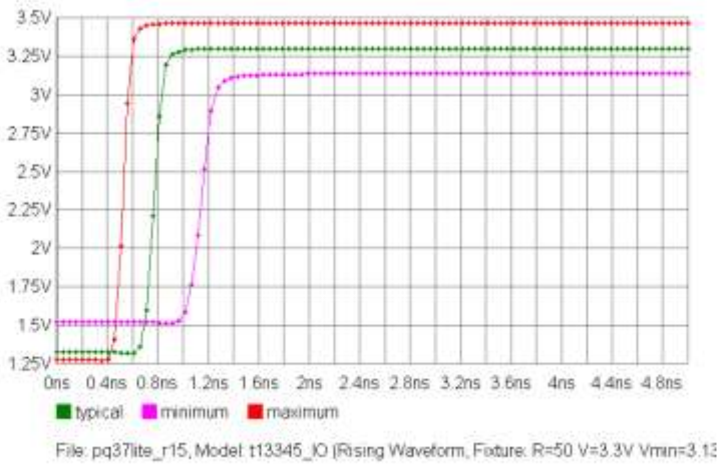
Sweep I vs. –Vdd to 2Vdd

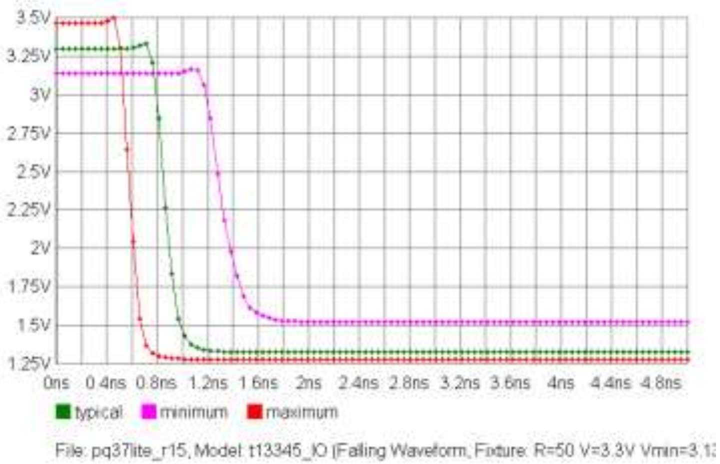


Transient Data: 50 Ohm Resistor Tied to VDD

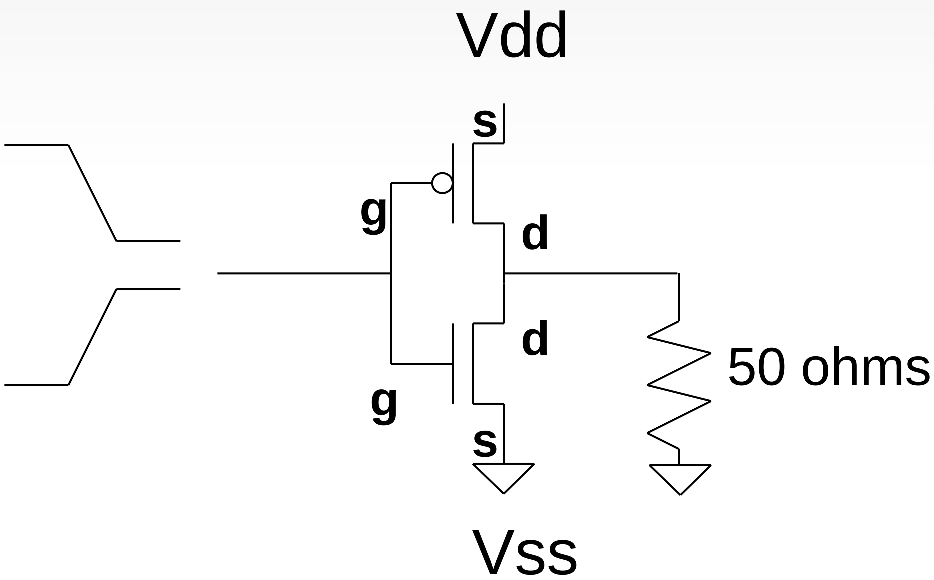


Rising and falling voltage vs. time table with 50 ohm resistive load tied high

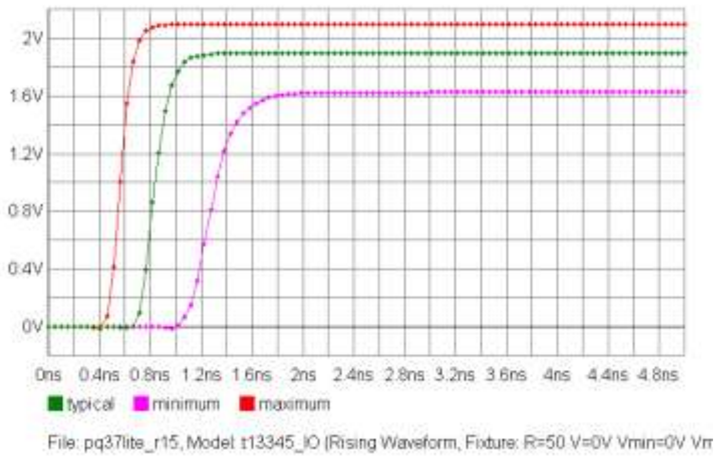


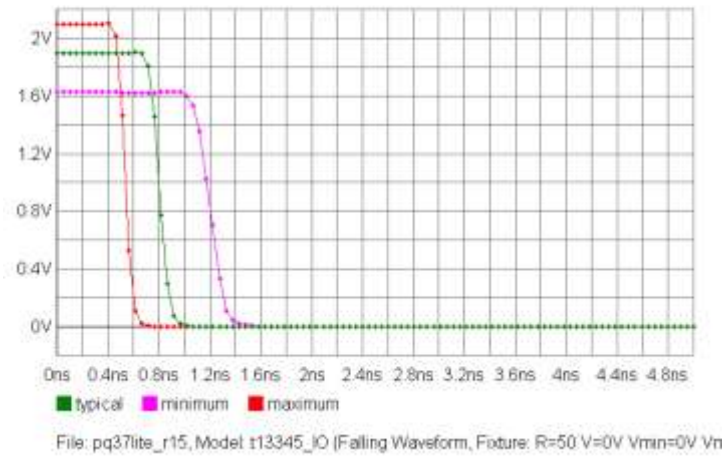


Transient Data: 50 Ohm Resistor Tied to Ground



Rising and falling voltage vs. time table with 50 ohm resistive load tied low





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IBIS ".ibs" File – Almost Same as Standard IBIS

```
[IBIS Ver] 5.0
[File Name]  sisoft_tx.ibs
[File Rev]   1.0
[Date]       8/25/2009
[Source]     Developed by: Signal Integrity Software, Inc.
[Notes]  Rev 1.0
[Component] SiSoft_Tx
[Manufacturer] SiSoft
[Package]
[Pin]    signal_name        model_name       R_pin L_pin  C_pin
1p       SiSoft_AMI_Tx      IBIS_AMI_Tx

[Model] IBIS_AMI_Tx

[Algorithmic Model]
Executable Windows_VisualStudio_32 IBIS_AMI_Tx.dll IBIS_AMI_Tx.ami
Executable linux_gcc3.2.3_32 libIBIS_AMI_Tx.so IBIS_AMI_Tx.ami
[End Algorithmic Model]
[END]
```

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IBIS ".ibs" Model File – Almost Same as Standard IBIS

[Model] IBIS_AMI_Tx

…

C_comp 0.5p 0.45p 0.55p

Cref = 0; Vref = 0.5; Rref = 50; Vmeas = 0.5

[Temperature_Range] 25 100 0

[Voltage Range] 1.0 0.9 1.1

[Pulldown]

-3.00	-0.060	-0.060	-0.060
3.00	0.060	0.060	0.060

[Pullup]

-3.00	0.060	0.060	0.060
3.00	-0.060	-0.060	-0.060

[GND Clamp]   [Power Clamp]

[Ramp] dV/dt_r .45/50p .42/55p .48/45p   dV/dt_f .45/50p .42/55p .48/45p

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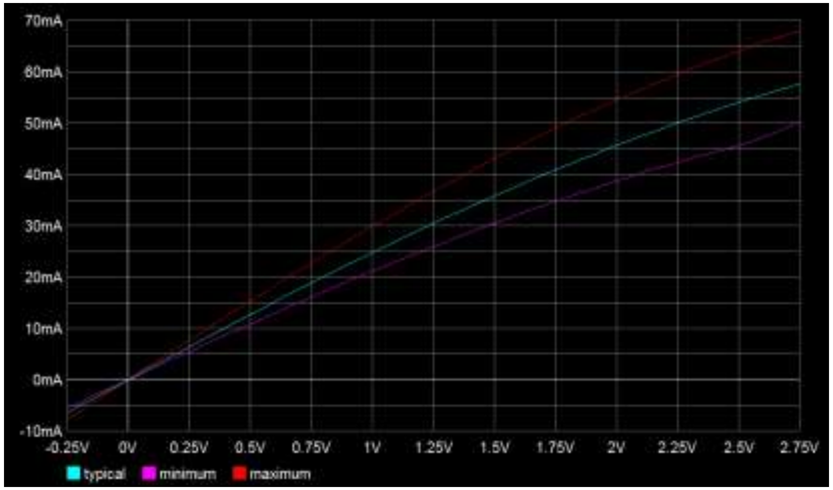
FSL IBIS-AMI: IBIS model file (.ibs)

```
[Model]    lynx_pcie_2p5g_tx
[Algorithmic Model]
Executable Windows_VisualStudio7.1.3088_32 Freescale_Lynx_Tx.dll lynx_pcie_2p5g_tx.ami
Executable Linux_gcc3.2.3_32 Freescale_Lynx_Tx.linux.so lynx_pcie_2p5g_tx.ami
[End Algorithmic Model]
|
[Temperature Range]  25   100  0
[Voltage Range]      1.0  1.0  1.0
|
[Pulldown]
-2.500 -5.00000E-02 -4.16667E-02 -6.25000E-02
0.000  +0.00000E+00 +0.00000E+00 +0.00000E+00
2.500  +5.00000E-02 +4.16667E-02 +6.25000E-02
[Pullup]
-2.500 +5.00000E-02 +4.16667E-02 +6.25000E-02
0.000  +0.00000E+00 +0.00000E+00 +0.00000E+00
2.500  -5.00000E-02 -4.16667E-02 -6.25000E-02
```

Compare Standard IBIS vs. IBIS-AMI IV Data:
LVCMOS vs. SERDES

- Standard IBIS (LVCMOS)



- IBIS-AMI (SERDES)

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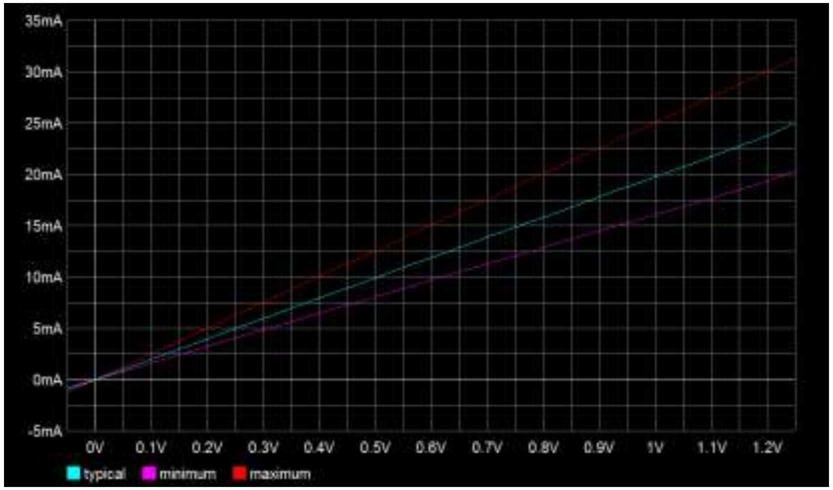
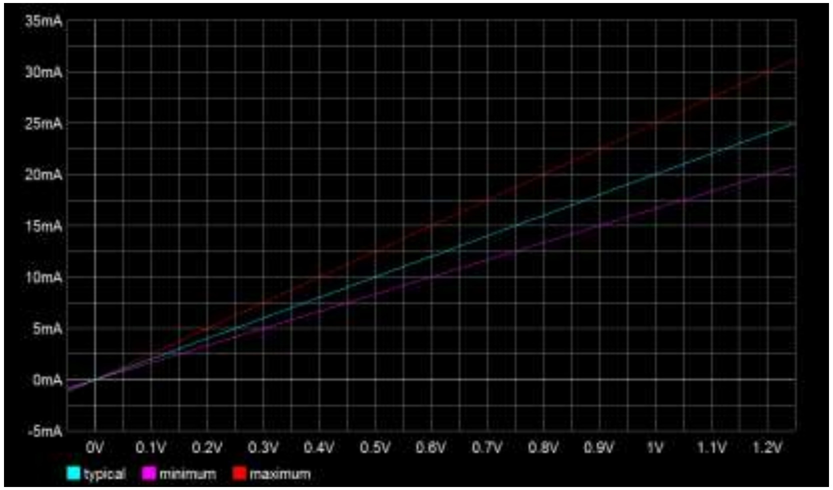
Compare Standard IBIS vs. IBIS-AMI IV Data

SERDES vs. SERDES

- Standard IBIS (SERDES)



- IBIS-AMI (SERDES)



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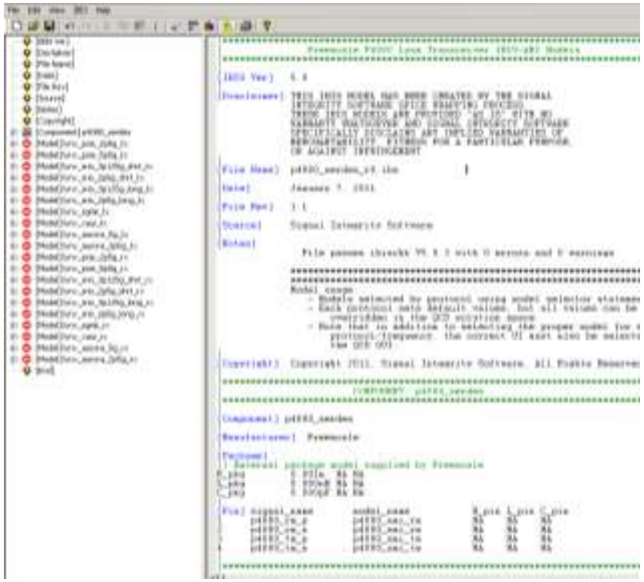
IBIS-AMI File Details

IBIS-AMI Example Data

- View of ".ibs", ".ami" and DLL/SO file listing



.ibs file header

.ami file listing

DLL/SO files

Example IBIS AMI File (Generic TX)

```
(IBIS_AMI_Tx
  (Description "Generic transmitter model published by SiSoft")
 (Reserved_Parameters …
    Ignore_Bits … Max_Init_Aggressors … Init_Returns_Impulse … GetWave_Exists … Use_Init_Output
 (Model_Specific
    (tap_filter (Description "Array of transmit de-emphasis tap weights")
      (-1 (Usage InOut)(Format Range 0.0 -1.0 1.0)(Type Tap)(Default 0)
         (Description "Pre-cursor tap weight"))
      (0  (Usage InOut)(Format Range 1.0 -1.0 1.0)(Type Tap)(Default 1)
         (Description "Main tap weight"))
      (1  (Usage InOut)(Format Range 0.0 -1.0 1.0)(Type Tap)(Default 0)
         (Description "First post-cursor tap weight"))
      (2  (Usage InOut)(Format Range 0.0 -1.0 1.0)(Type Tap)(Default 0)
         (Description "Second post-cursor tap weight"))
    ) | End tap_filter
    (tx_swing (Usage In)(Format Range 0.8 0.3 1.0)(Type Float)(Default 0.8)
           (Description "Peak differential output voltage")
    ) | End tx_swing
  ) | End Model_Specific
) | End IBIS_AMI_Tx
```

Example Requirements for TX Model

72.7.1.11 Transmitter output waveform requirements

The test pattern for the transmitter output waveform is the square wave test pattern defined in 52.9.1.2, with a run of at least eight consecutive ones. The transmitter output waveform test is based on the voltages v_1 through v_6, Δv_2, and Δv_5, which shall be measured as shown in Figure 72–12 and described below.

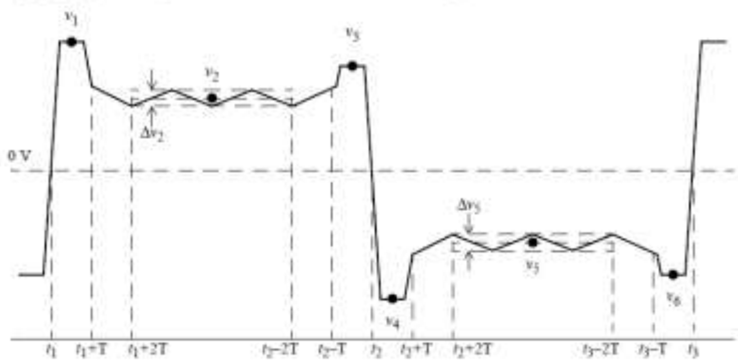


Figure 72–12—Transmitter output waveform

T	=	symbol period
t_1	=	zero-crossing point of the first rising edge of the AC-coupled signal
t_2	=	zero-crossing point of the falling edge of the AC-coupled signal
t_3	=	zero-crossing point of the second rising edge of the AC-coupled signal
v_1	=	maximum voltage measured in the interval t_1 to t_1 + T
v_2	=	positive steady-state voltage measured as the average voltage in the interval t_1 + 2T to t_2 − 2T
v_3	=	maximum voltage measured in the interval t_2 − T to t_2
v_4	=	minimum voltage measured in the interval t_2 to t_2 + T
v_5	=	negative steady-state voltage measured as the average voltage in the interval t_2 + 2T to t_3 − 2T
v_6	=	minimum voltage measured in the interval t_3 − T to t_3
Δv_2	=	positive voltage ripple measured as the peak-to-peak value of the difference between the voltage in the range t_1 + 2T to t_2 − 2T and v_2
Δv_5	=	negative voltage ripple measured as the peak-to-peak value of the difference between the voltage in the range t_2 + 2T to t_3 − 2T and v_5

SERDES RX EQ: Big Benefit for IBIS-AMI (at faster speeds)

- SERDES RX EQ may be difficult to model
  - EQ Types
    - FFE
    - DFE
    - CTLE
- Algorithmic modeling may not fit into standard IBIS or SPICE modeling techniques
- IBIS-AMI can take multiple types of input
  - C code
  - Verilog
  - MatLab
  - Internal Scripts/Code
- IBIS-AMI simulates fast as compared to most detailed SPICE models
  - **Hours/days vs 5-15 minutes**

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Freescale IBIS-AMI Model Background

FSL First Generation (5G) IBIS-AMI Model

- TX Model Includes EQ (TEQ_TYPE)
  - No Tap
  - 2-Tap
  - 3-Tap
  - 4-Tap
- TX Model Includes Amplitude Adjustment
  - Matches to protocol
- TX Model: De-emphasis levels
  - Includes standard 3.5 dB and 6 dB
  - Includes intermediate values
- RX Model: Includes Adaptive EQ

5G SERDES TX Description from Reference Manual:

Table 3-29. B1TECRA0–B1TECRJ0 Field Descriptions

Bits	Name	Description
0–1	—	Reserved
2–3	TEQ_TYPE	Selects amount/type of Transmit Equalization 00 No TX Equalization 01 2 Levels of TX Equalization (+1 postcursor) 10 3 Levels of TX Equalization (+1 precursor and +1 postcursor) 11 4 Levels of TX Equalization (+1 precursor and +2 postcursors) Recommended Settings: 01
12–15	RATIO_PST1Q	Ratio of full swing transition bit to postcursor for 2-tap equalization B1TECR(lane)0[12]: 0 Negative Sign 1 Positive Sign B1TECR(lane)0[13:15]: 000 No Equalization 001 1.09x 010 1.20x 011 1.33x 100 1.50x 101 1.71x 110 2.00x 111 Reserved Recommend Settings per protocol converter: 2.5 Gbps PCI Express 1100 5.0 Gbps PCI Express 1110 SRIO: 1011 SGMII: 1100 XGMII: 1100 Aurora: 1100
26–31	AMP_RED	Amount of amplitude reduction for all bits B1TECR(lane)0[26] = Reserved B1TECR(lane)0[27:31]: 00000 = Full Swing Vdiffpk- pk 01000 = 0. 75x Full Swing Vdiffpk- pk 01011 = 0. 68x Full Swing Vdiffpk- pk 10011 = 0. 50x Full Swing Vdiffpk- pk Recommend settings per protocol converter: PCI Express: 000000 SRIO: 000000 SGMII: 001011 XGMII: 000000 Aurora: 000000

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5G SERDES TX AMI Model Settings

```
(Freescale_Lynx_Tx
    (TEQ_TYPE    (List 0 1 2 3)(Usage In)(Type Integer)(Default 1)
            (Labels "00: No TX Equalization"
                "01: 2 level of TX Equalization"
                "10: 3 levels of TX Equalization"
                "11: 4 levels of TX Equalization")
            (Description "Transmitter Equalization type selection"))

    (AMP_RED     (Range 0 0 63)(Usage In)(Type Integer)(Default 0)
            (Description "Transmitter Output Amplitude Control:
                    00 0000 (0) =Highest output amplitude.
                    11 1111 (63) =Lowest output amplitude."))

    (RATIO_PST1Q (List -6 -5 -4 -3 -2 -1 -0 0 1 2 3 4 5 6)(Usage In)(Type Integer)(Default 6)
            (Labels "0 110, +25%: Max HF reduction" "0 101, +21%" "0 100, +17%" "0 011, +12%"
                "0 010, +8%" "0 001, +4%: Min HF reduction"
                "0 000, +0%: Off"
                "1 000, -0%: Off" "1 001, -4%: Min HF boost" "1 010, -8%" "1 011, -12%"
                "1 100, -17%" "1 101, -21%" "1 110, -25%: Max HF Boost")
            (Description "Transmitter 1st Post-Cursor Control"))
    …
```

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10G SERDES IBIS-AMI Model

- TX Model Includes EQ (TEQ_TYPE)
  - No Tap
  - 2-Tap
  - 3-Tap
  - ***4-Tap → Was in 5G, not in 10G***
- TX Model Includes Amplitude Adjustment
  - Matches to protocol
- TX Model: De-emphasis levels
  - ***Ranges from: 0 to 3x***
- RX Model: Includes Adaptive EQ
  - May have ability to communicate with TX

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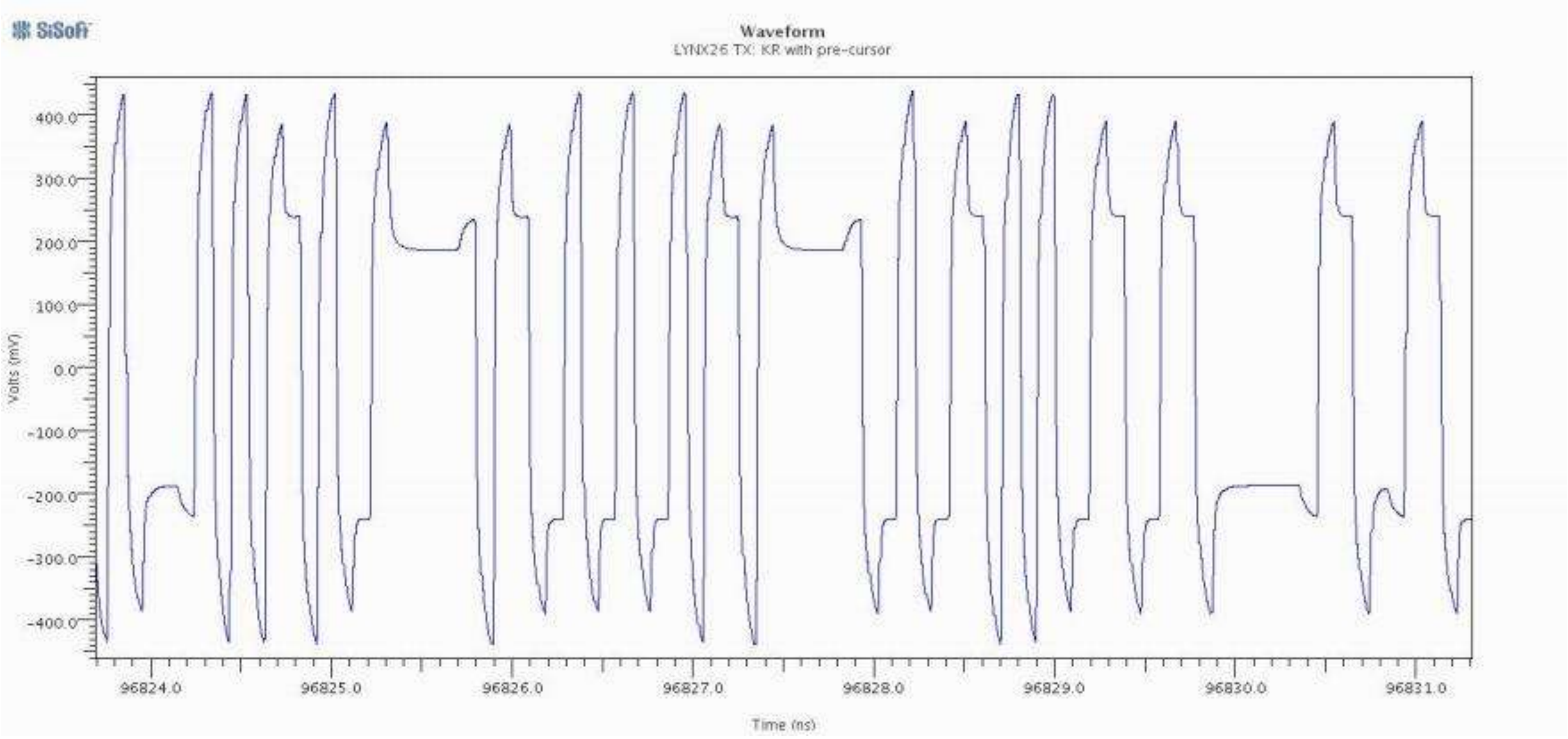
SERDES 10G TX: 3-tap EQ



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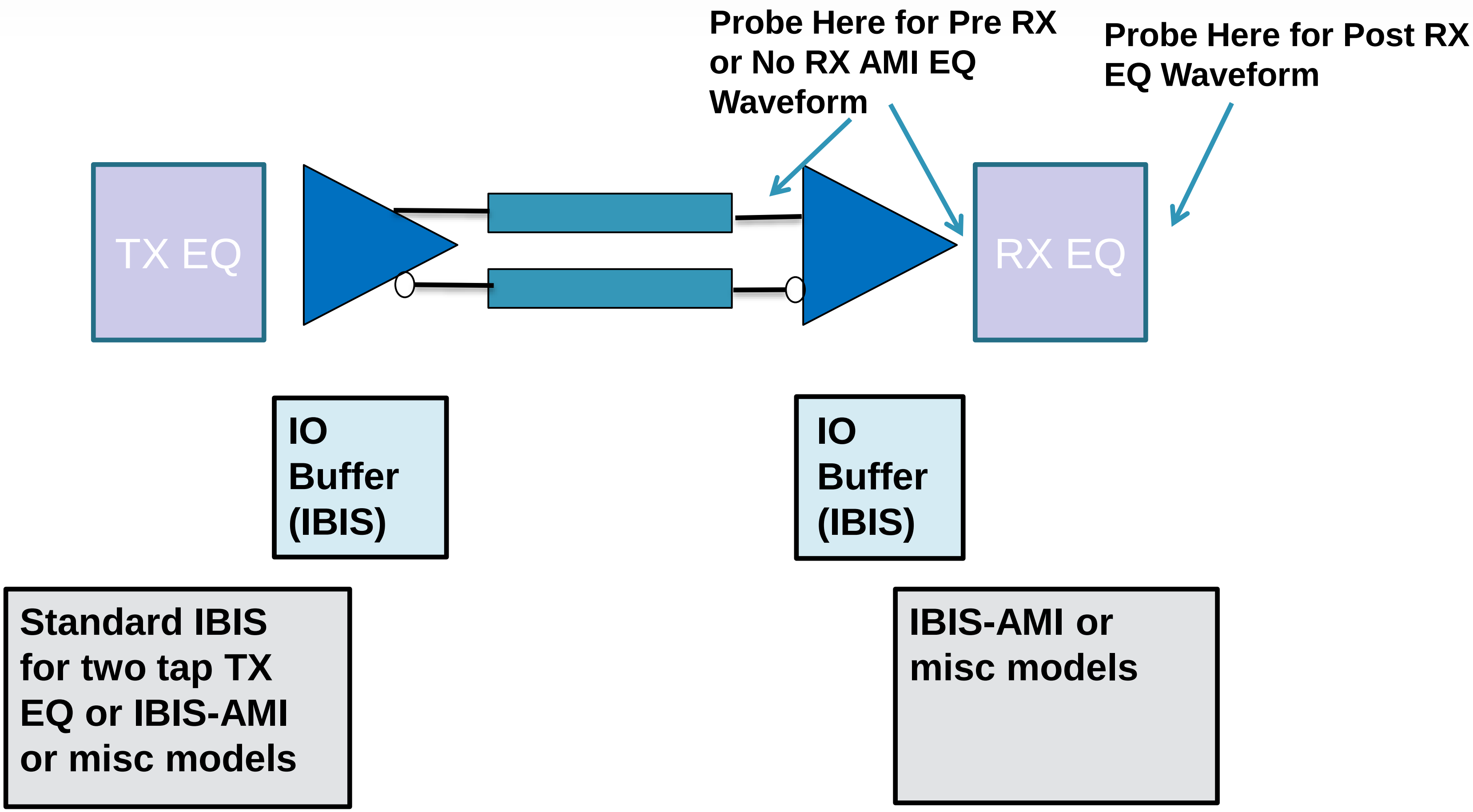
Freescale IBIS-AMI Model Running in Multiple Tools

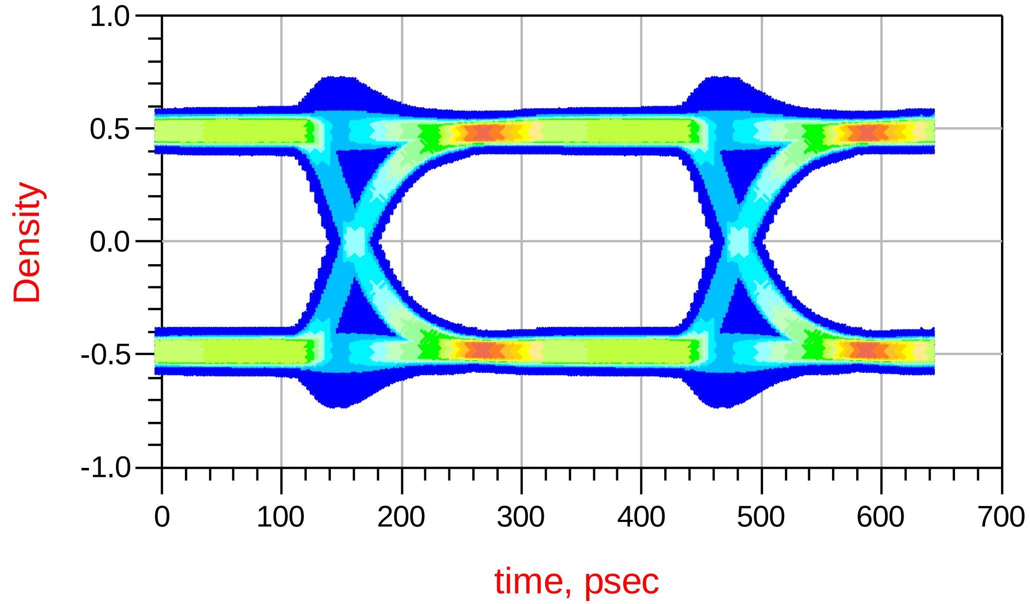
SERDES 5G IBIS-AMI Running in Multiple Tools

- SiSoft Quantum Channel Designer (QCD)
- Sigrity Channel Designer
- Agilent ADS 2011.01 and later
- Mentor Hyperlynx 8.1 and later
- Cadence PCB SI 16.5 and later
- HSPICE 2010 and later

Waveform Probing Locations

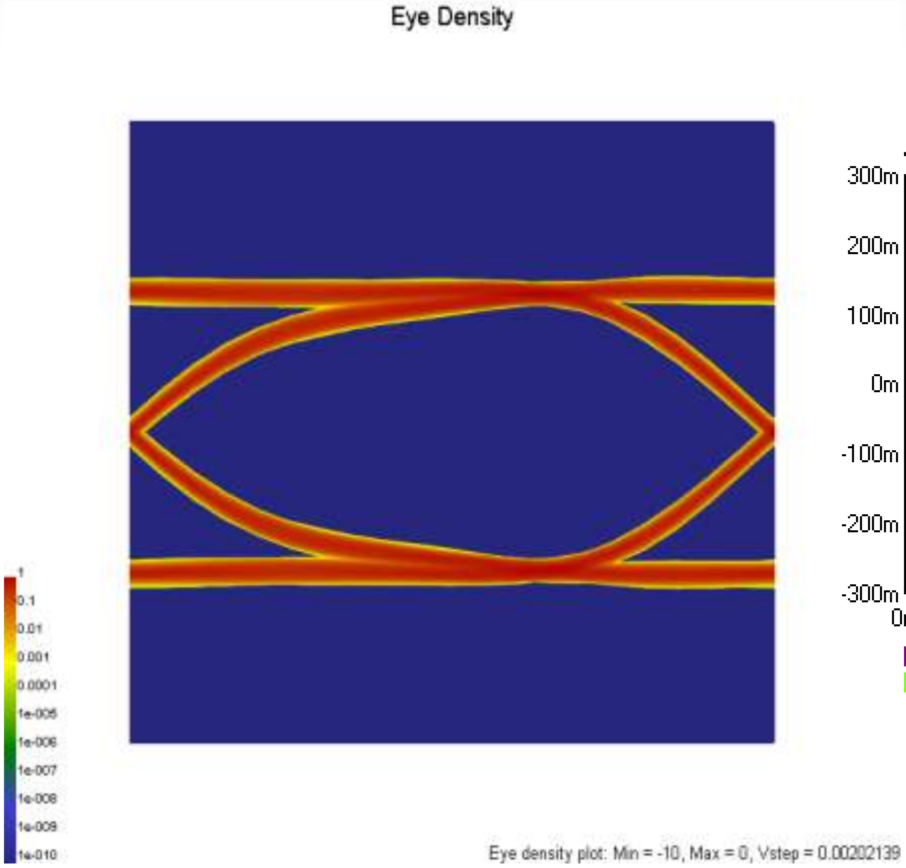


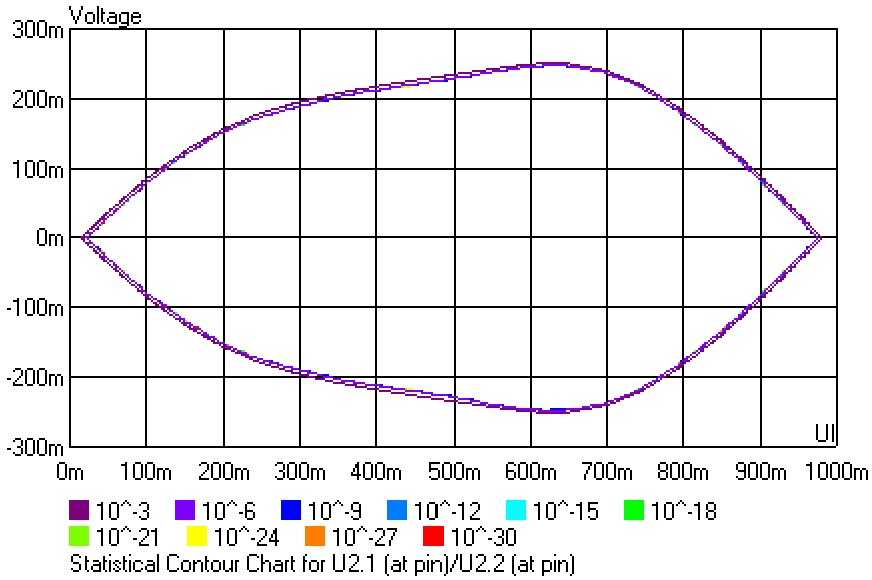
SERDES 5G IBIS-AMI Running in Agilent ADS @ 3.125 Gbps



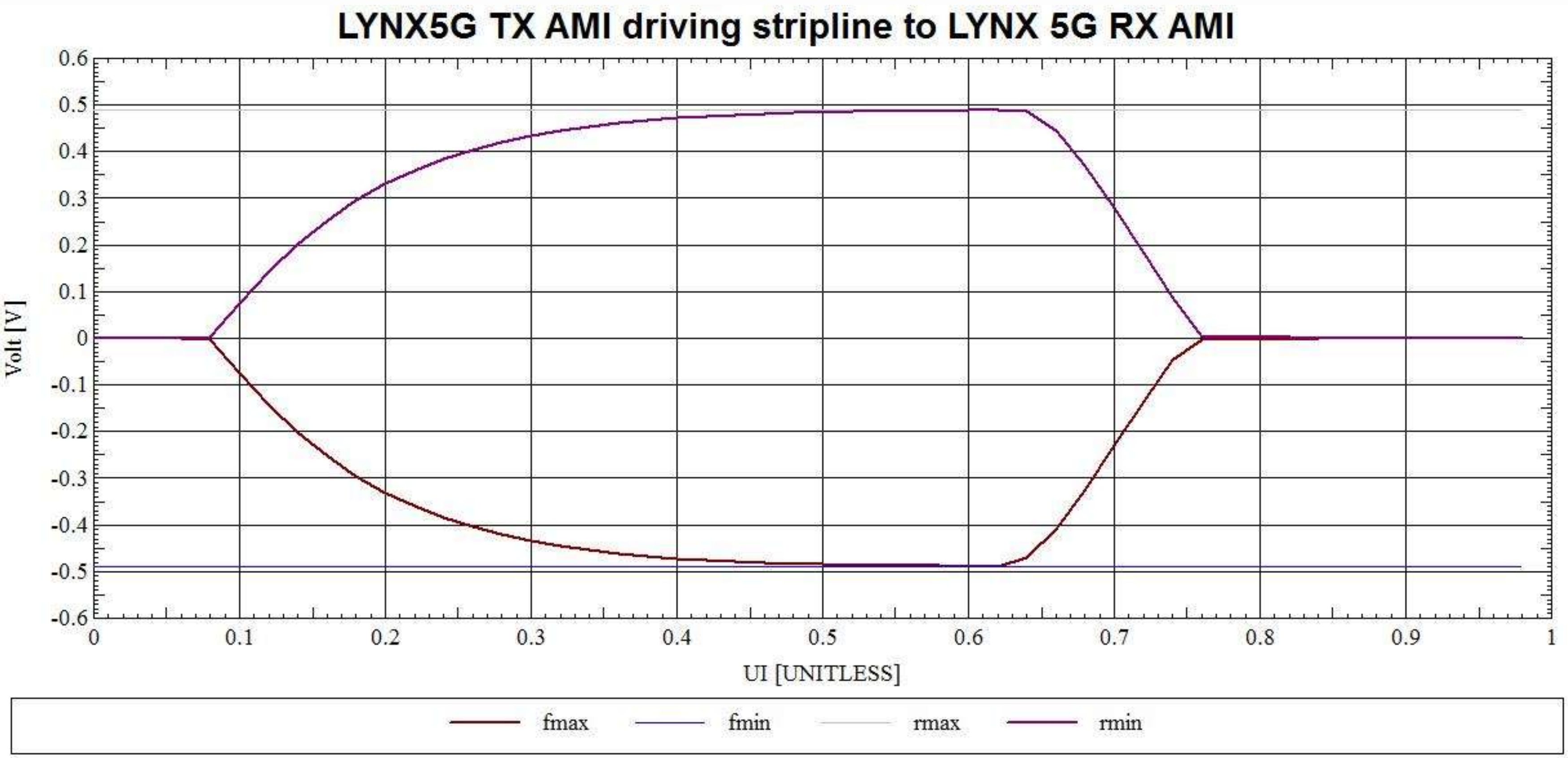
measurement	Summary
Level1	0.488
Level0	-0.487
Height	0.857
Width	2.976E-10

SERDES 5G IBIS-AMI Running in Hyperlynx 8.1

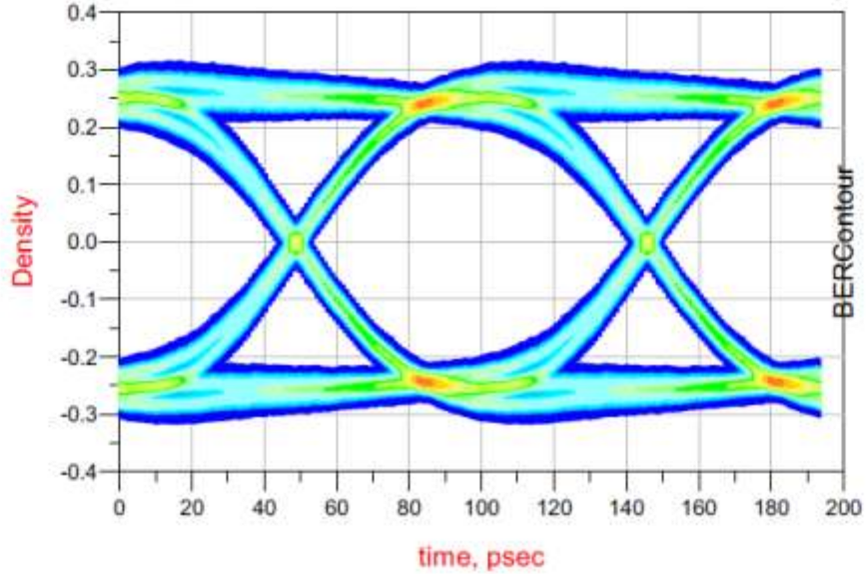


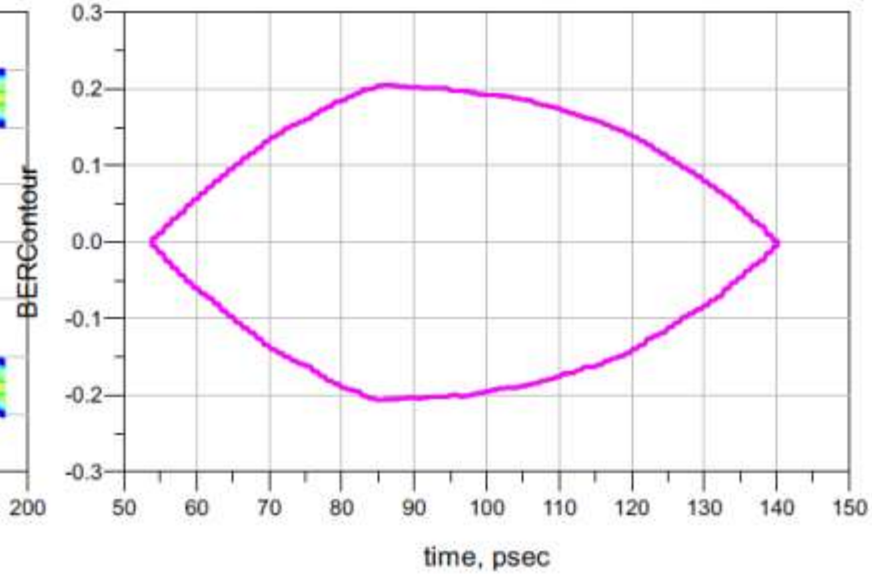


SERDES 5G Running in Cadence 16.5



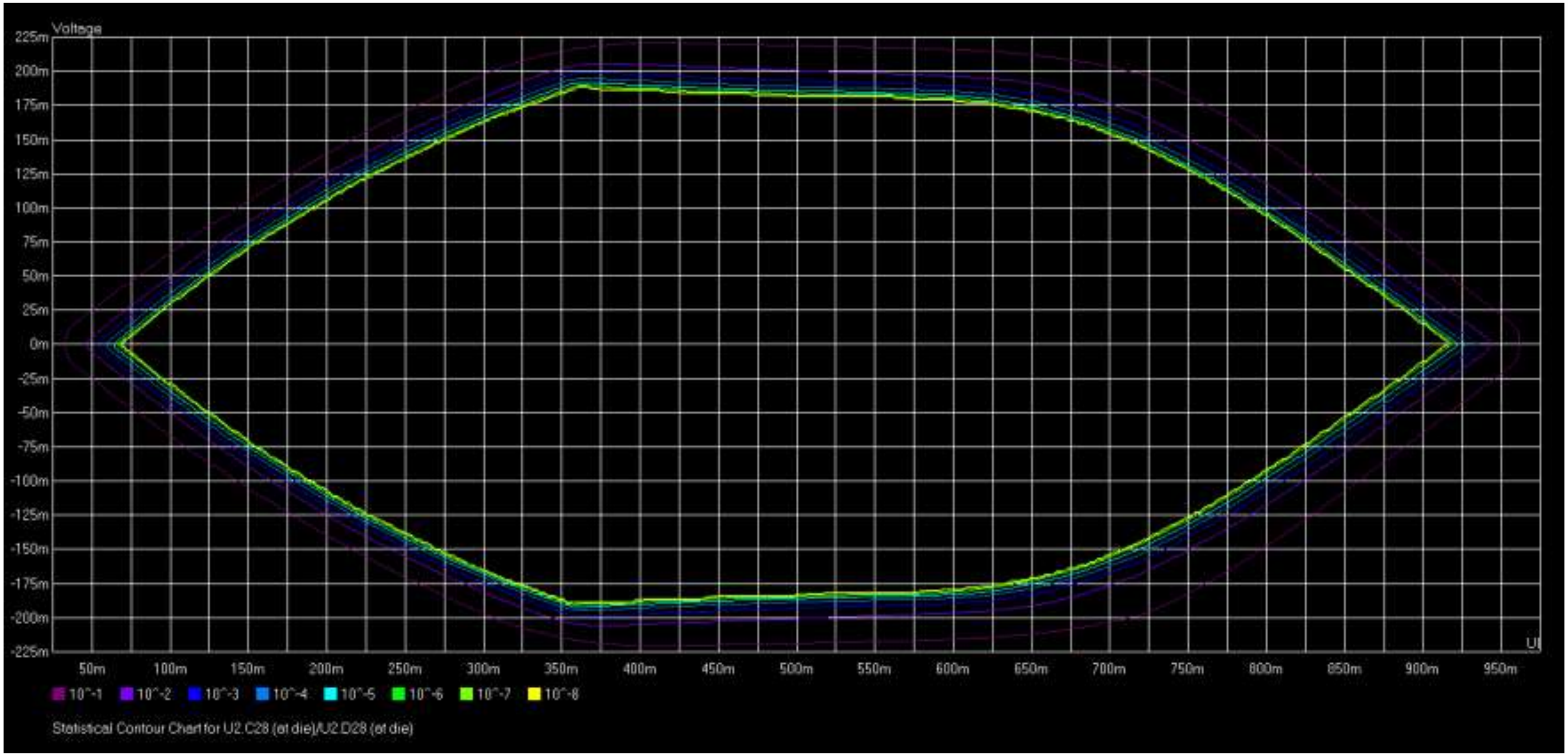
SERDES 10G TX IBIS-AMI Running in Agilent ADS



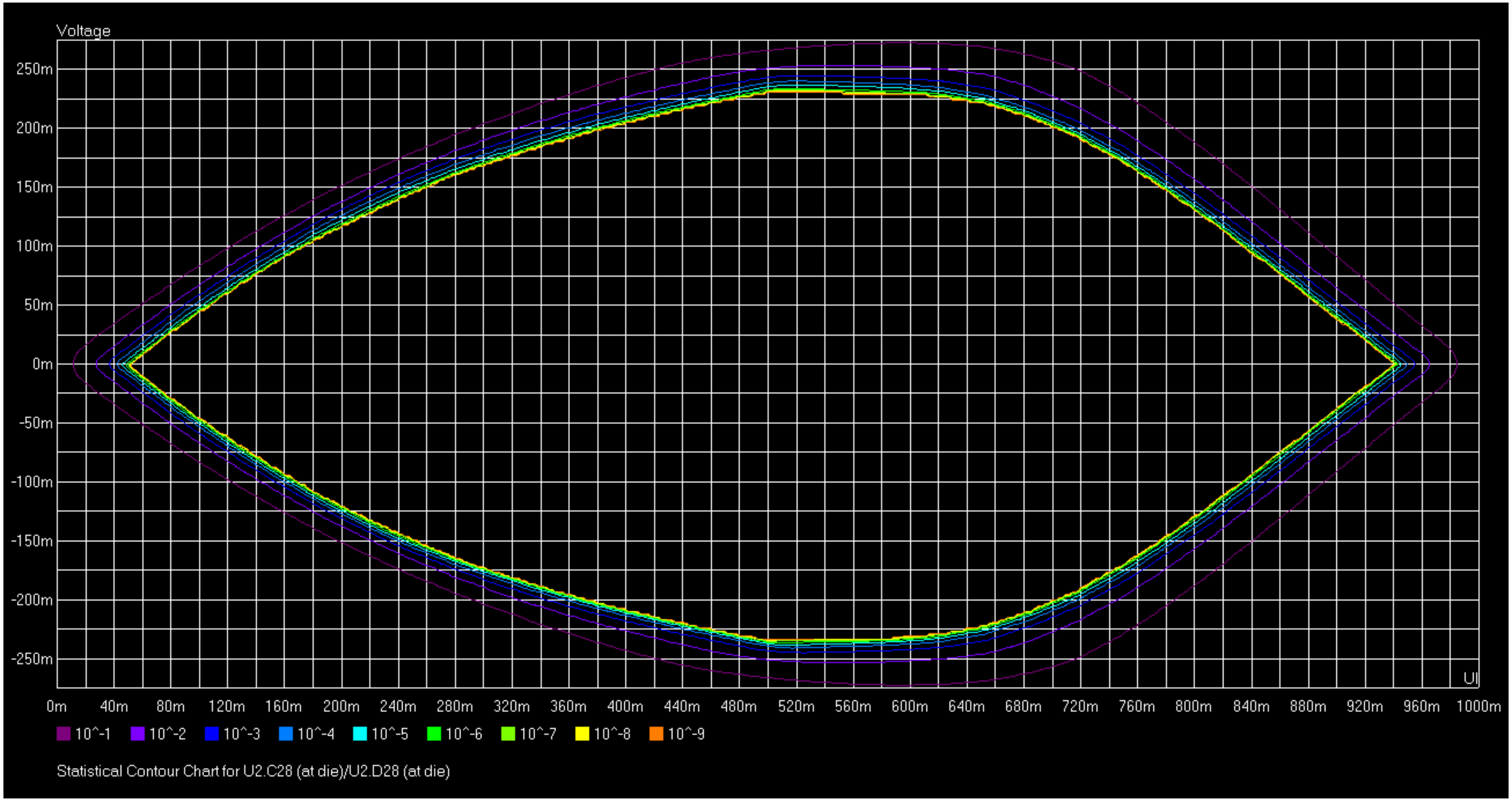


measurement	Summary
Level1	0.250
Level0	-0.252
Height	0.387
Width	8.727E-11

Hyperlynx Running TX EQ Post1Q changes



Hyperlynx Running TX EQ Post1Q changes



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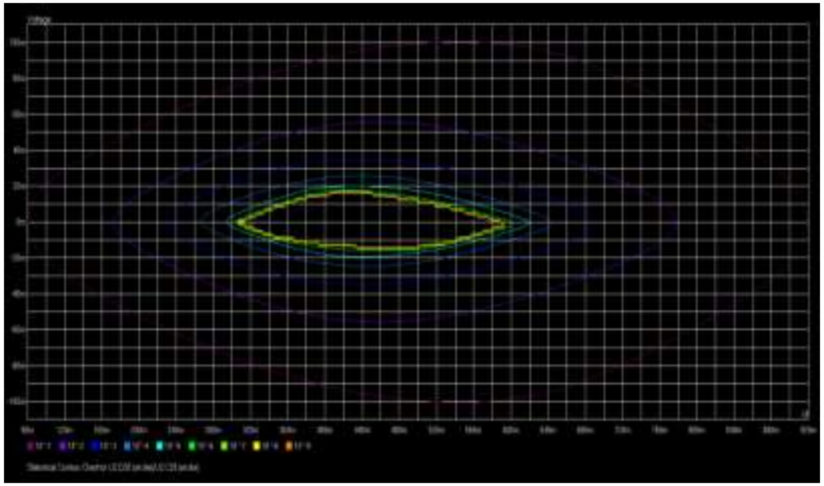
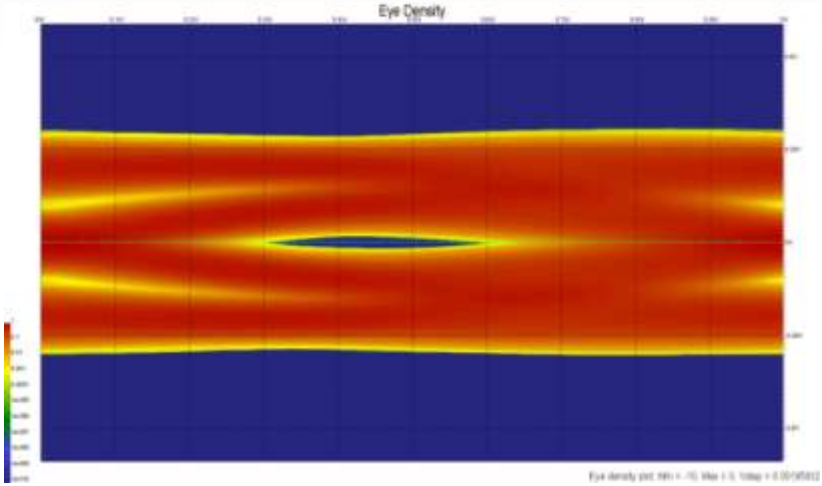
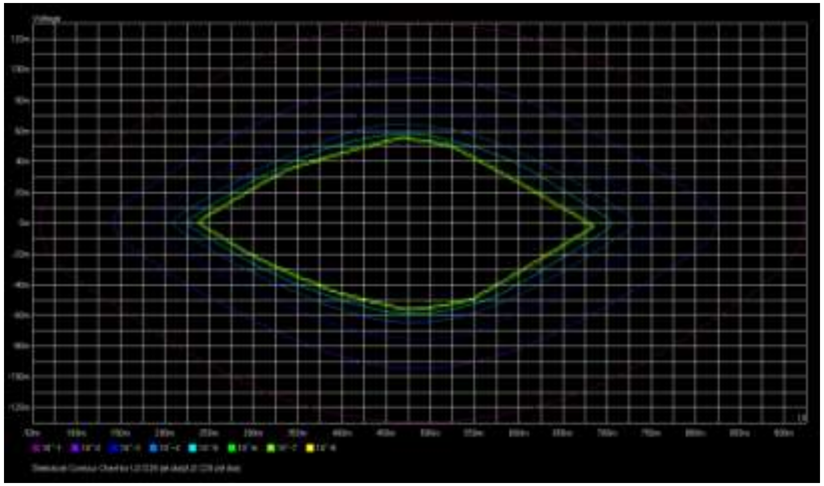
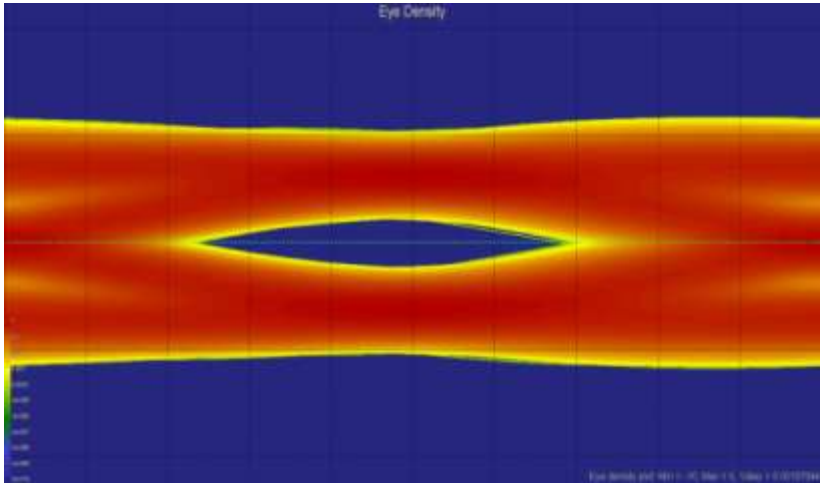
SERDES 10G TX IBIS-AMI Running in Hyperlynx 8.2

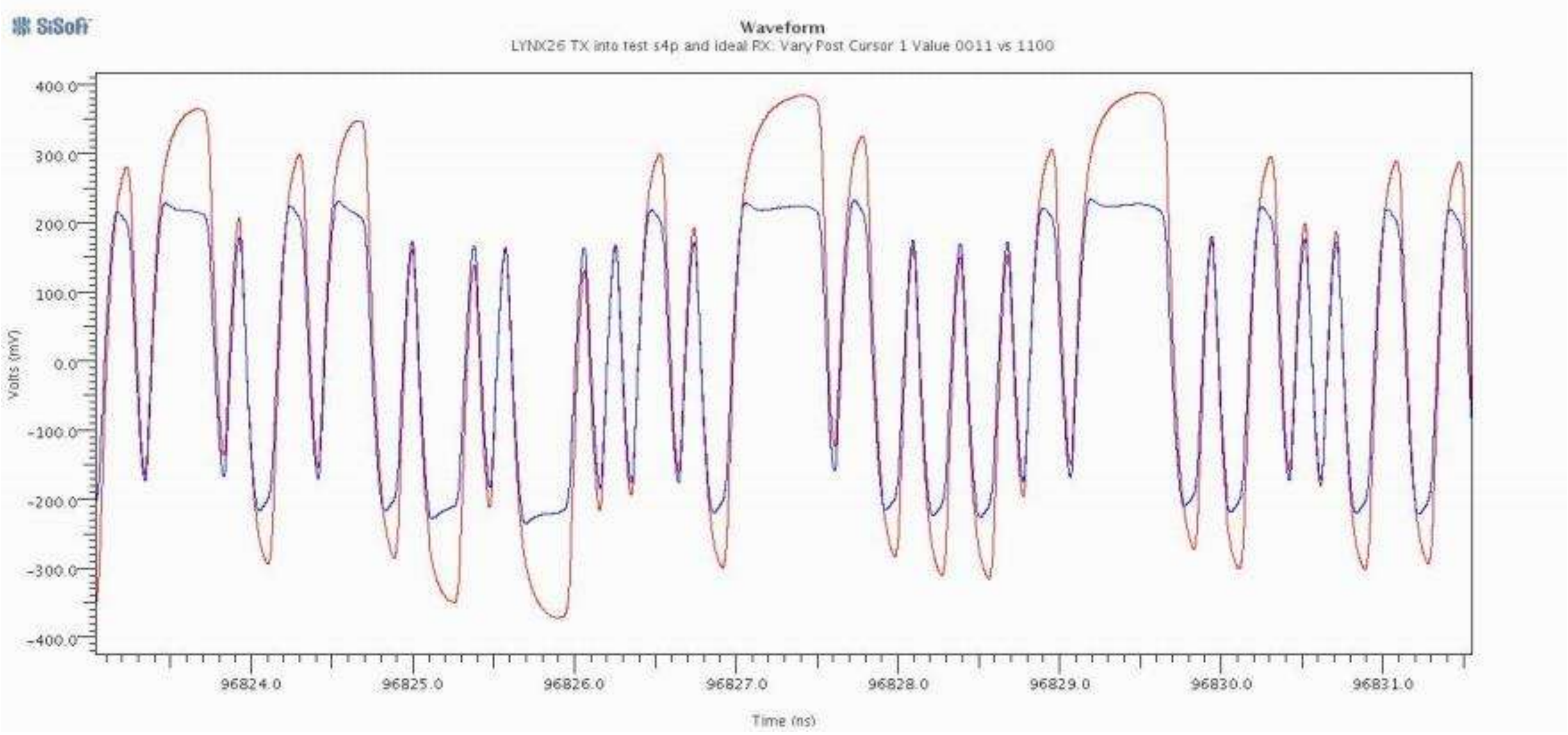




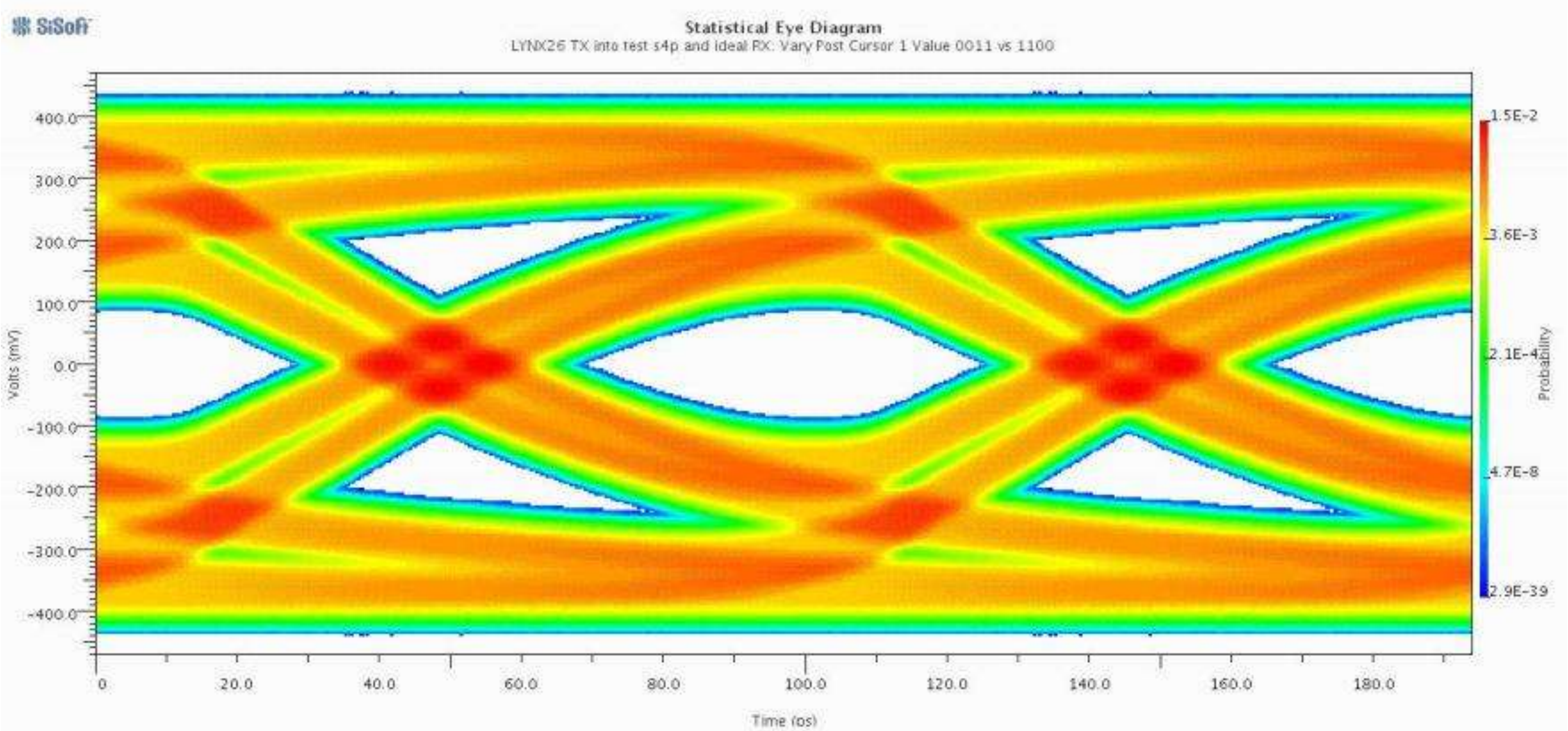




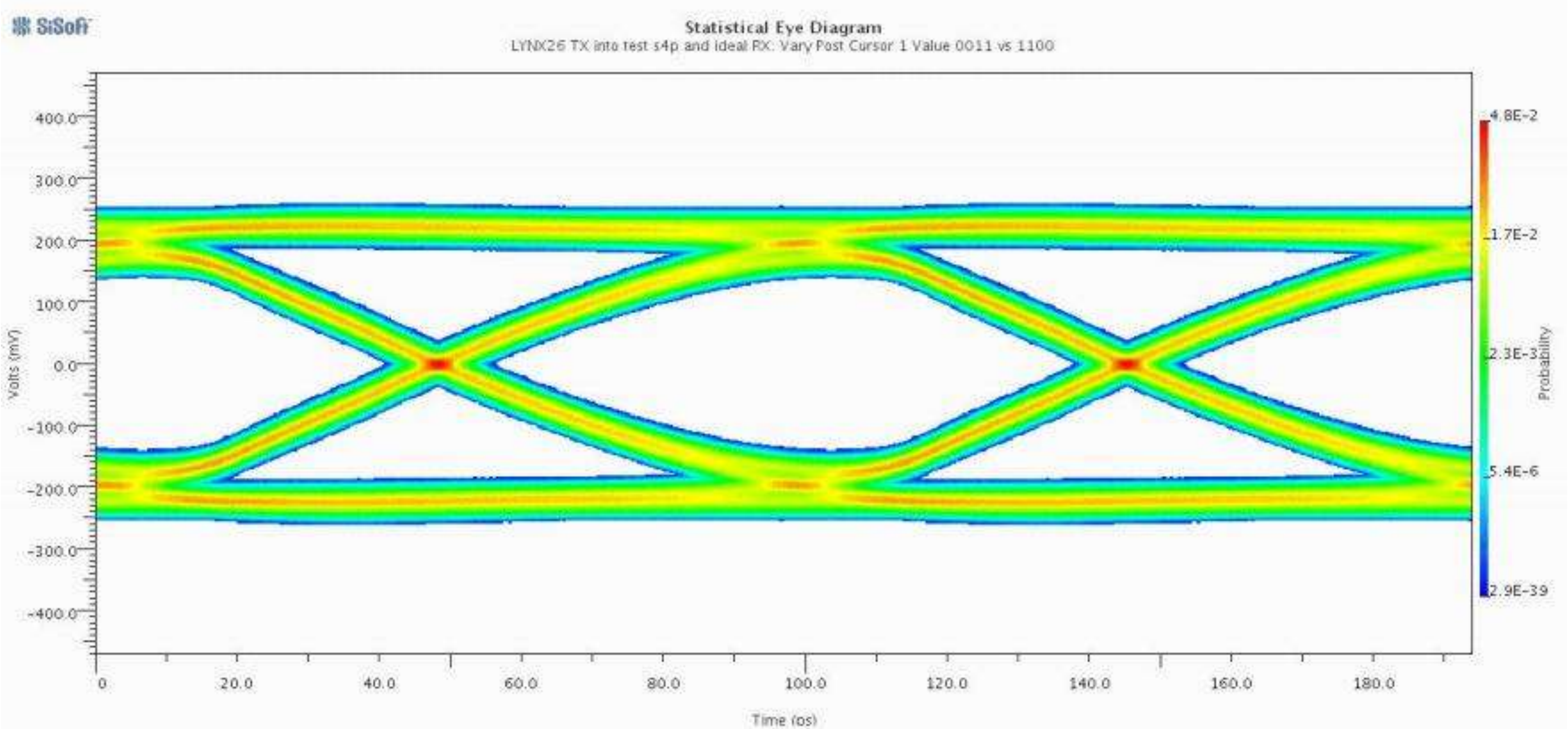
SERDES 10G TX IBIS-AMI Running in SiSoft QCD: Vary Post1Q



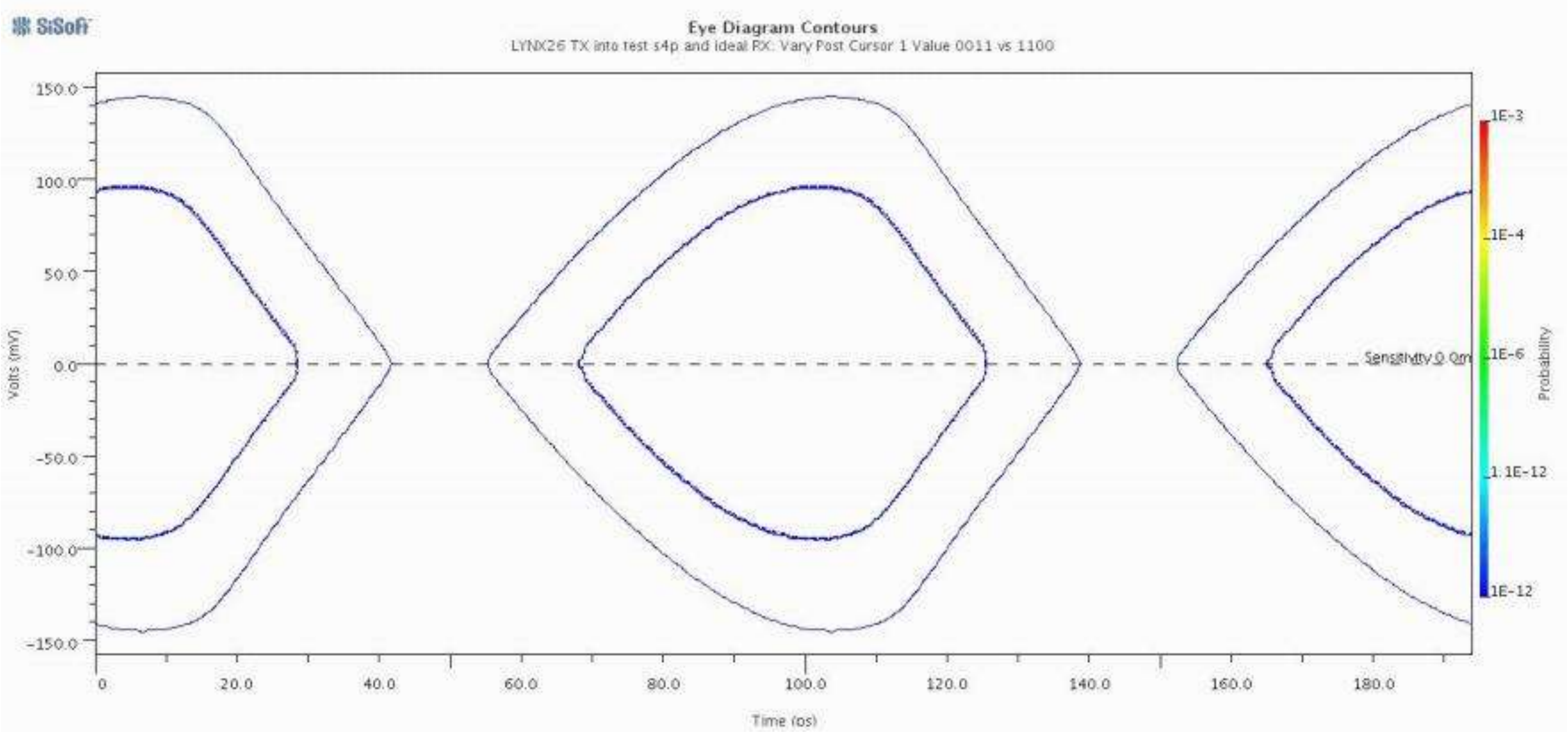
SERDES 10G TX IBIS-AMI Running in SiSoft QCD: Vary Post1Q – small TX EQ



SERDES 10G TX IBIS-AMI Running in SiSoft QCD: Vary Post1Q, Large TX EQ



SERDES 10G TX IBIS-AMI Running in SiSoft QCD: Vary Post1Q



IBIS-AMI Model Correlation

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SERDES 5G IBIS AMI Correlation

- 95+% Figure of Merit between SiSoft Simulation FSL Internal SPICE simulation

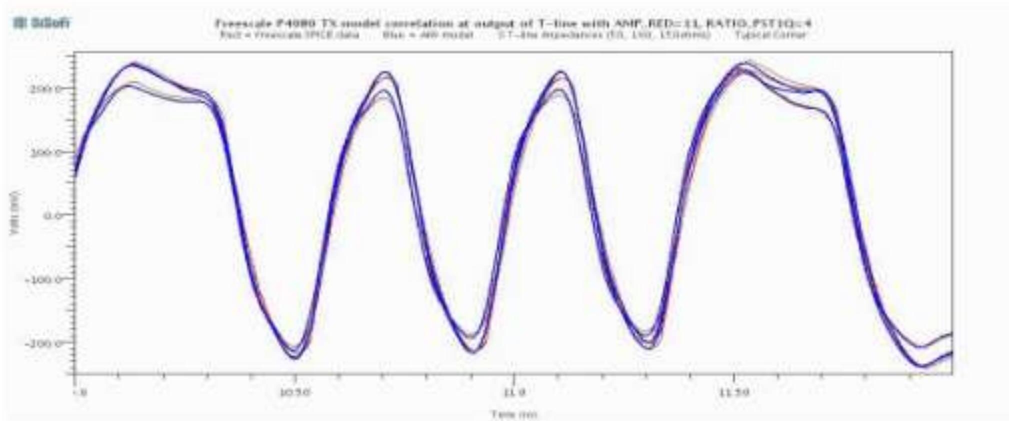

Figure 18: TX waveform at Load; Amplitude=11, Equalization=4, TT-PVT Corner

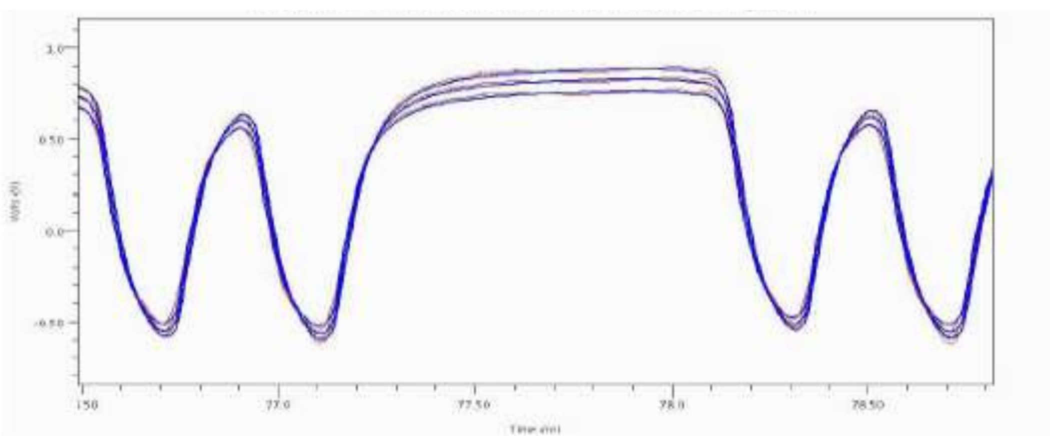

Figure 30: RX analog model correlation, 1.8V input swing, 25ps input rise-time, 100ohm etch model

SERDES 26 IBIS AMI Correlation

- 95+% Figure of Merit between SiSoft Simulation FSL Internal SPICE simulation

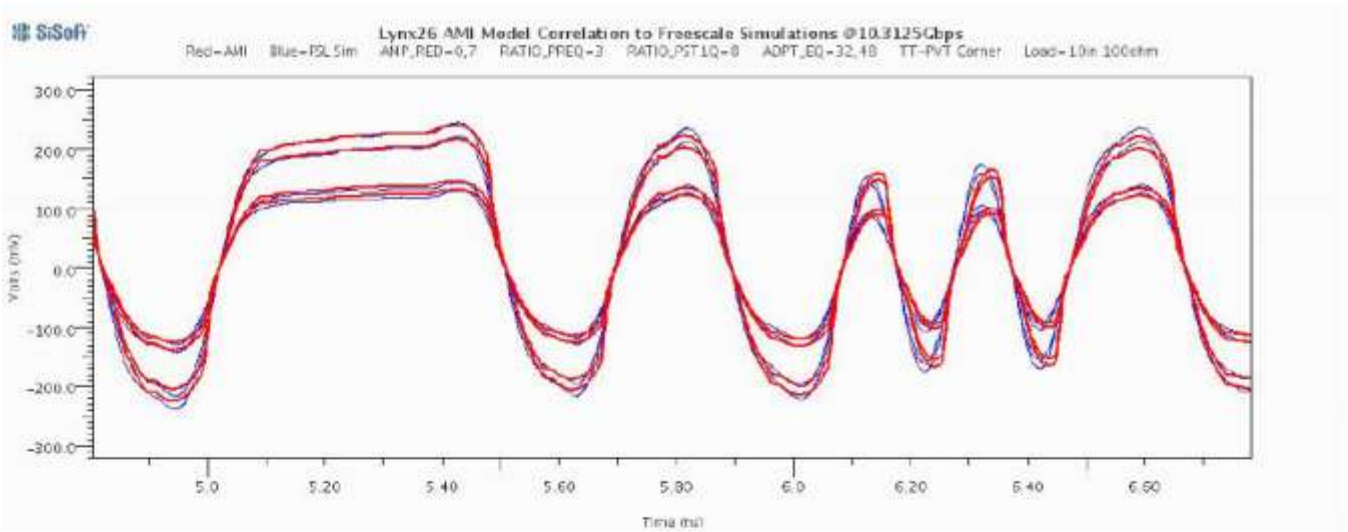

Figure 20: TX waveform at load: 10.3125Gbps; AMP_RED=0,7; RATIO_PREQ=3; RATIO_PST1Q=8; ADPT_EQ=32,48; 100ohm etch; TT-PVT Corner

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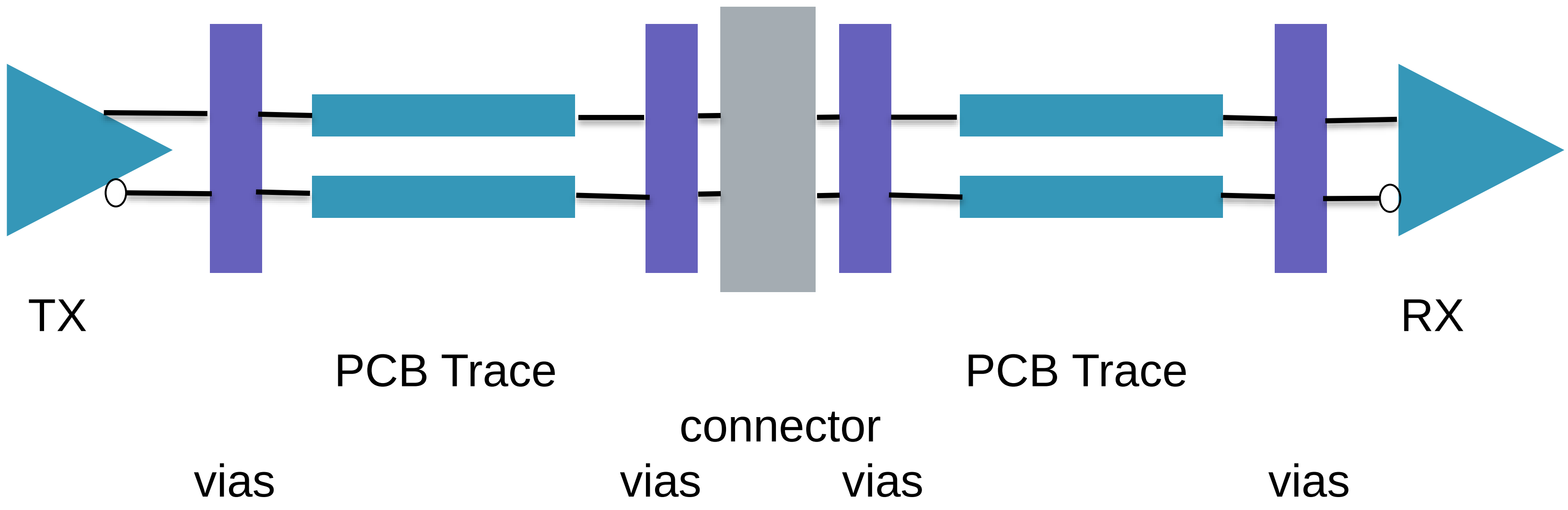
Channel Analysis and Printed Circuit Board Considerations

Channel Analysis Example



Design Considerations

- PCB Stackup
  - Trace width
  - Material:
    - Lost Tangent, Dissipation Factor
    - Dielectric Constant
  - Impedance

- PCB Routing
  - Via Breakout
  - Trace Length
  - Trace Separation (Crosstalk)

- Connector
  - Impedance
  - Crosstalk

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PCB Trace Losses

- PCB Interconnect losses due to traces can be seen in S parameter data.

- Insertion Loss (S12, S21)
  - The PCB dielectric materials and traces have losses that increase with the frequency of the signal. As the SERDES bus speeds increase, the PCB losses become a larger factor in signal degradation.

- Return Loss (S11, S22)
  - Signal losses are also caused by mismatches in impedance. Impedance mismatches occur in packages, PCB traces, vias, connectors, and sockets.

IEEE Spec Document: 10GBase-KR Insertion Loss

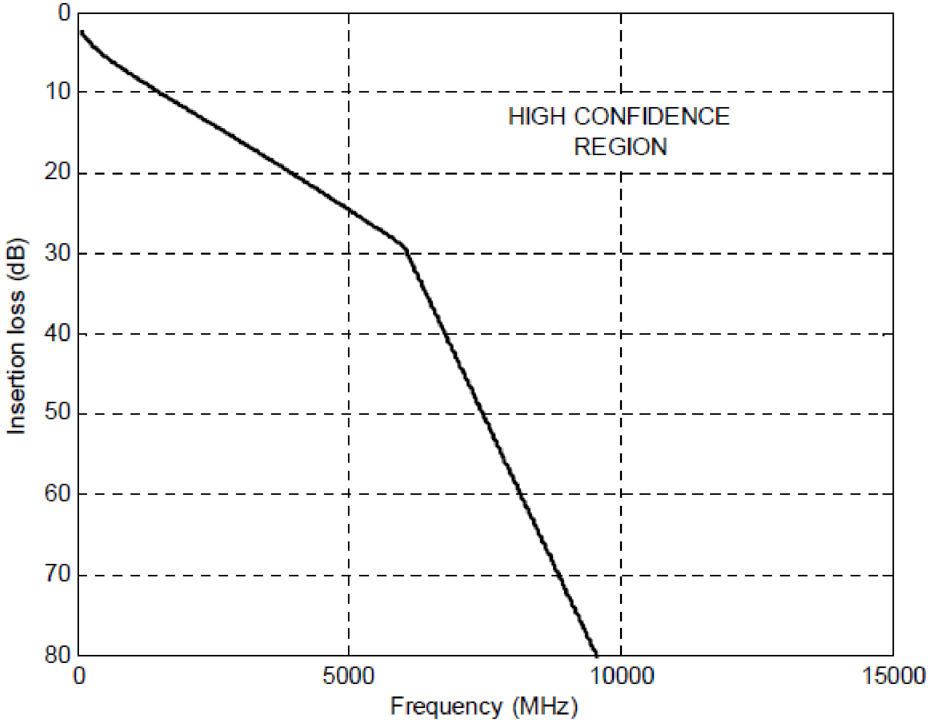

Figure 69B–5—Insertion loss limit for 10GBASE-KR

IEEE Spec Document: Return Loss

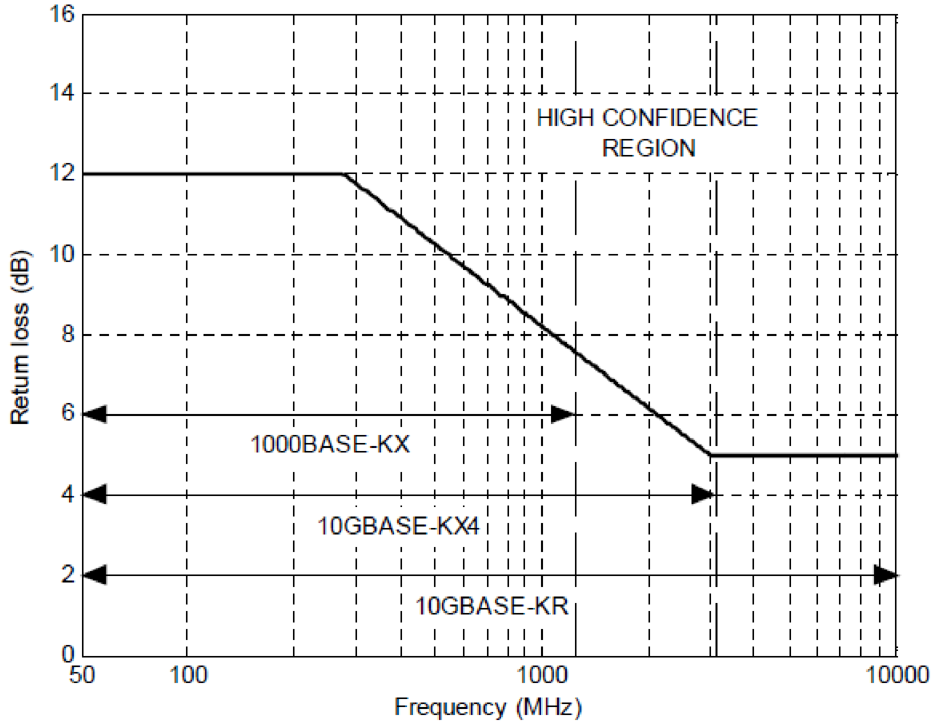

Figure 69B–7—Return loss limit

How to Overcome or Offset Channel Losses

- Overcoming Losses using TX circuit
  - De-emphasis uses a larger voltage difference for transition bits (switching 1-0 or 0-1) and a smaller voltage difference for the non-transition bits. This technique provides a better starting position for the switching signal and reduces inter-symbol interference (ISI).
  - TX equalization options include Feed Forward Equalization (FFE) and Finite Impulse Response (FIR) Filter Equalization.

- Overcoming Losses using the RX circuit
  - Equalization is used at the RX to help recover the data eye.
  - Common forms of equalization are Feed Forward Equalization (FFE), Decision Feedback Equalization (DFE) and Continuous Time Linear Equalization (CTLE).

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PCB Losses: Conductor

PCB Routing: Trace Width

- Trace Width affects the loss of the SERDES channel
- Narrower traces produce more loss due to skin effect
- Increases at Square Root of Frequency

Frequency Dependent
Skin Effect Loss

$$\alpha \propto \sqrt{f} \,/\, t_w$$

t_w = **trace width**
(worse with narrow traces)

PCB Trace Width Examples

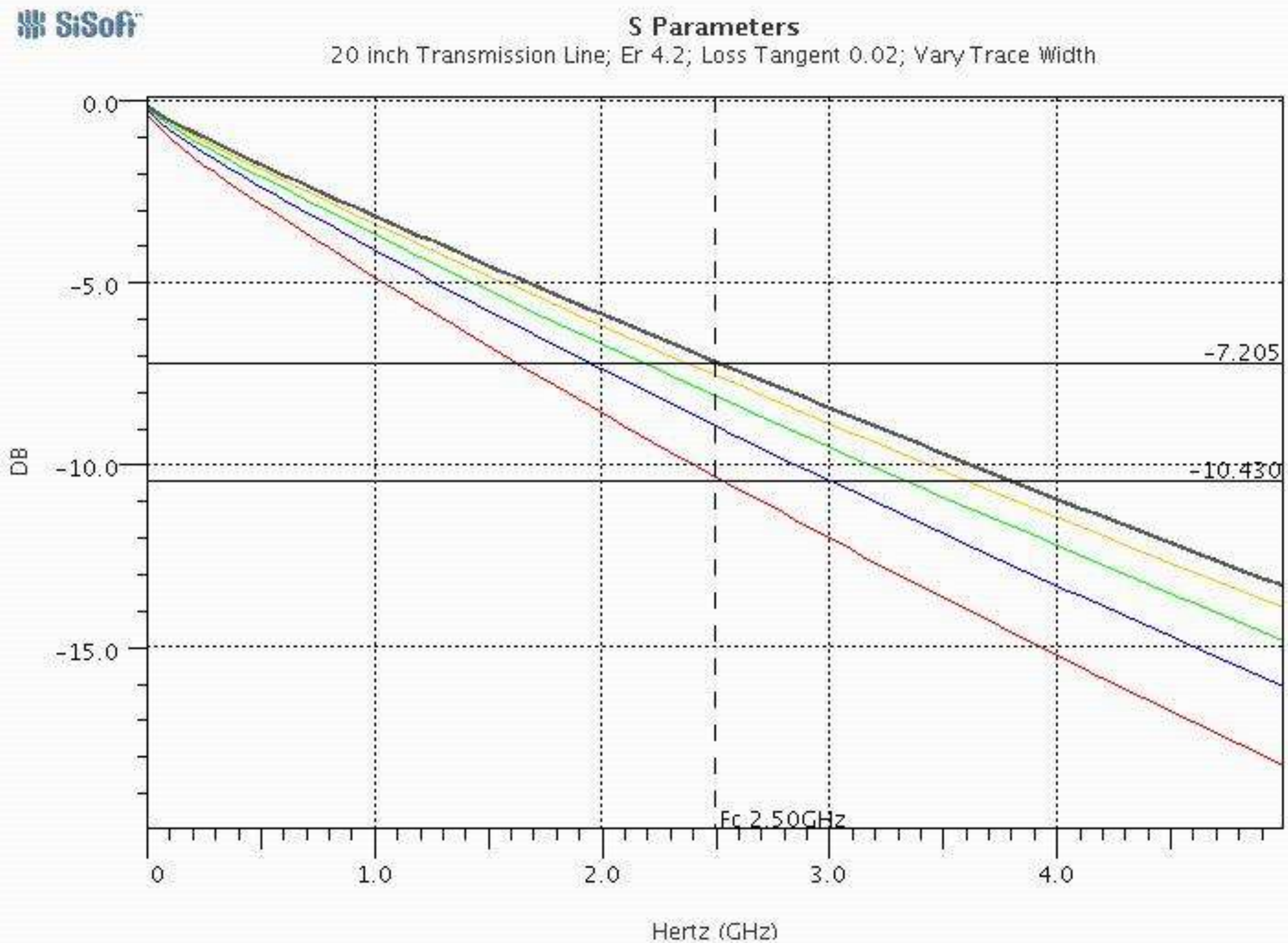
- PCB Trace Widths to be examined:
  - 4 mils
  - 6 mils
  - 8 mils
  - 10 mils
  - 12 mils

- Data eyes for narrower trace widths have a smaller amplitude and smaller UI due to conductor loss

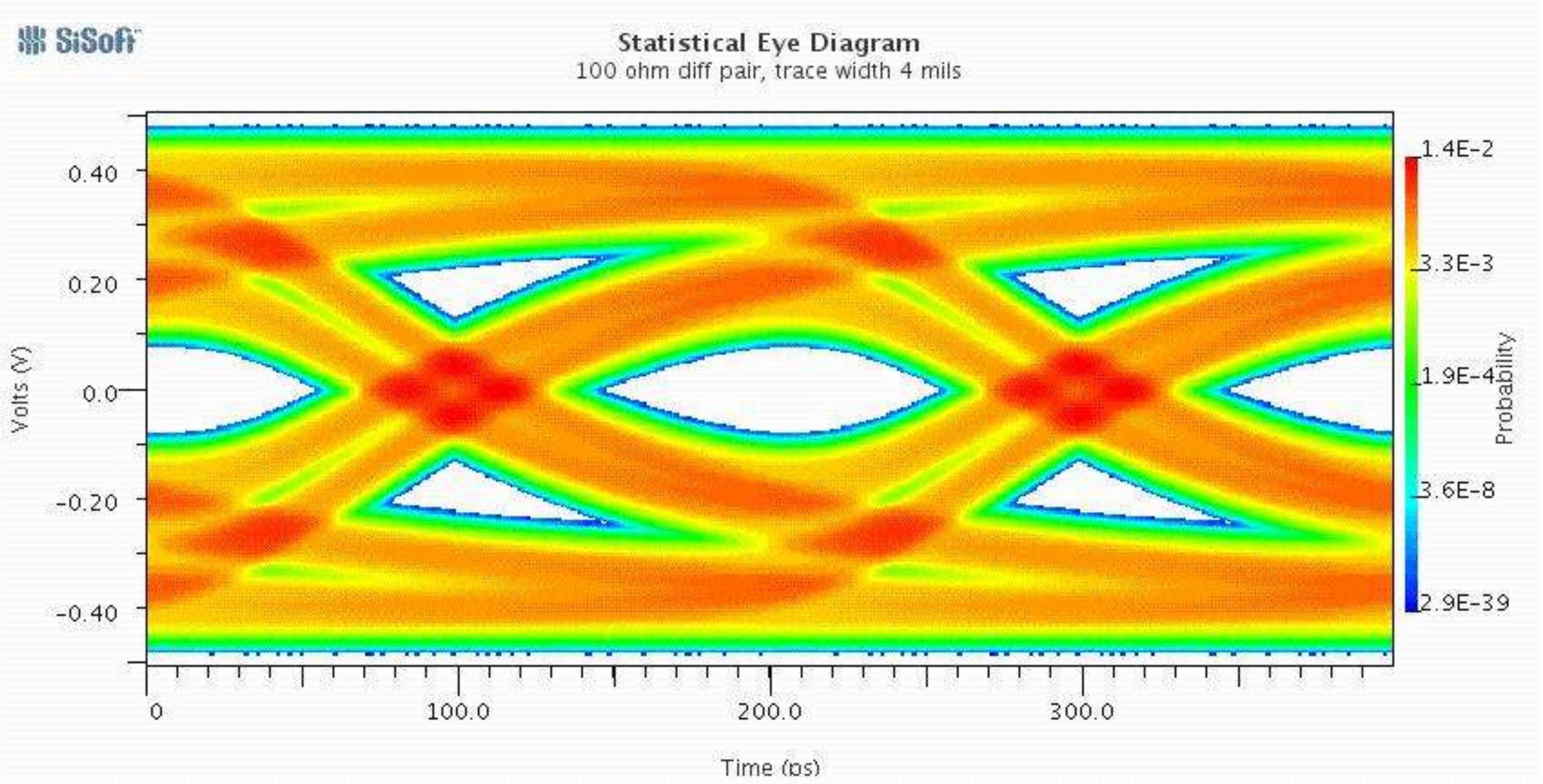
Example Channel: Simulated at 5Gbps without EQ

PCB Trace:
- 20 inches
- Dielectric Constant: 4.2
- Loss Tangent: 0.02
- Vary Trace Width:
  - 4, 6, 8, 10, 12 mils

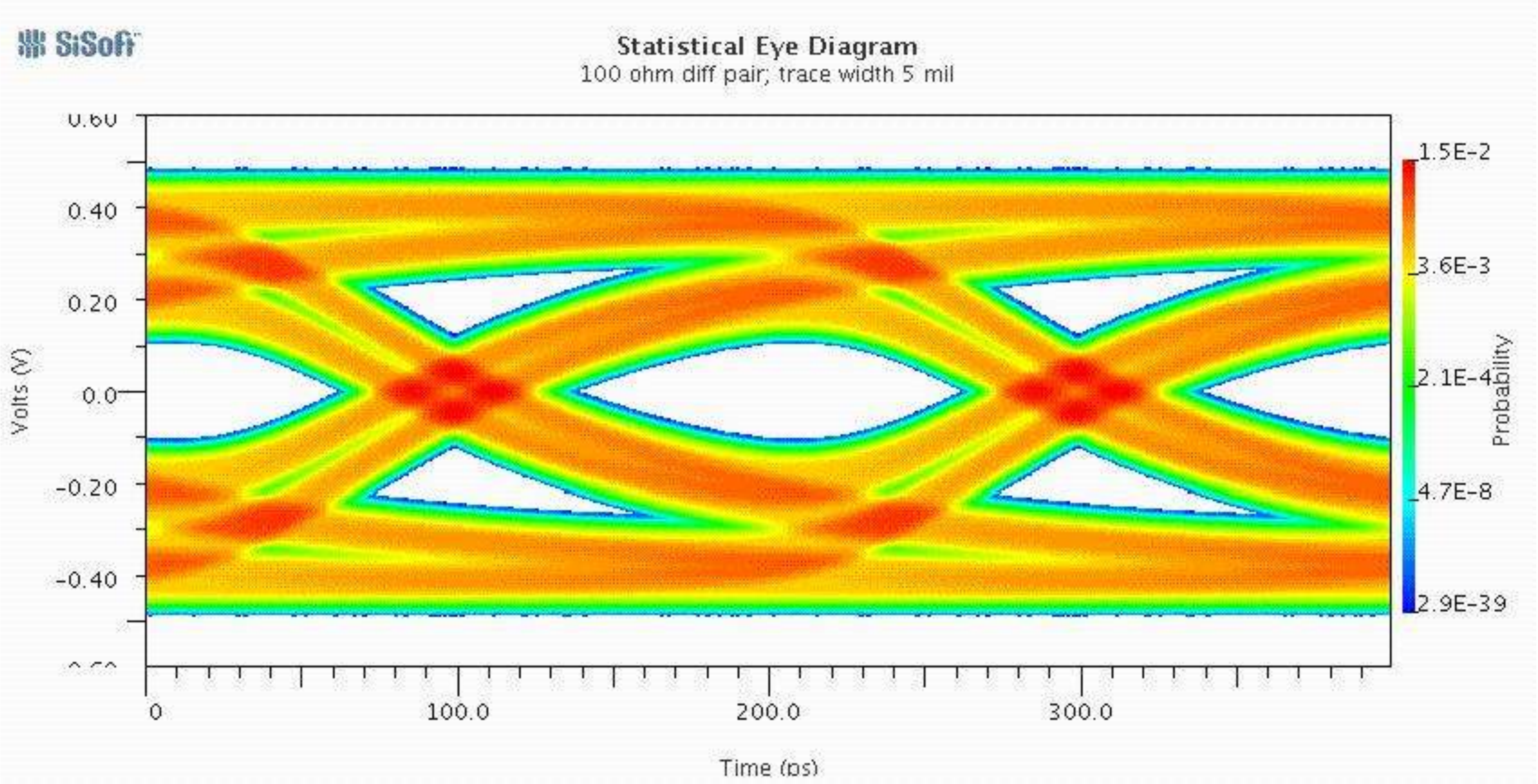
PCB Trace Width Examples: Insertion Loss



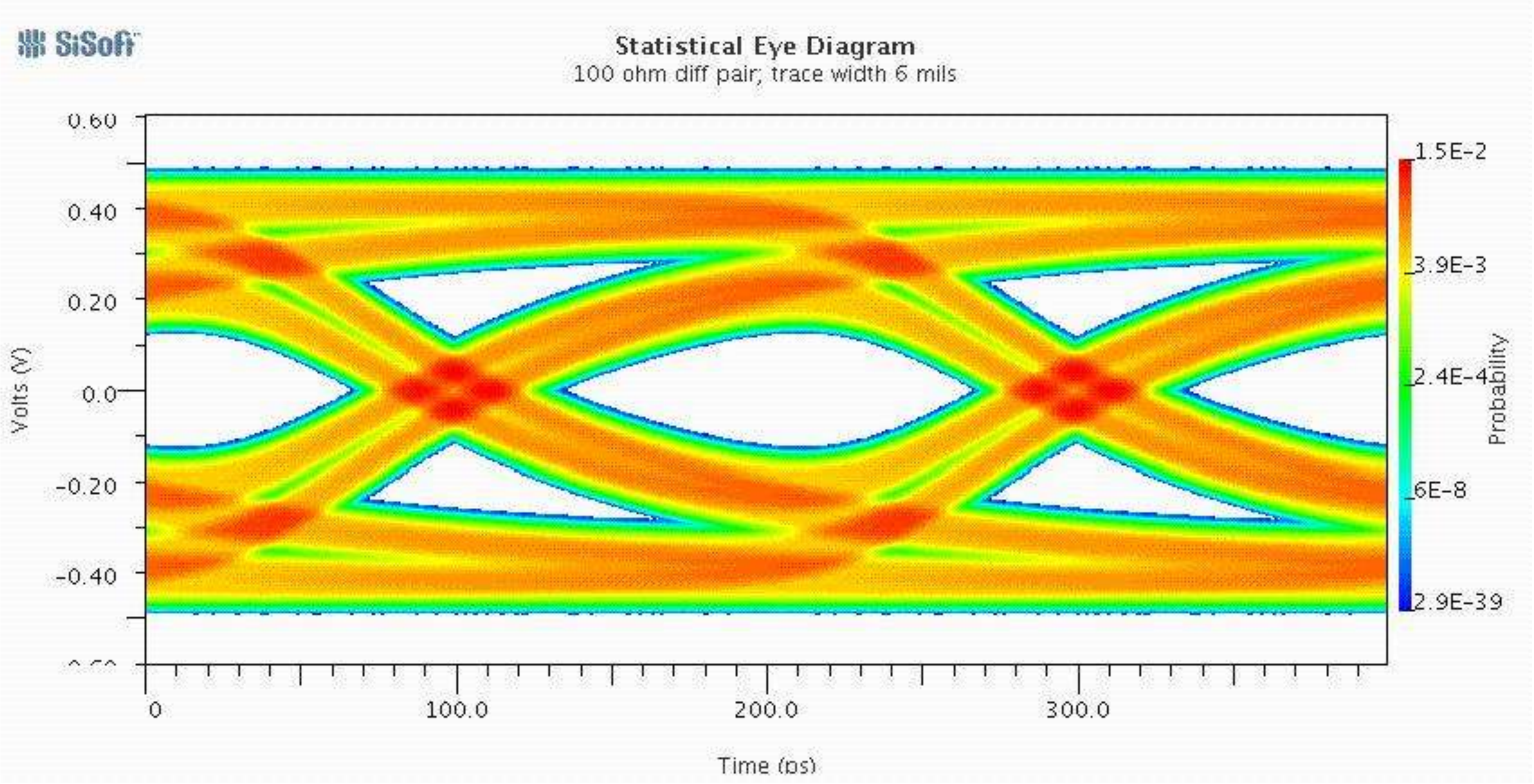
PCB Trace Width Results: 4 mils



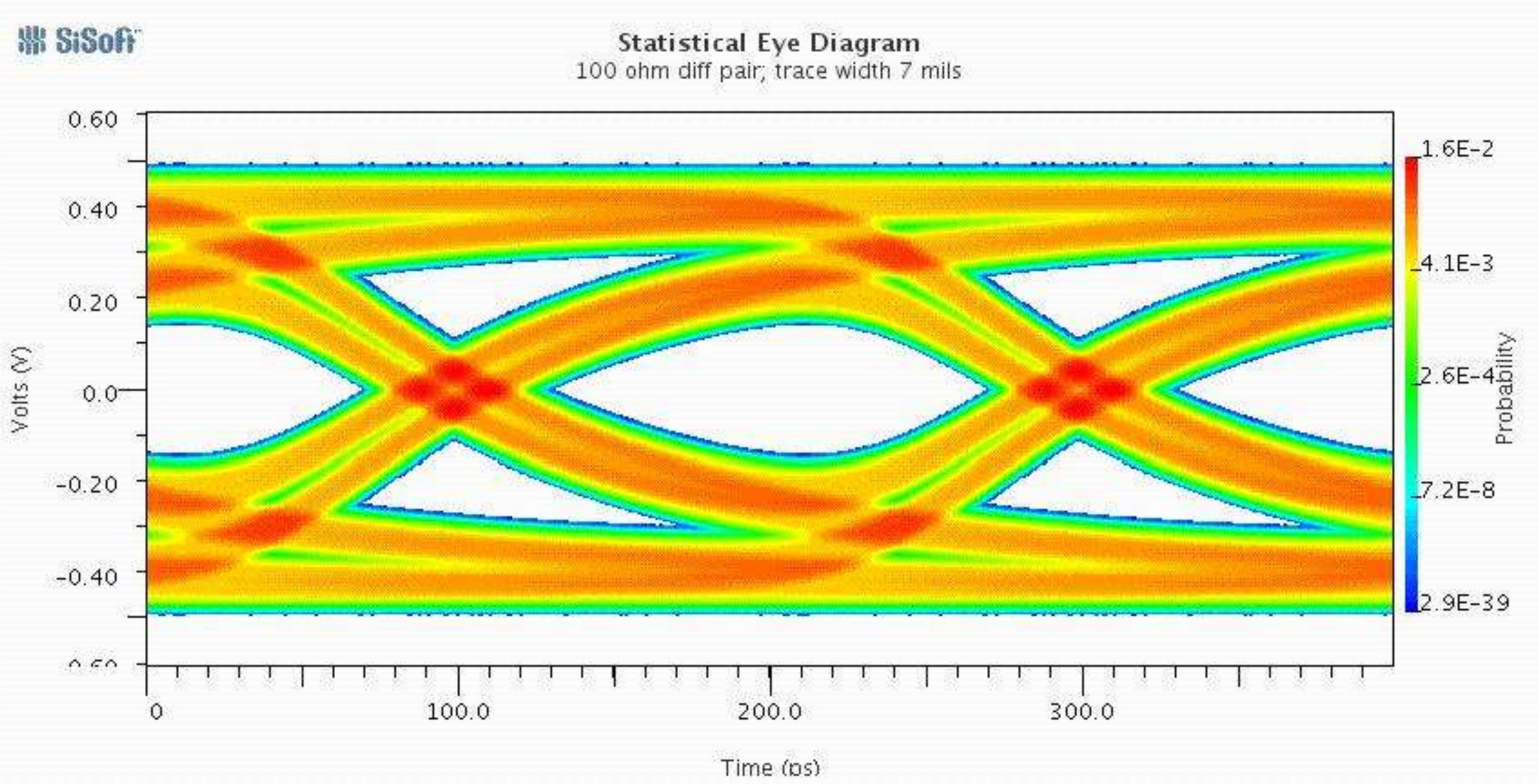
PCB Trace Width Results: 5 mils



PCB Trace Width Results: 6 mils



PCB Trace Width Results: 7 mils



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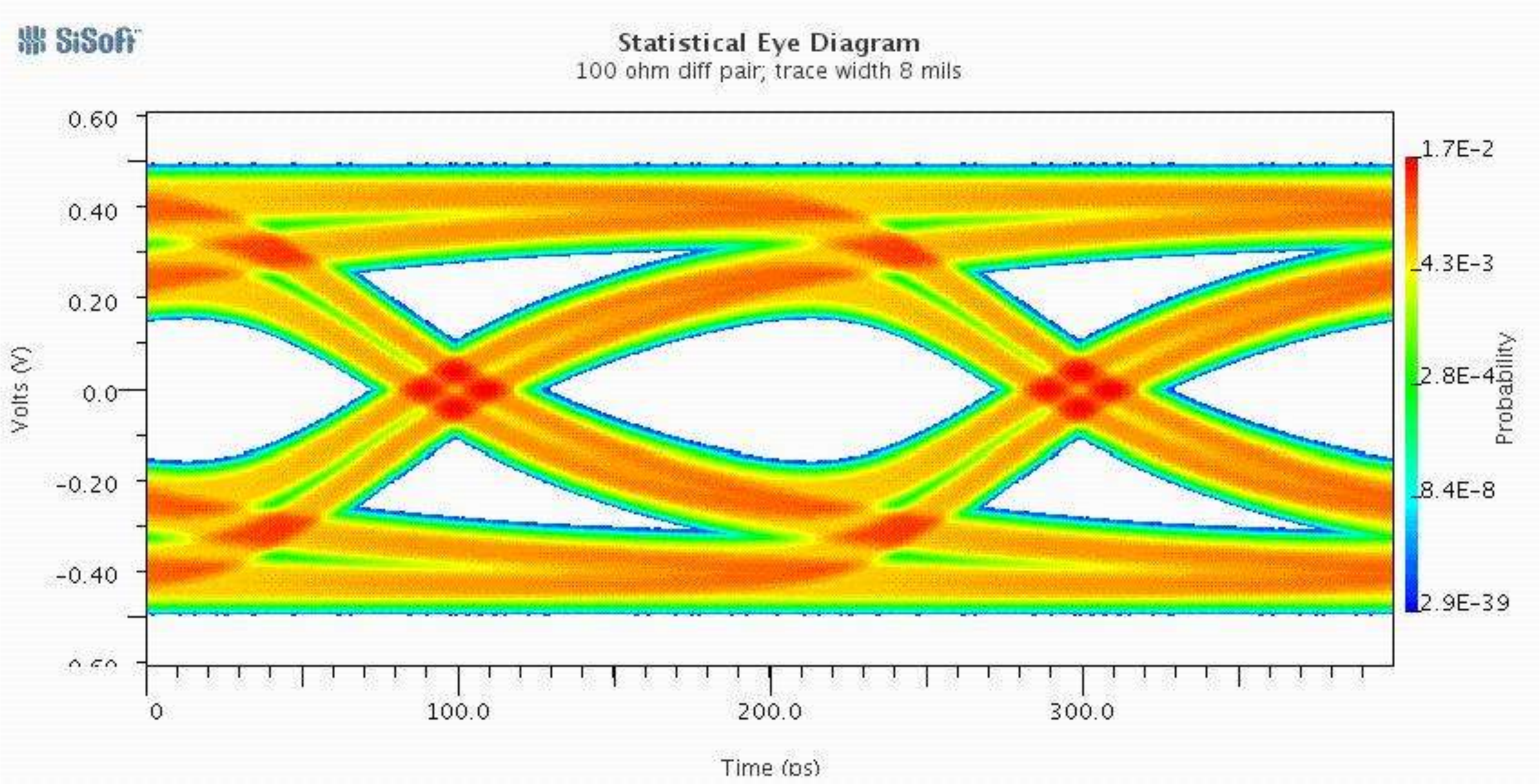
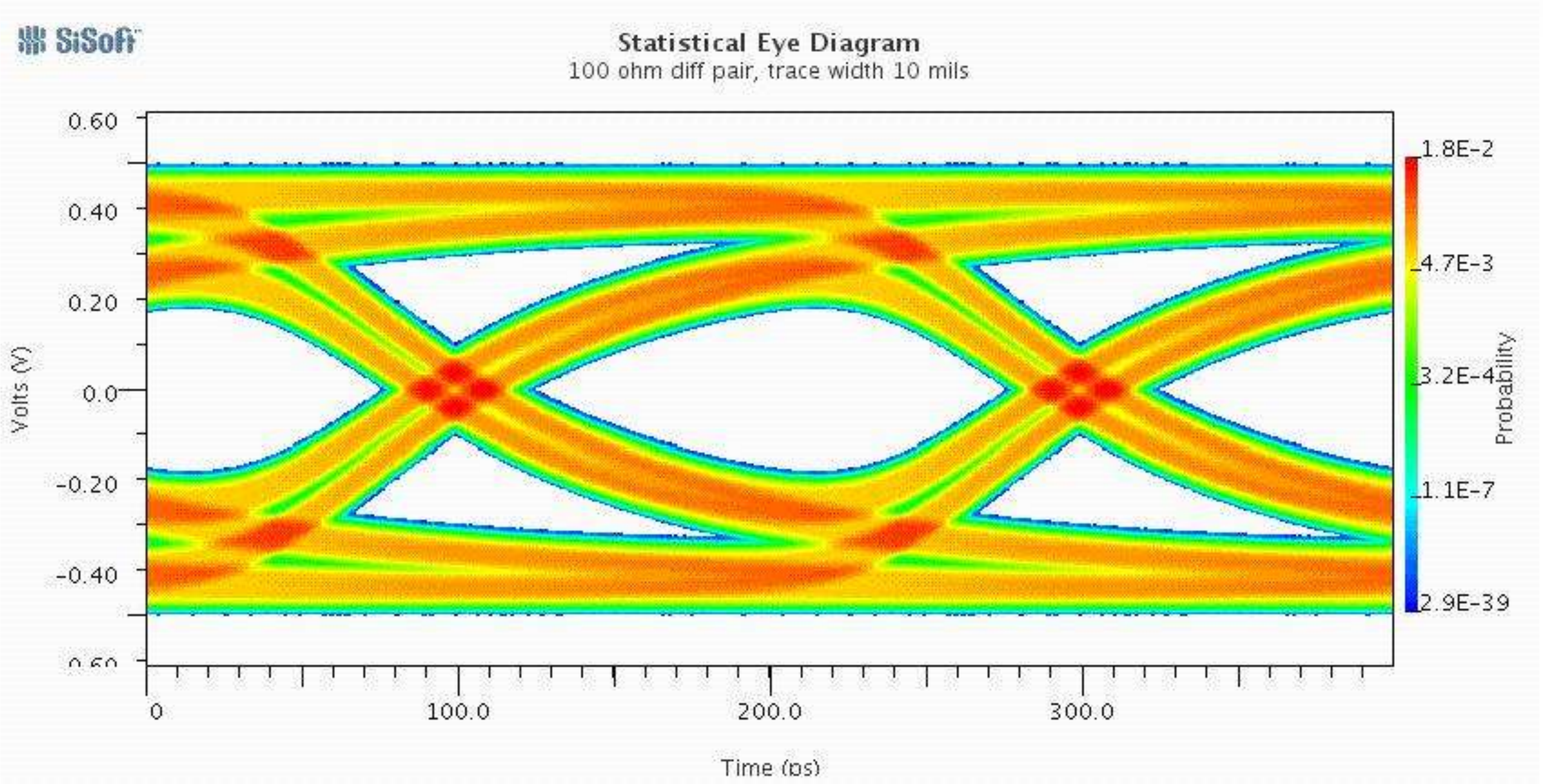
PCB Trace Width Results: 8 mils



PCB Trace Width Results: 10 mils



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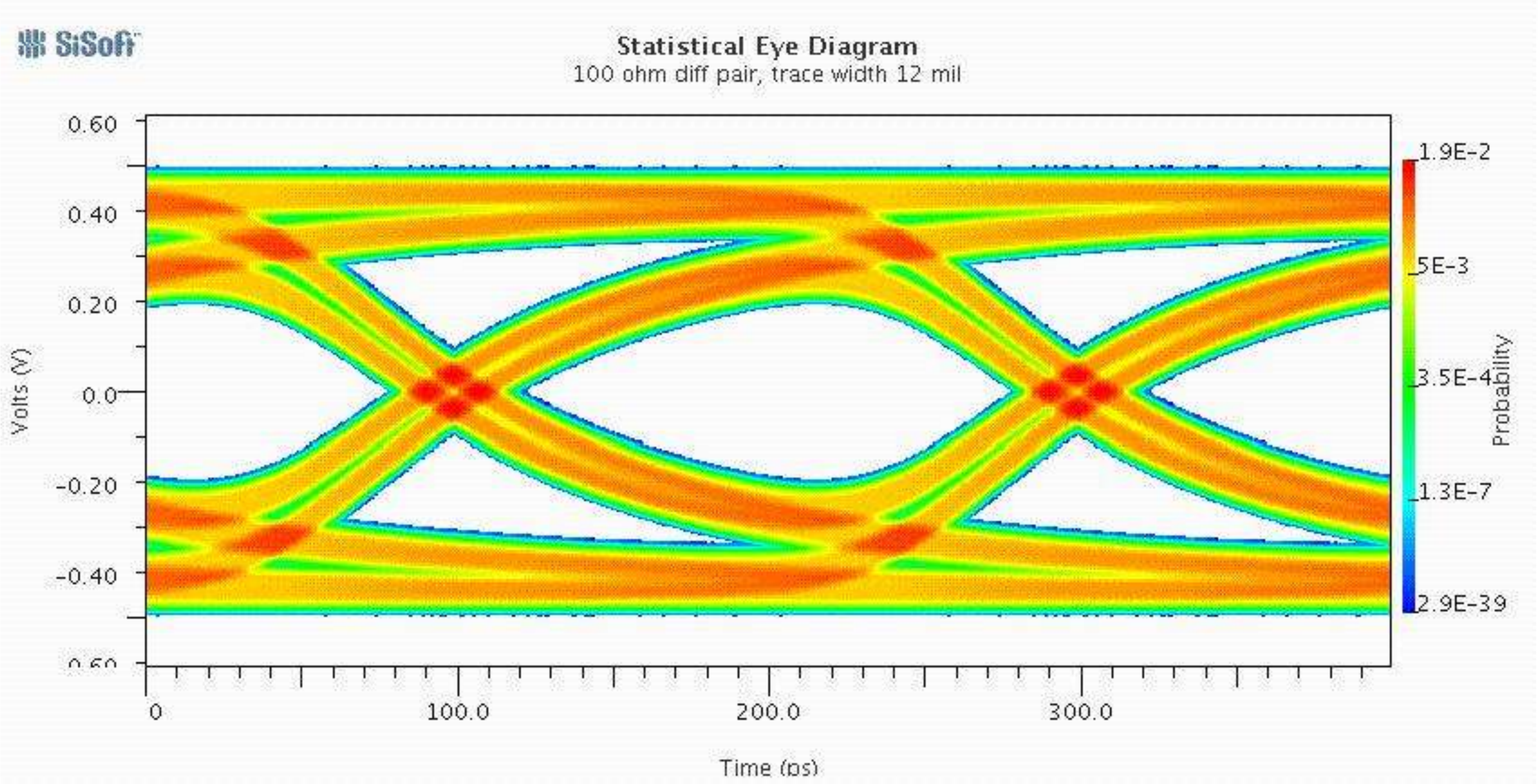
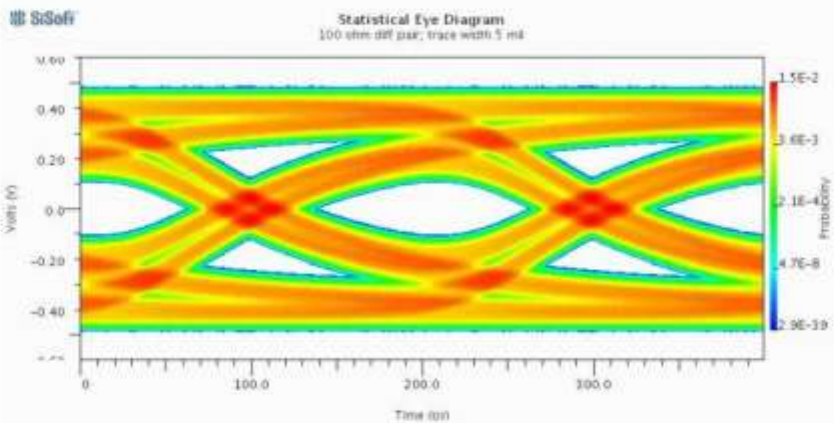
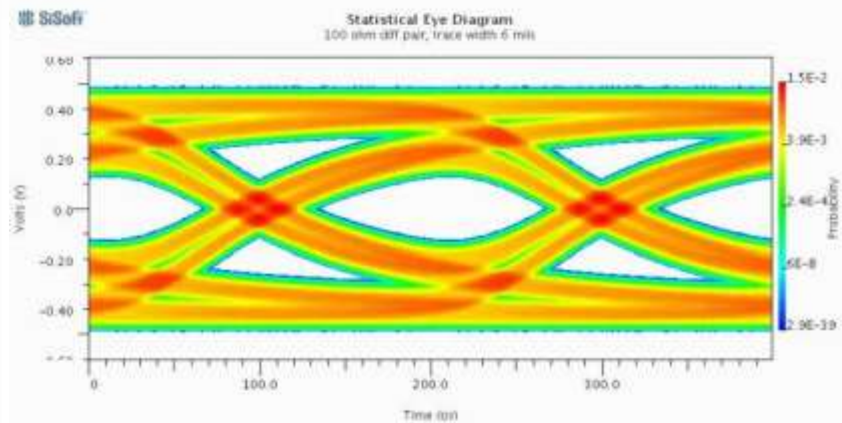
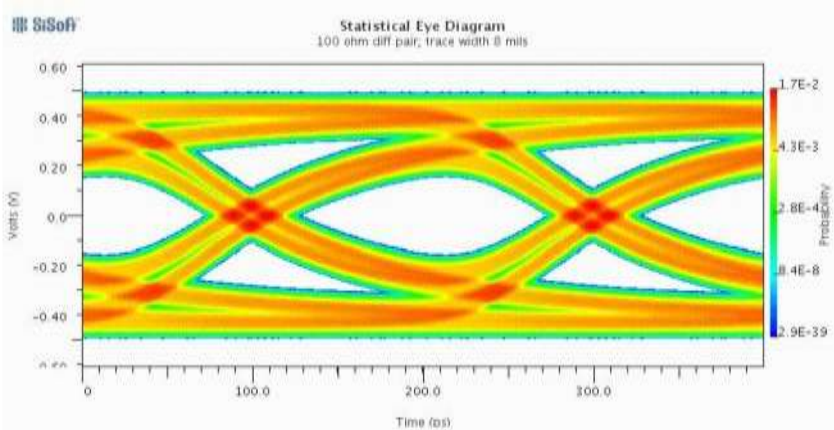
PCB Trace Width Results: 12 mils

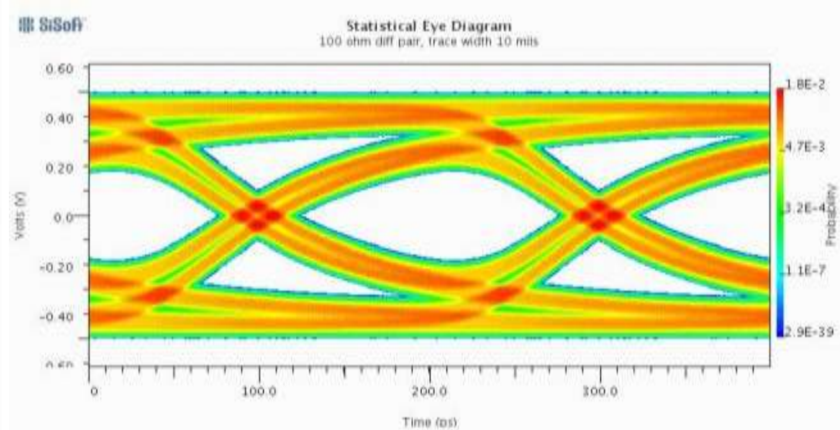


PCB Trace Width Results No EQ: Compare



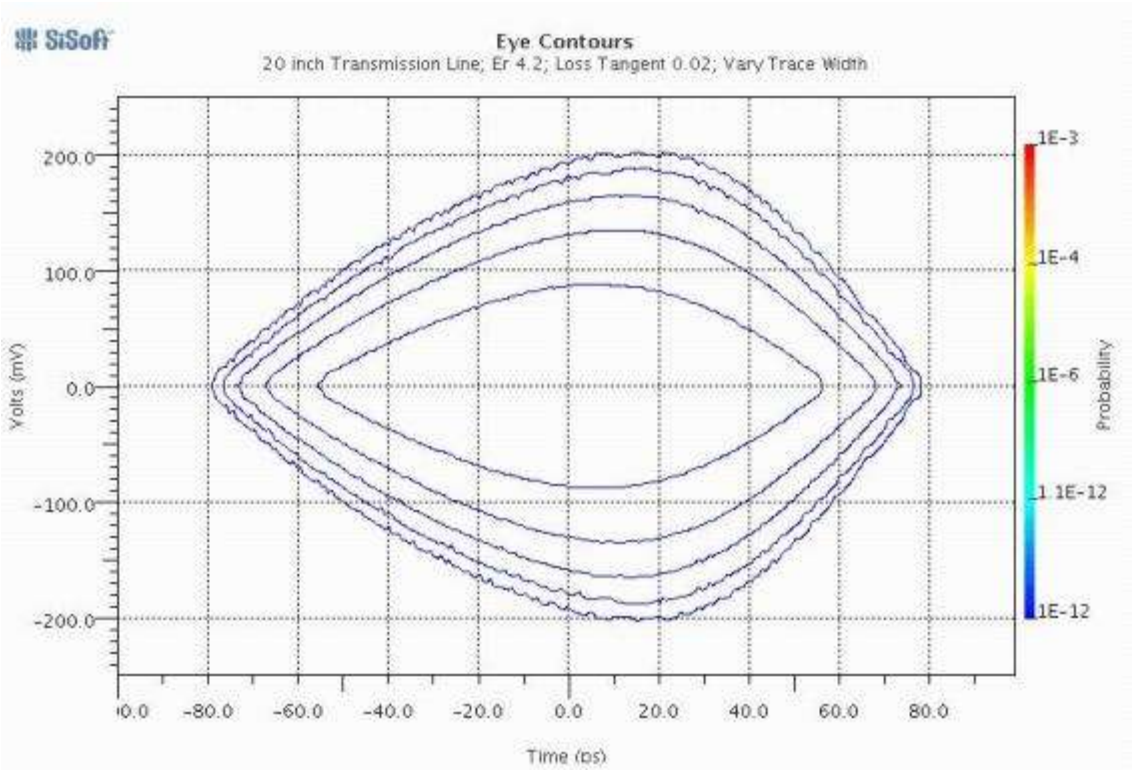






PCB Trace Width Results No EQ: Compare Contour Plots

Trace Width (mils)	Eye Ht (mV)	Eye Width (ps)
4	173.7	113.3
6	261.6	136.7
8	317.9	148.4
10	360.8	154.7
12	380.9	158.6



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PCB Losses: Dielectric

PCB Routing: PCB Material

- PCB Dielectric Material includes a loss tangent value
- Higher loss tangent values produce greater loss in the SERDES Channel
- Increases Proportionally to Frequency

Frequency Dependent Dielectric Loss

$$\alpha = 2.3\,(f)\,\tan(\theta)\,\sqrt{e_r}$$

$\tan(\theta)$ = **loss tangent,**
(better with low loss tangent)

Example Channel: Simulated at 5Gpbs No EQ

PCB Trace:

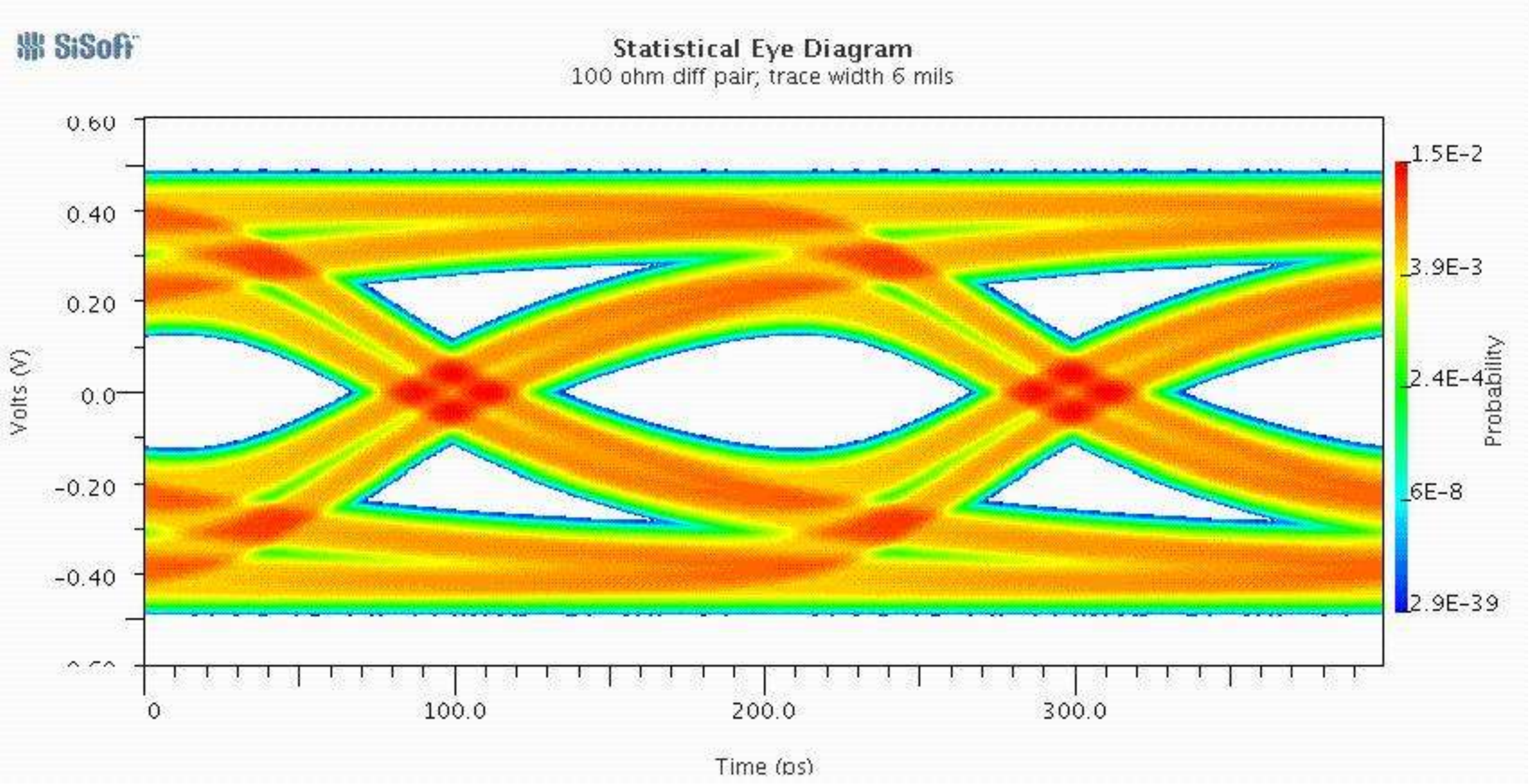
- 20 inches
- Trace Width: 6 mils
- Vary PCB Materials
  - Dielectric Constant & Loss Tangent
    - 4.2 & 0.0200
    - 3.7 & 0.0090
    - 3.5 & 0.0037
    - 3.0 & 0.0013

PCB Material Examples

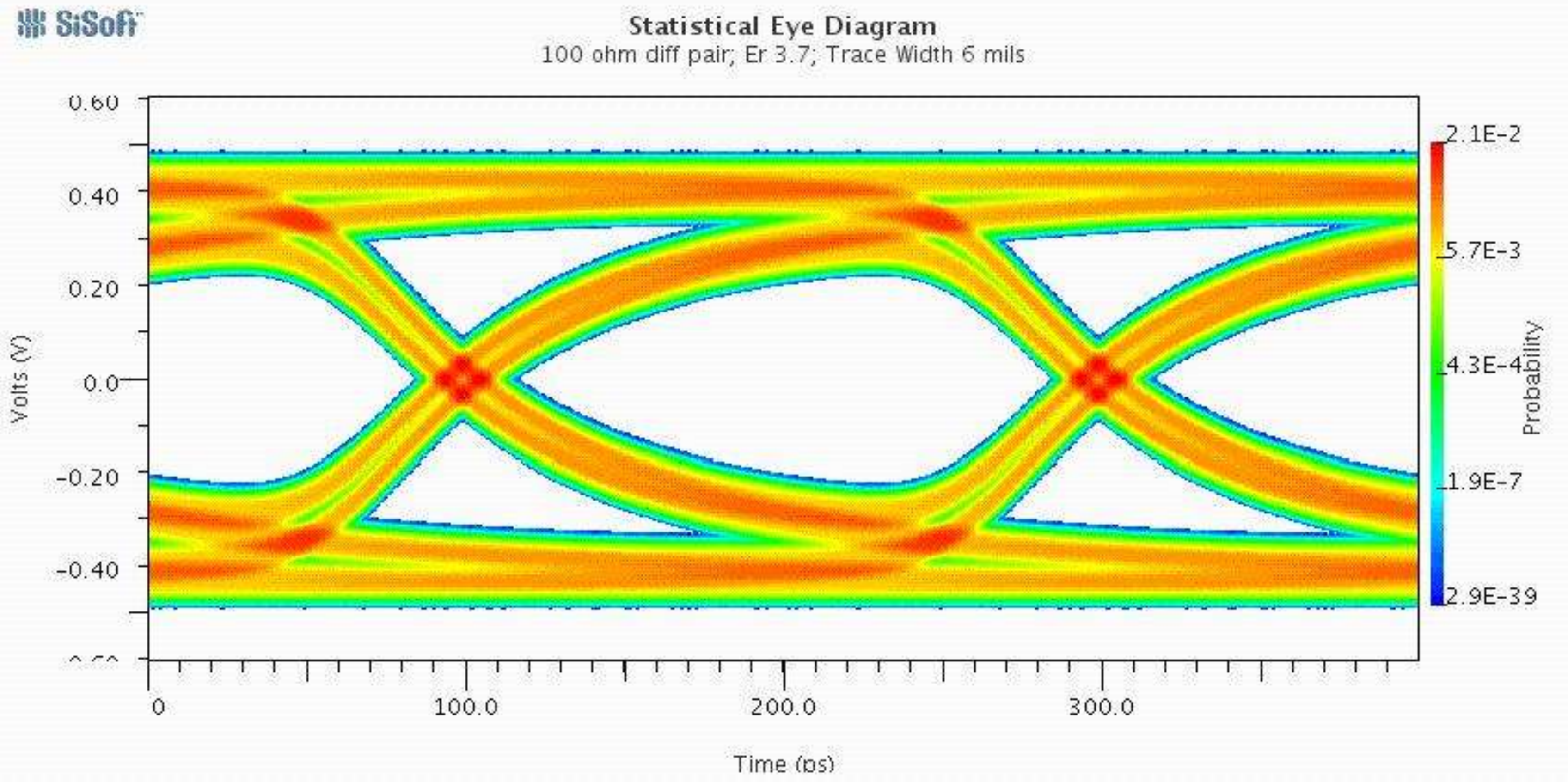
- Common PCB materials to be examined:
  - Dielectric Constant (Er, Dk) = 4.2, Loss Tangent/Dissipation Factor (Df) = 0.02
  - Dielectric Constant (Er, Dk) = 3.7, Loss Tangent/Dissipation Factor (Df) = 0.009
  - Dielectric Constant (Er, Dk) = 3.5, Loss Tangent/Dissipation Factor (Df) = 0.0037
  - Dielectric Constant (Er, Dk) = 3.0, Loss Tangent/Dissipation Factor (Df) = 0.0013

- Data eyes for higher loss tangent dielectrics generally have a smaller amplitude and smaller UI due to dielectric loss.

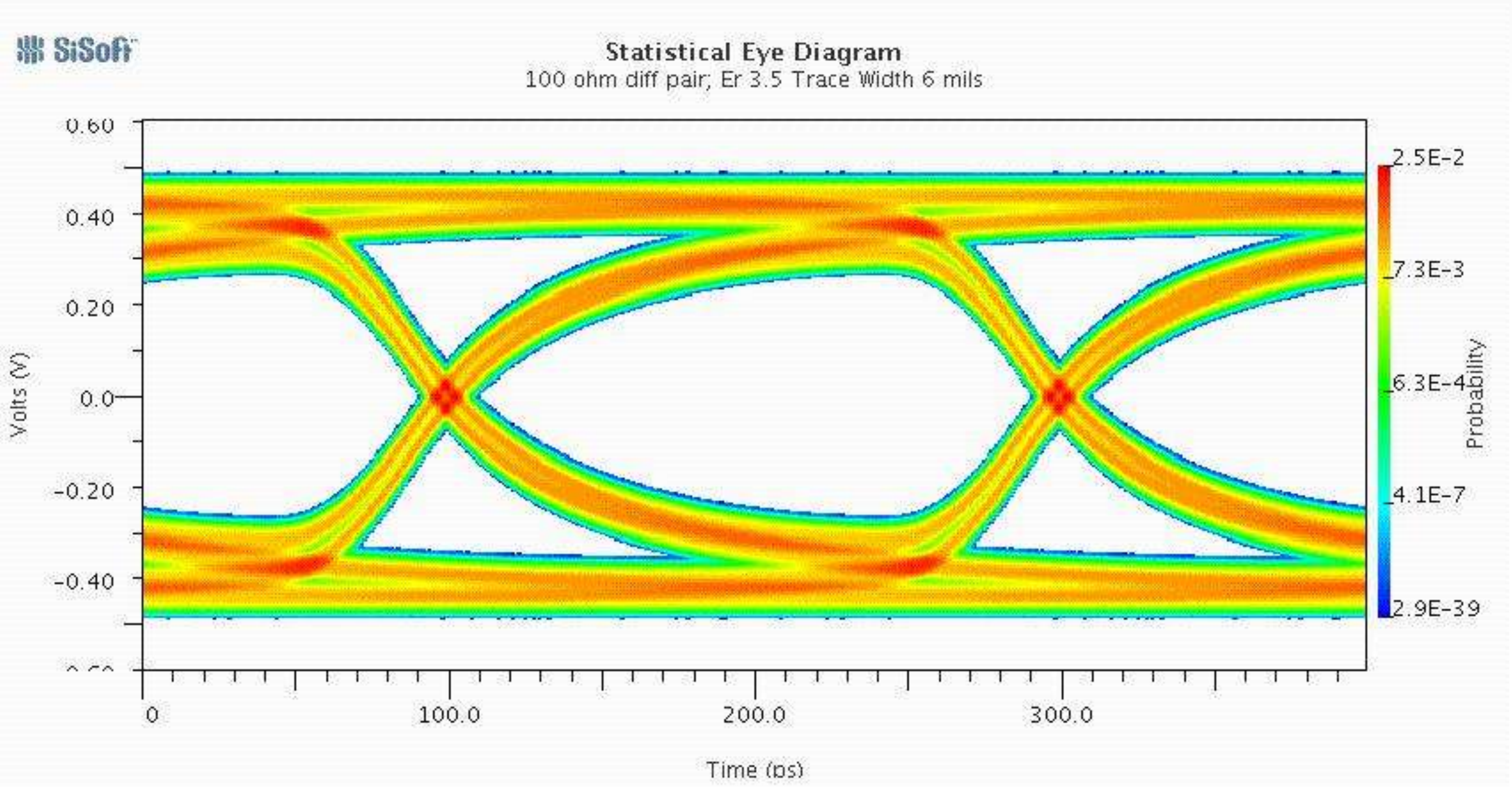
PCB Materials Results: Er 4.2, Df 0.02



PCB Materials Results: Er 3.7, Df 0.009



PCB Materials Results: Er 3.5, Df 0.037



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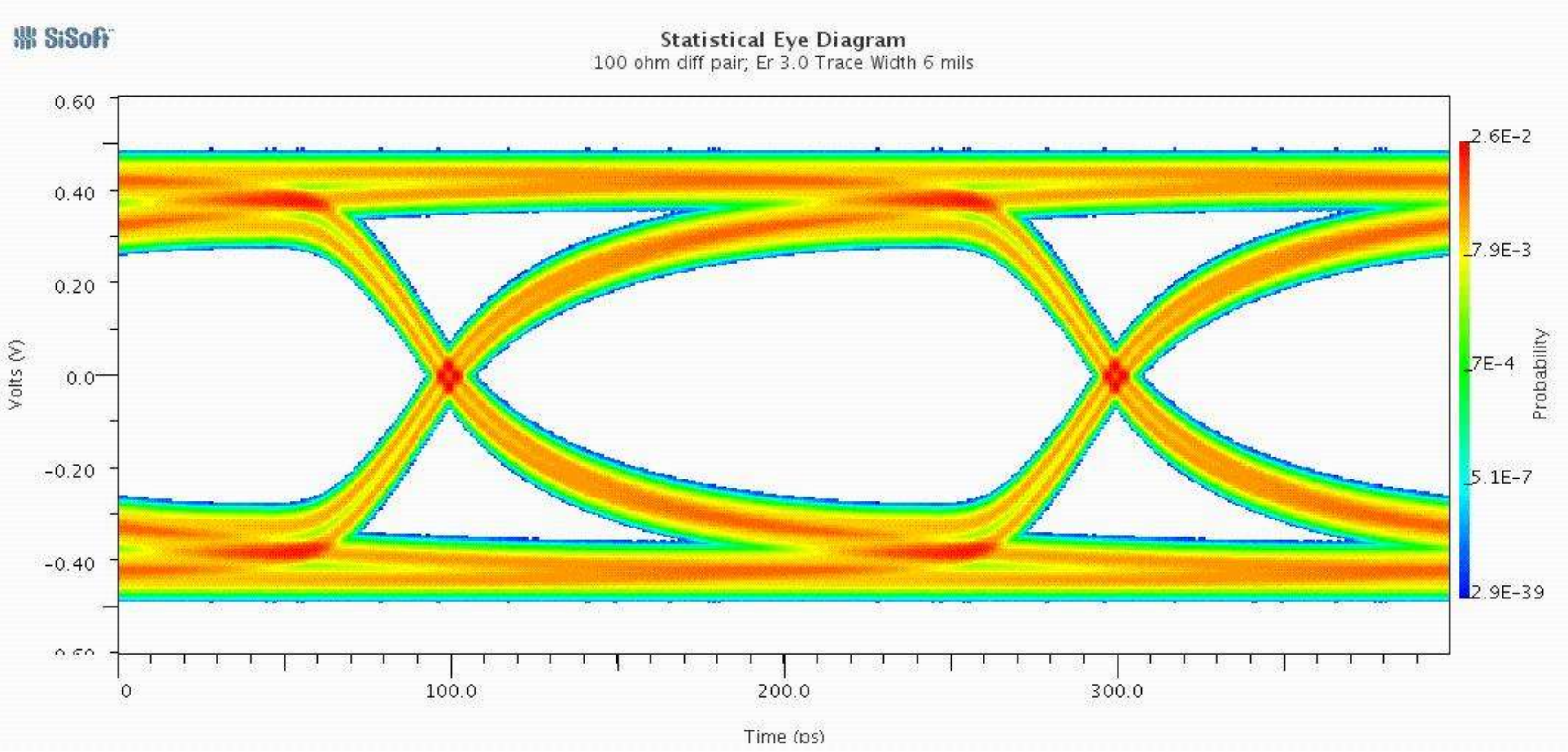
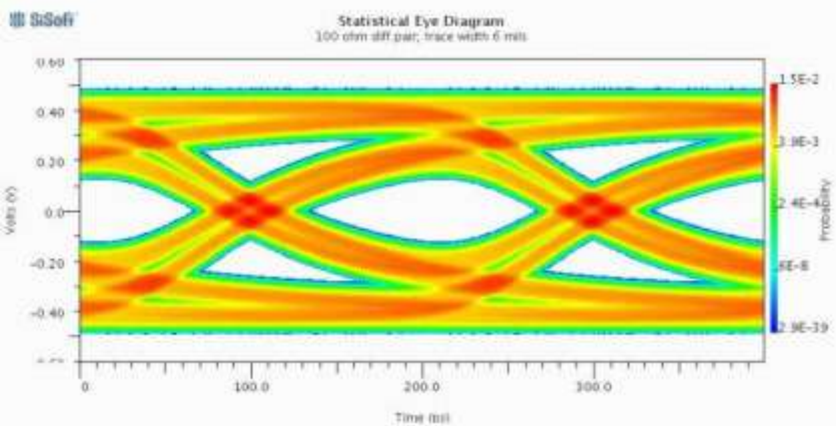
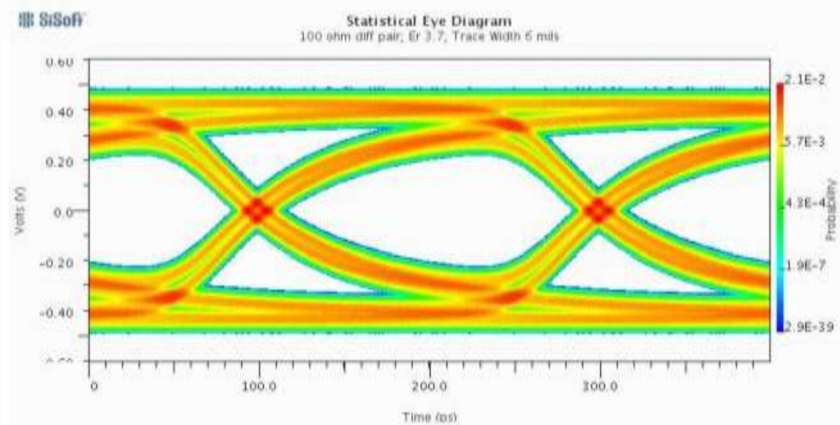
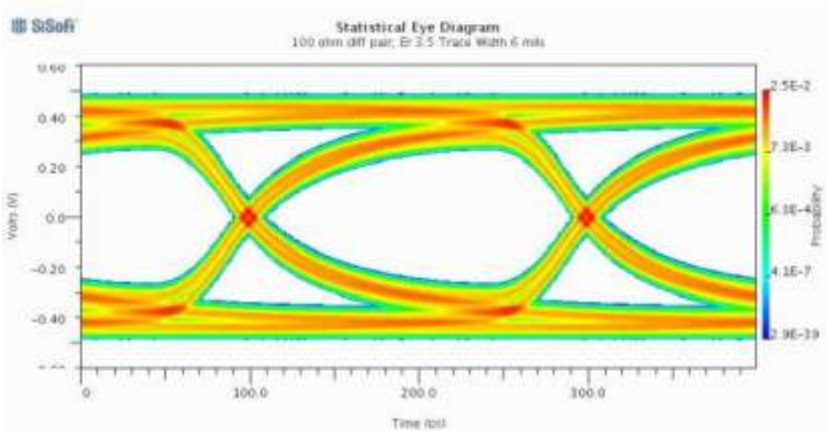
PCB Materials Results: Er 3.0, Df 0.0013

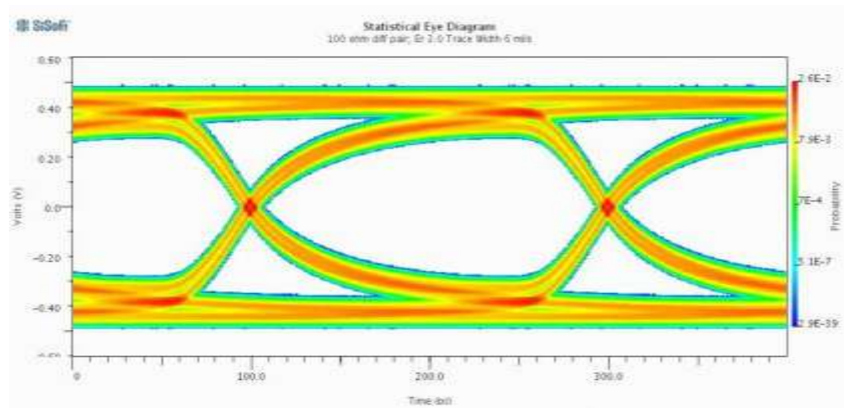


PCB Materials Results: Compare



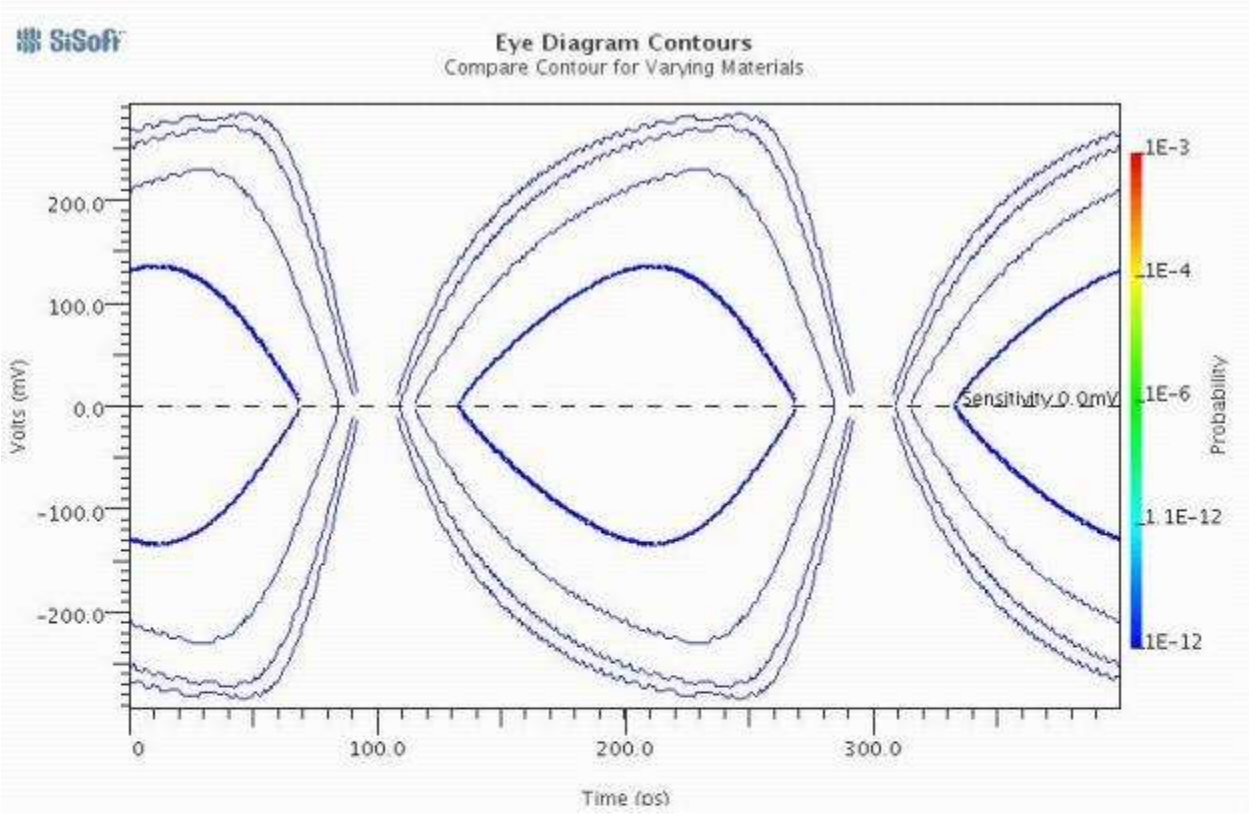






PCB Materials Results: Compare 1e-12 Contour Plot

Material	Eye Ht (mV)	Eye Width (ps)
Er 4.2, 0.02	261.6	136.7
Er 3.7, 0.009	414.7	170.3
Er 3.5, 0.0037	506.0	182.8
Er 3.0, 0.0013	536.9	185.9



Summary Data on PCB Trace Width & Materials (1)

- Trace width: Use wider traces

(+) Improves skin-effect loss

(+) No increase in material cost

(-) Uses more routing area

(-) Increases PCB thickness to maintain impedance targets

Use of wider traces on internal layers may be limited due to board thickness requirements

Summary Data on PCB Trace Width & Materials (2)

PCB materials: Use “high-speed” FR4

(+) Lower loss tangent ➔ lowers dielectric loss

- Loss tangent can be cut in half with modified FR4 materials

- Use “smooth” copper

(+) Lower dielectric loss

(-) Caution! Peel strength is reduced

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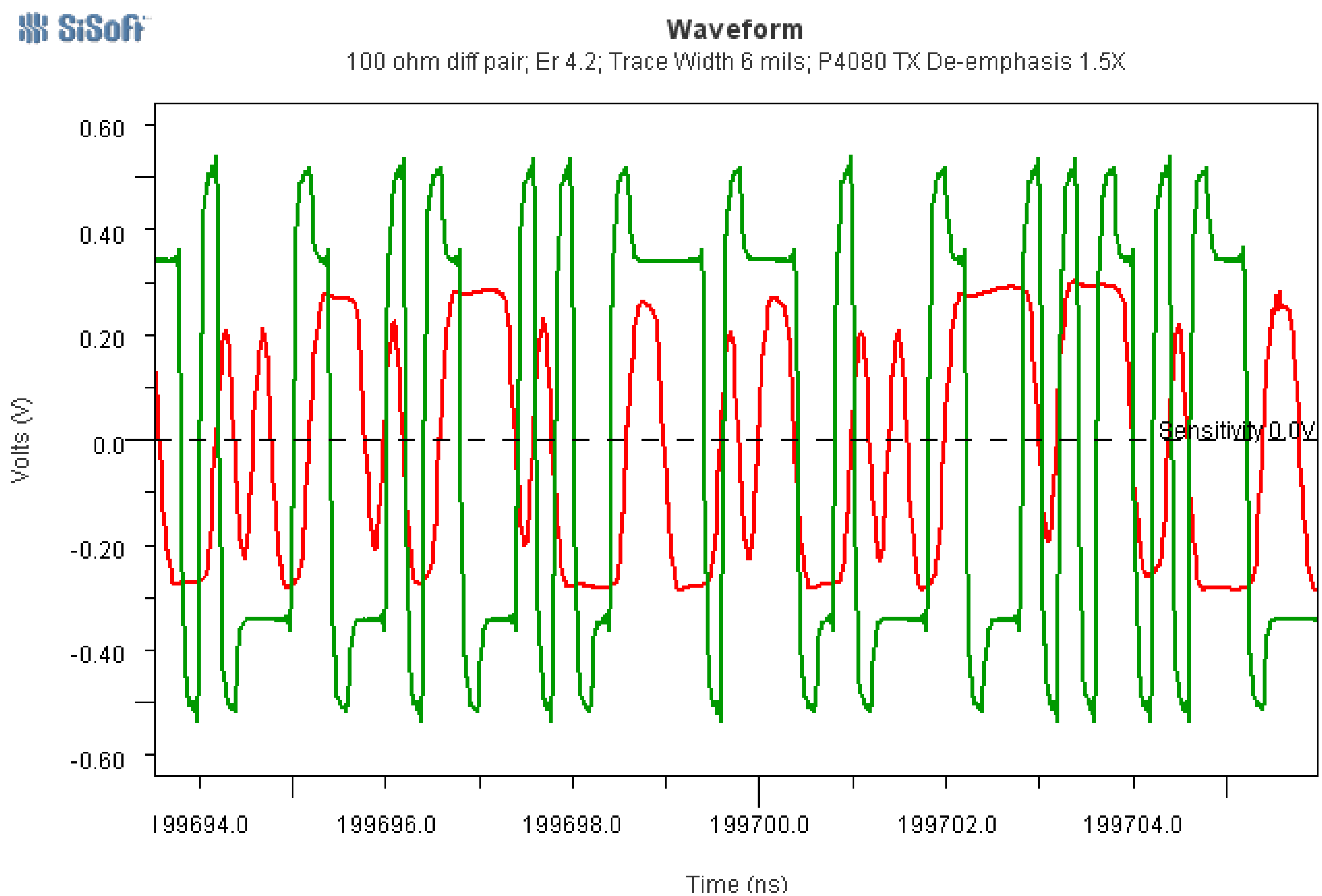
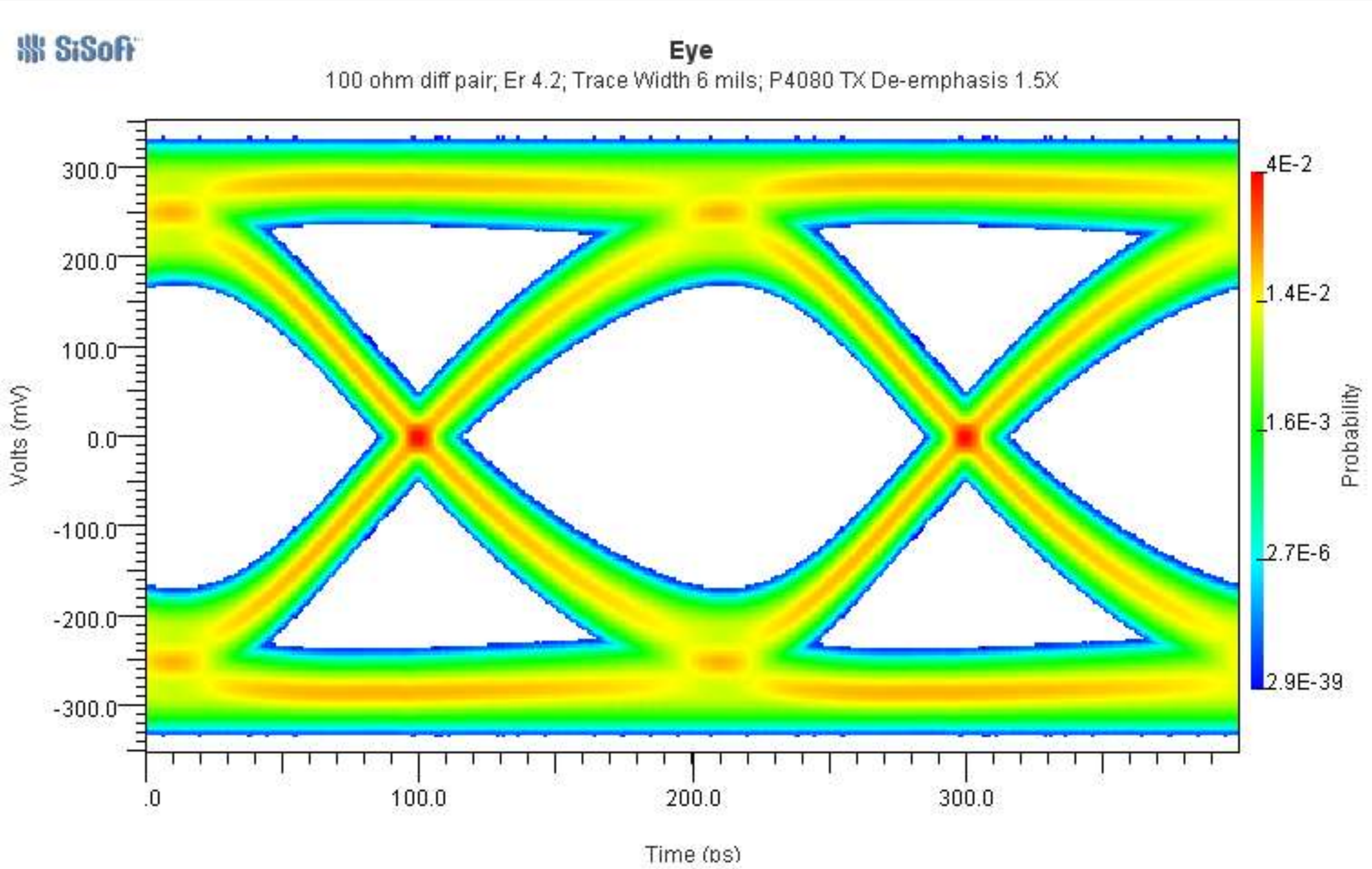
IBIS-AMI Model: Transmitter (TX) and Receiver (RX) Simulations

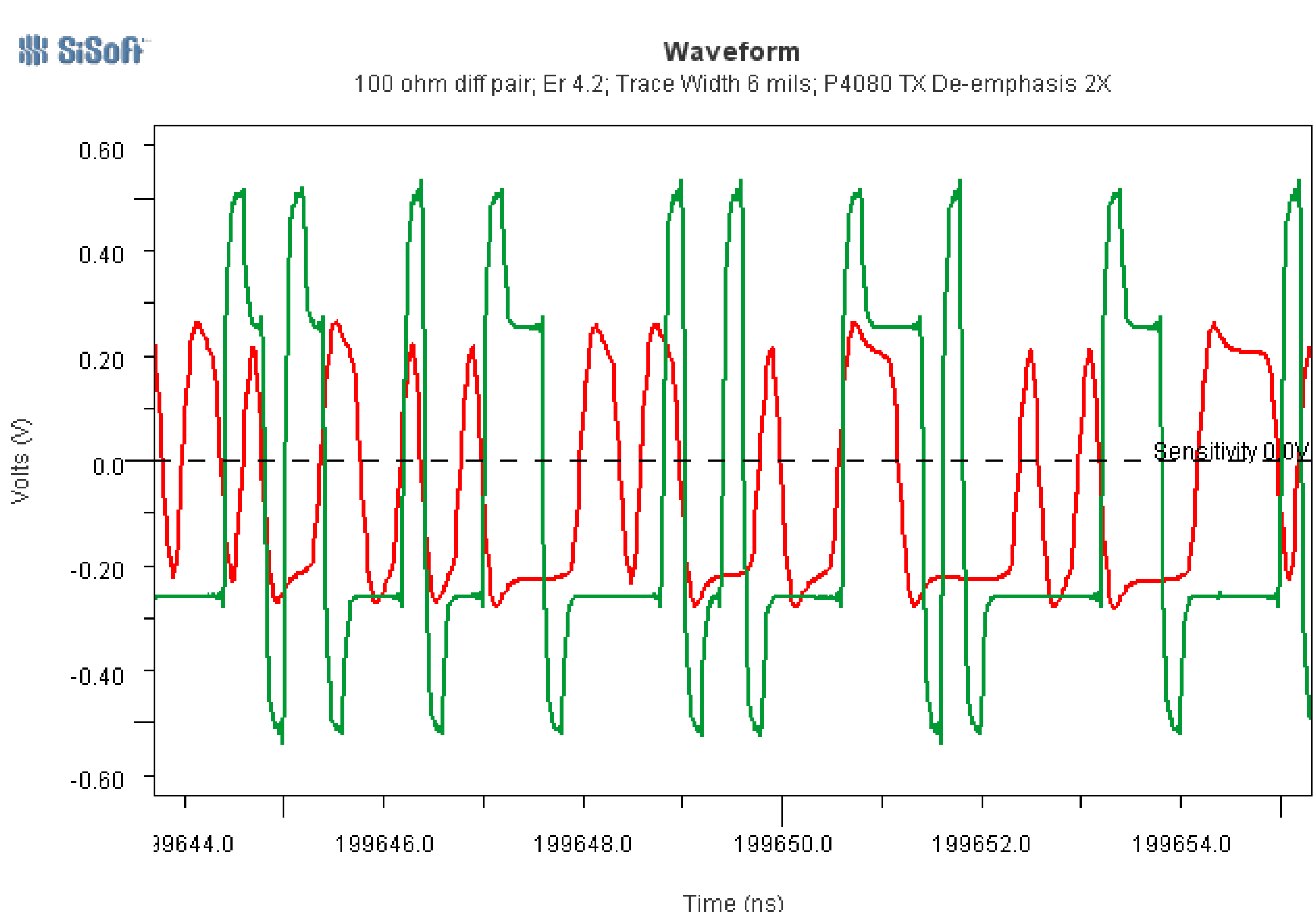
SERDES TX EQ Example: TX EQ 2 Tap 1.5X (3.5dB)



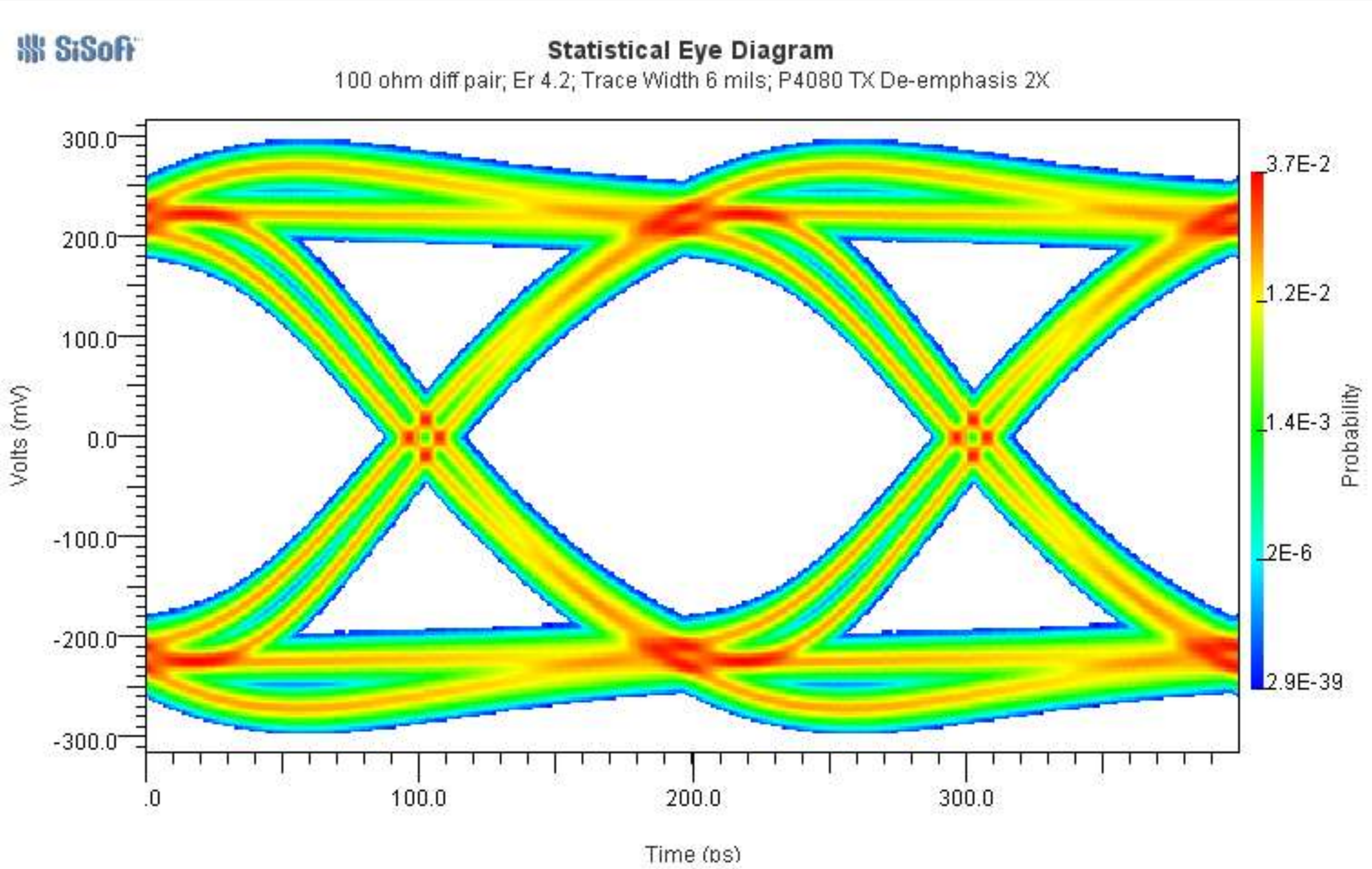
SERDES TX EQ Example: TX EQ 2 Tap 1.5X (3.5dB)



SERDES TX EQ Example: TX EQ 2 Tap 2X (6dB)



SERDES TX EQ Example: TX EQ 2 Tap 2X (6dB)



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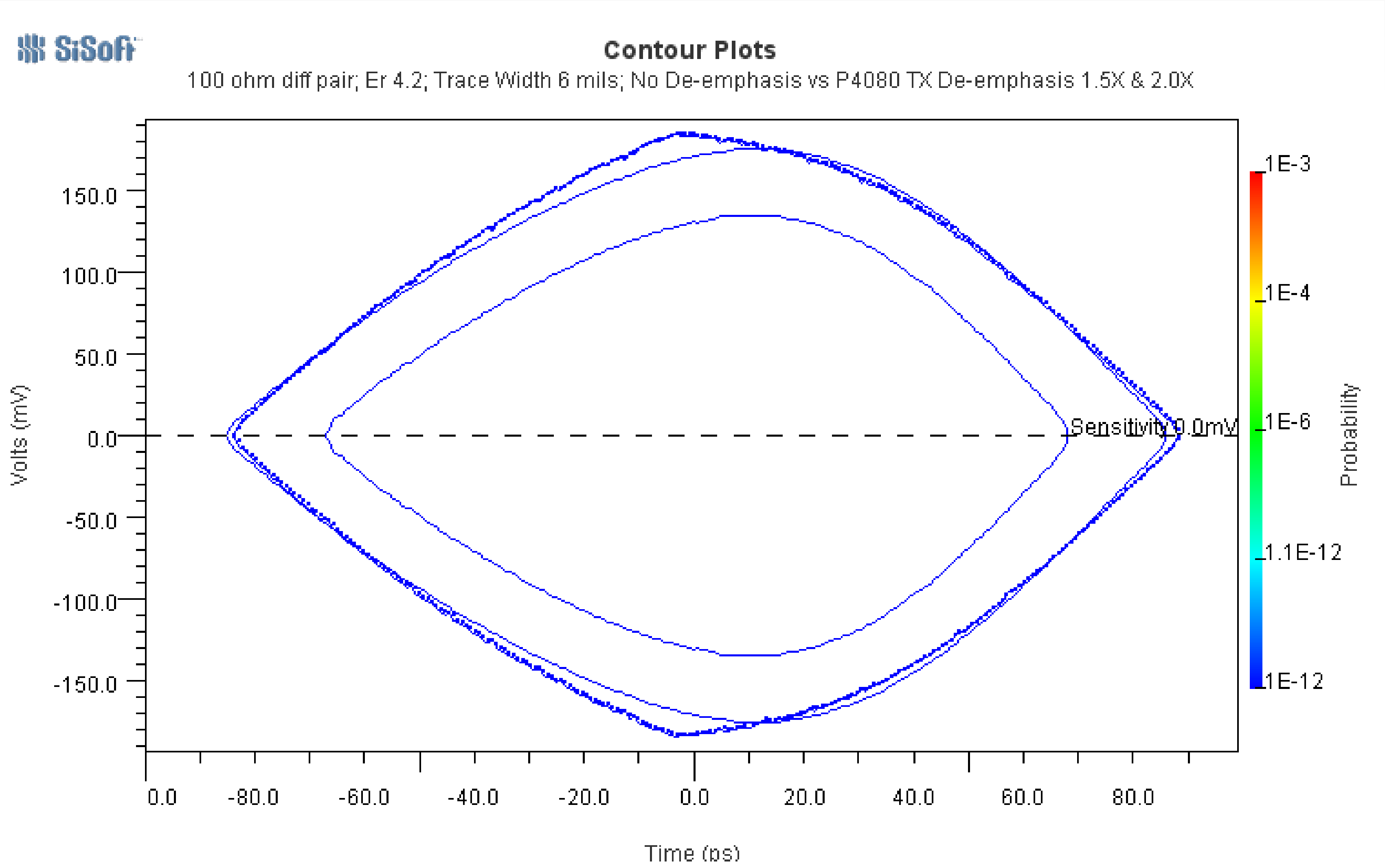
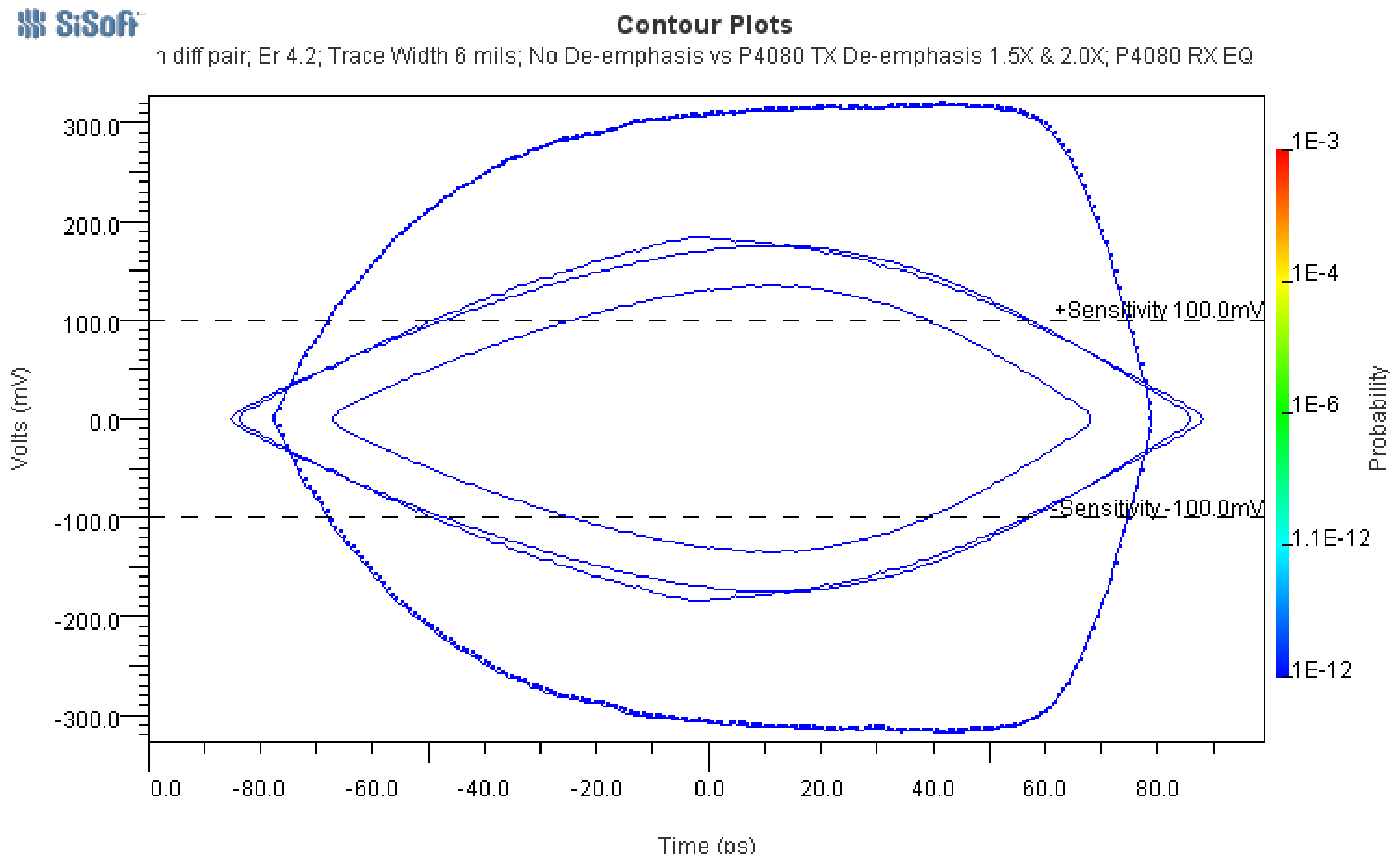
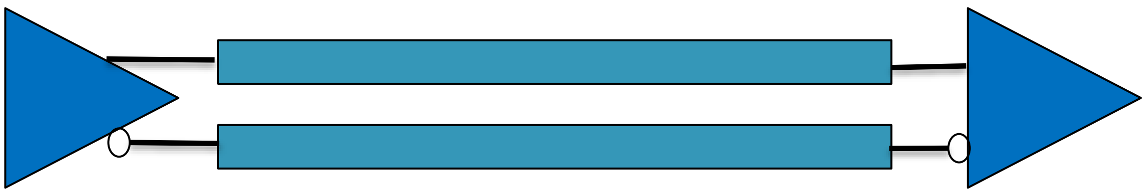
SERDES TX EQ Example: Compare Contours



SERDES RX EQ Example: Compare 6 mil



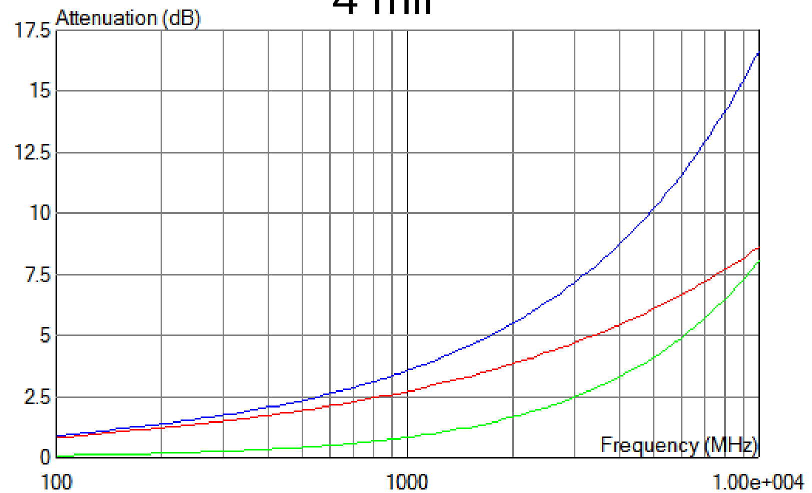
Example Channel: Simulated at 5Gbps with TX EQ



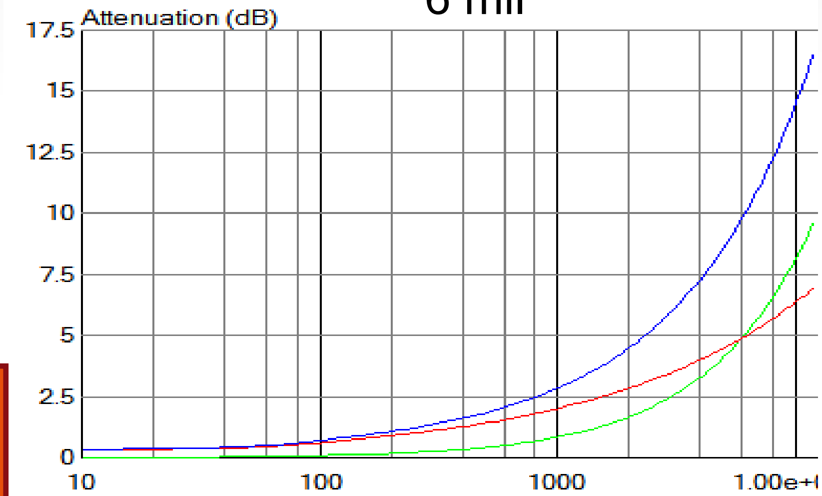
PCB Trace:
- 20 inches
- Dielectric Constant: 4.2
- Loss Tangent: 0.02
- Vary Trace Width:
  - 4, 6, 8, 10, 12 mils

Attenuation: Blue (total), Red (*conductor*), Green (dielectric)

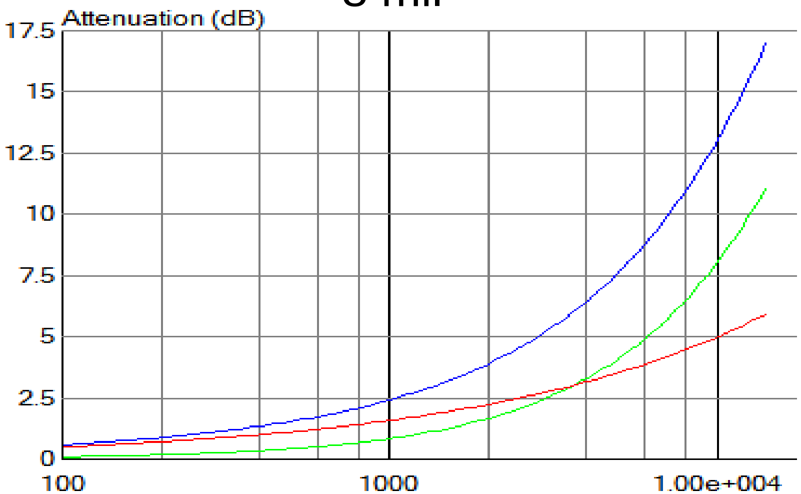
4 mil



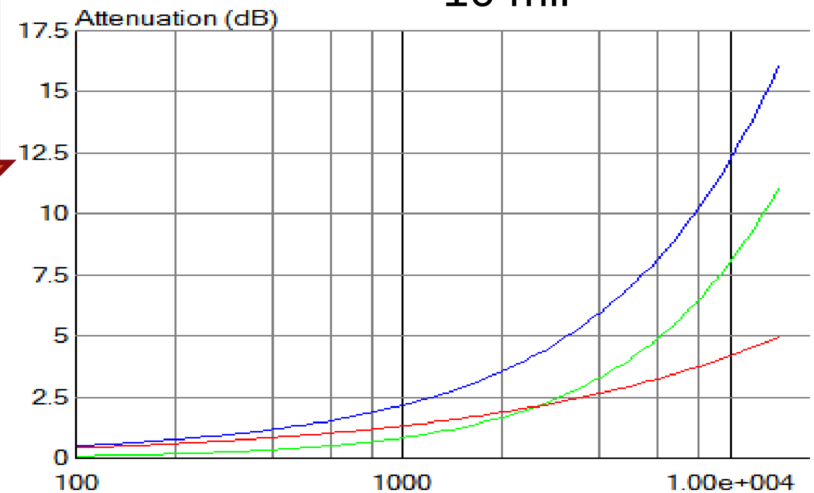
6 mil



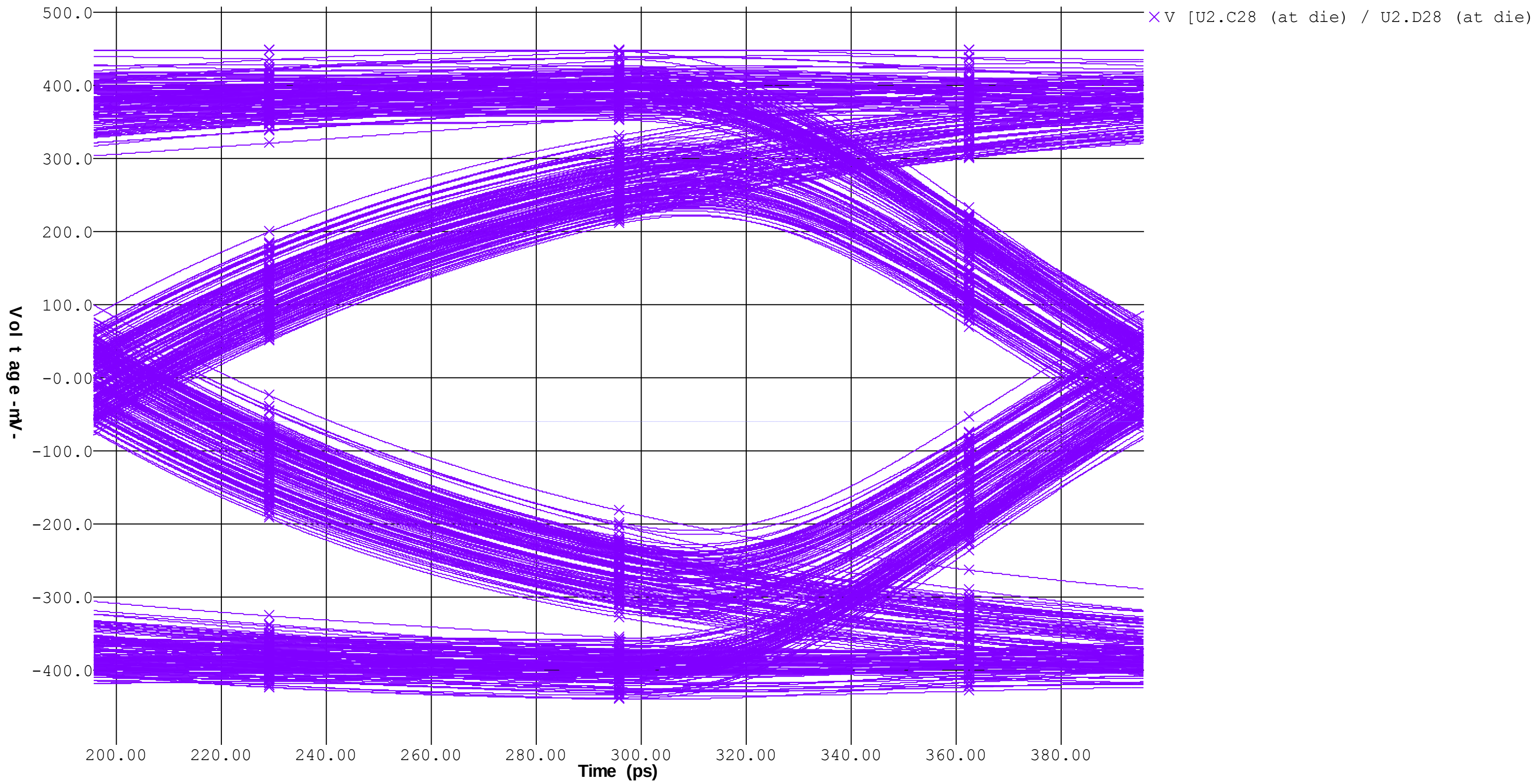
8 mil



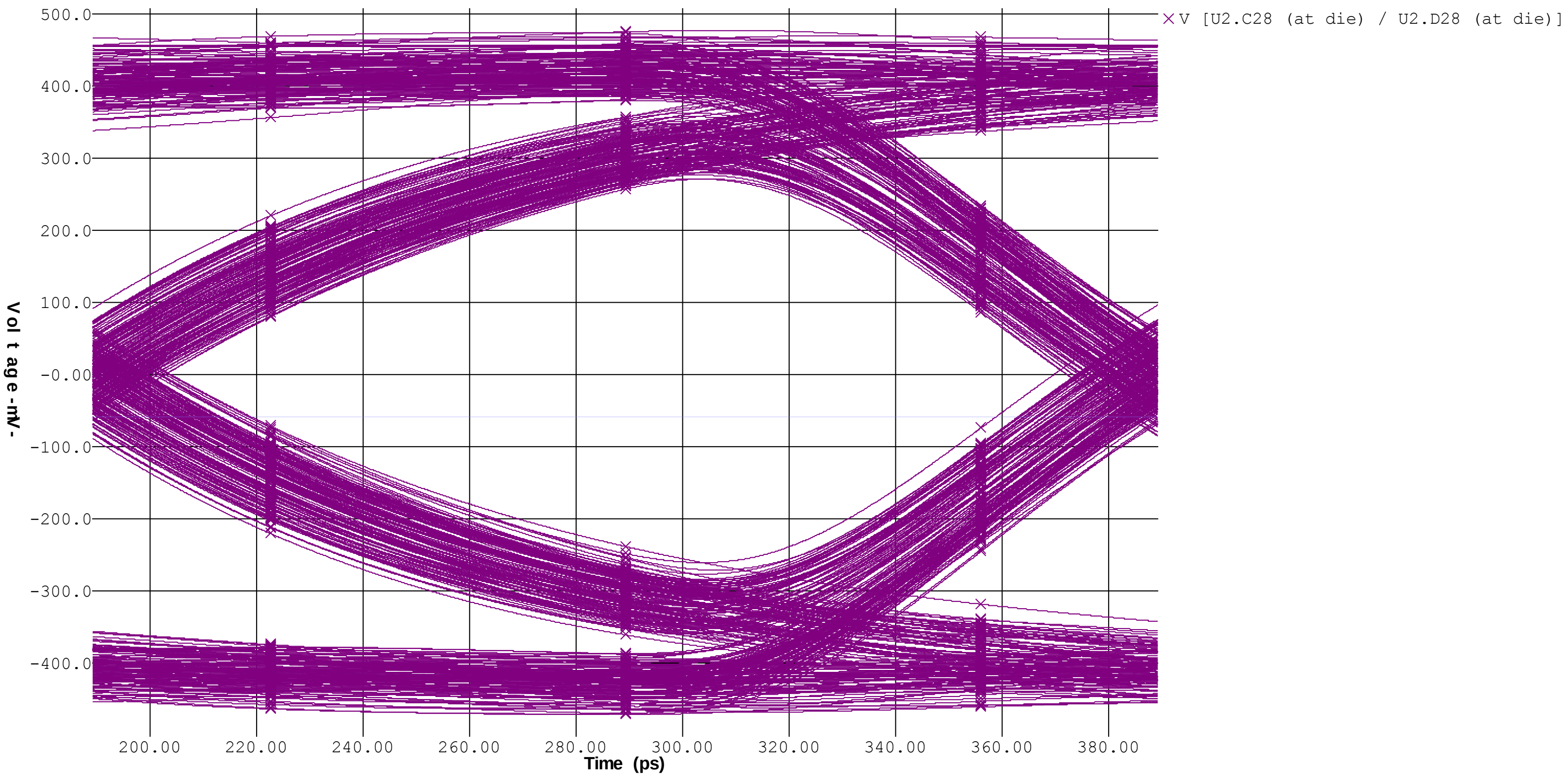
10 mil



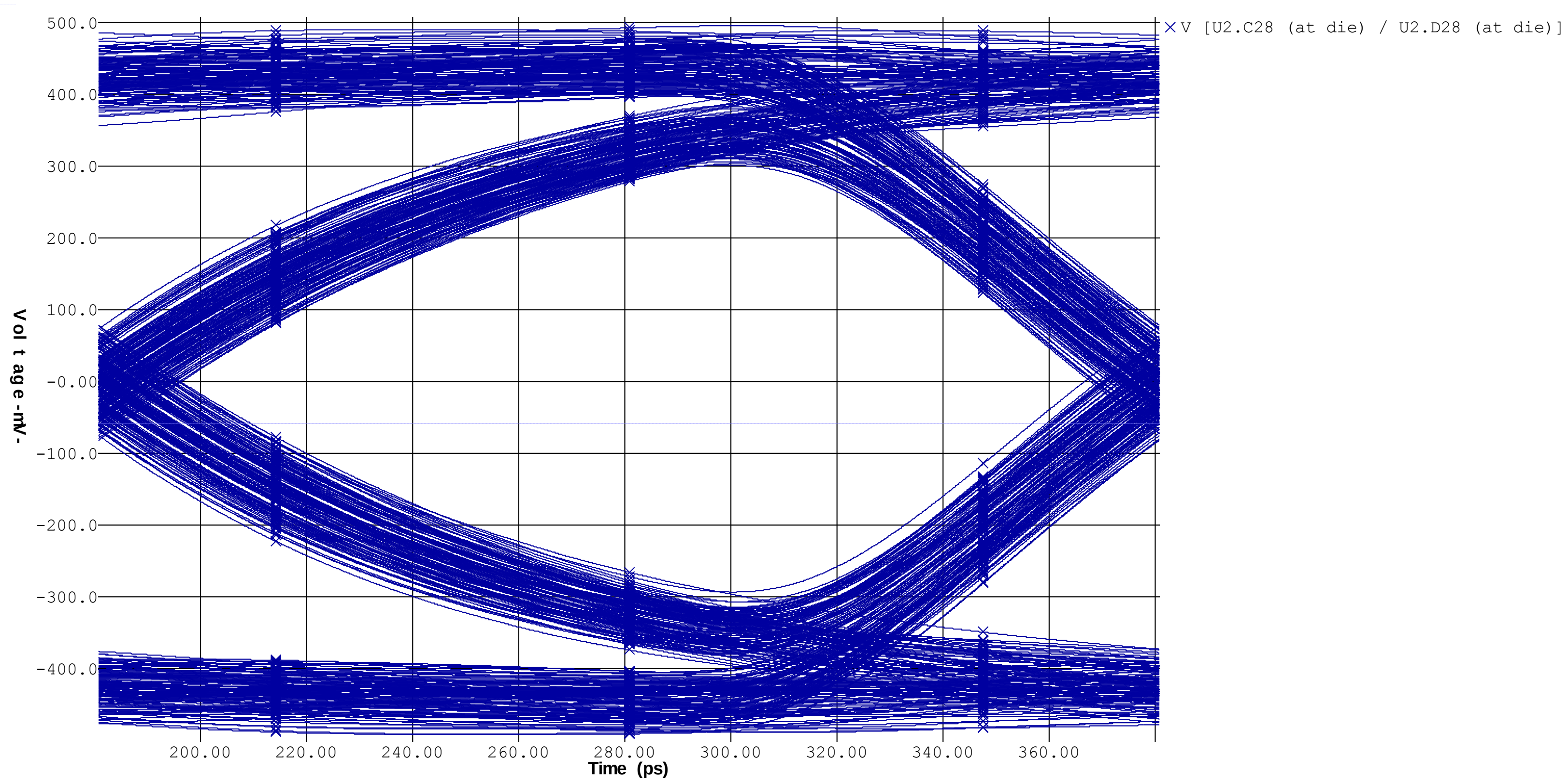
20 inch Trace Width 4 mils:
Eye Width: 152.856 ps Eye Height: 388.5 mV



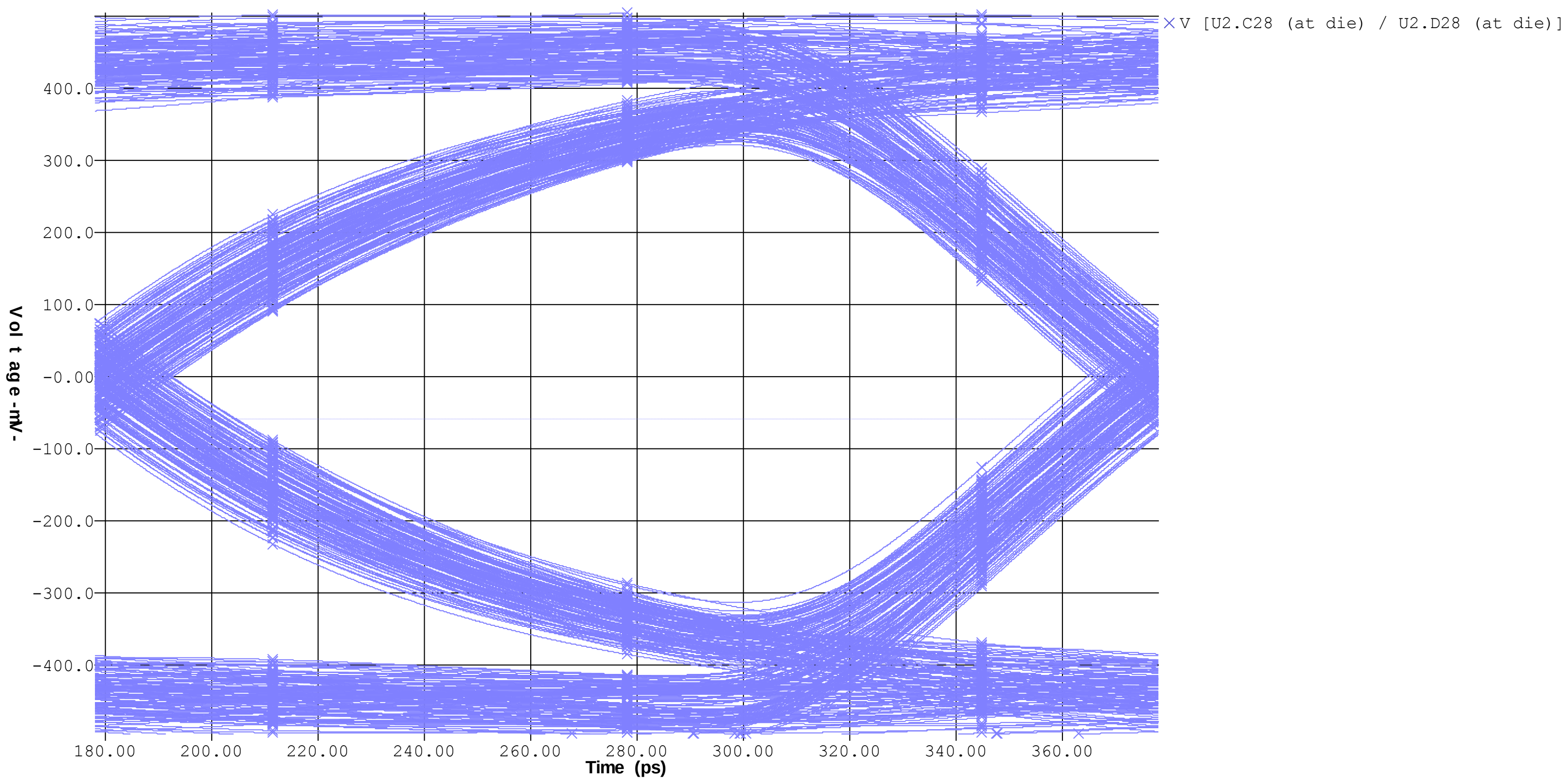
20 inch; Trace Width 6 mils
Eye Width: 164.043 ps Eye Height: 479.1 mV



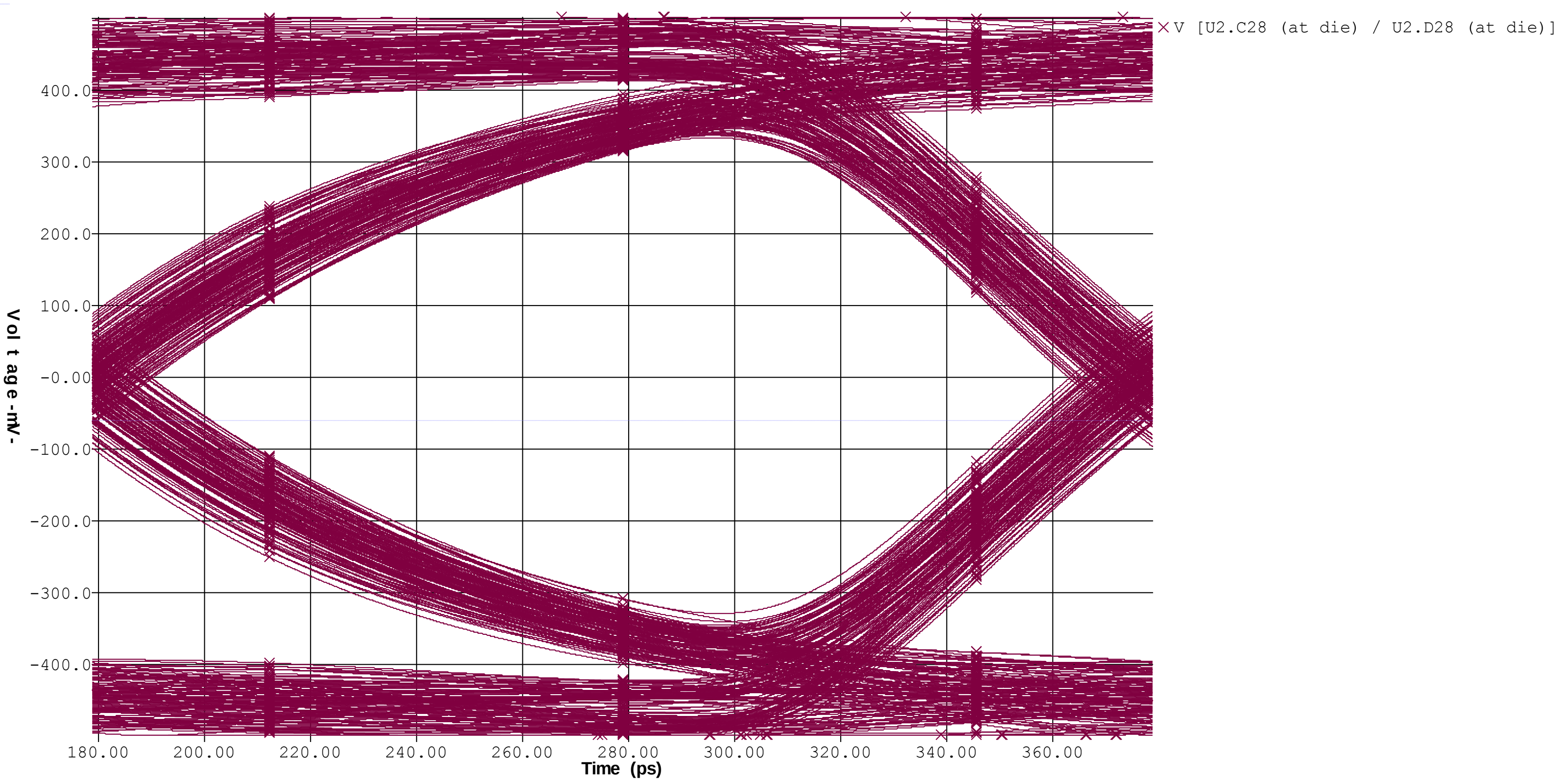
20 inch Trace Width 8 mils
Eye Width: 168.008 ps Eye Height: 540.0 mV



20 inch; Trace Width 10 mils
Eye Width: 169.713 ps Eye Height: 578.9 mV



20 inch, Trace Width 12 mils
Eye Width: 170.687 ps Eye Height: 606.9 mV



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Summary of Eye Attributes from 5Gbps TX IBIS Simulations with De-emphasis for 20 inch Diff Pair of Varied Trace Widths

Trace Width	Eye Height (mV) @ 50% Eye Width	Eye Width (ps)
4 mils	388	153
6 mils	479	164
8 mils	540	168
10 mils	579	170
12 mils	607	171

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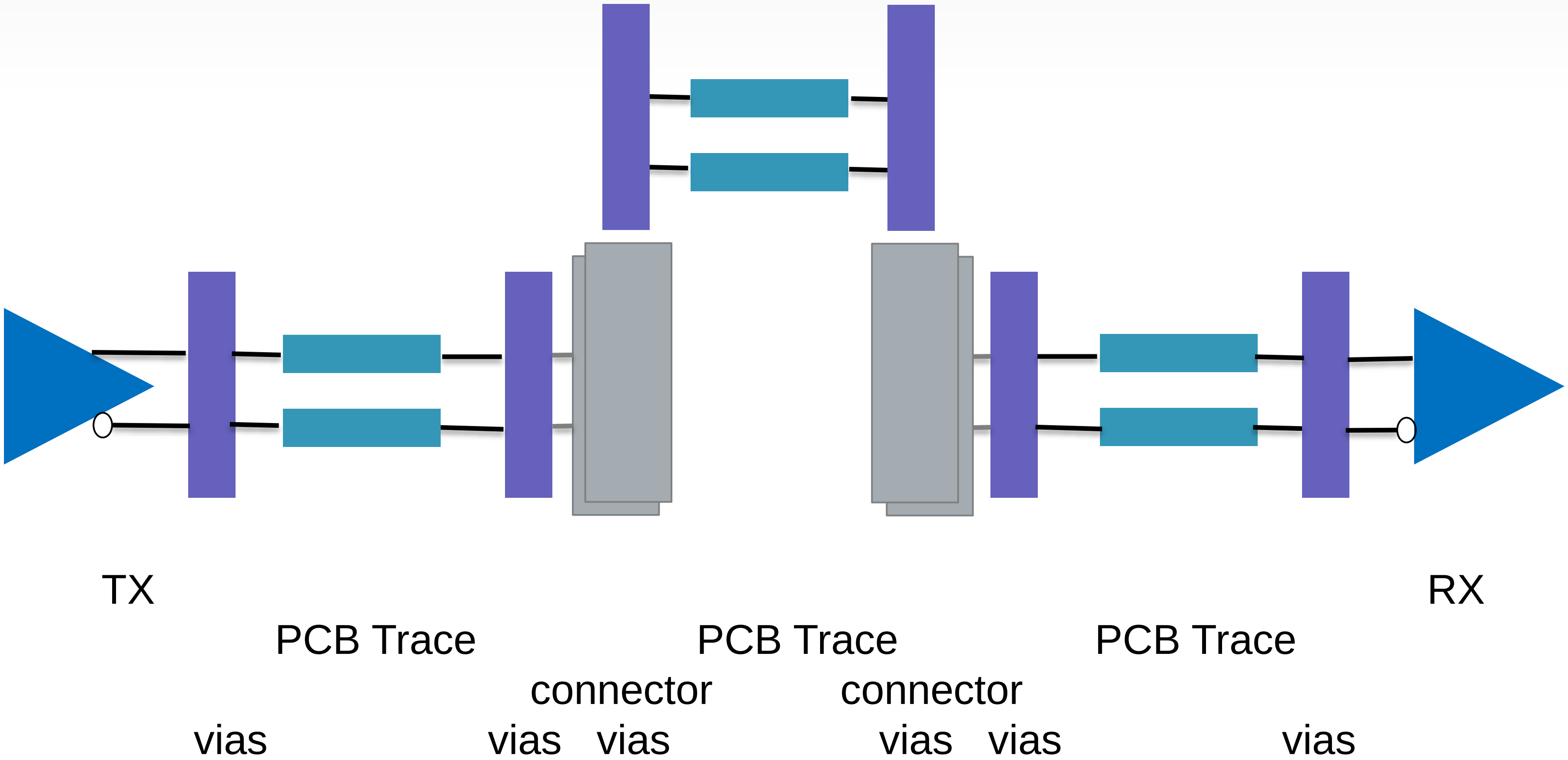
Channel Simulations with and without IBIS-AMI Models

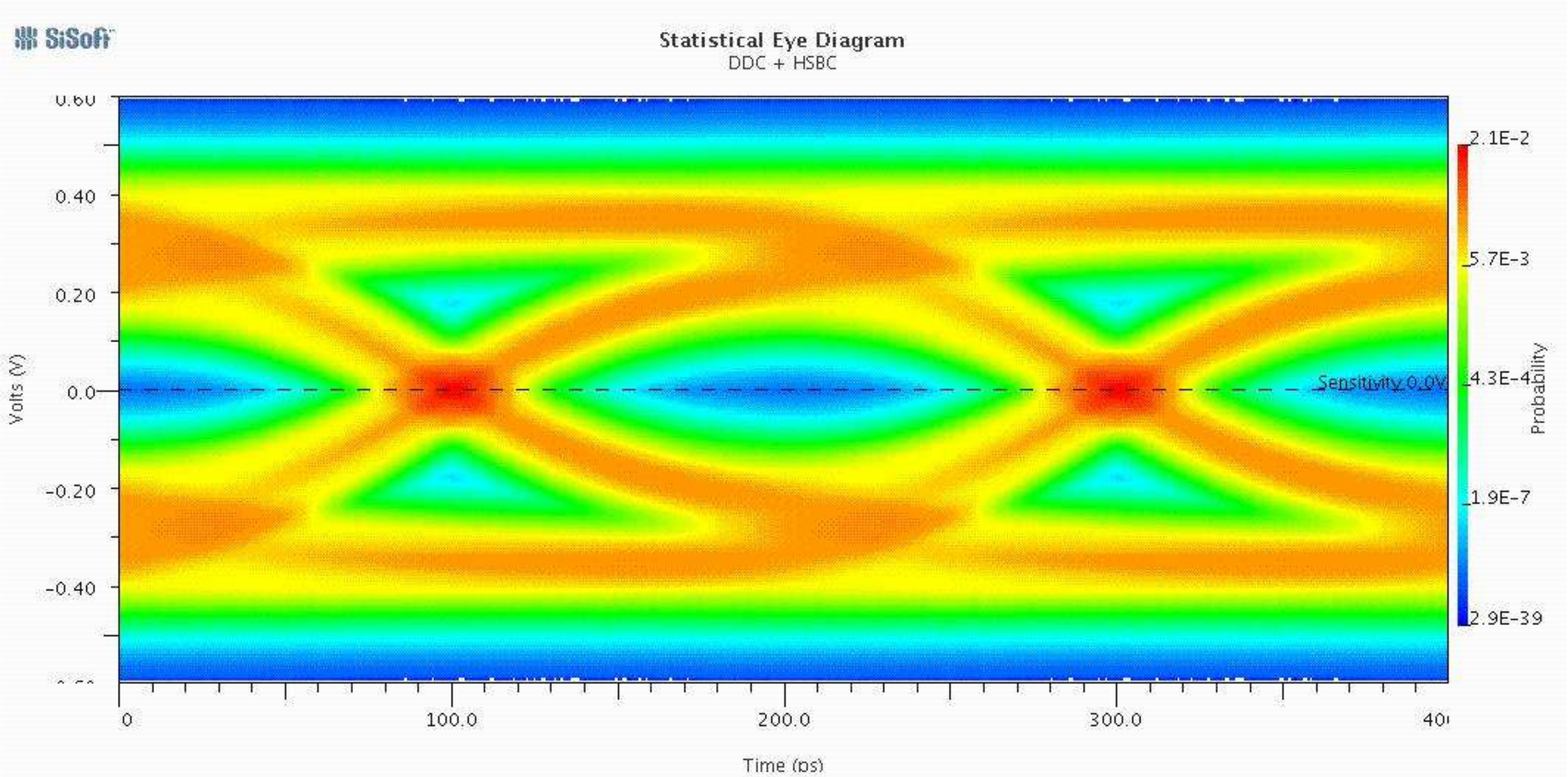
Channel Analysis Example: Multi-Board



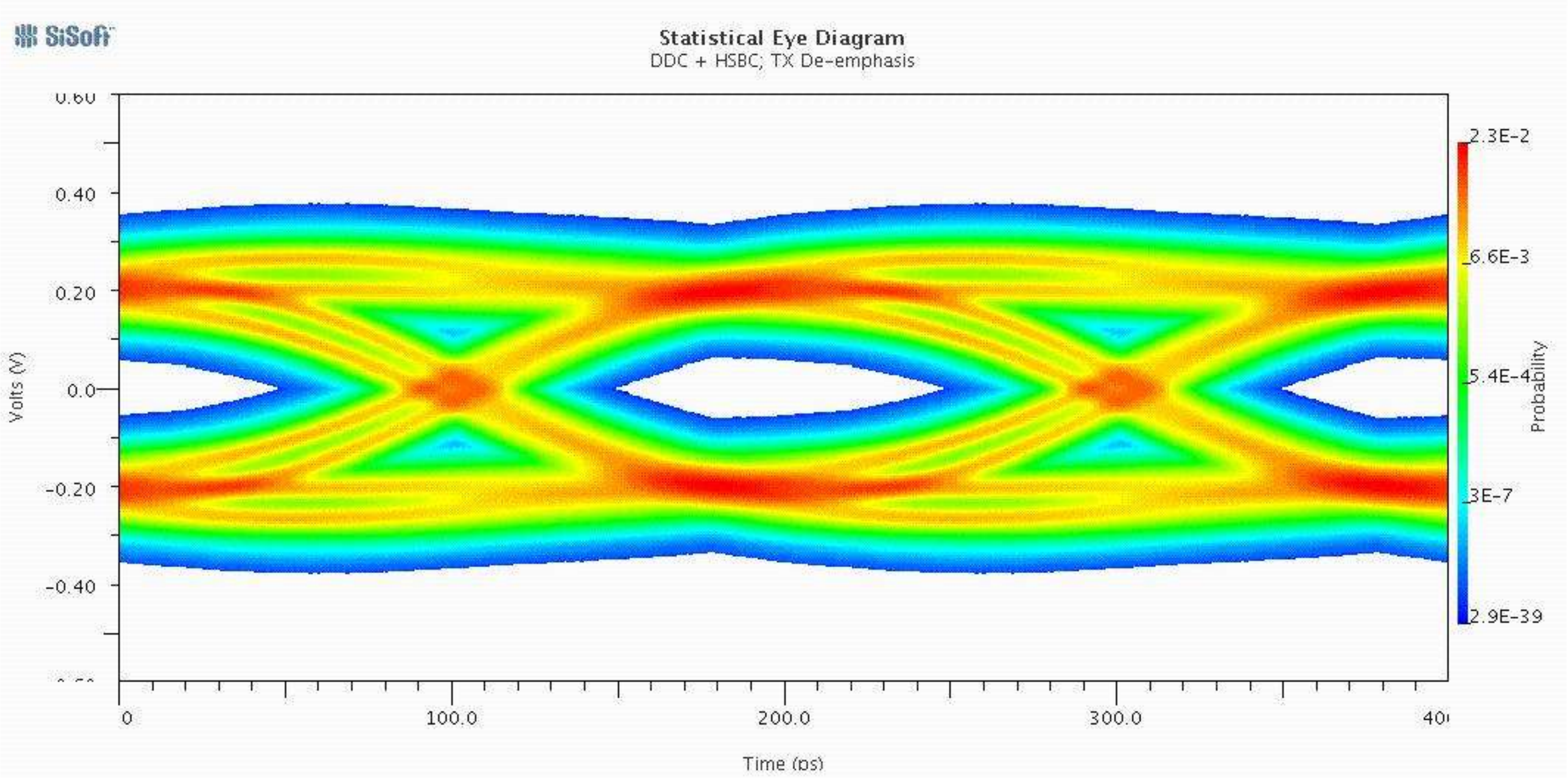
Examples in this section

- Multi-Board Channel 1, 5G, No EQ, TX EQ, RX EQ, TX + RX EQ
- Multi-Board Channel 1, 8G, No EQ, TX EQ, RX EQ, TX + RX EQ
- Multi-Board Channel 2, 5G, TX EQ, TX + RX EQ
- Multi-Board Channel 2, 8G, TX EQ, TX + RX EQ
- Multi-Board Channel 2, 10G, TX + RX EQ
- Multi-Board Channel 2, 8G, TX + RX EQ → sweep TX EQ values

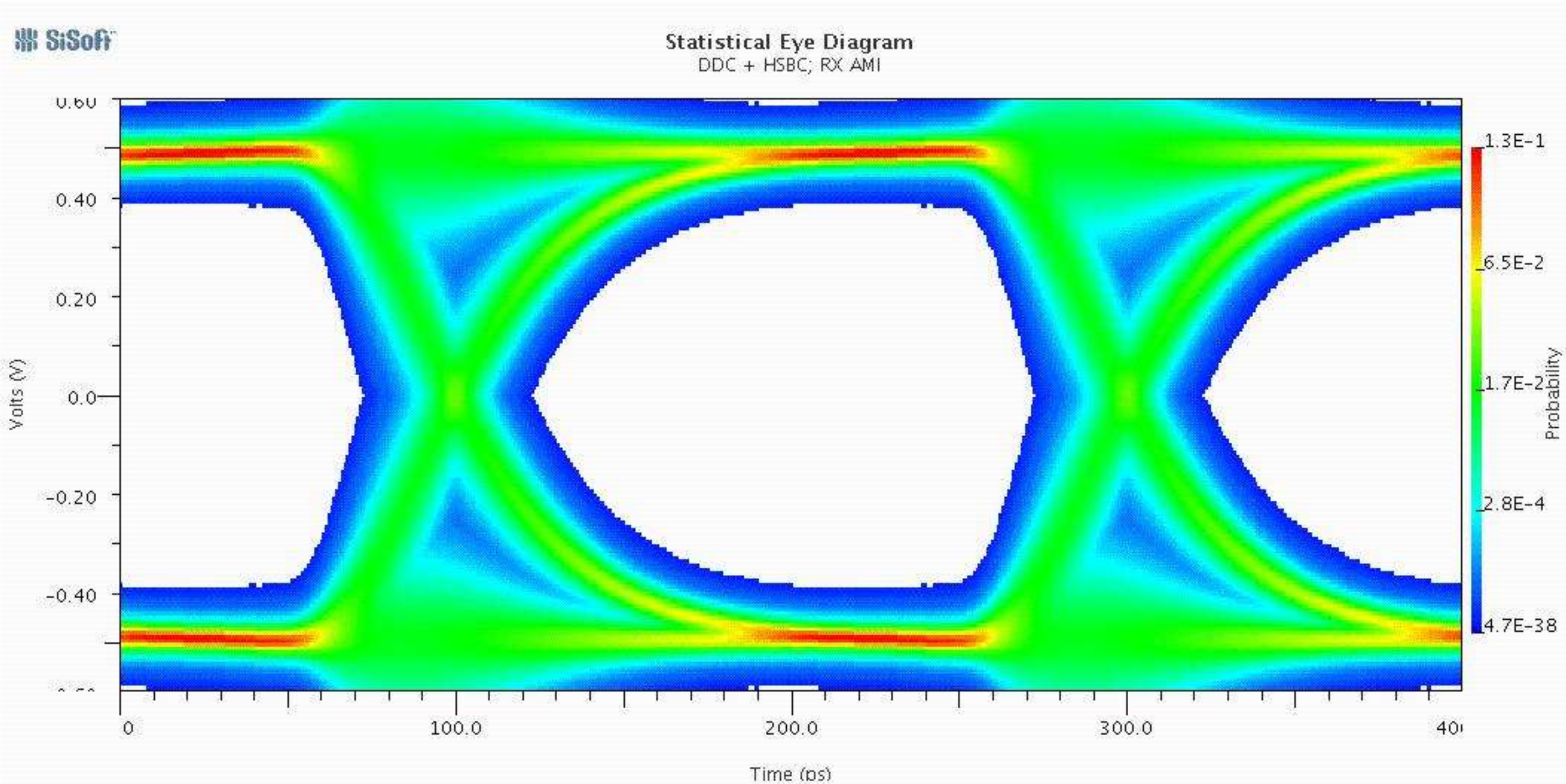
Multi-Board 5G: No TX EQ, No RX EQ



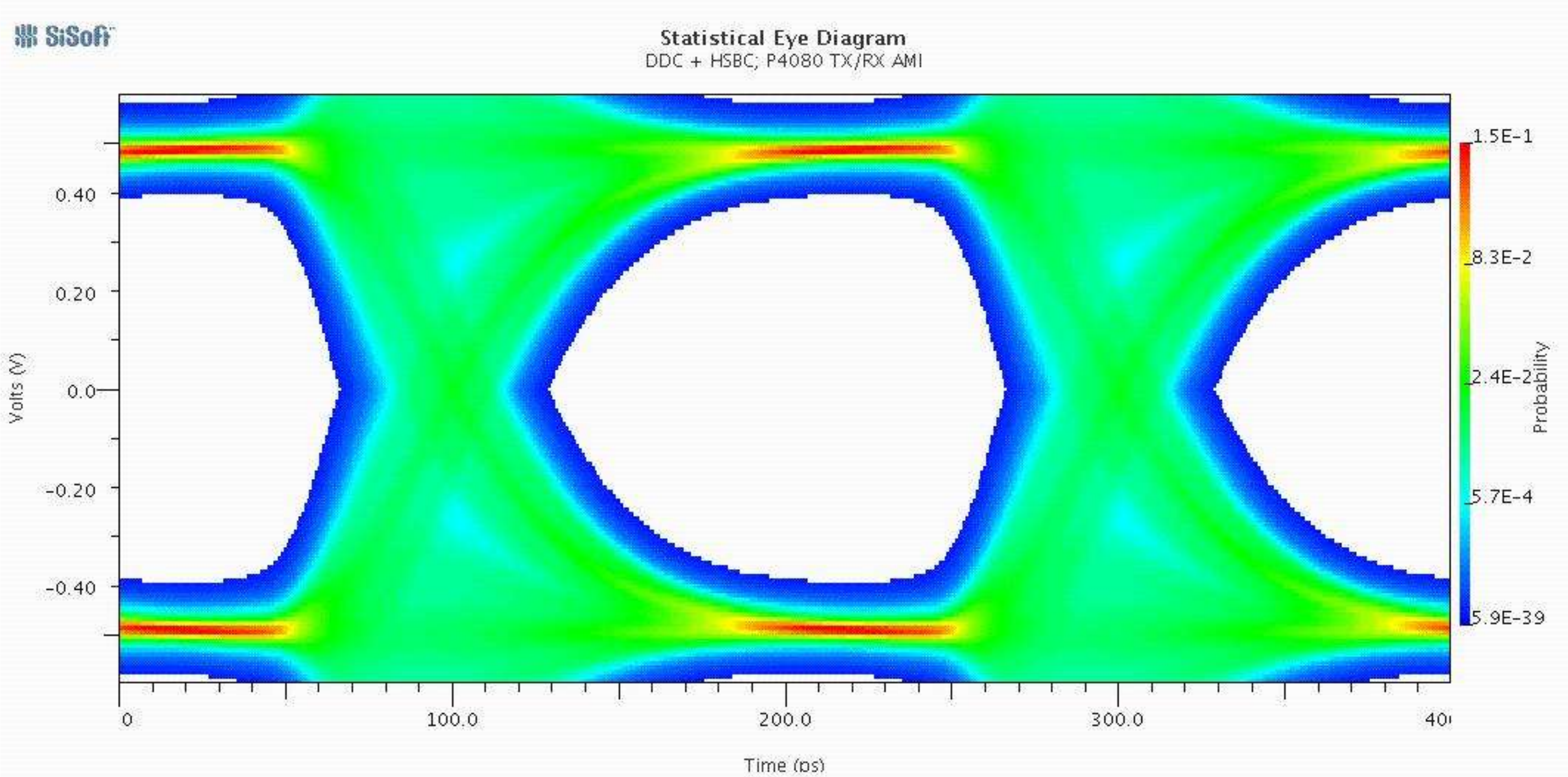
Multi-Board 5G: TX EQ, No RX EQ



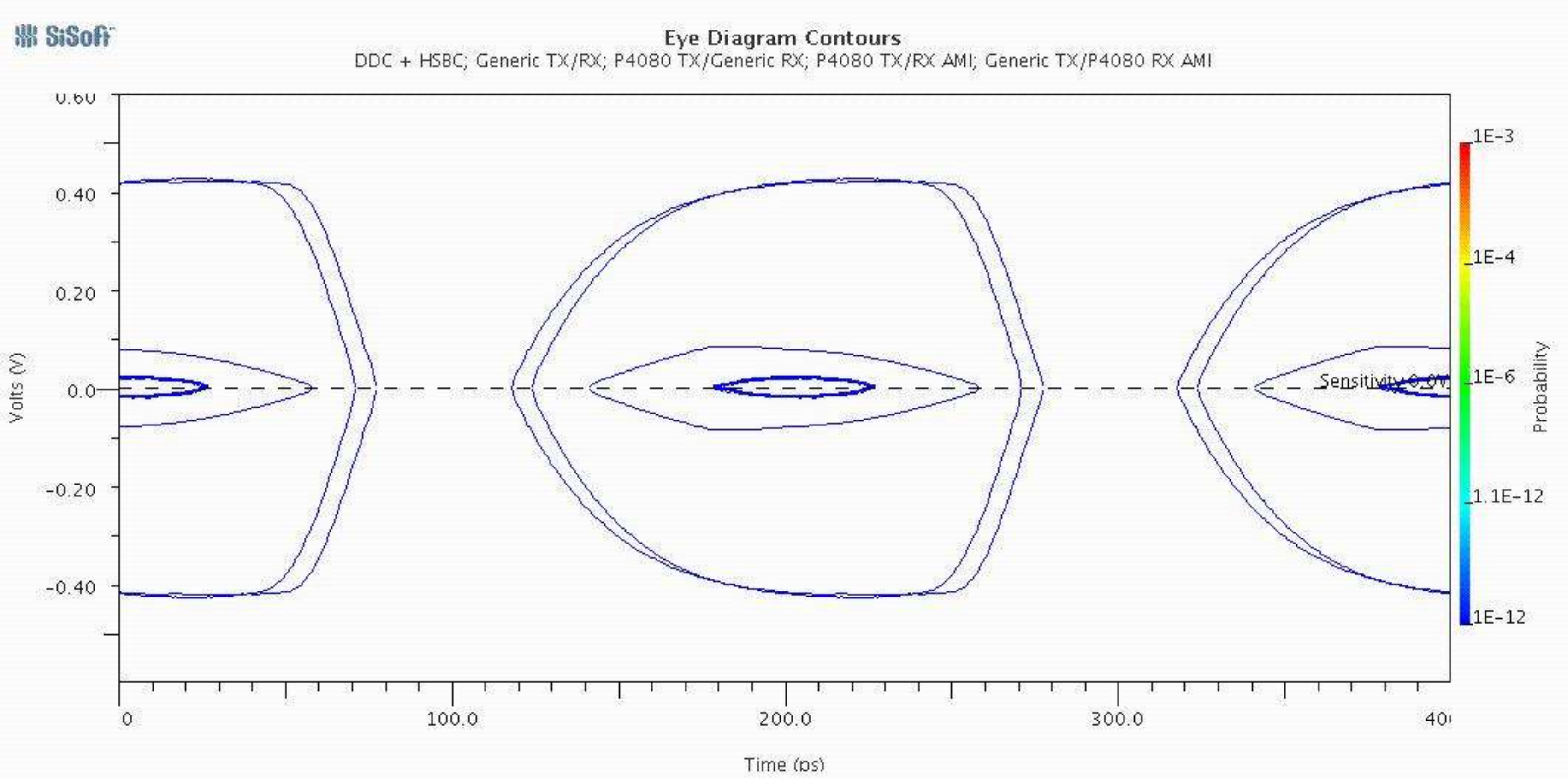
Multi-Board 5G: TX No EQ, RX EQ



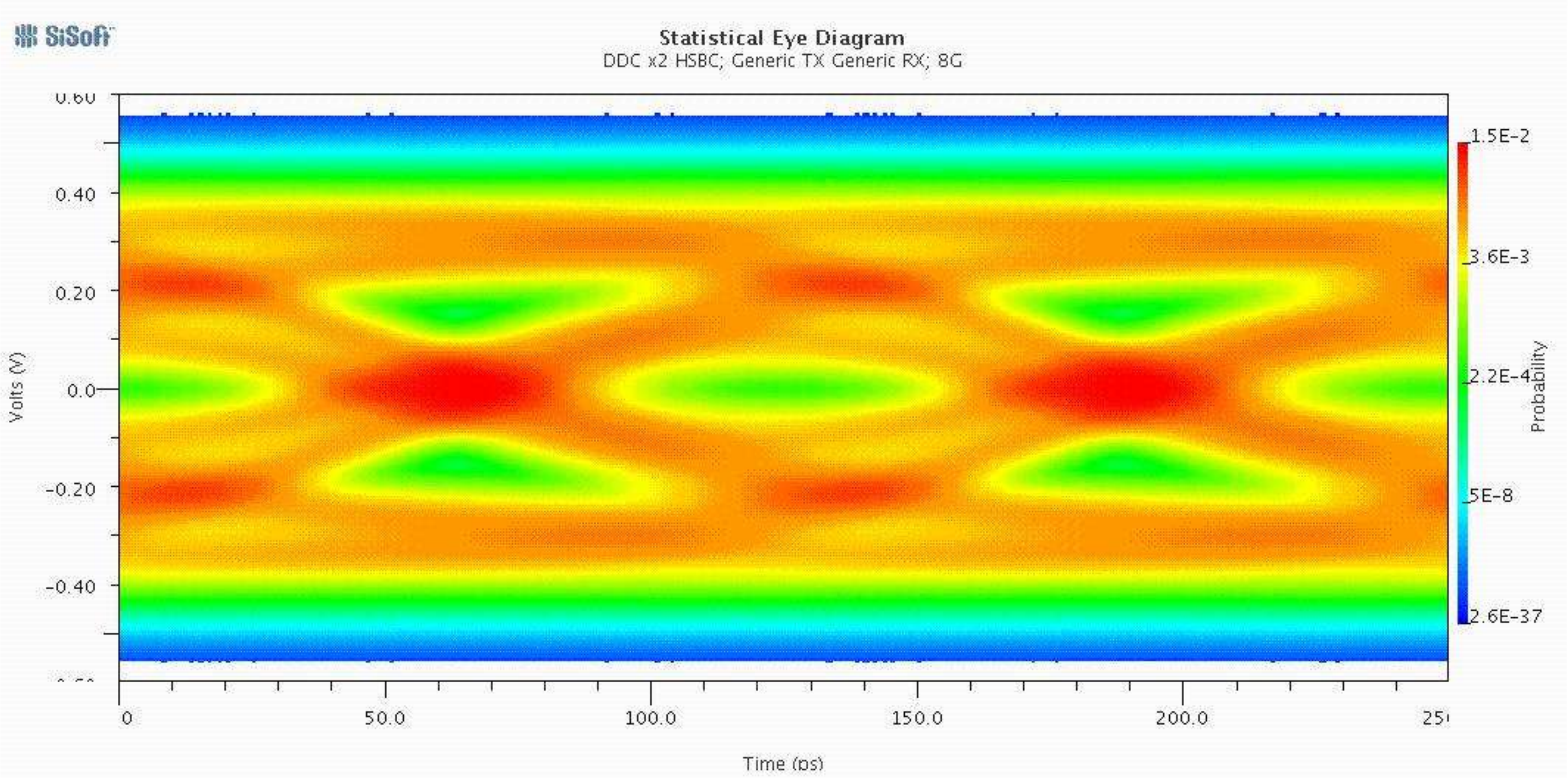
Multi-Board 5G: TX EQ, RX EQ



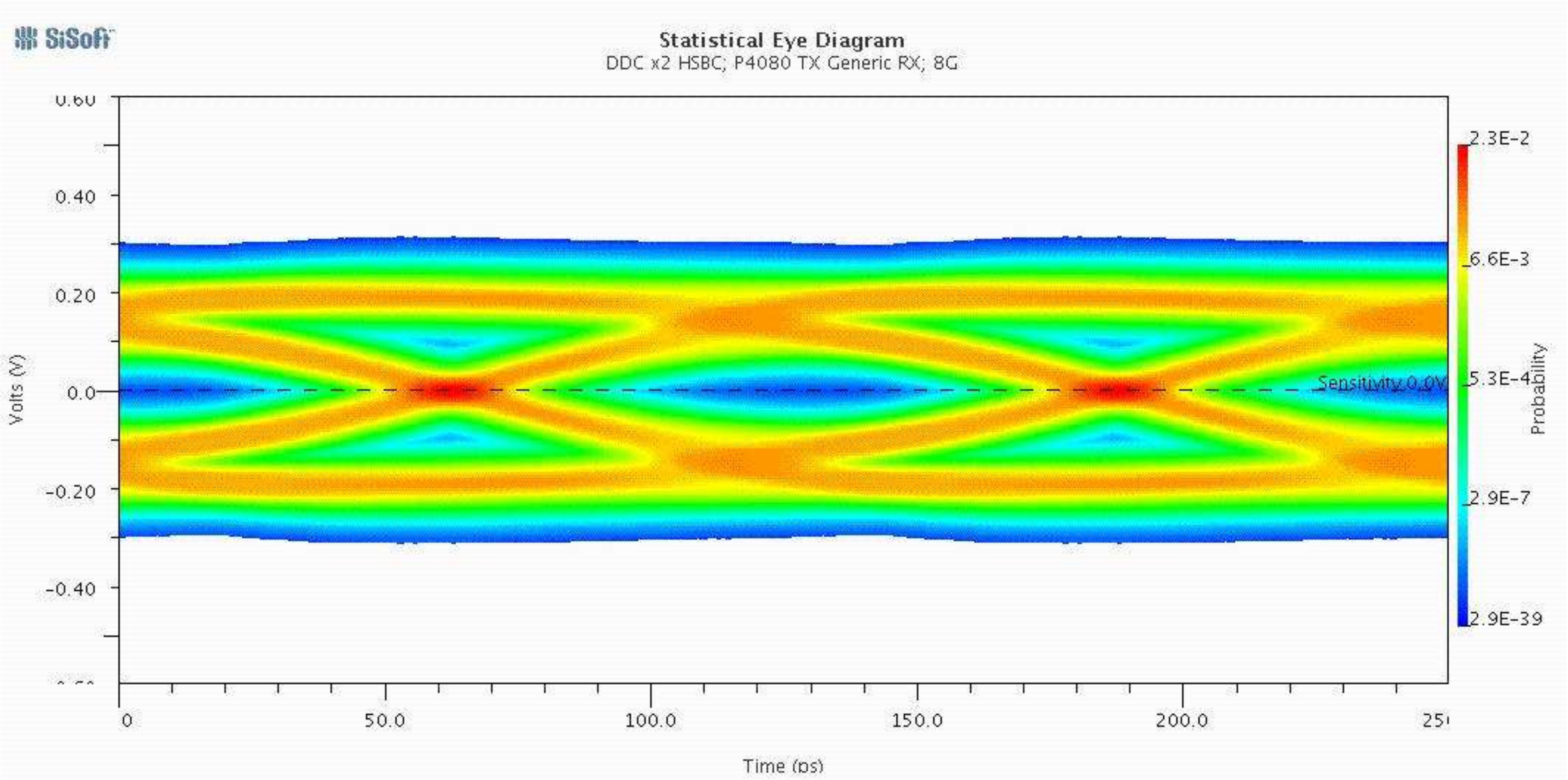
Compare Multi-Board Schemes 5G



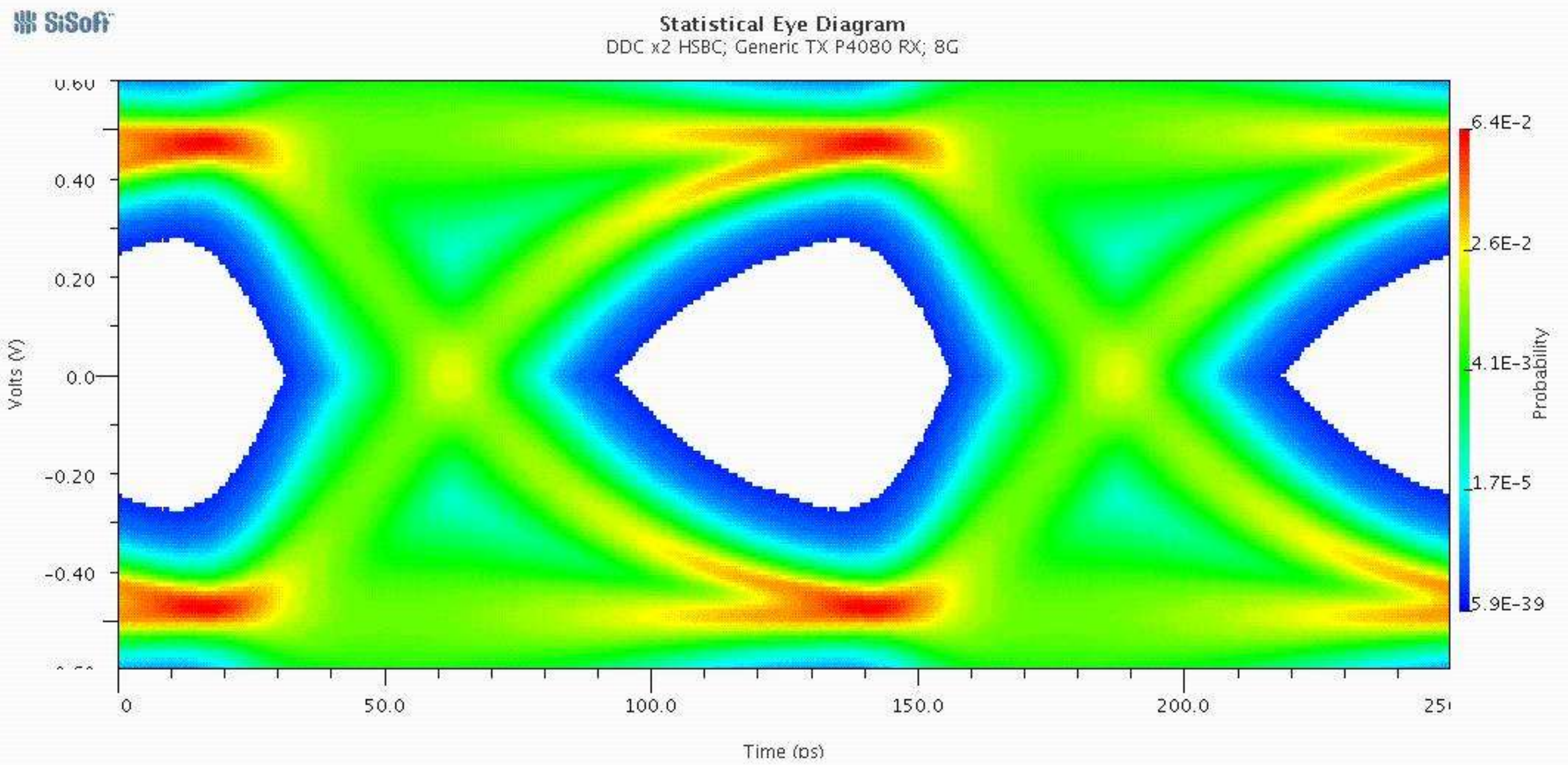
Multi-Board 8G: No TX EQ, No RX EQ



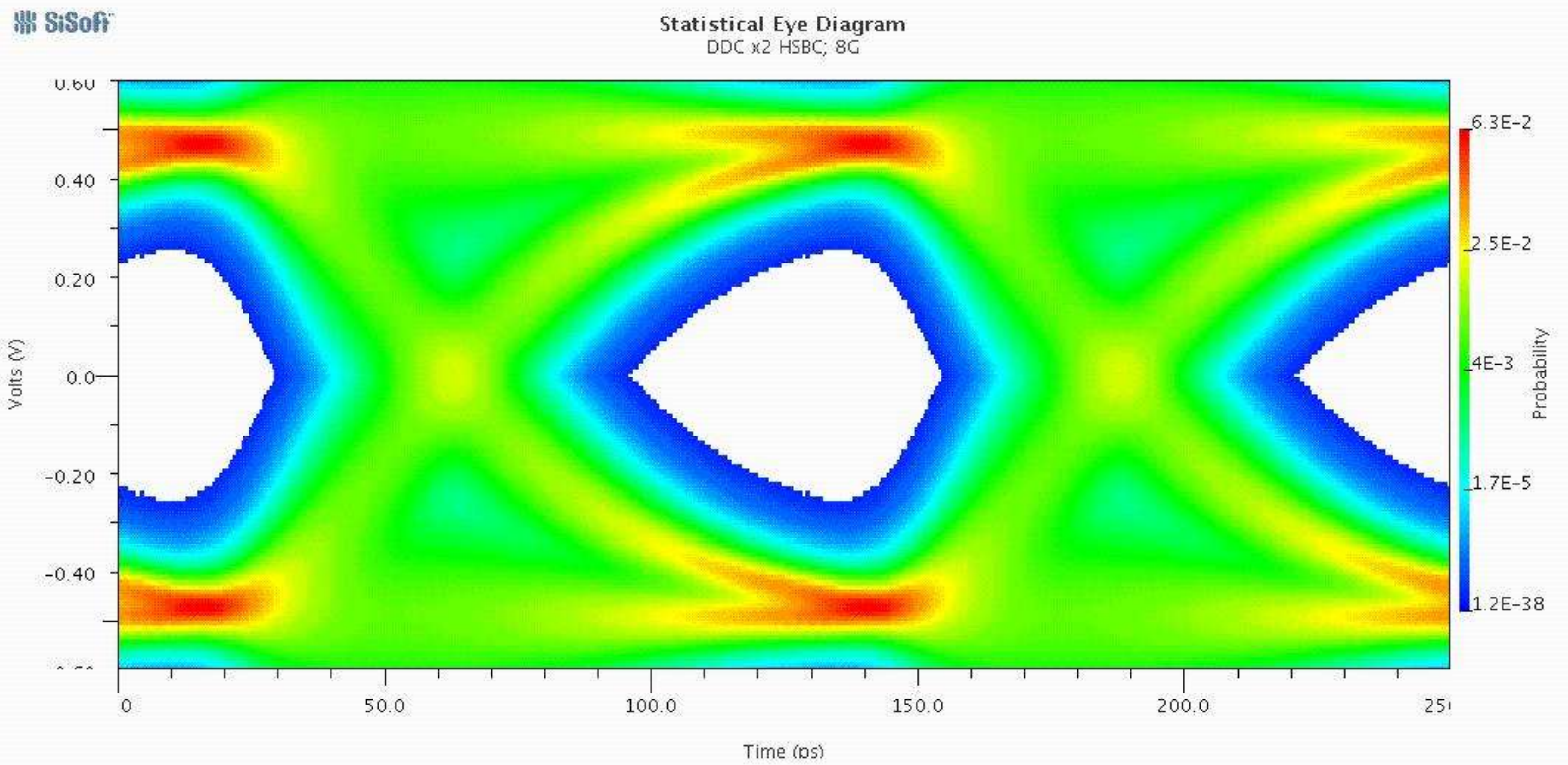
Multi-Board 8G: TX EQ, No RX EQ



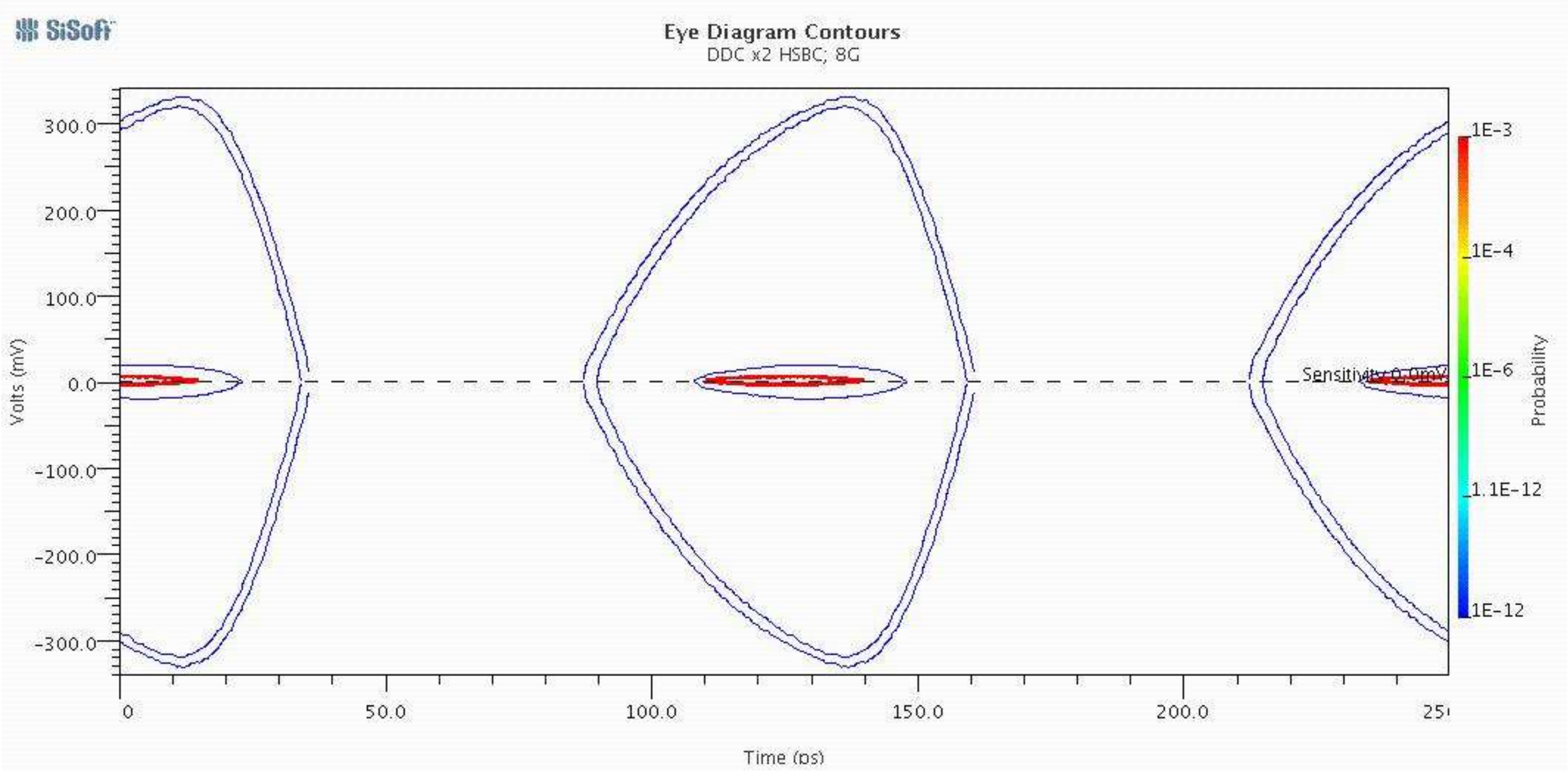
Multi-Board 8G: TX No EQ, RX EQ



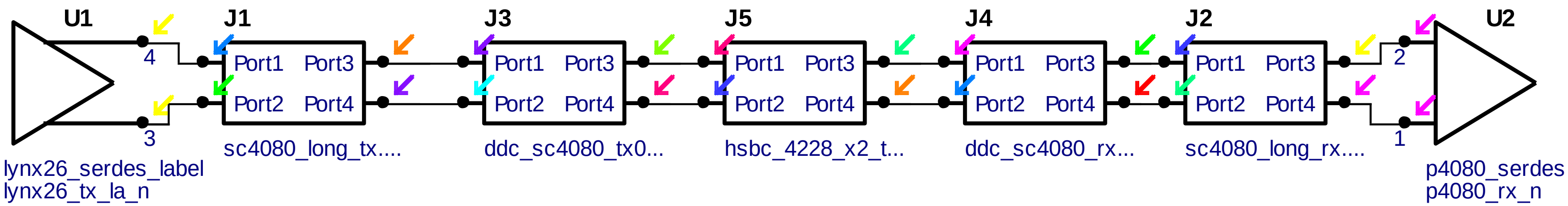
Multi-Board 8G: TX EQ, RX EQ



Compare Multi-Board Schemes 8G



SERDES 5G, Channel 2 with package models, RX: at 5Gbps



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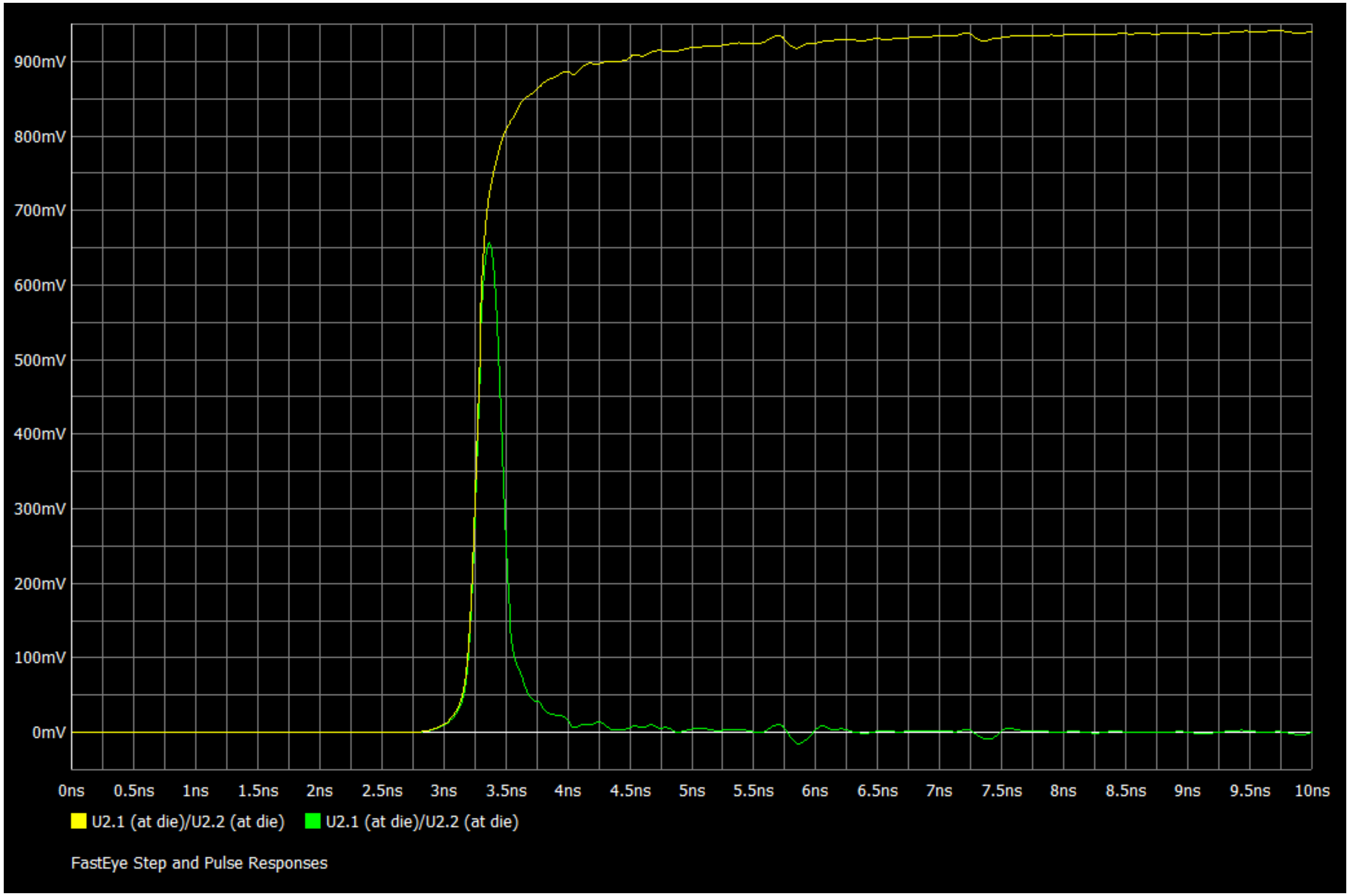
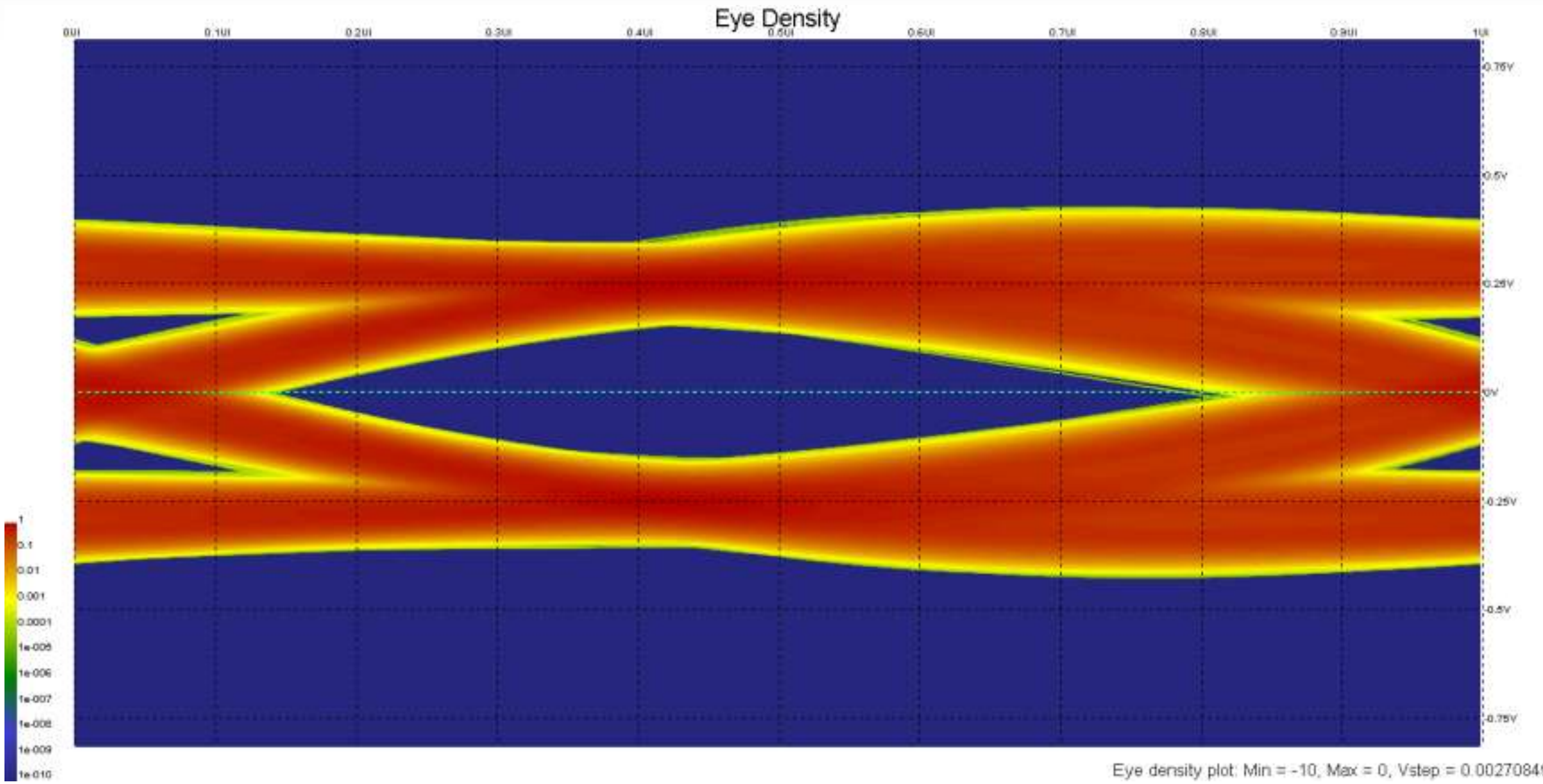
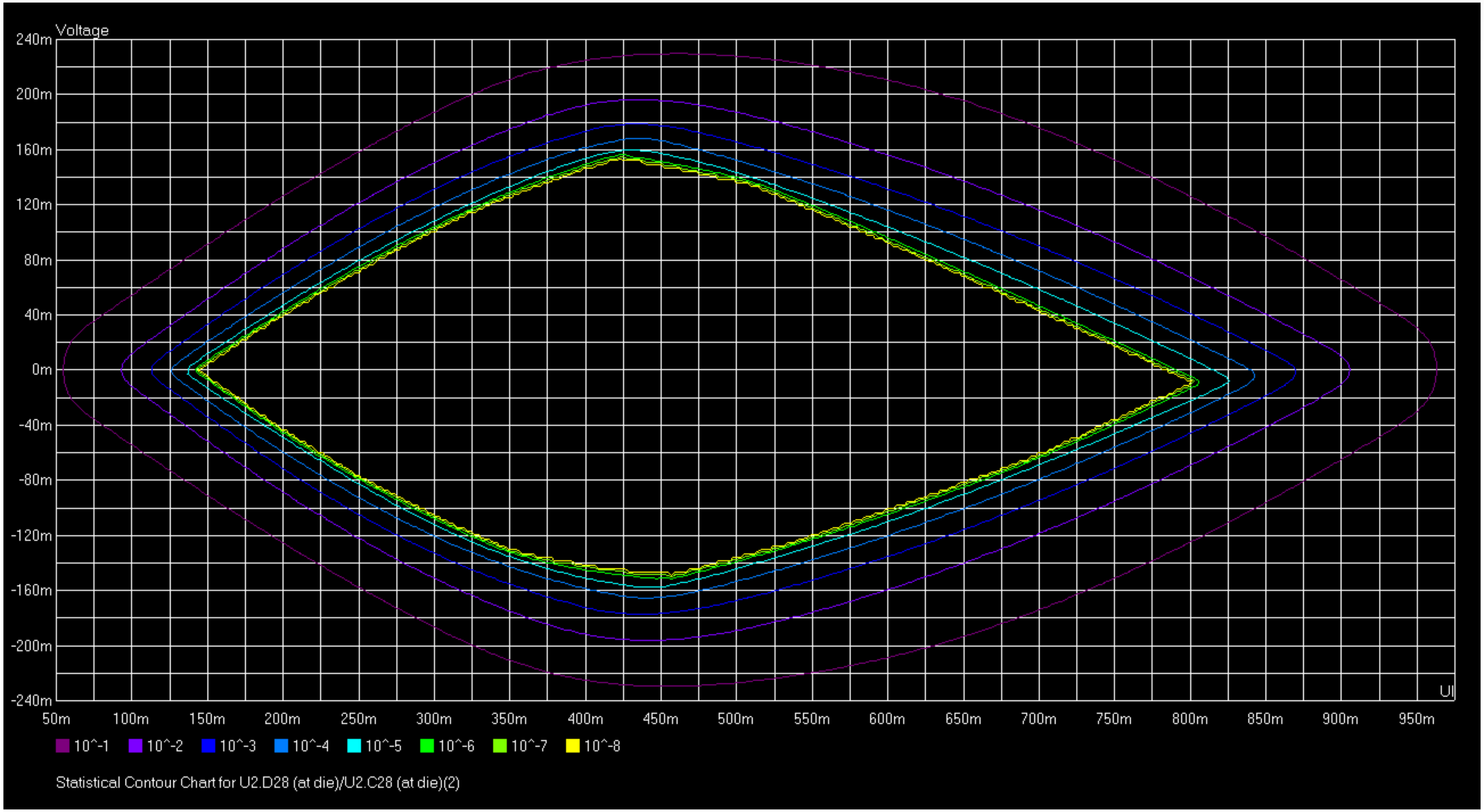
SERDES 5G, Channel 2 with package models, RX no AMI: at 5Gbps



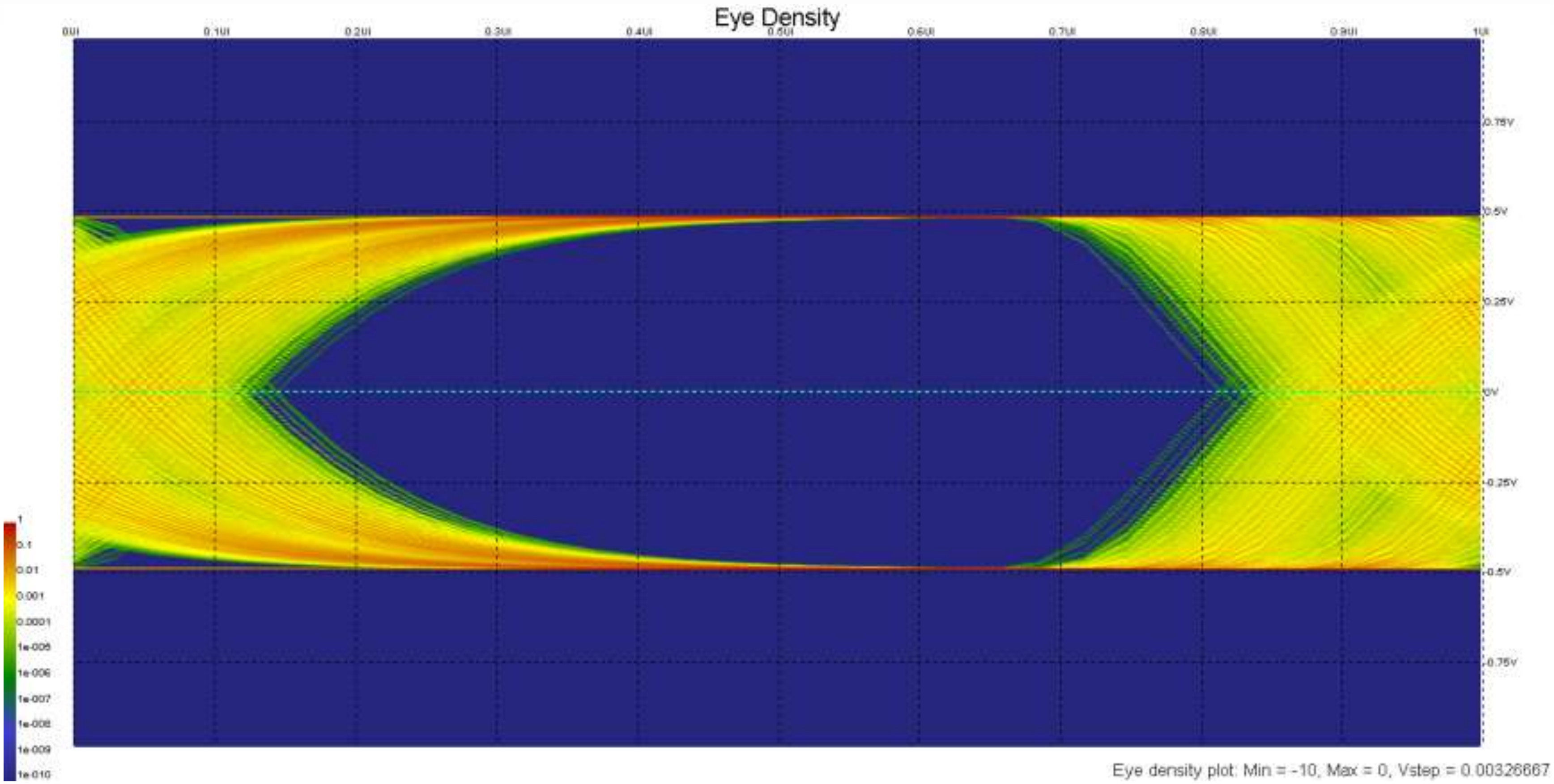
SERDES 5G, Channel 2 with package models, RX no AMI: at 5Gbps



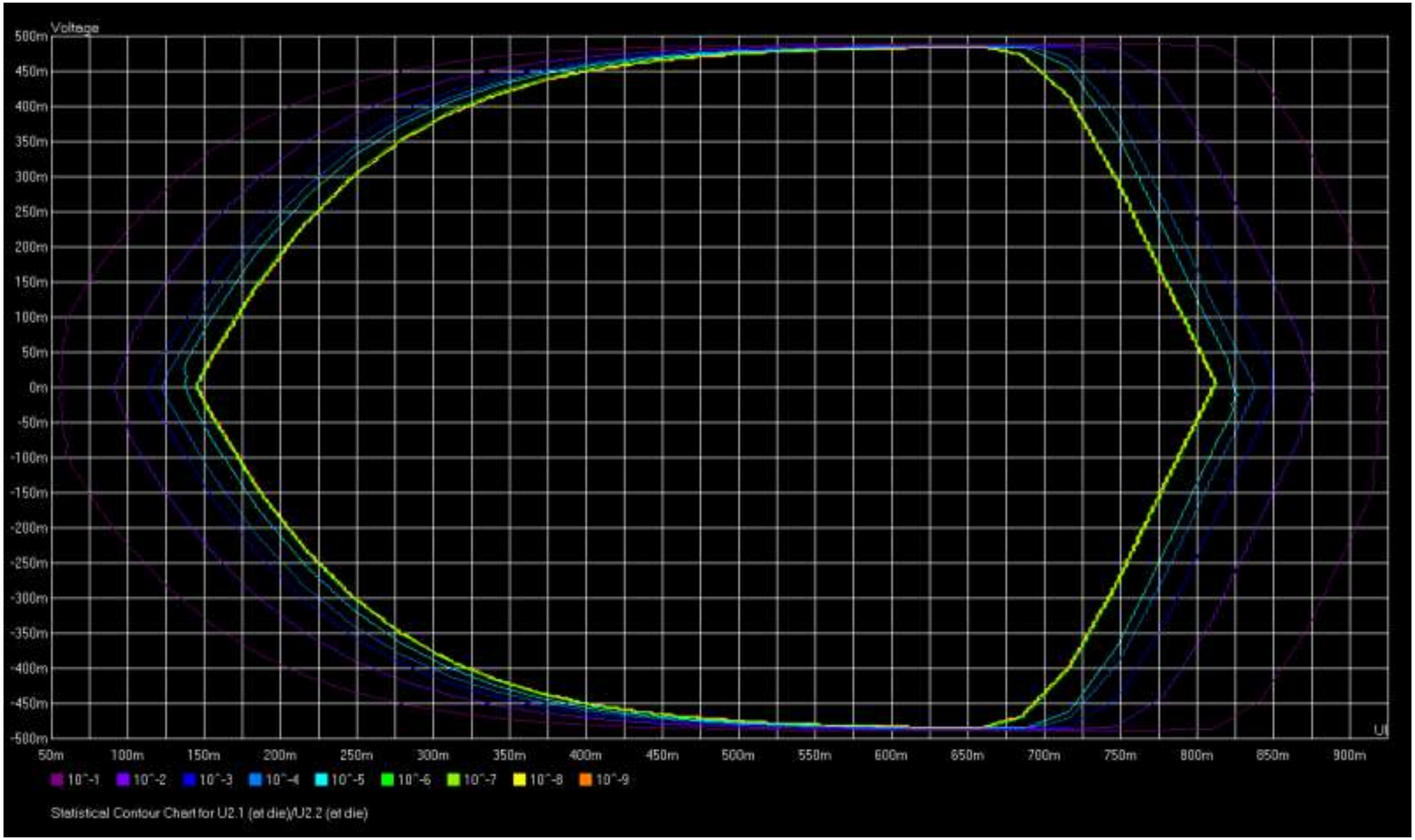
SERDES 5G, Channel 2 with package models, RX no AMI: at 5Gbps



SERDES 5G, Channel 2 with package models, RX AMI: at 5Gbps



SERDES 5G, Channel 2 with package models, RX AMI: at 5Gbps



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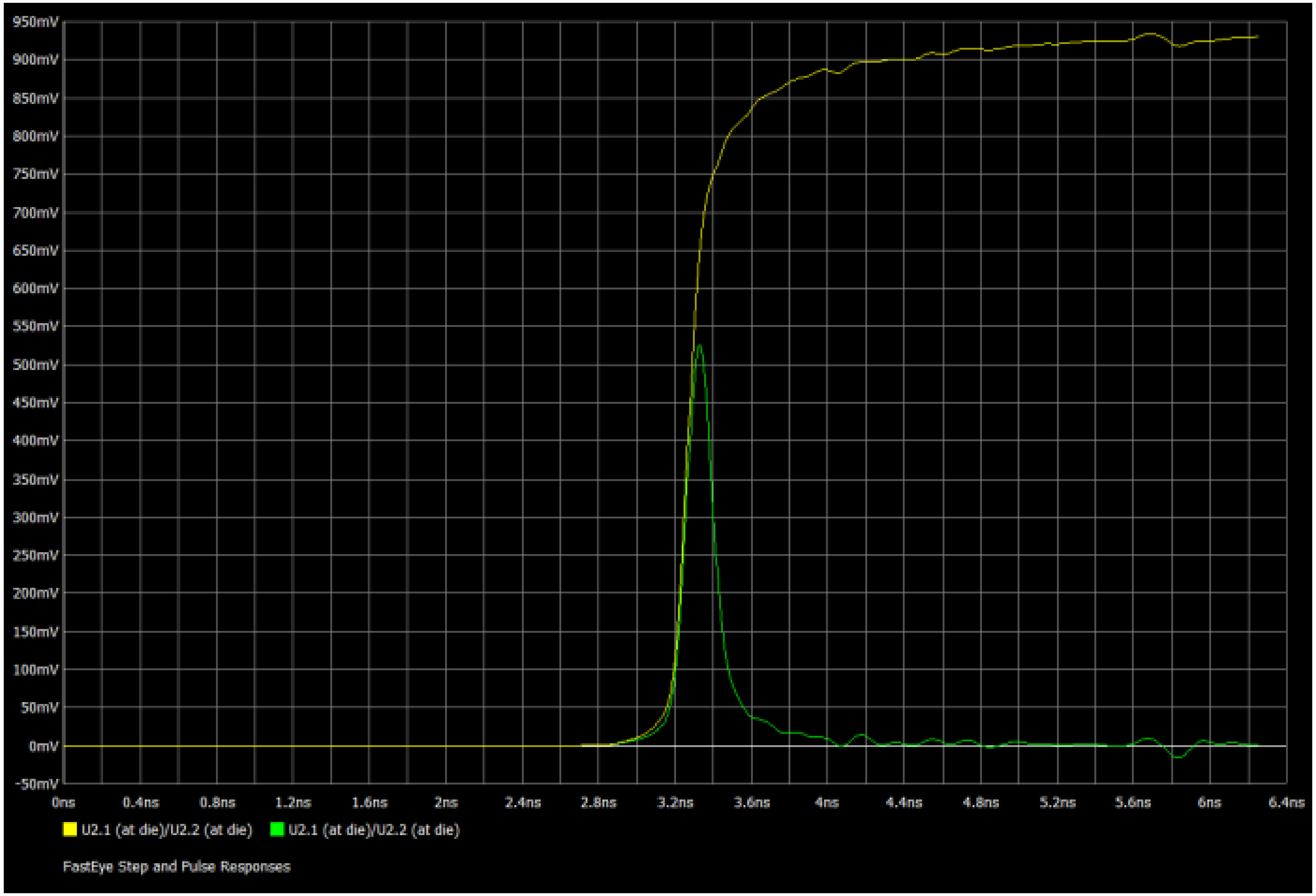
SERDES 5G, Channel 2 with package models, RX no AMI: at 8Gbps



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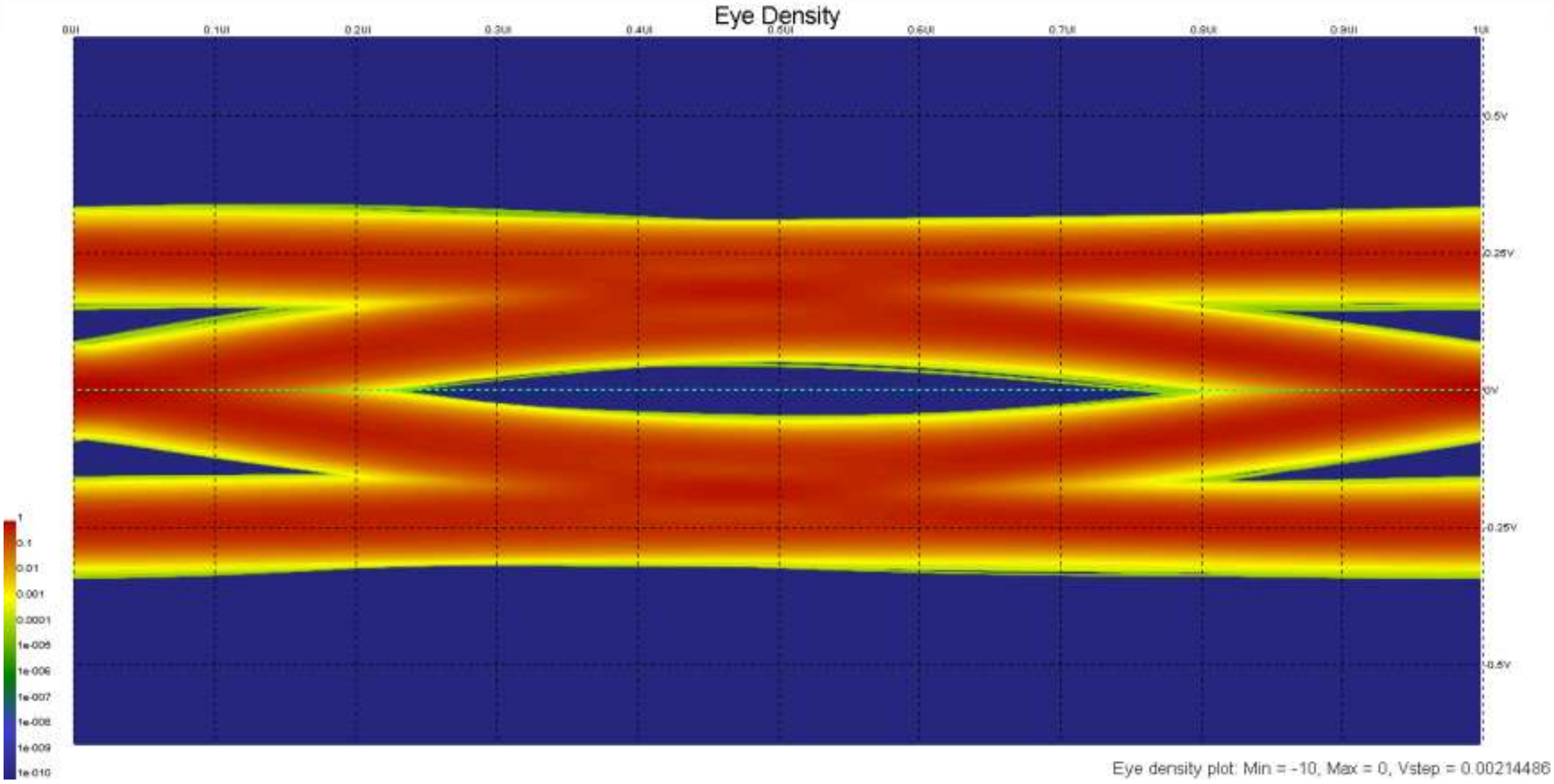
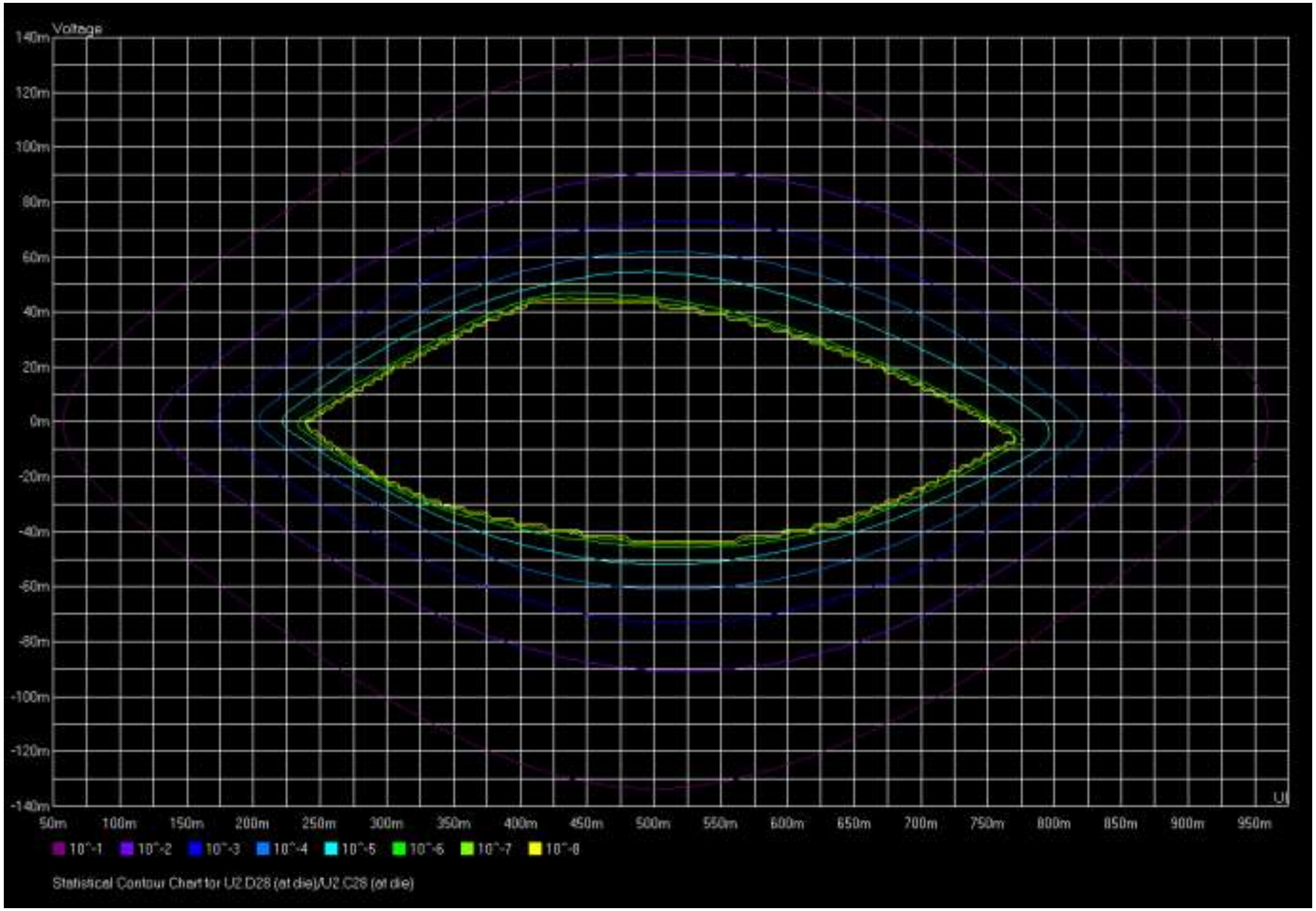
SERDES 5G, Channel 2 with package models, RX no AMI: at 8Gbps



SERDES 5G, Channel 2 with package models, RX no AMI: at 8Gbps



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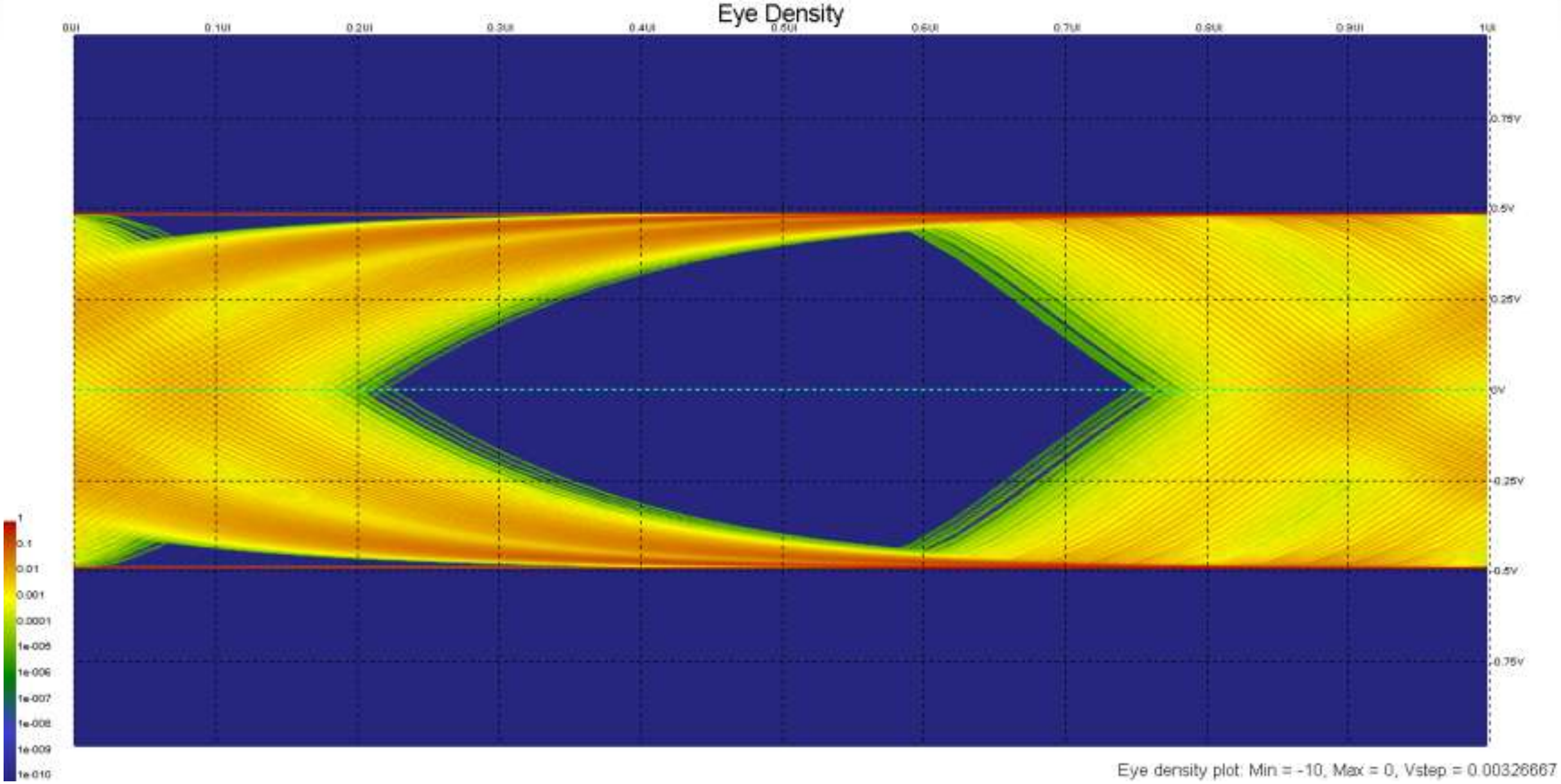
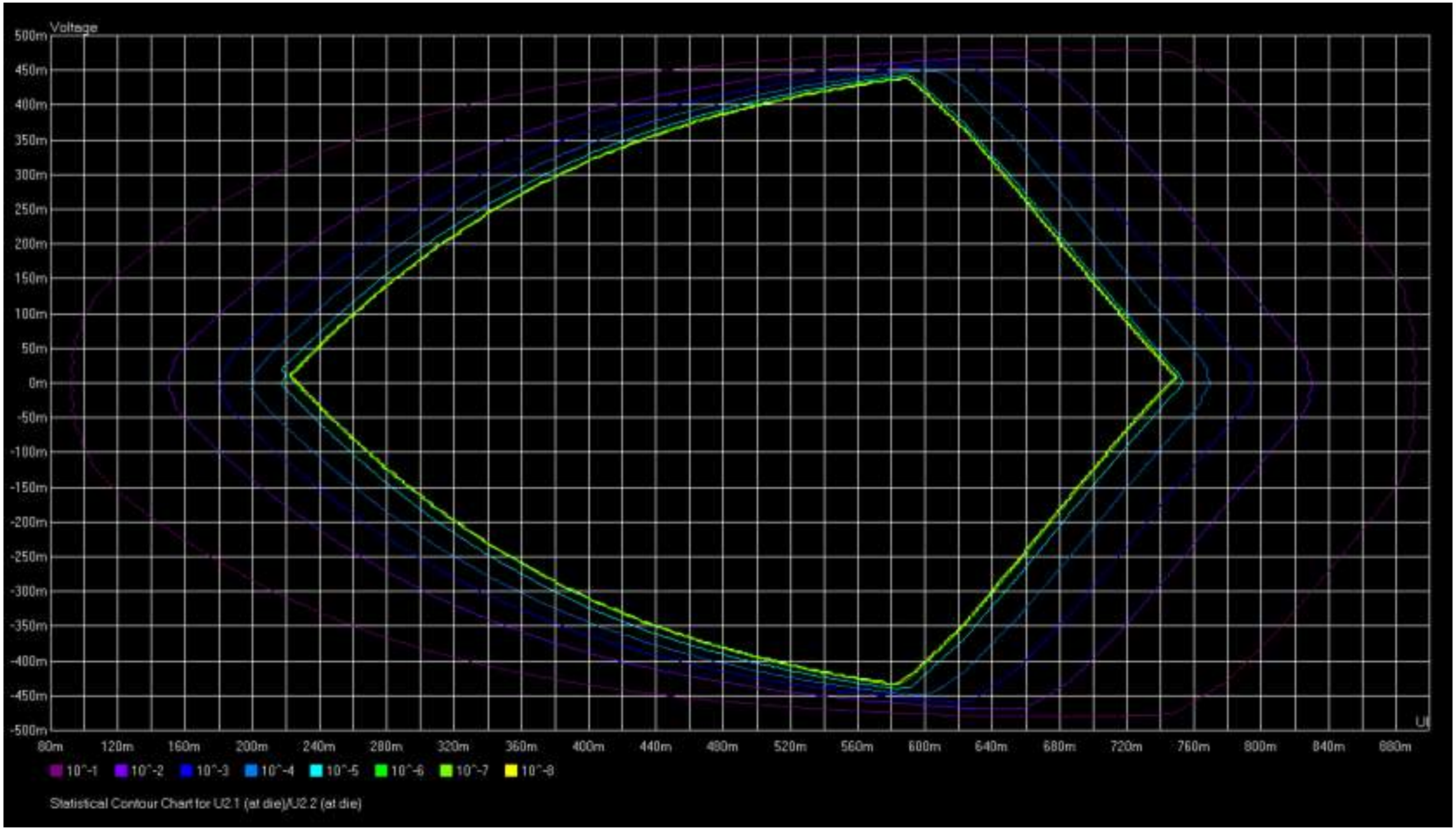
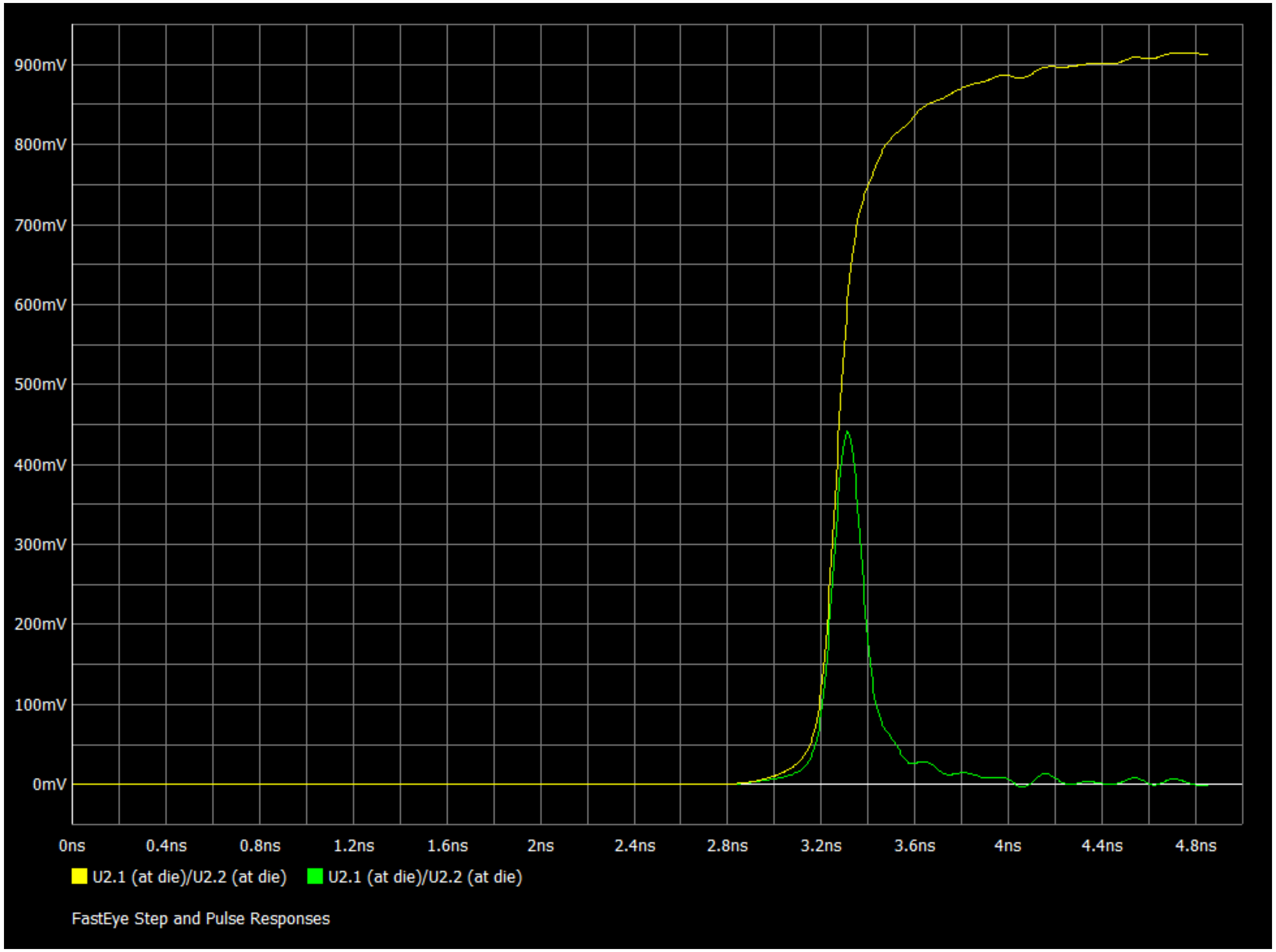
SERDES 5G, Channel 2 with package models, RX AMI: at 8Gbps



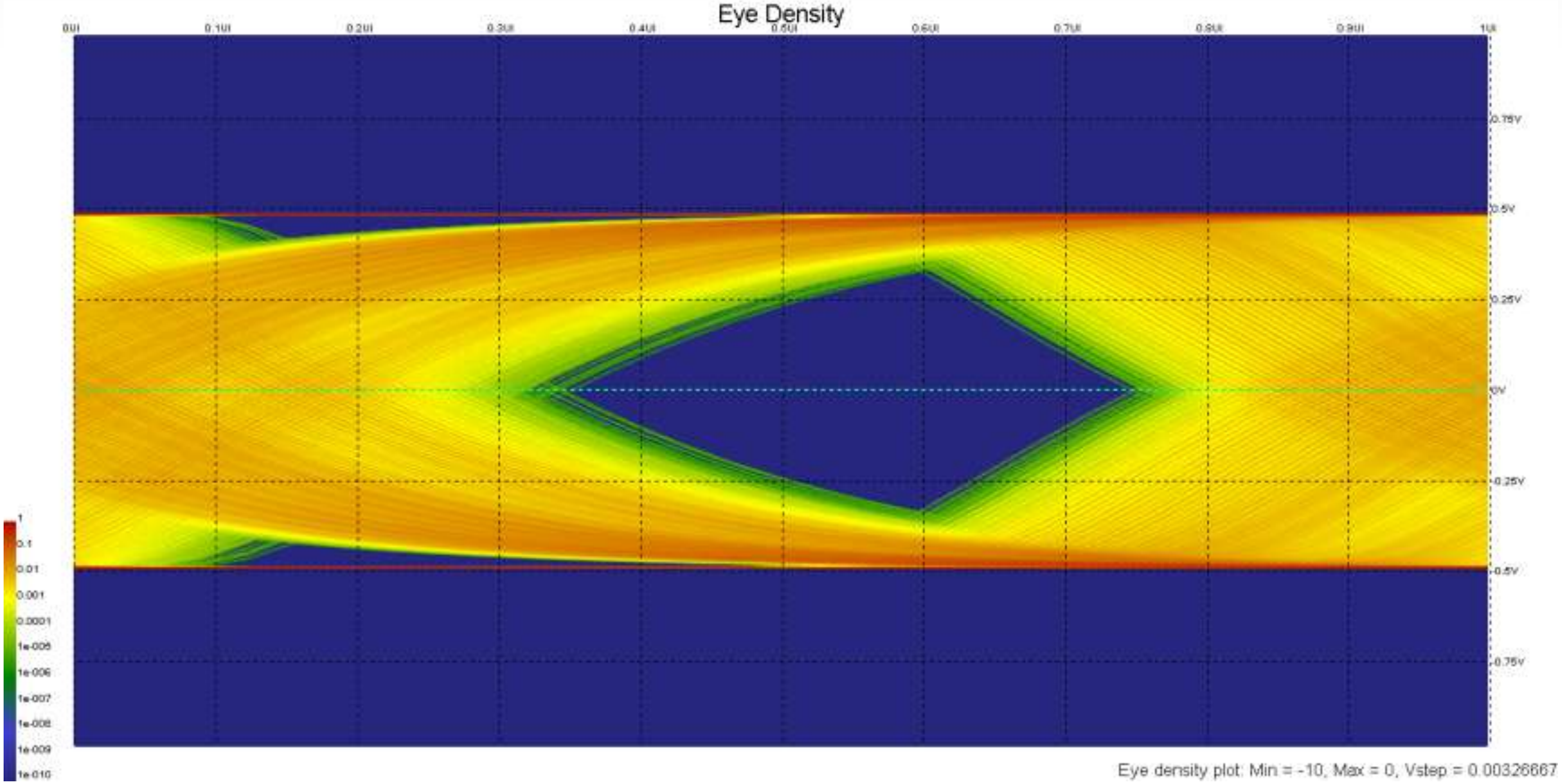
SERDES 5G, Channel 2 with package models, RX AMI: at 8Gbps



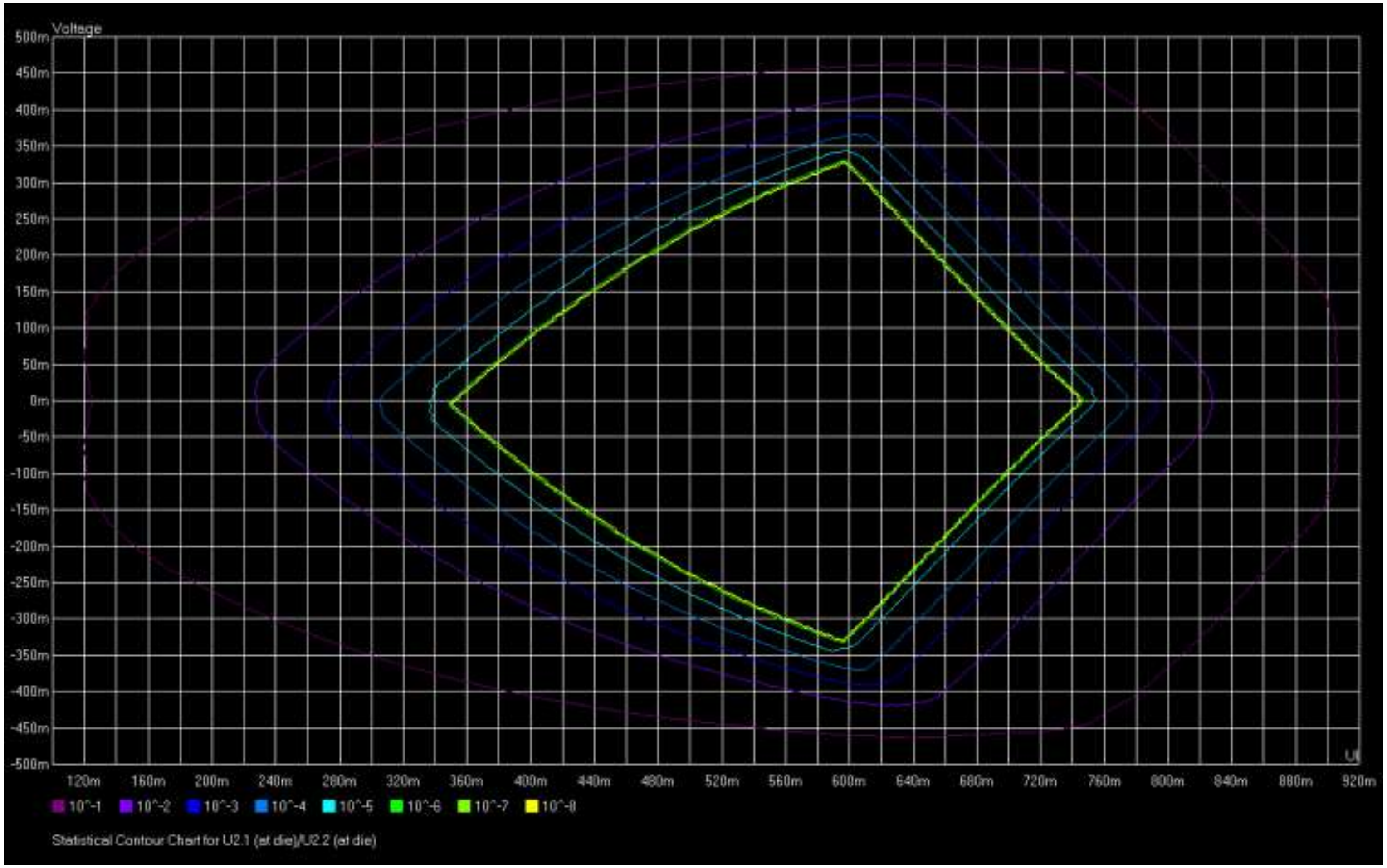
SERDES 5G, Channel 2 with package models, RX AMI: at 10Gbps



SERDES 5G, Channel 2 with package models, RX AMI: at 10Gbps



SERDES 5G, Channel 2 with package models, RX AMI: at 10Gbps



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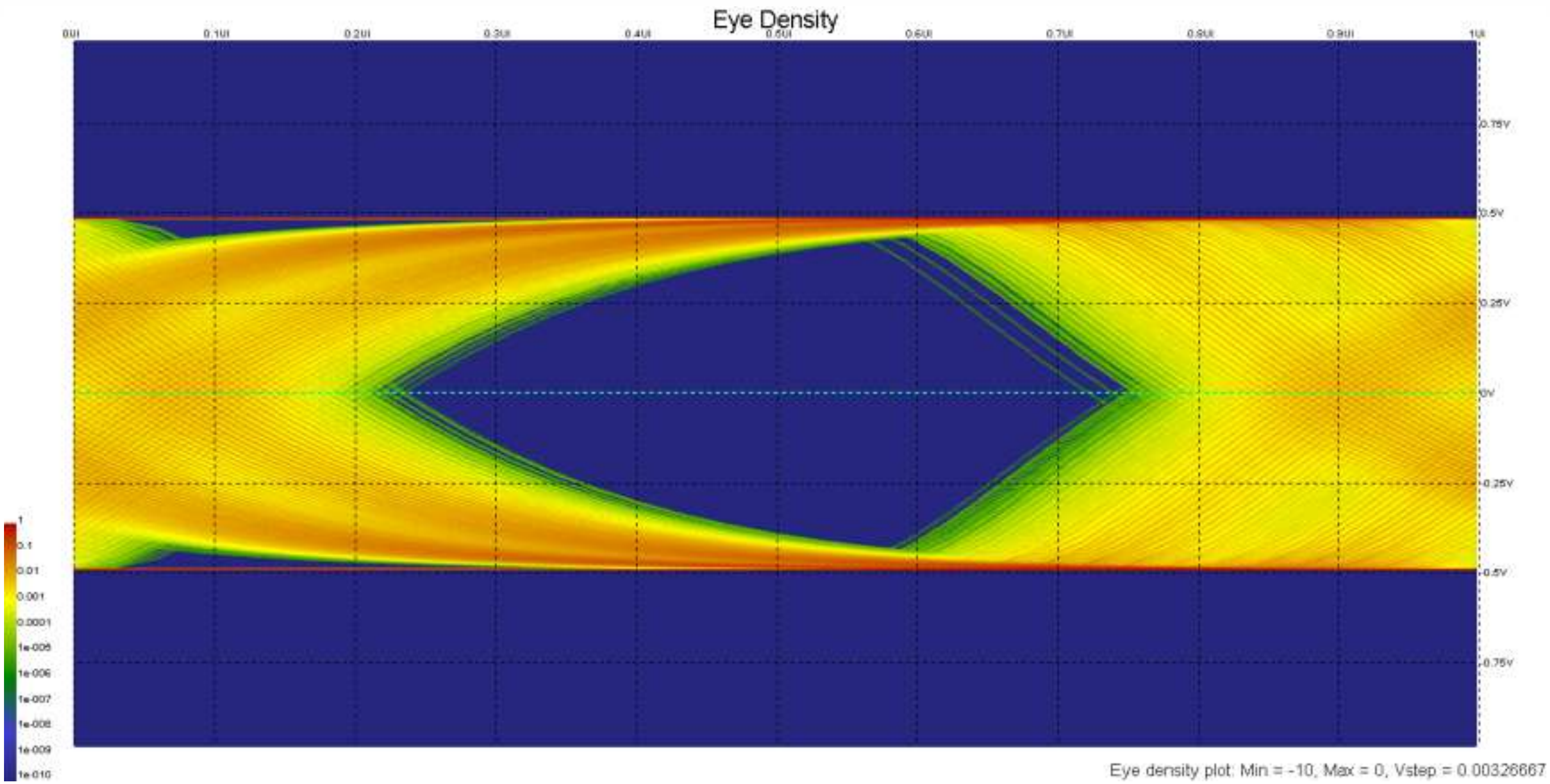
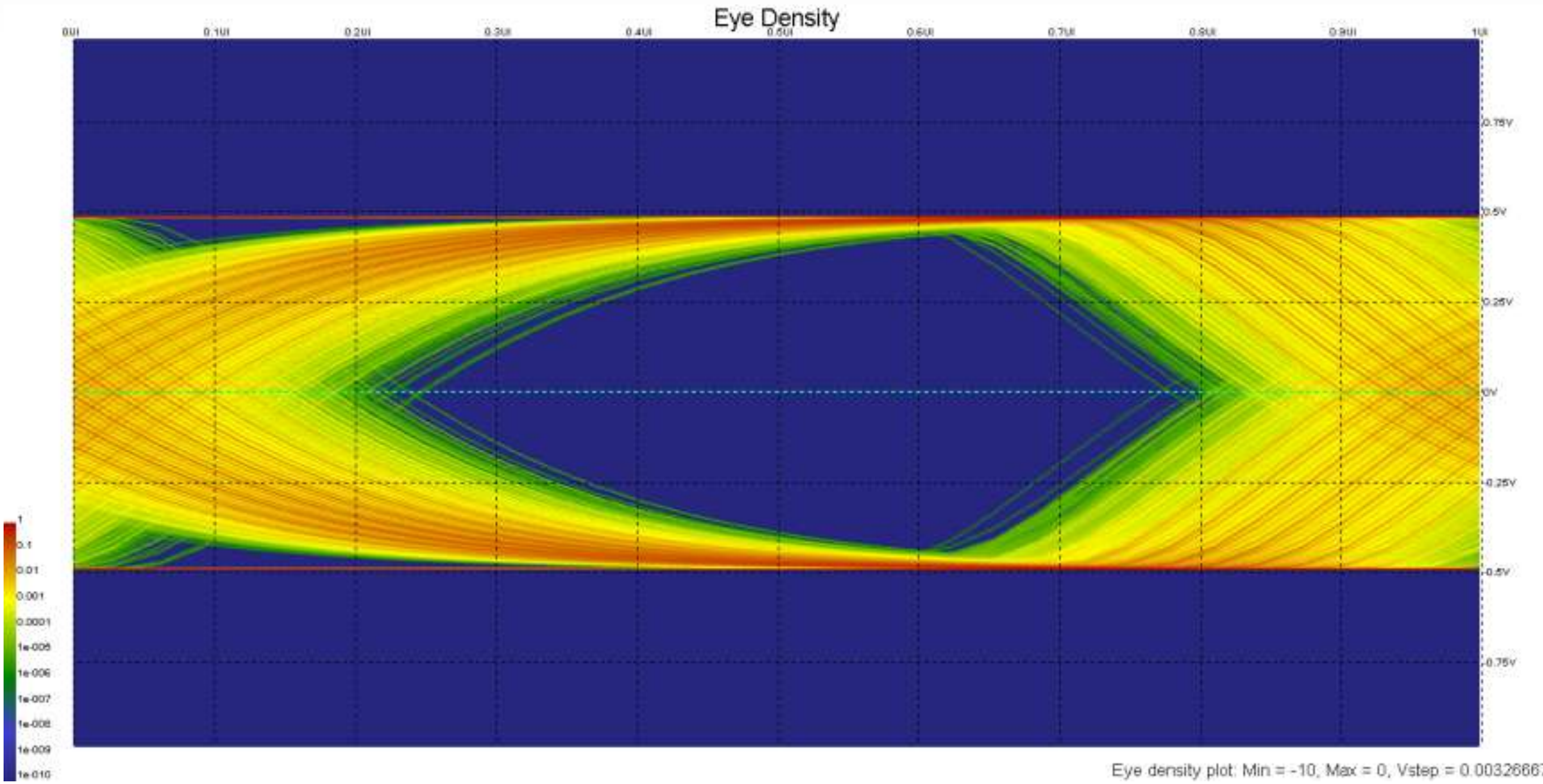
Sweep TX to find better eye?

LYNX 10G, Channel 2 with package models, RX AMI: at 8Gbps (default)



LYNX 10G, Channel 2 with package models, RX AMI: at 8Gbps; TX0



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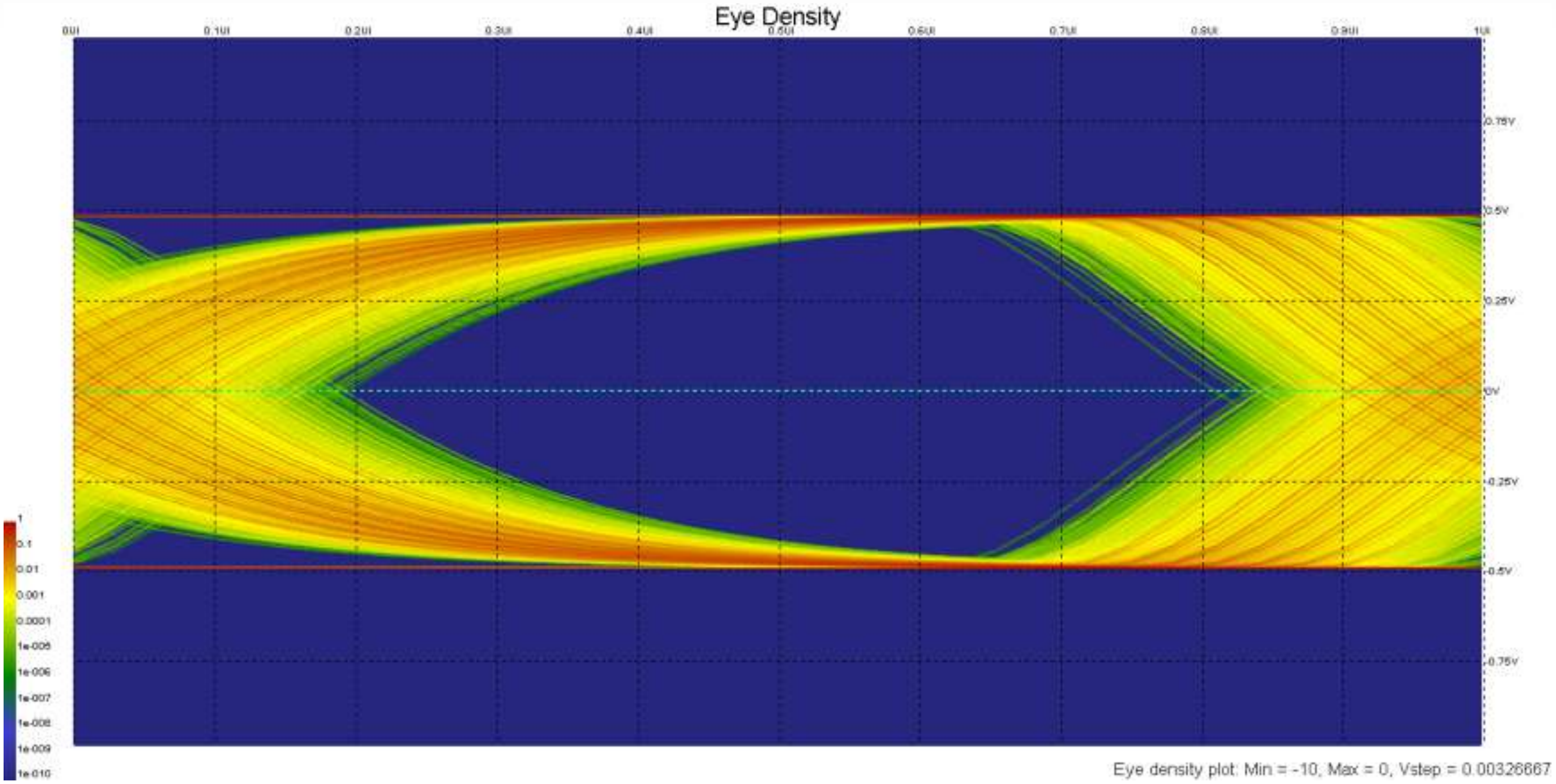
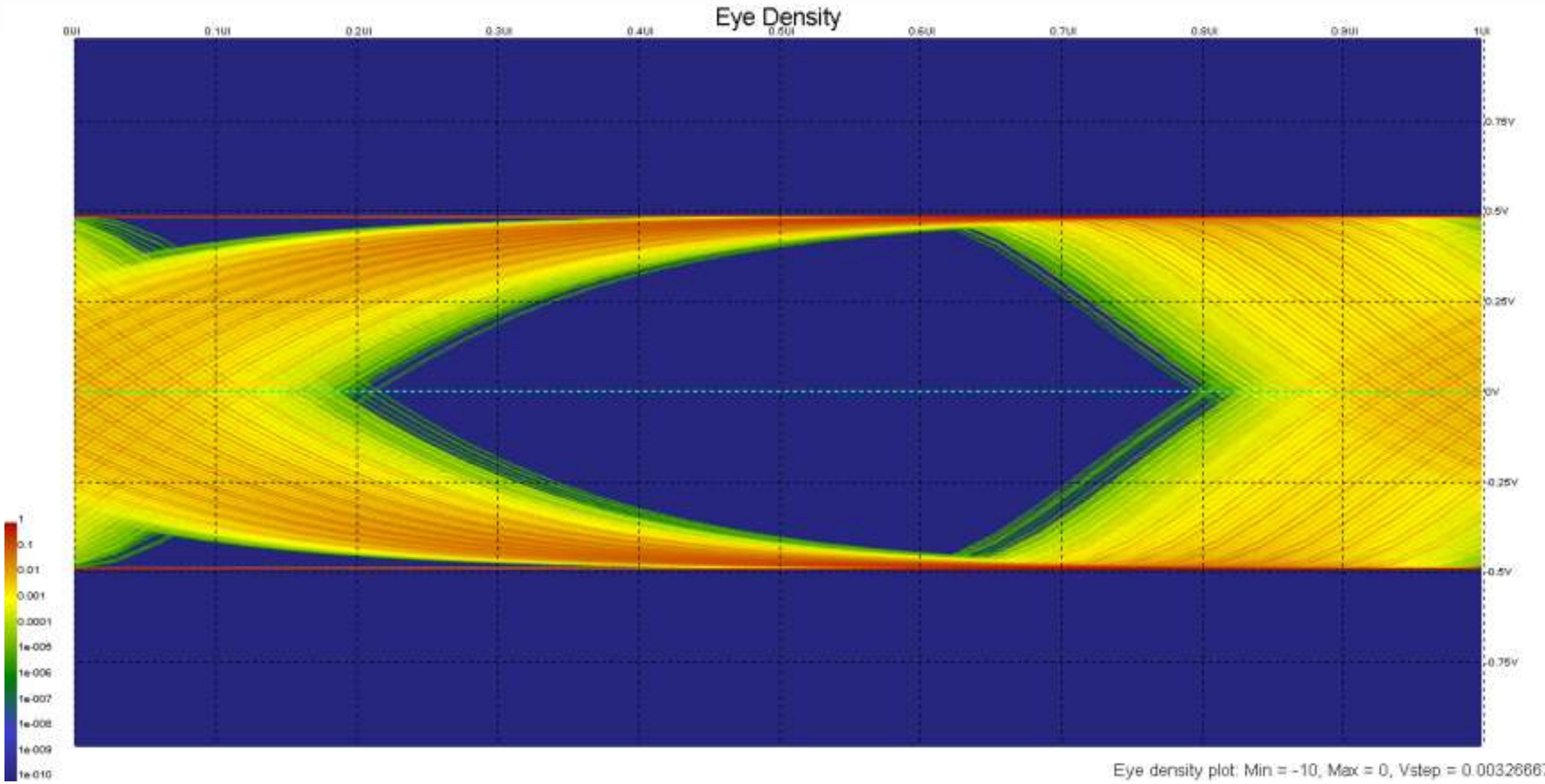
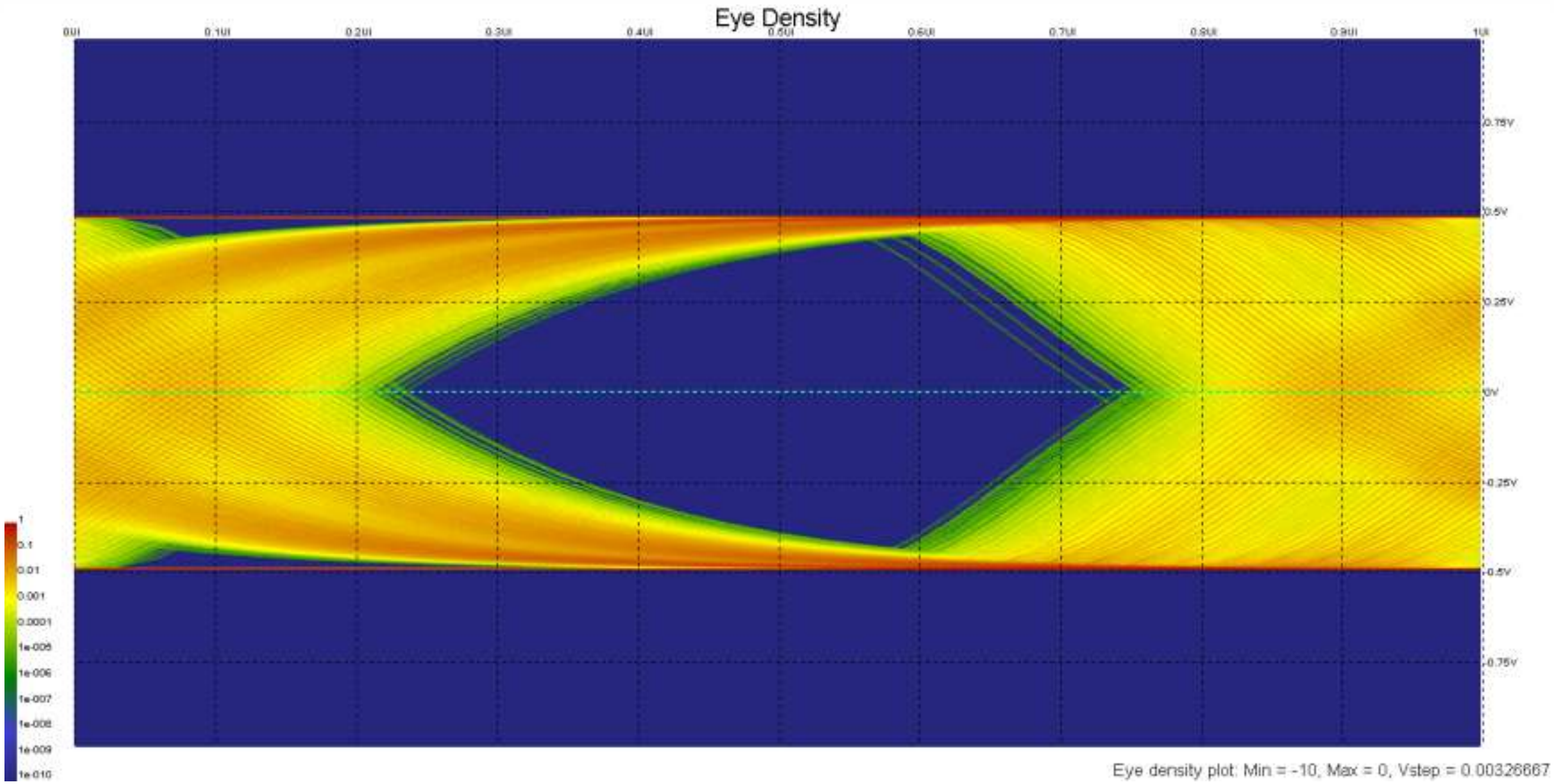
LYNX 10G, Channel 2 with package models, RX AMI: at 8Gbps; TX 1.2



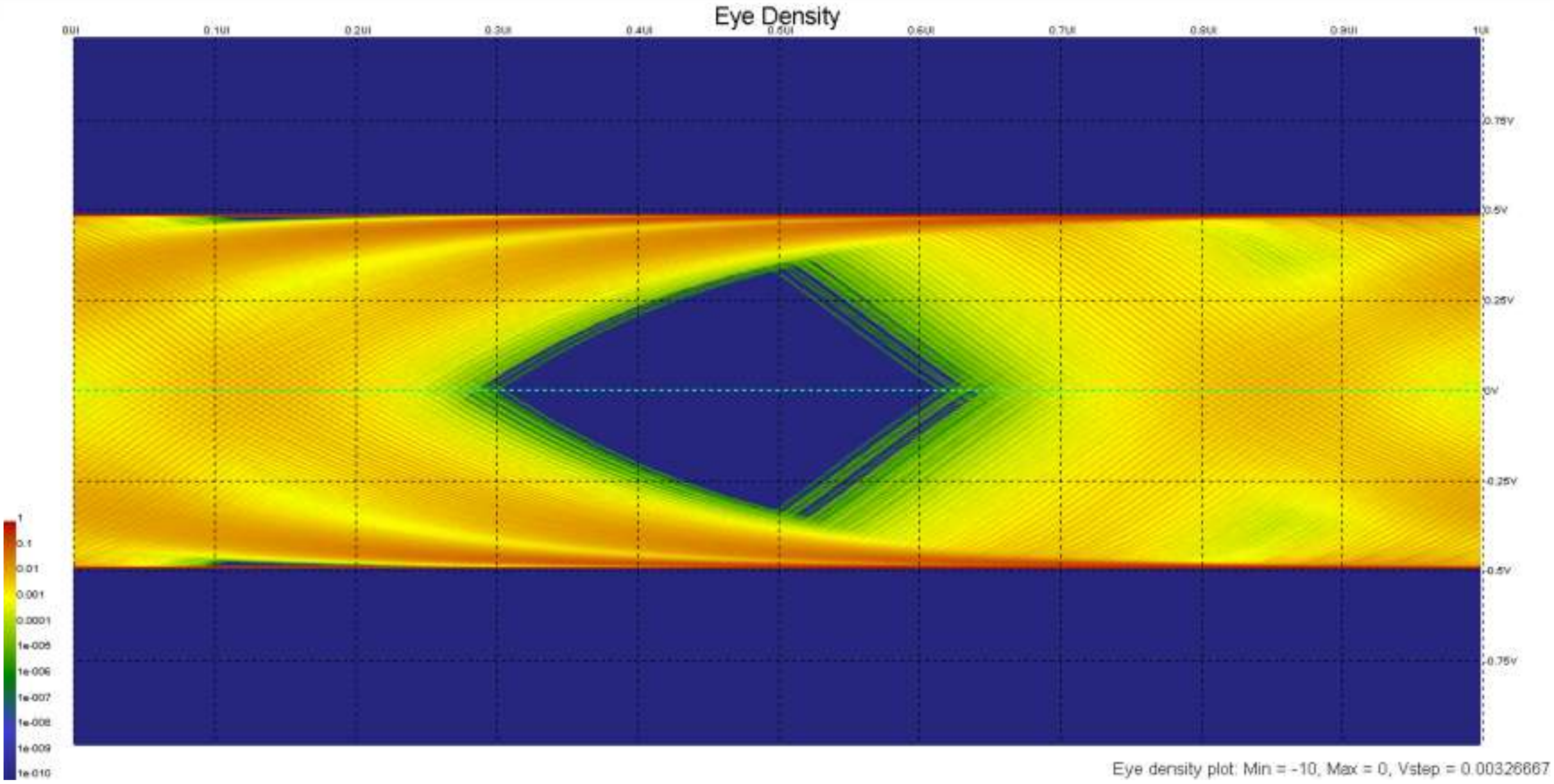
LYNX 10G, Channel 2 with package models, RX AMI: at 8Gbps; TX 1.5



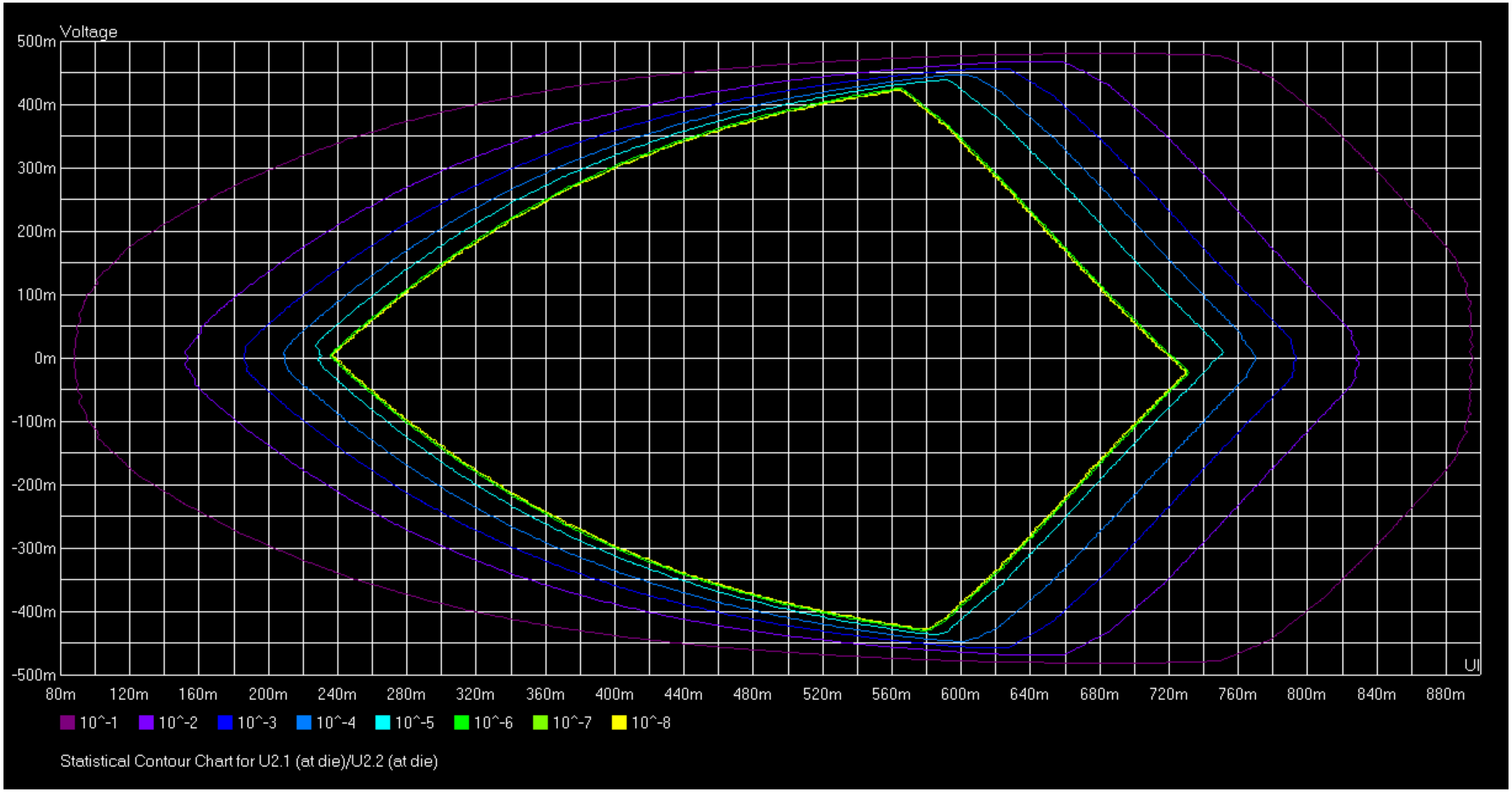
LYNX 10G, Channel 2 with package models, RX AMI: at 8Gbps; TX 2.0



LYNX 10G, Channel 2 with package models, RX AMI: at 8Gbps; TX 3.0



LYNX 10G, Channel 2 with package models, RX AMI: at 8Gbps (default)



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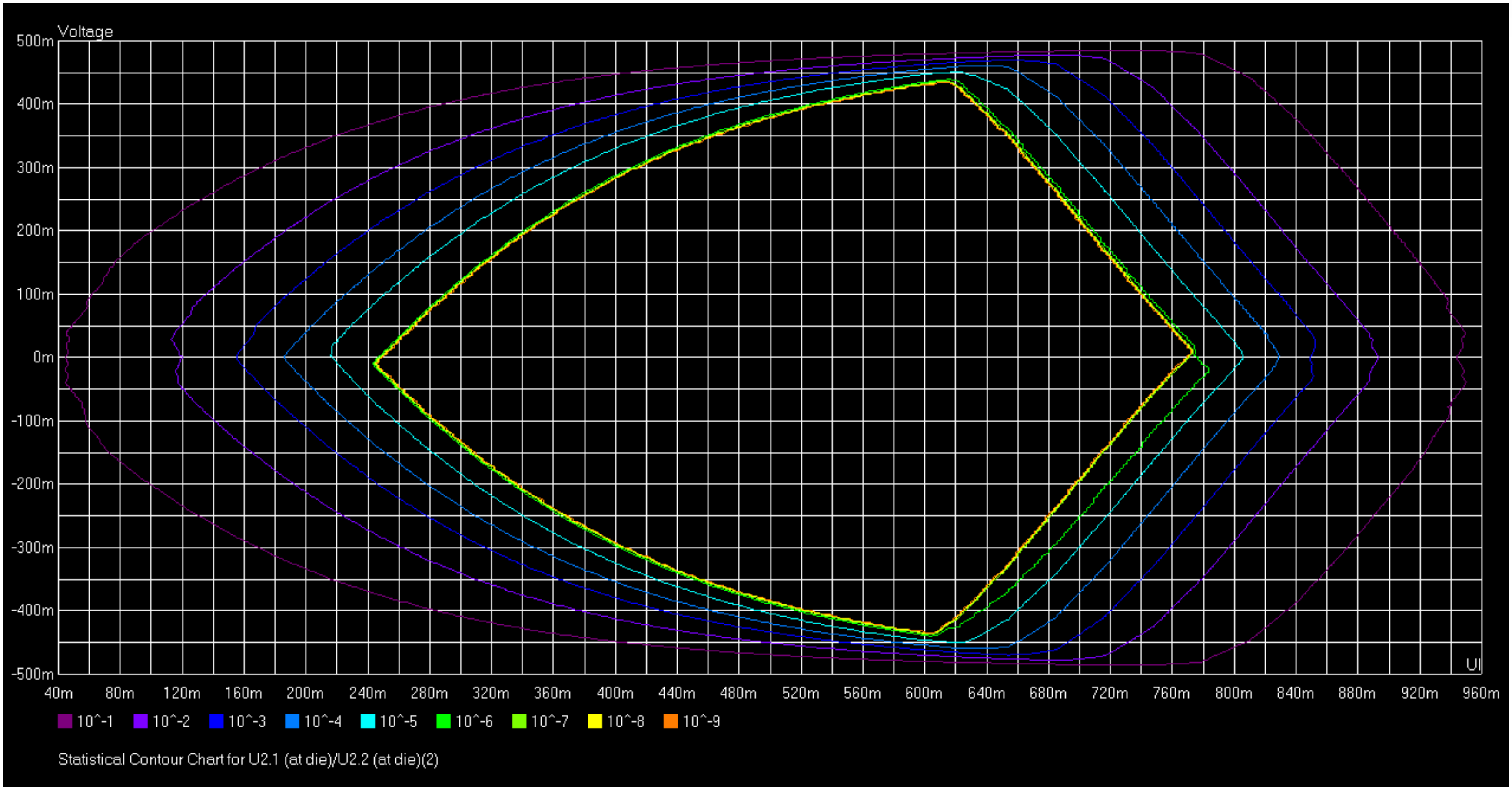
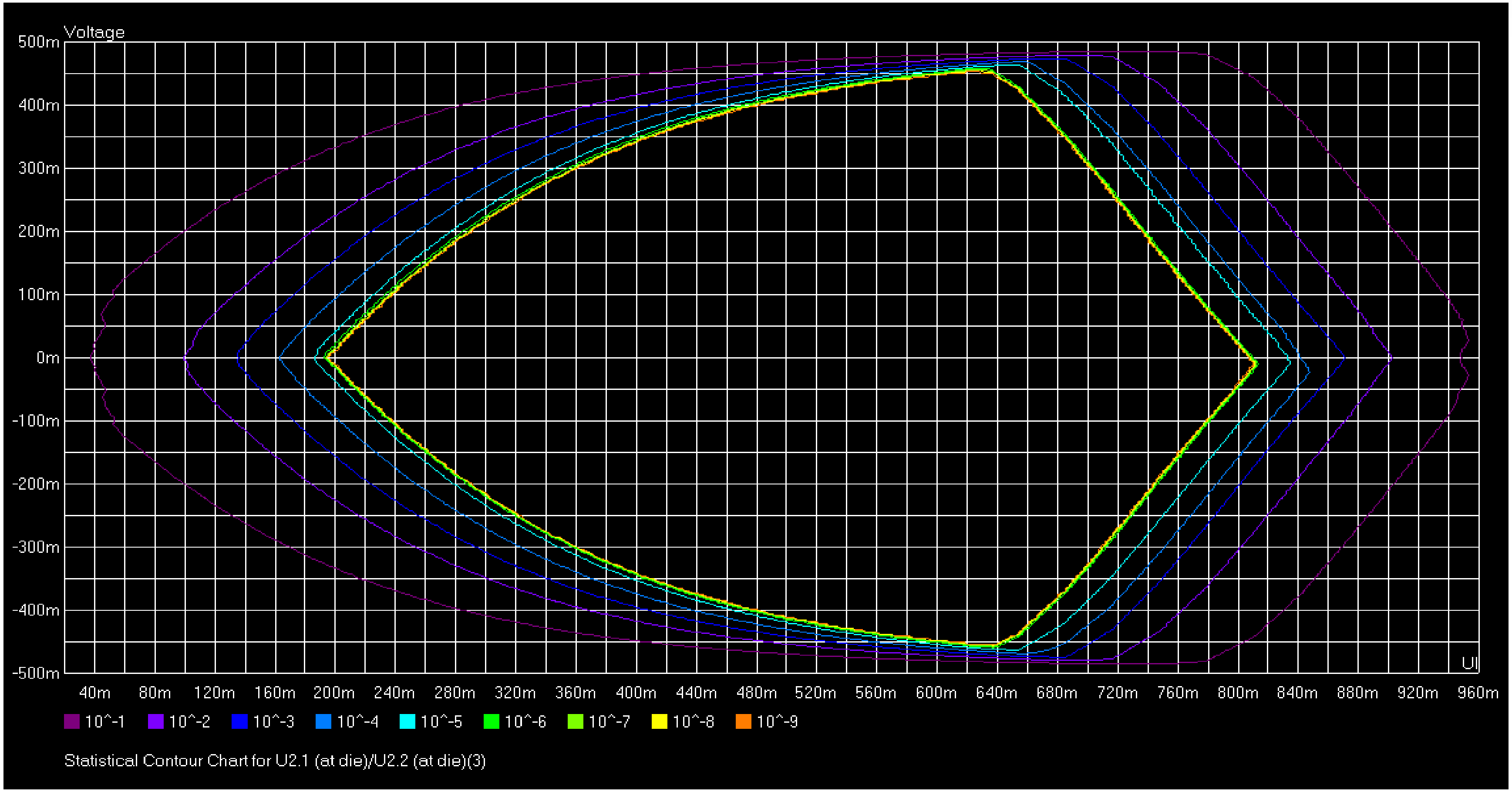
LYNX 10G, Channel 2 with package models, RX AMI: at 8Gbps; TX0



LYNX 10G, Channel 2 with package models, RX AMI: at 8Gbps; TX 1.2



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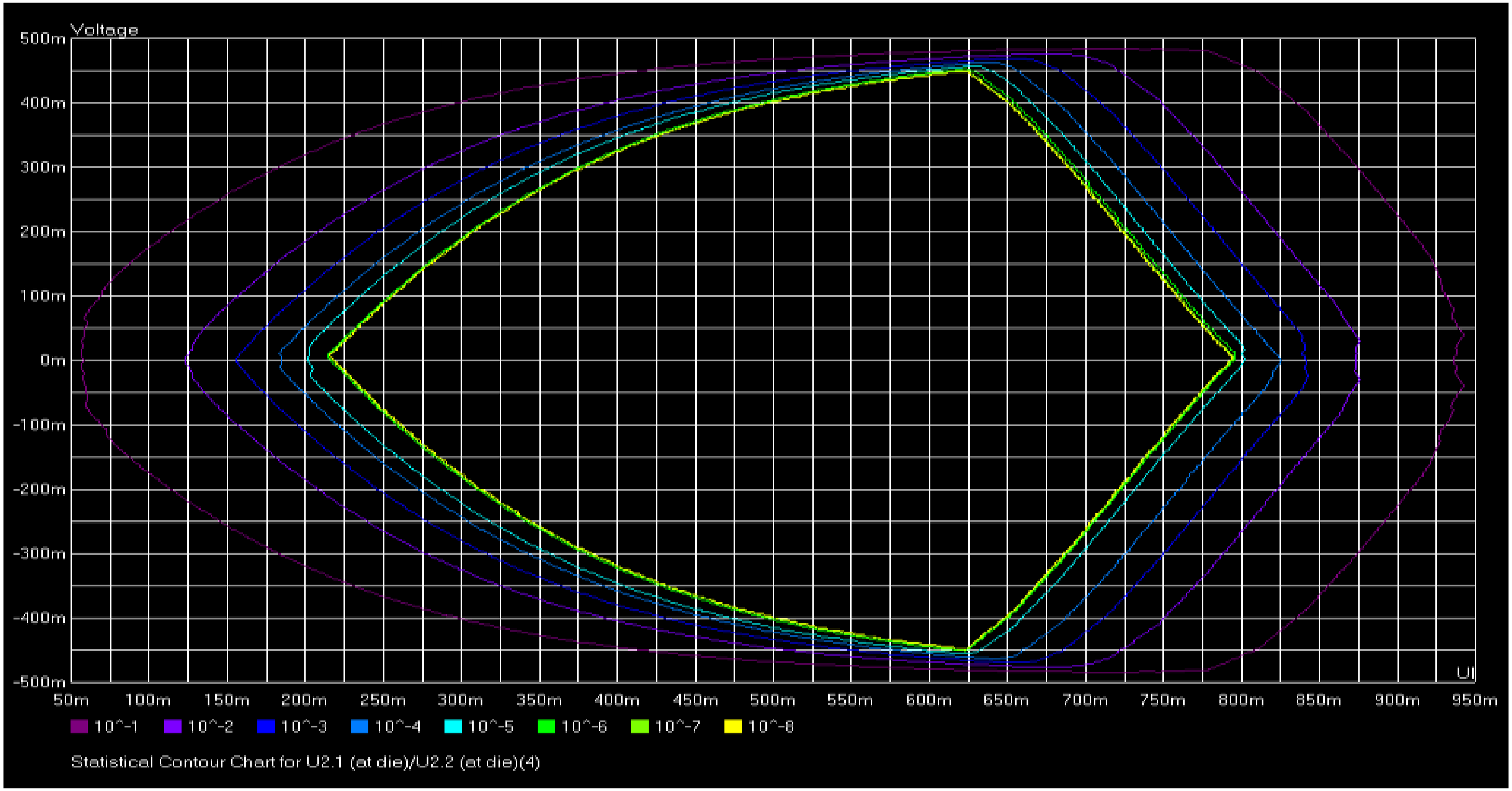
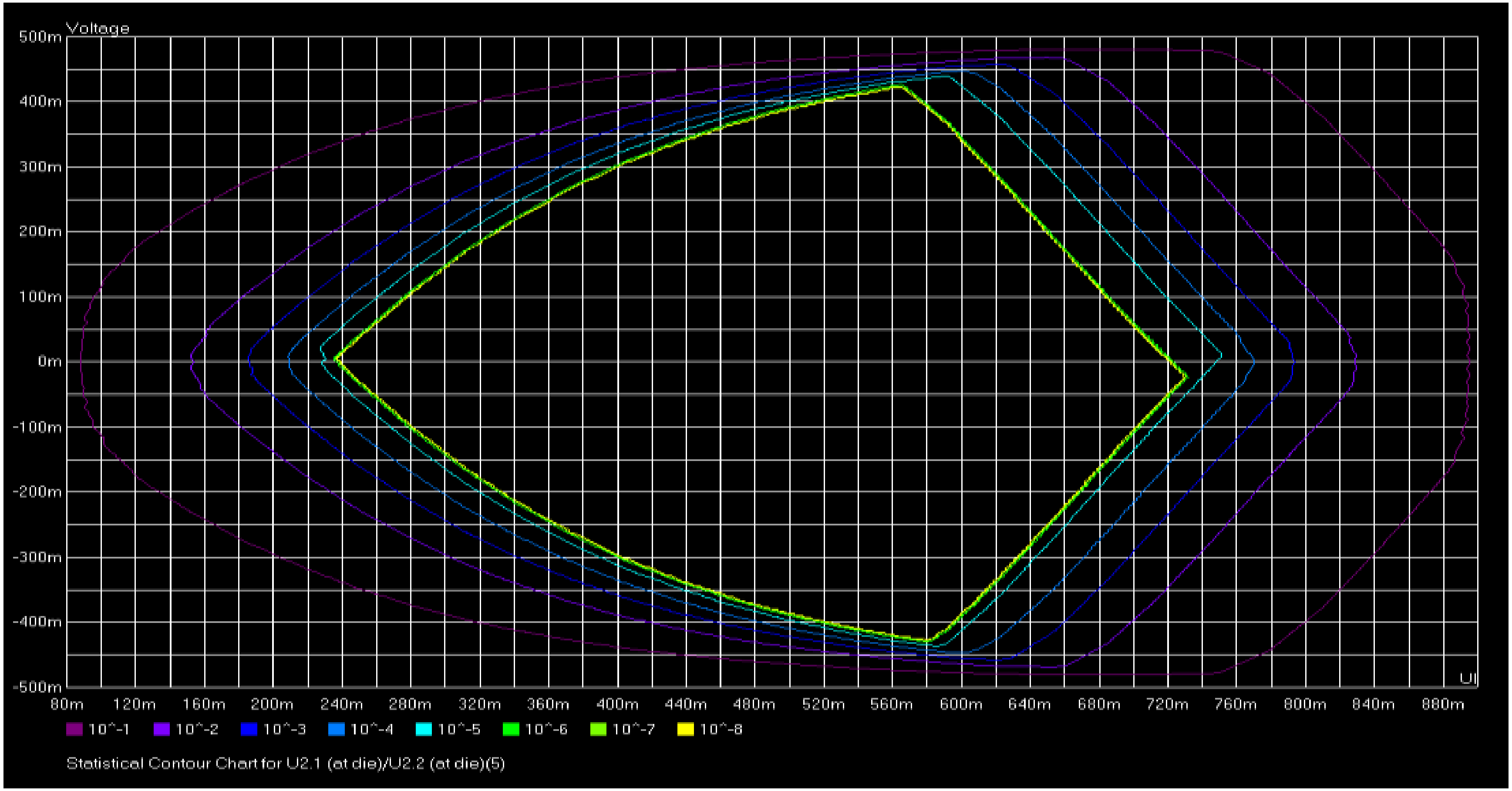
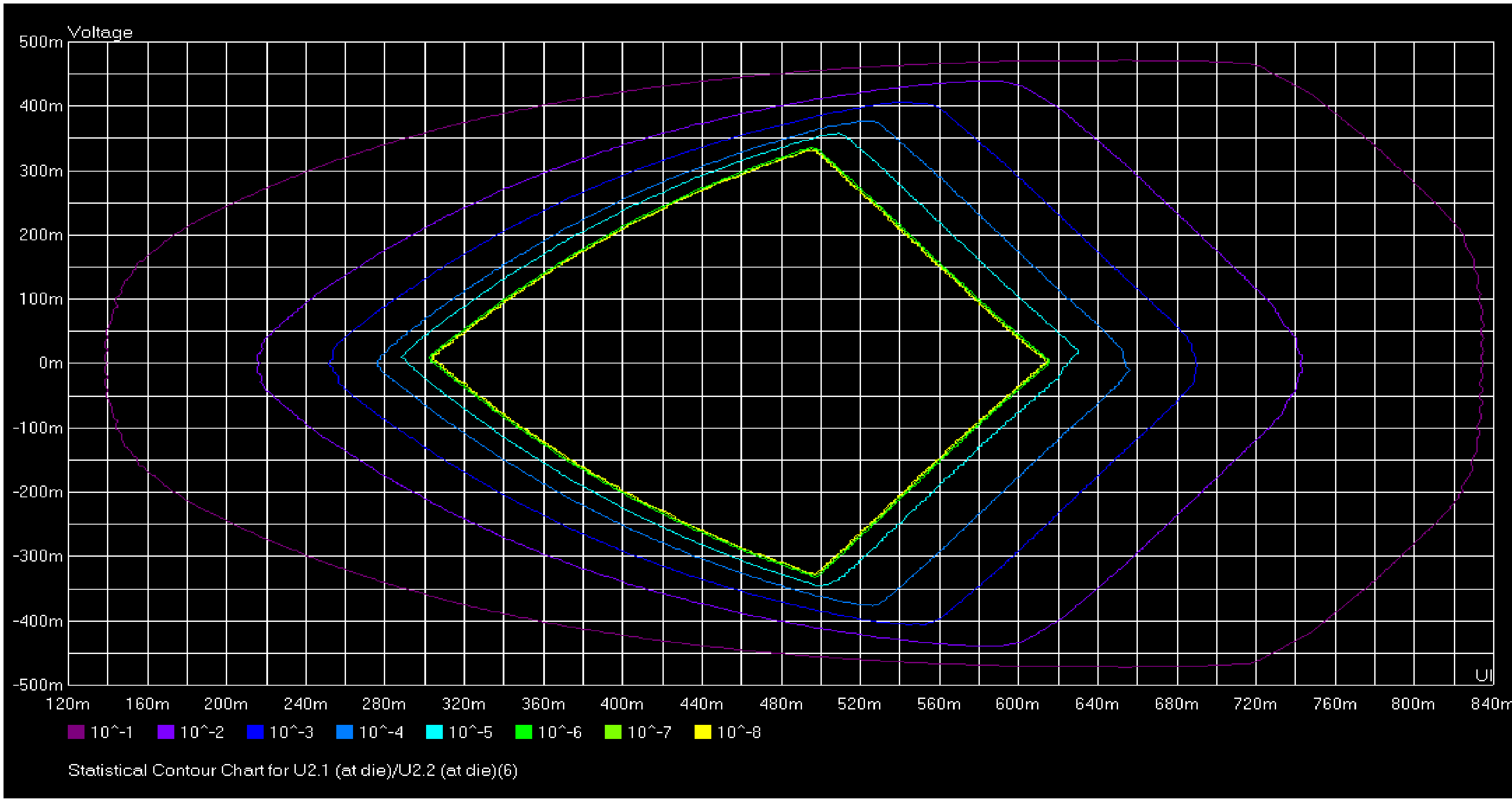
LYNX 10G, Channel 2 with package models, RX AMI: at 8Gbps; TX 1.5



LYNX 10G, Channel 2 with package models, RX AMI: at 8Gbps; TX 2.0

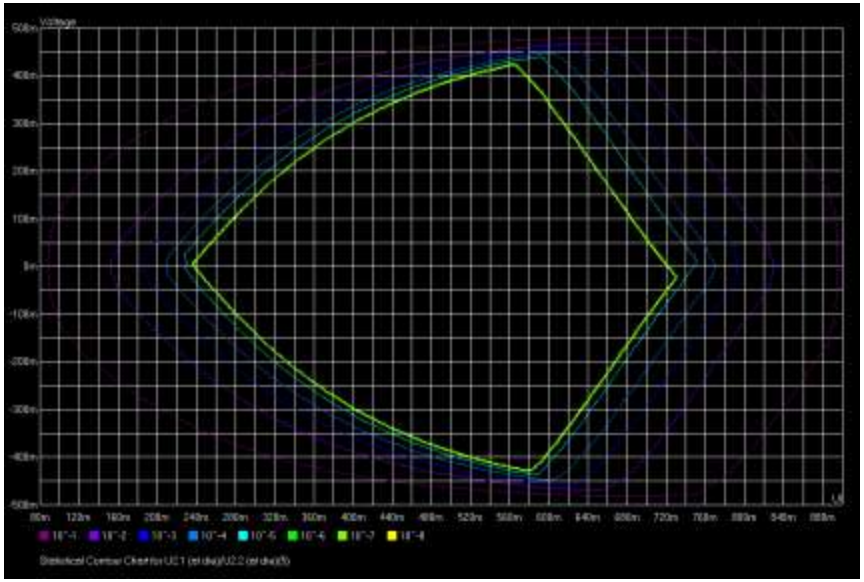


LYNX 10G, Channel 2 with package models, RX AMI: at 8Gbps; TX 3.0

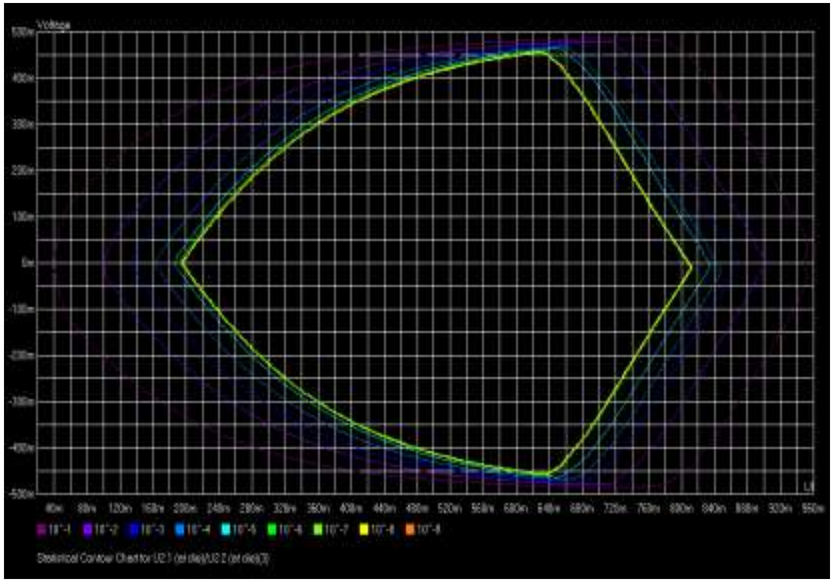


Compare Contours

- Default TX EQ 2.0



- Swept Value TX EQ 1.2



Summary of Eye UI and Eye Height from TX EQ Sweep

TX EQ	Eye Height (mV)	Eye UI
0	0.764	0.531
1.2x	0.823	0.620
1.5x	0.800	0.582
2.0x	0.774	0.495
3.0x	0.663	0.313

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Summary of IBIS-AMI Benefits

- TX EQ modeling
  - 2 tap, 3 tap, 4 tap TX EQ

- RX EQ modeling
  - Multiple types of RX EQ
  - Proprietary Circuits can be modeled
  - AMI Model can be tailored specifically for a device’s design

- IBIS-AMI based simulation tools permit effective sweeping of TX and RX parameters to determine optimal settings
  – EDA tools are building in GUI-based means to sweep parameters easily

- TX EQ and RX EQ can be significant tools for improving SERDES channel response
  - May permit design using lower cost materials and narrower traces
    - Translates to << $$ and << board space

Q&A

- Thank you

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