

Board Bringup: LCD and Display Interfaces

Slides and Resources at
<http://www.elinux.org/elc-lcd>

Introduction

- Dave Anders aka prplague

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- Currently Contracted with TI

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- Partners in TinCanTools

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- Board Bring Up: LCD and Display Interfaces

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- Board Bring Up: LCD and Display Interfaces
 - Challenges of LCD Bring Up

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 - Interface Timings

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 - Display Interface Types

Introduction

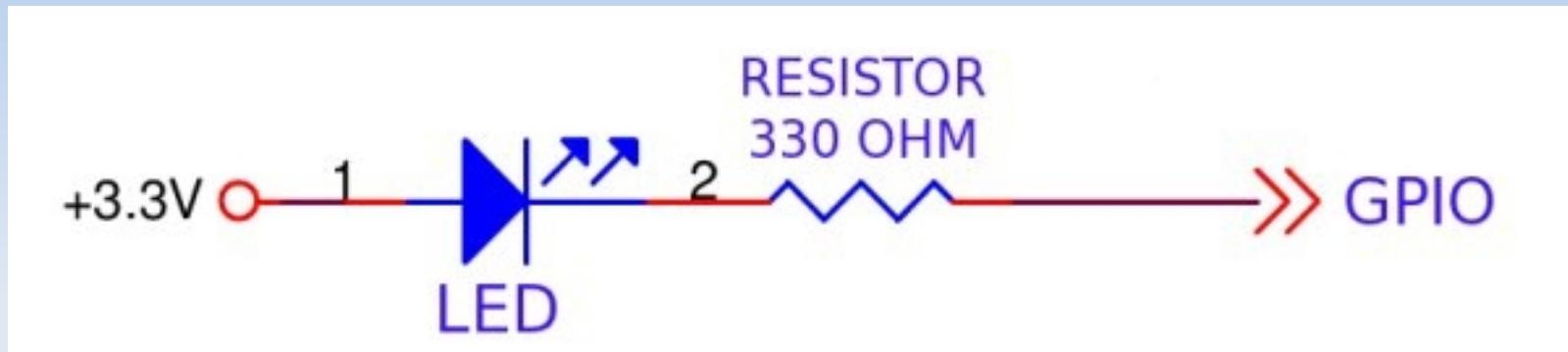
- Dave Anders aka prpplaque
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- Board Bring Up: LCD and Display Interfaces
 - Challenges of LCD Bring Up
 - Interface Timings
 - Display Interface Types
 - Debugging

Challenges of LCD Bring Up

- Simple User Display

Challenges of LCD Bring Up

- Simple User Display



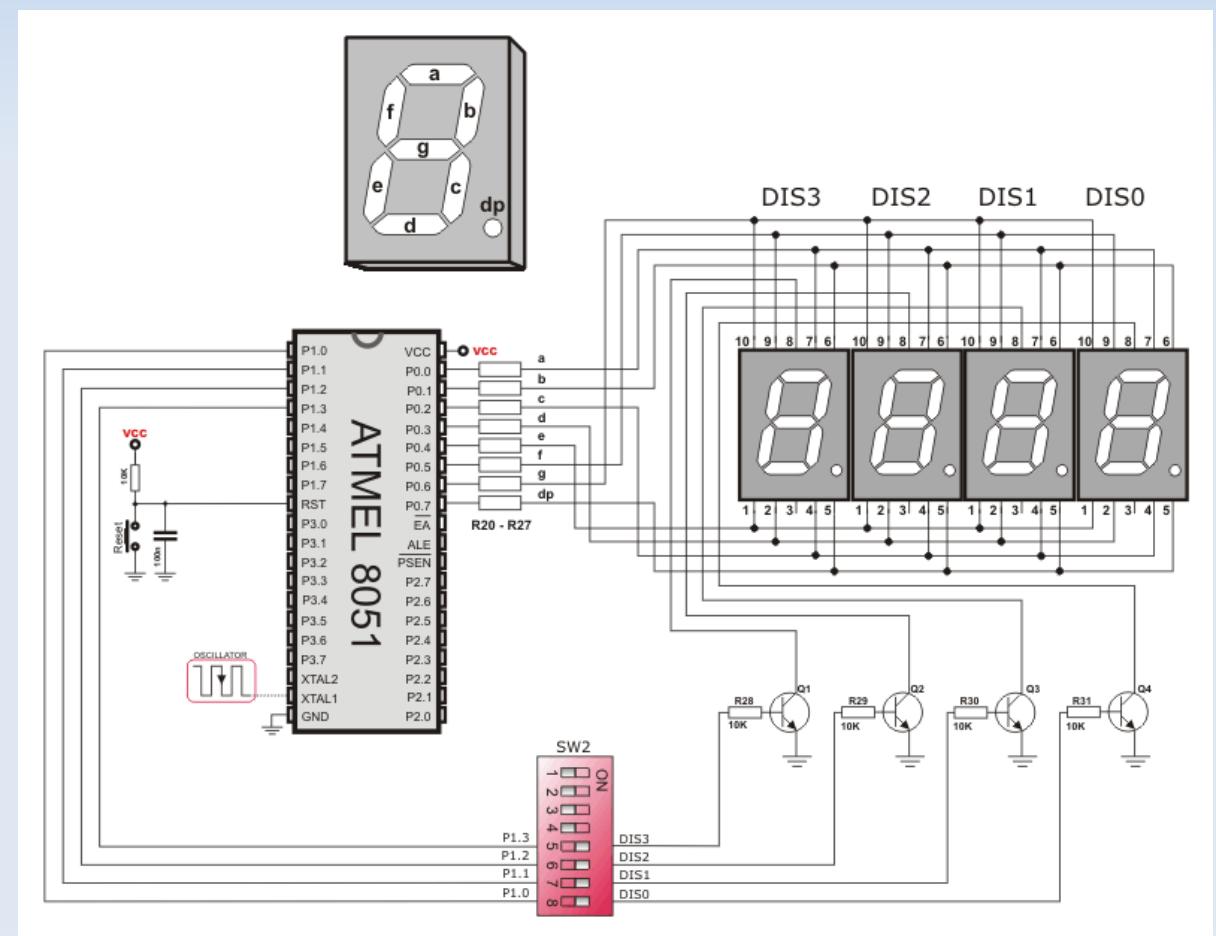
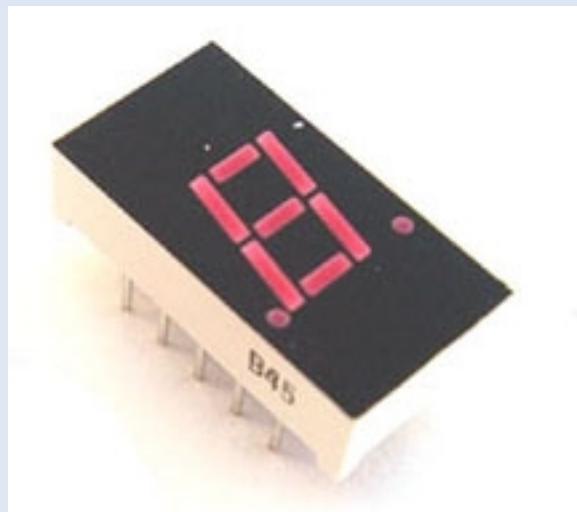
Challenges of LCD Bring Up

- Simple User Display
 - Easy to visualize
 - Easy to measure
 - Easy to program



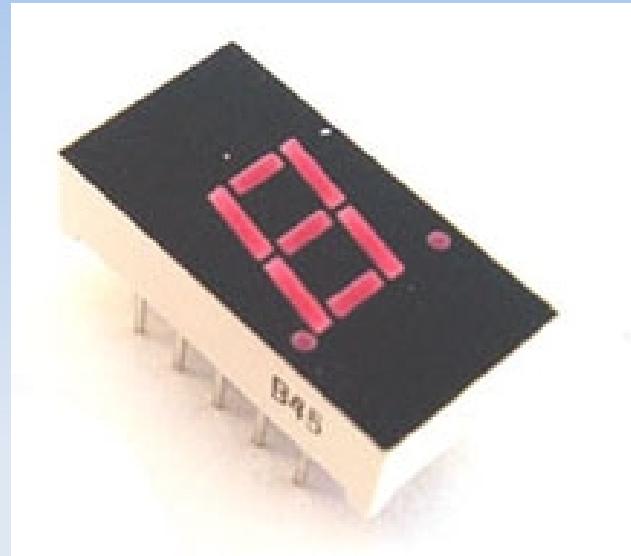
Challenges of LCD Bring Up

- Simple User Display
- Evolution of Displays



Challenges of LCD Bring Up

- Simple User Display
- Evolution of Displays
 - Clocking
 - Multiple signals
 - Introduction of controllers



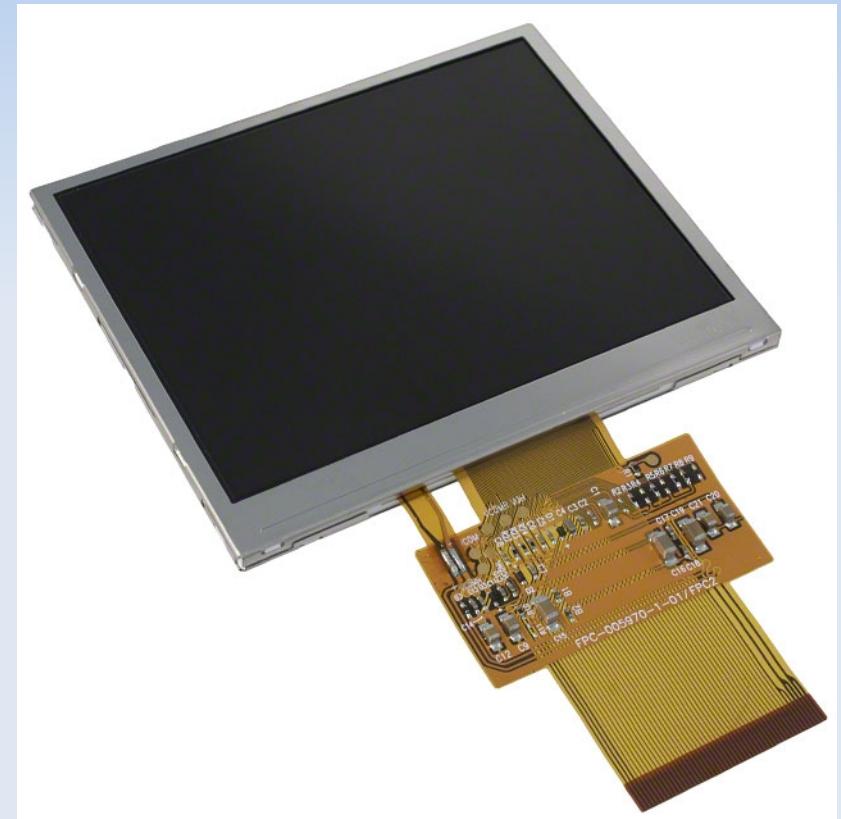
Challenges of LCD Bring Up

- Simple User Display
- Evolution of Displays
- Transition to LCD



Challenges of LCD Bring Up

- Simple User Display
- Evolution of Displays
- Transition to LCD
 - Higher frequency
 - More signals
 - Complex Controllers

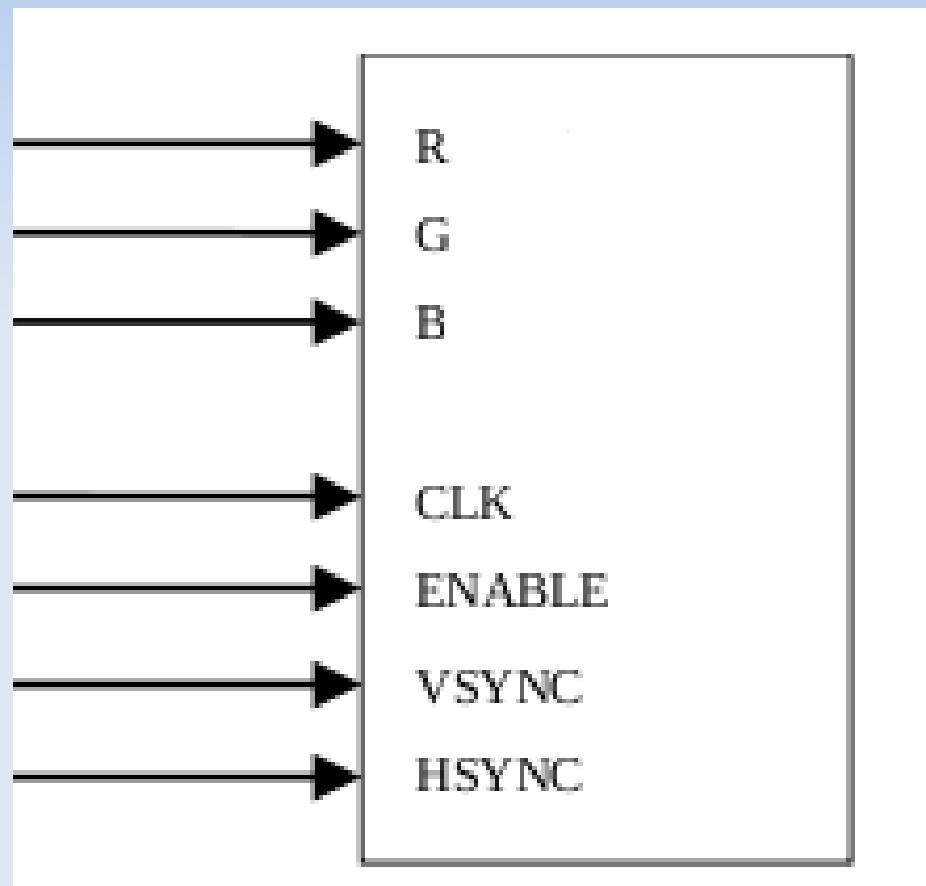


Interface Timings

- TFT Parallel Interface

Interface Timings

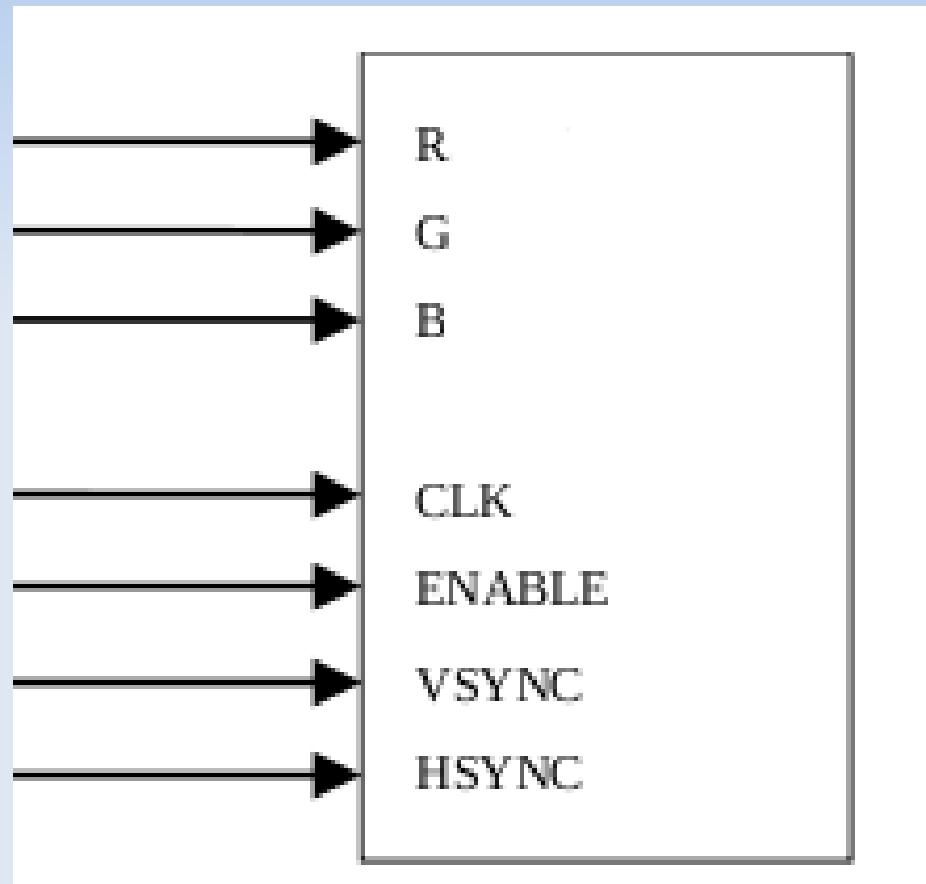
- TFT Parallel Interface
 - PCLK (Pixel Clock)



Interface Timings

- TFT Parallel Interface

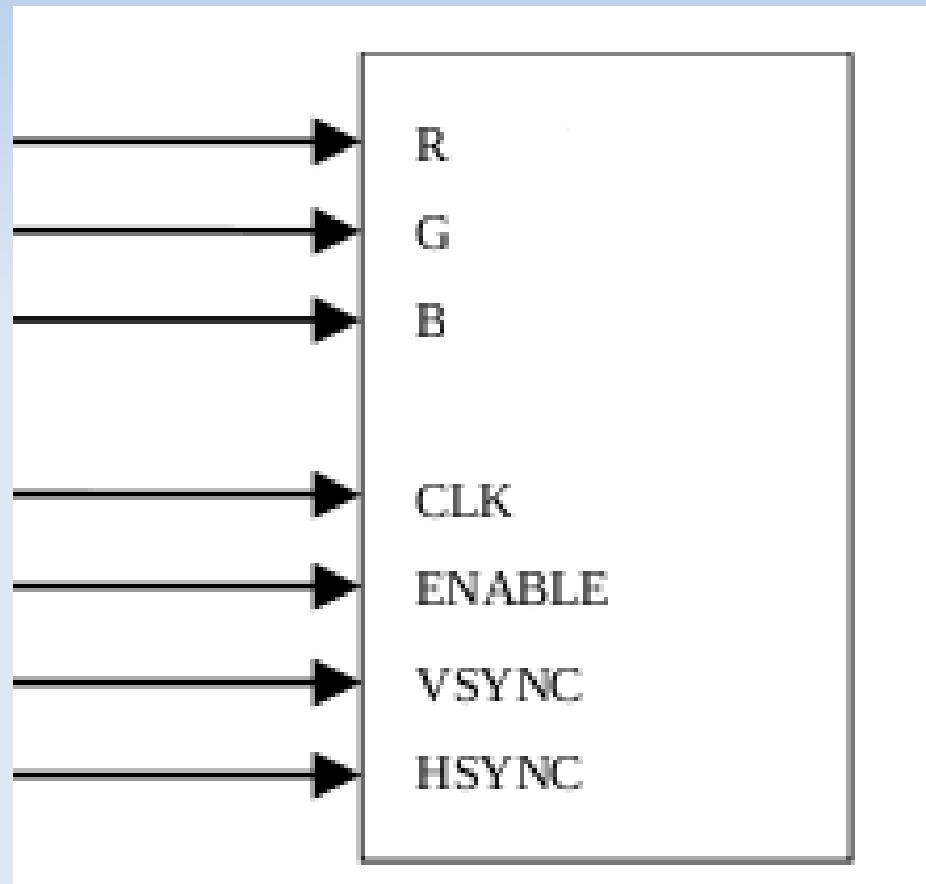
- PCLK (Pixel Clock)
- HSYNC (Horizontal Sync)



Interface Timings

- TFT Parallel Interface

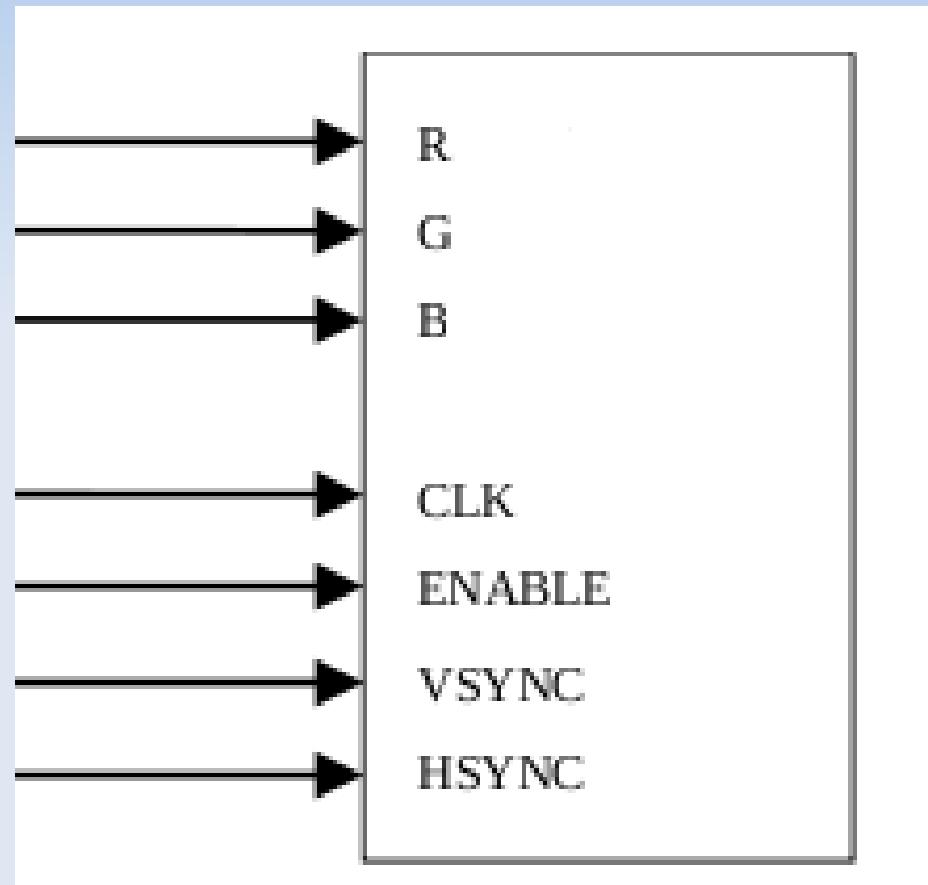
- PCLK (Pixel Clock)
- HSYNC (Horizontal Sync)
- VSYNC (Verticle Sync)



Interface Timings

- TFT Parallel Interface

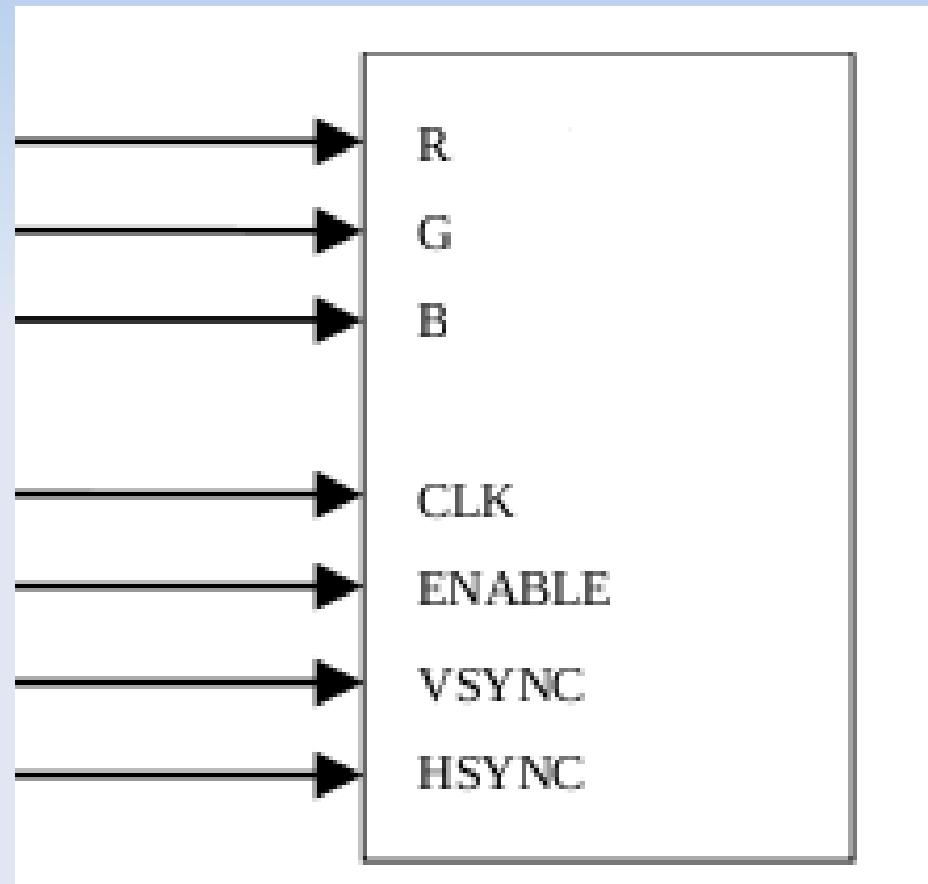
- PCLK (Pixel Clock)
- HSYNC (Horizontal Sync)
- VSYNC (Verticle Sync)
- DE (Data Enable)



Interface Timings

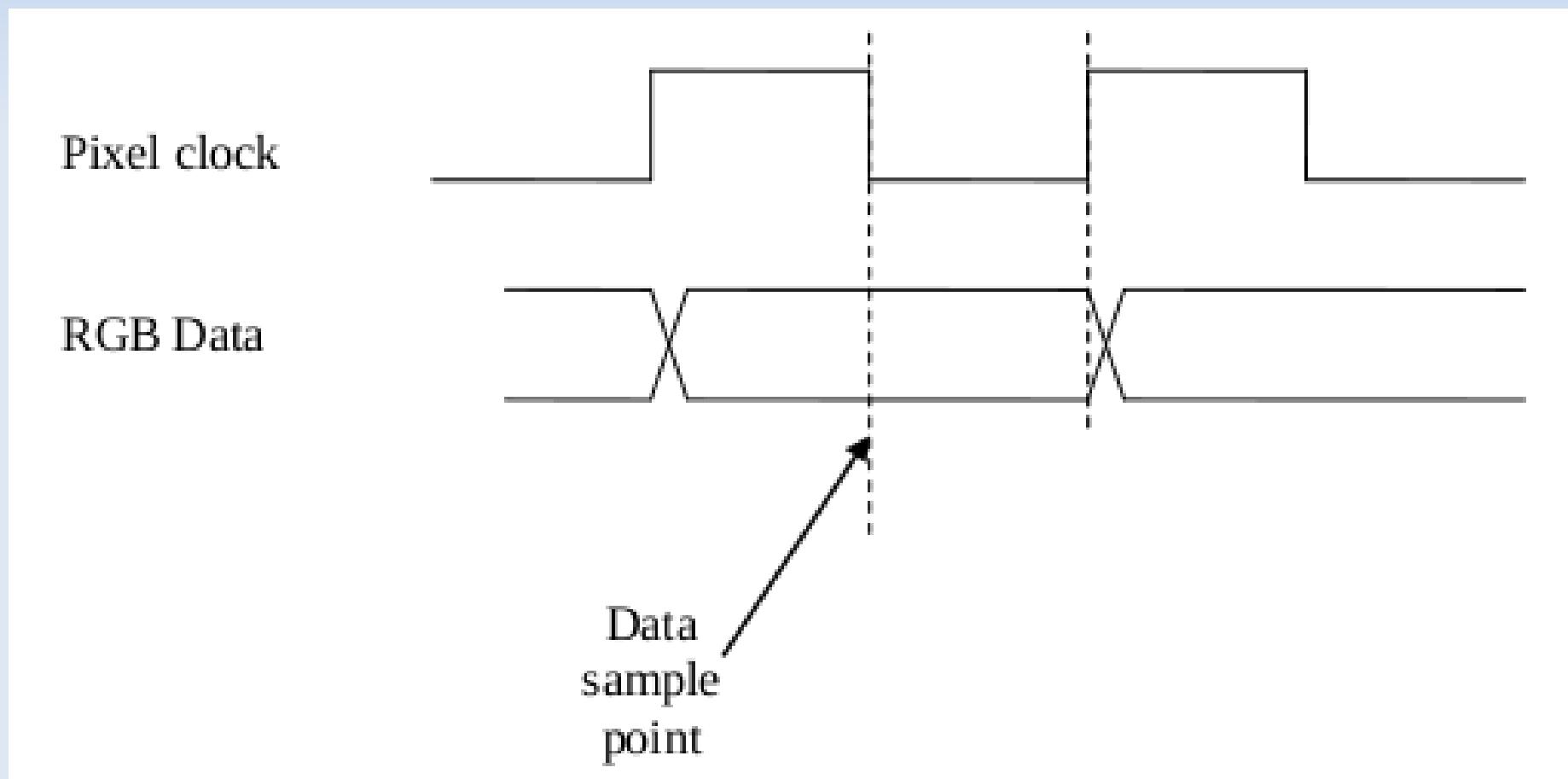
- TFT Parallel Interface

- PCLK (Pixel Clock)
- HSYNC (Horizontal Sync)
- VSYNC (Verticle Sync)
- DE (Data Enable)
- R/G/B (Data Lines)



Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data



Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
 - 640 Width x 480 Height

Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
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 - $640 \times 480 = 307200$ clocks for one frame

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 - $640 \times 480 = 307200$ clocks for one frame
 - $307200 \times 60 = 18432000$ for 60 frames per second

Interface Timings

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 - $640 \times 480 = 307200$ clocks for one frame
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 - Estimated PCLK = 18.432MHz

Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
 - 640 Width x 480 Height
 - $640 \times 480 = 307200$ clocks for one frame
 - $307200 \times 60 = 18432000$ for 60 frames per second
 - Estimated PCLK = 18.432MHz
 - What if your SoC can not create exactly 18.432MHz?

Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
 - 640 Width x 480 Height
 - $640 \times 480 = 307200$ clocks for one frame
 - $307200 \times 60 = 18432000$ for 60 frames per second
 - Estimated PCLK = 18.432MHz
 - What if your SoC can not create exactly 18.432MHz?
 - Good question!!!!

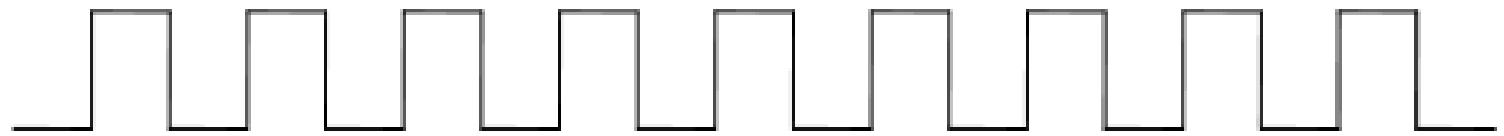
Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
- Line Timing – HSYNC and DE

Interface Timings

Horizontal SYNC and Data Enable

Pixel clock



RGB Data



Enable



Horizontal Sync

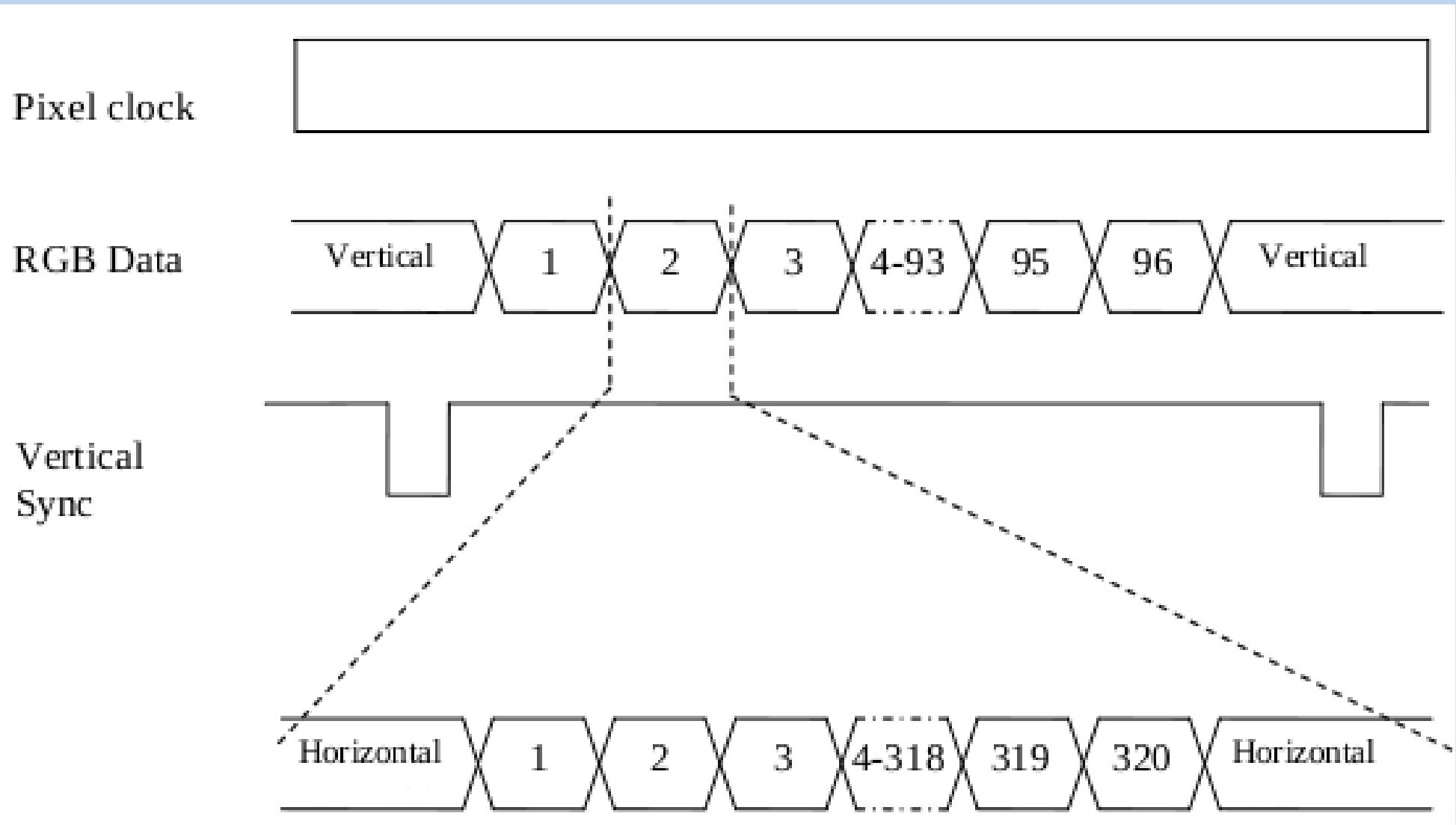


Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
- Line Timing – HSYNC and DE
- Frame Timing - VSYNC

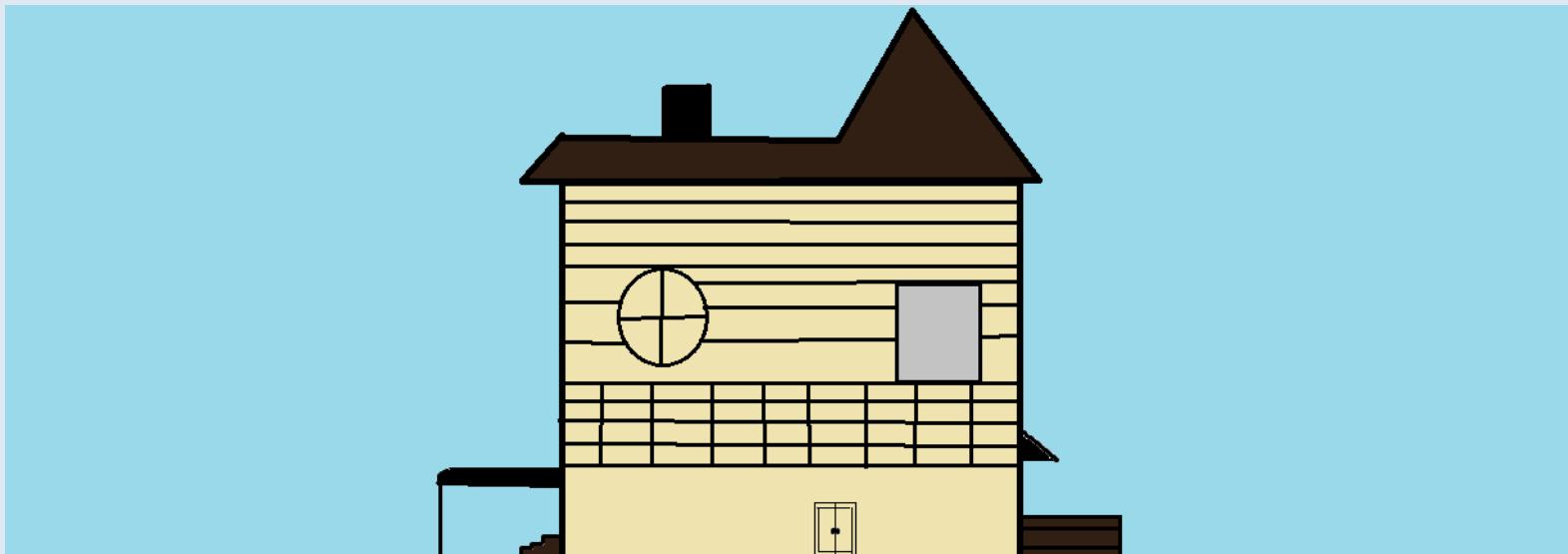
Interface Timings

Vertical SYNC



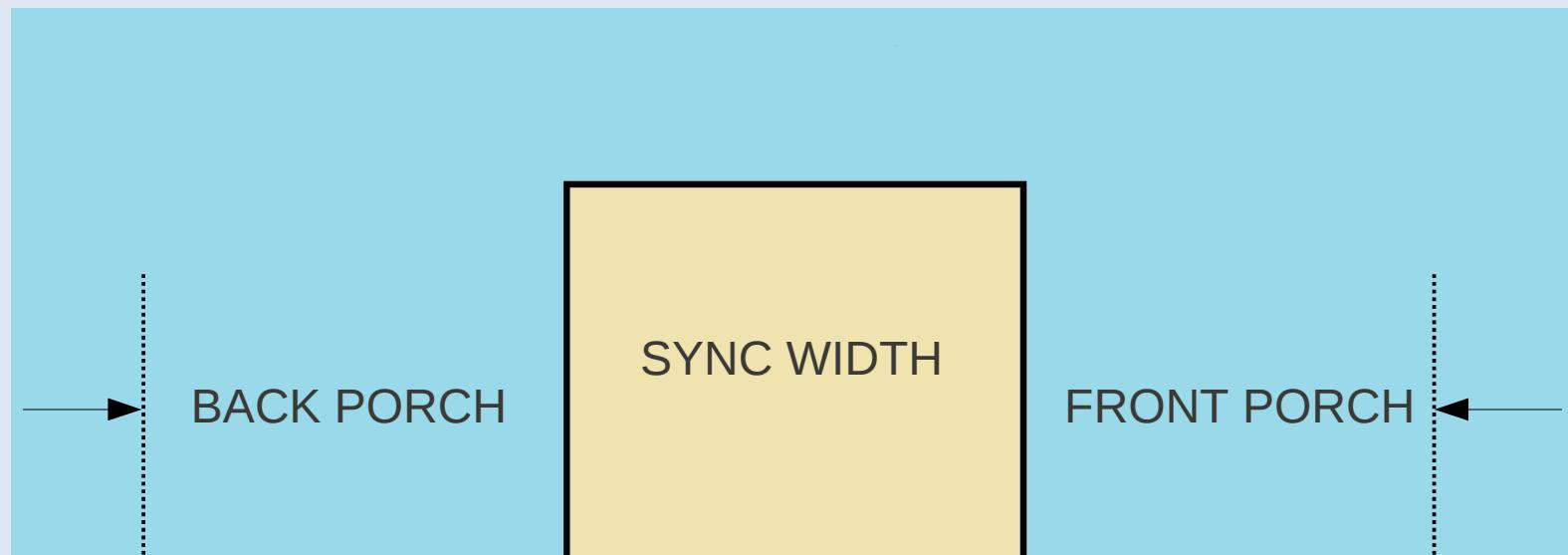
Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
- Line Timing – HSYNC and DE
- Frame Timing – VSYNC
- Front Porch / Back Porch / Sync Width



Interface Timings

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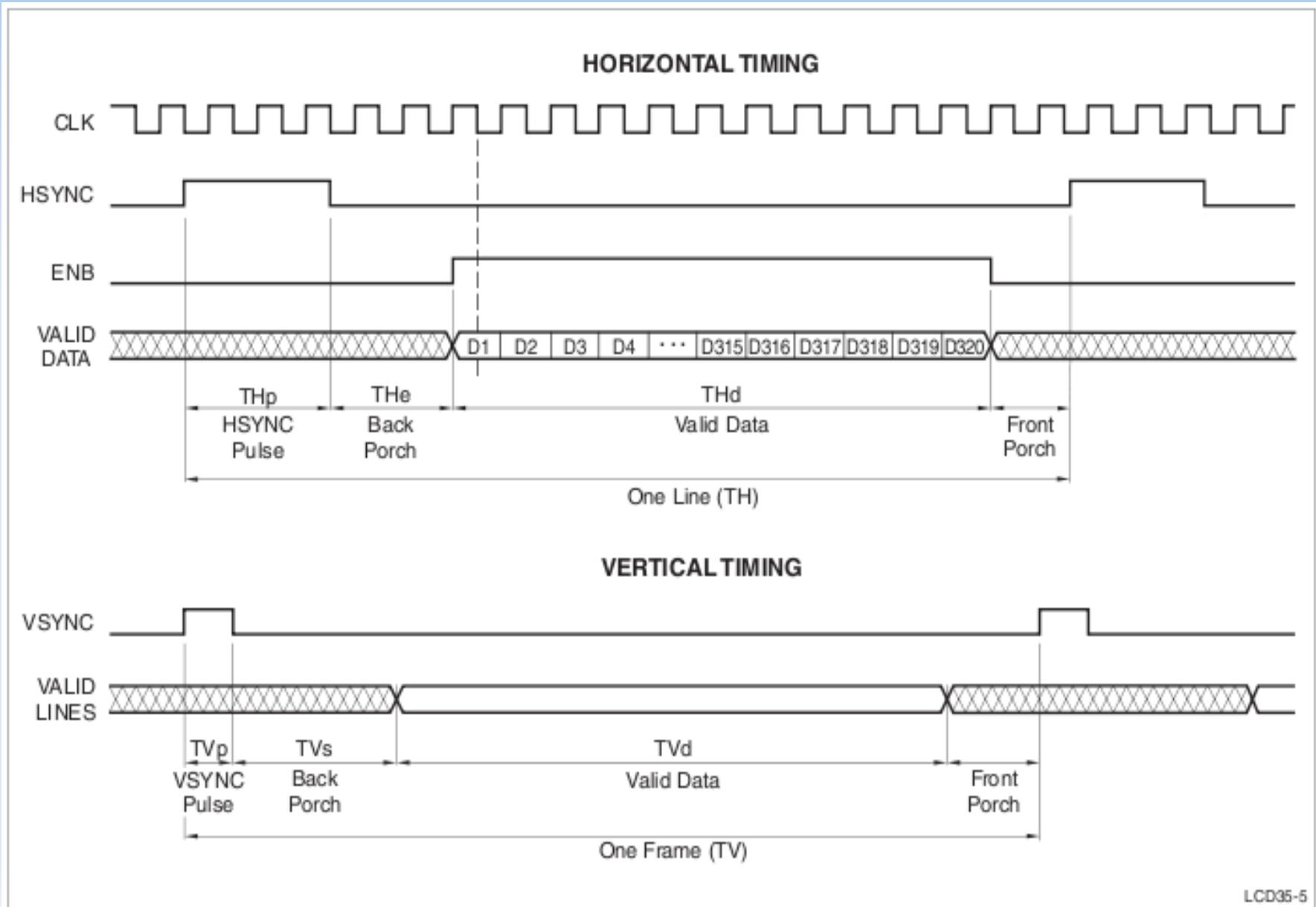


Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
- Line Timing – HSYNC and DE
- Frame Timing – VSYNC
- Front Porch / Back Porch / Sync Width
 - Remember the question about exact pixel clock?
 - Use FP/BP/SW to pad timings

Interface Timings

TIMING OVERVIEW



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Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
- Line Timing – HSYNC and DE
- Frame Timing – VSYNC
- Front Porch / Back Porch / Sync Width
- EDID

Interface Timings

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- EDID
 - Lots of numbers to keep track of

Interface Timings

- TFT Parallel Interface
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- Front Porch / Back Porch / Sync Width
- EDID
 - Lots of numbers to keep track of
 - Extended Display Identification Data

Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
- Line Timing – HSYNC and DE
- Frame Timing – VSYNC
- Front Porch / Back Porch / Sync Width
- EDID
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 - Extended Display Identification Data
 - I2C EEPROM at 0x50

Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
- Line Timing – HSYNC and DE
- Frame Timing – VSYNC
- Front Porch / Back Porch / Sync Width
- EDID
 - Lots of number to keep track of
 - Extended Display Identification Data
 - I2C EEPROM at 0x50
 - Parse-edid and sysfs entries

Interface Timings

- EDID Contents
 - Multiple Configurations
 - Pixel Clock Frequency
 - Resolution
 - Color Depth
 - Front Porch / Back Porch
 - SYNC width

Display Interface Types

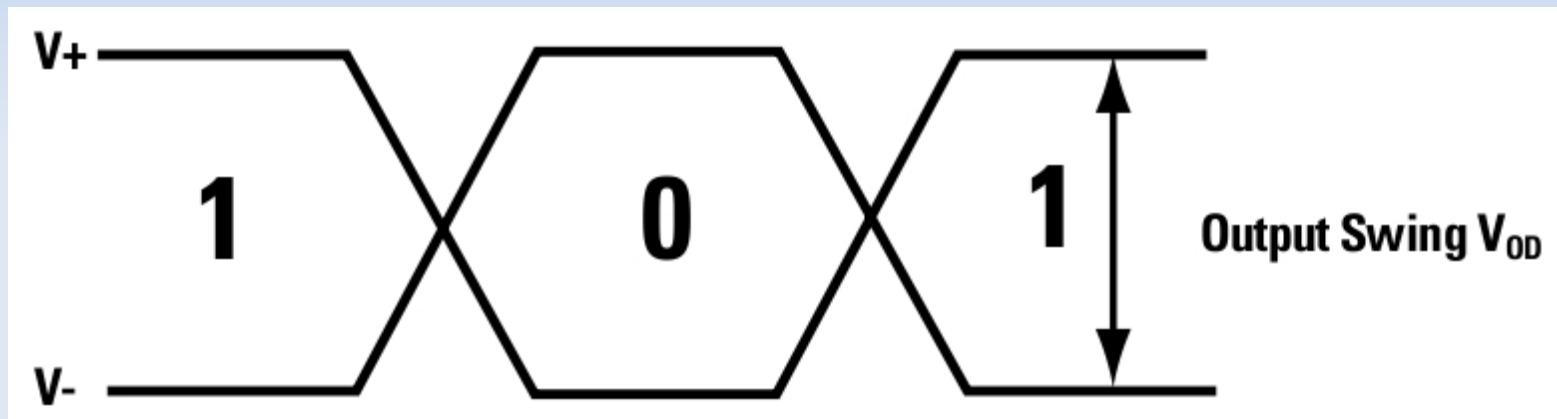
- Disadvantages of Parallel Interface

Display Interface Types

- Disadvantages of Parallel Interface
 - Large Number of Signals
 - Limited Distance
 - Lack of Standardization

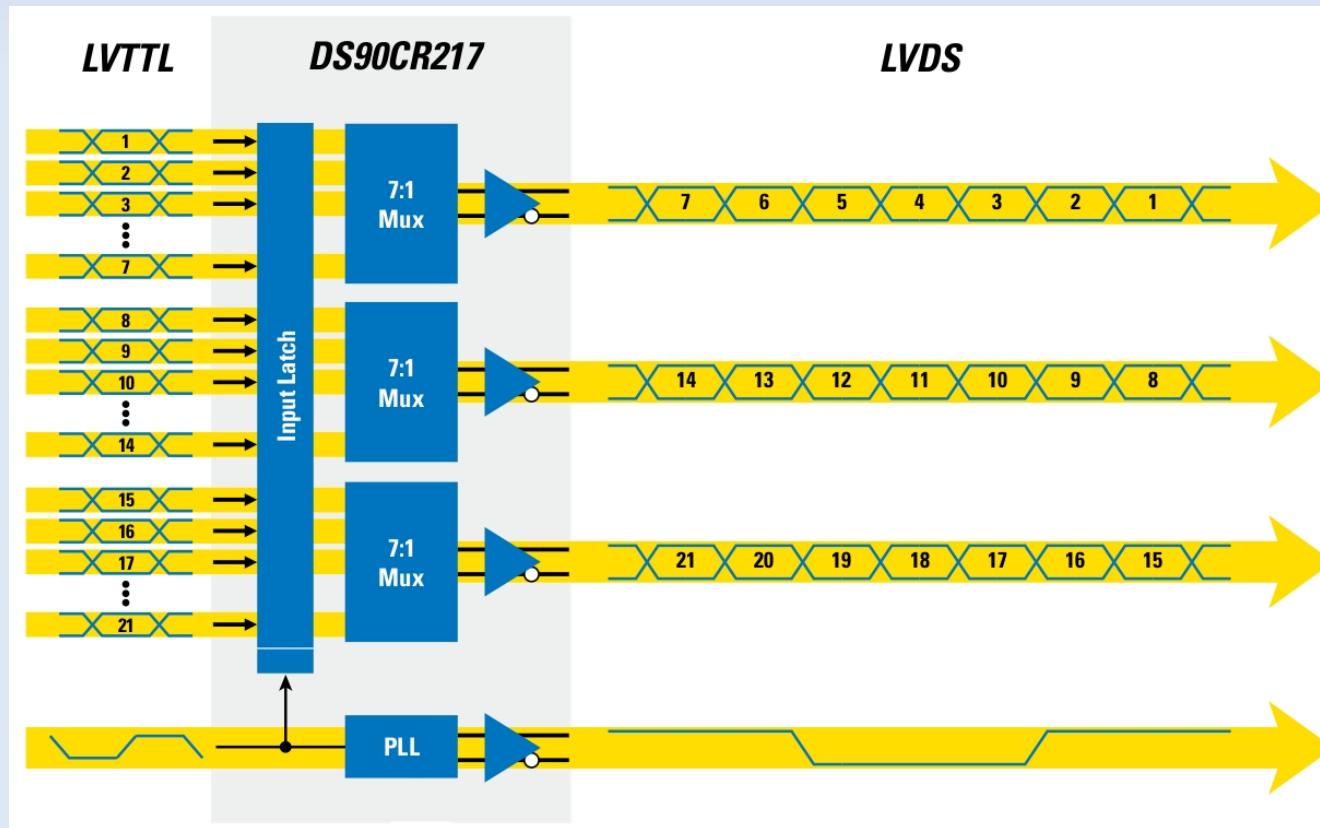
Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces



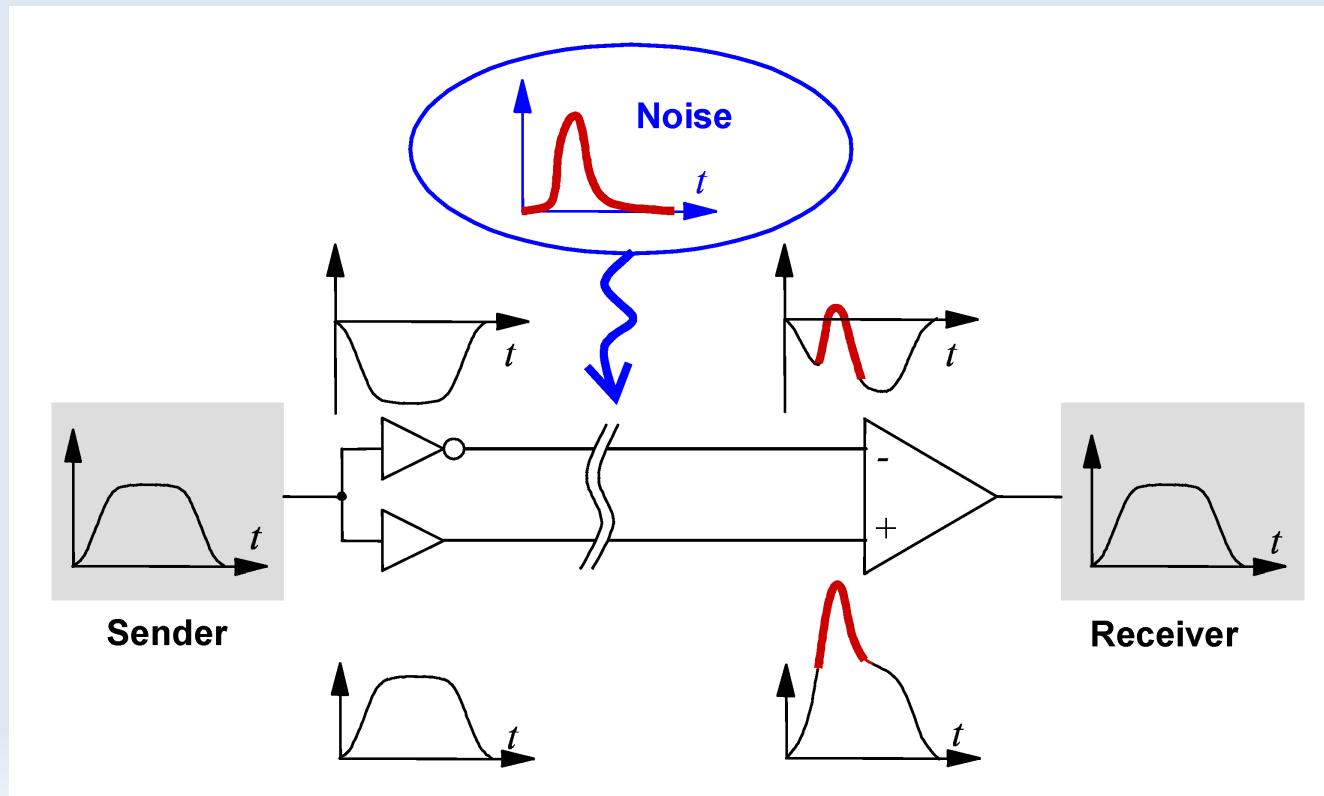
Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
 - Reduced number of signals



Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
 - Reduced number of signals
 - Longer distances



Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
- Common Differential Interfaces

Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
- Common Differential Interfaces
 - LVDS – Low Voltage Differential Signaling

Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
- Common Differential Interfaces
 - LVDS – Low Voltage Differential Signaling
 - DVI - Digital Visual Interface

Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
- Common Differential Interfaces
 - LVDS – Low Voltage Differential Signaling
 - DVI - Digital Visual Interface
 - HDMI - High-Definition Multimedia Interface

Display Interface Types

- Disadvantages of Parallel Interface
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- Common Differential Interfaces
 - LVDS – Low Voltage Differential Signaling
 - DVI - Digital Visual Interface
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 - DisplayPort

Display Interface Types

- Disadvantages of Parallel Interface
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- Common Differential Interfaces
 - LVDS – Low Voltage Differential Signaling
 - DVI - Digital Visual Interface
 - HDMI - High-Definition Multimedia Interface
 - DisplayPort
 - MIPI DSI

Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
- Common Differential Interfaces
- Why learn TFT when working with Differential?

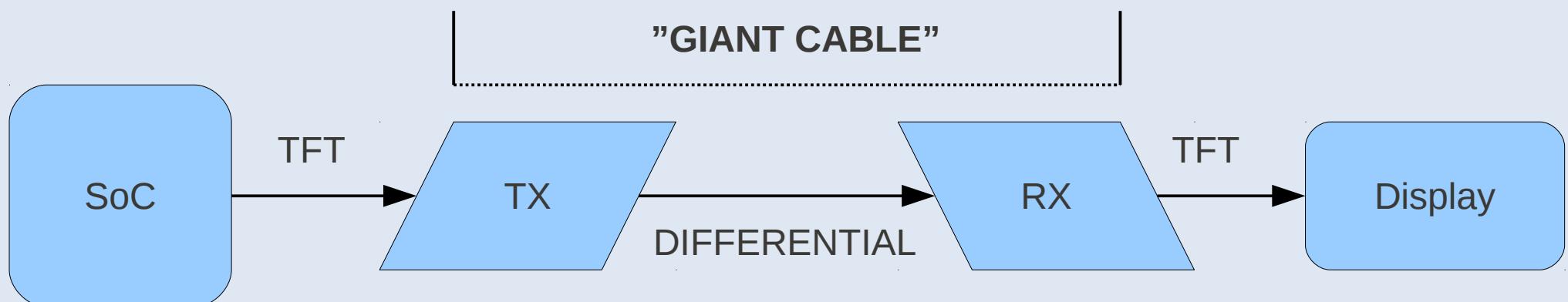
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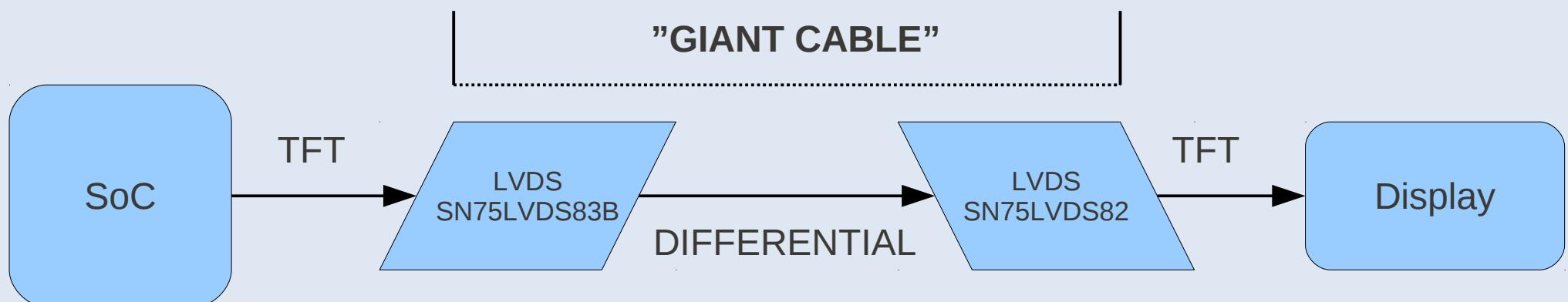
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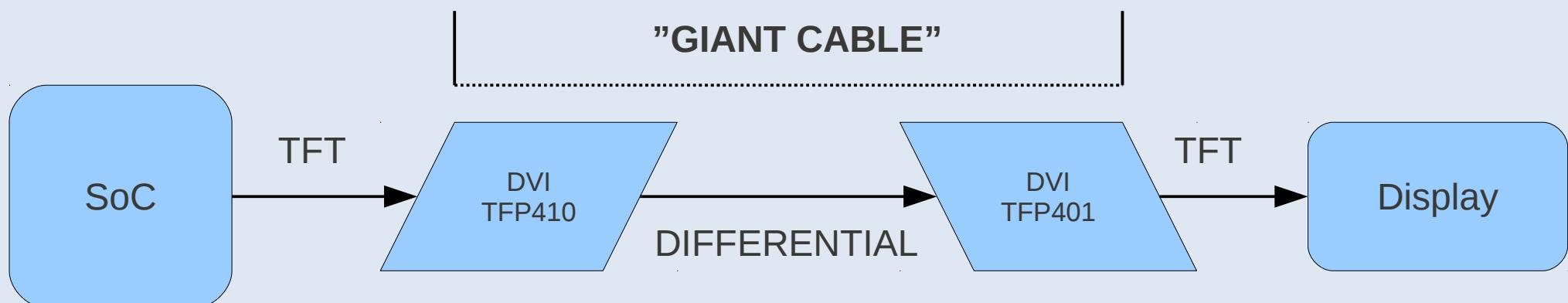
Display Interface Types

- Disadvantages of Parallel Interface
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- Common Differential Interfaces
- Why learn TFT when working with Differential?
 - LVDS SN75LVDS83B – SN75LVDS82



Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
- Common Differential Interfaces
- Why learn TFT when working with Differential?
 - LVDS SN75LVDS83B – SN75LVDS82
 - DVI TFP410 – TFP401



Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
- Common Differential Interfaces
- Why learn TFT when working with Differential?
- Combination Interfaces



Debugging

- Logic Analyzer / Oscilloscope
 - Importance of visualization



Debugging

- Logic Analyzer / Oscilloscope
 - Importance of visualization
 - Pixel clock frequency
 - Small Displays < 50MHz
 - Midsized Displays < 100MHz
 - Large Display < 200MHz

Debugging

- Logic Analyzer / Oscilloscope
 - Importance of visualization
 - Pixel clock frequency
 - Open source (or open source friendly)

Debugging

- Logic Analyzer / Oscilloscope
 - Importance of visualization
 - Pixel clock frequency
 - Open source (or open source friendly)
 - SIGROK
 - ChronoVu LA8 (less than \$200)

Debugging

- Logic Analyzer / Oscilloscope
- Reference Platform

Debugging

- Logic Analyzer / Oscilloscope
- Reference Platform
 - Same platform – different display

Debugging

- Logic Analyzer / Oscilloscope
- Reference Platform
 - Same platform – different display
 - Different platform – same display

Debugging

- Logic Analyzer / Oscilloscope
- Reference Platform
 - Same platform – different display
 - Different platform – same display
 - Compatible display

Debugging

- Logic Analyzer / Oscilloscope
- Reference Platform
 - Same platform – different display
 - Different platform – same display
 - Compatible display
 - Kernel sources

Debugging

- Logic Analyzer / Oscilloscope
- Reference Platform
- Display Simulation

Debugging

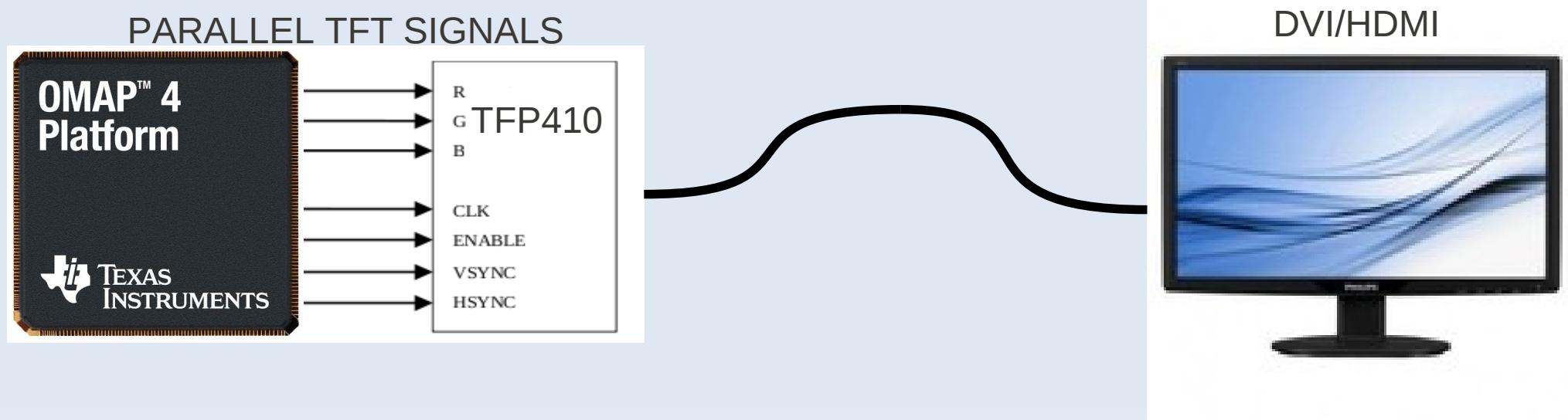
- Logic Analyzer / Oscilloscope
- Reference Platform
- Display Simulation
 - Use a Lower resolution

640x480@18.5MHz

1920x1200@140MHz

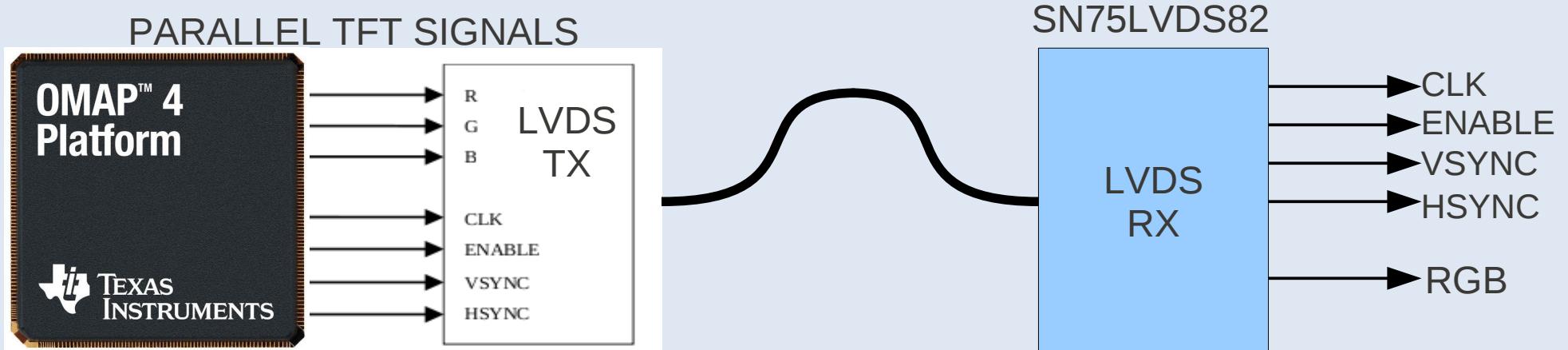
Debugging

- Logic Analyzer / Oscilloscope
- Reference Platform
- Display Simulation
 - Use a Lower resolution
 - Transmitter Chips TFP410 to DVI display



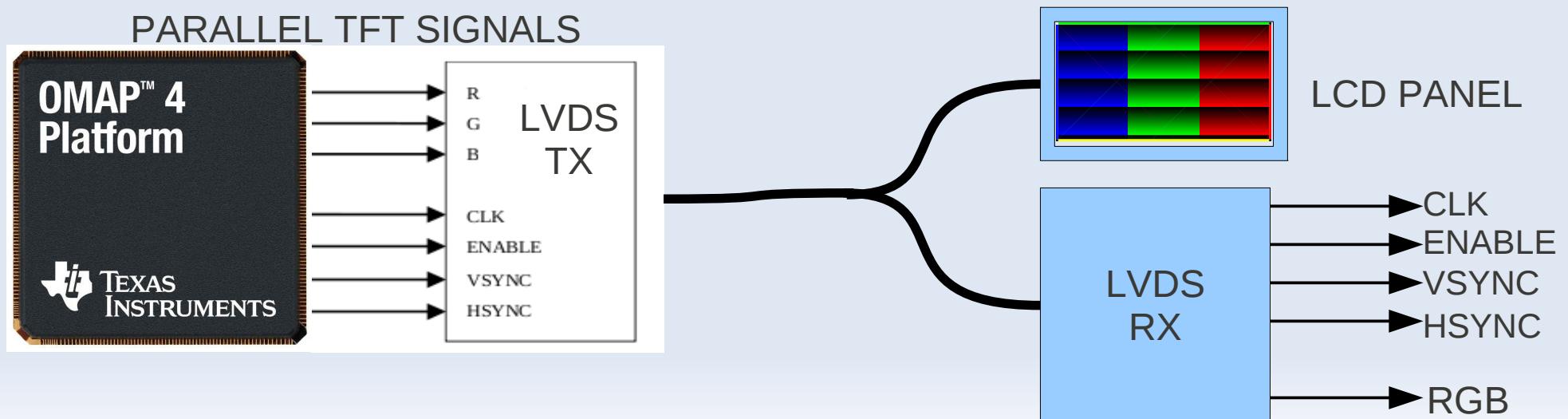
Debugging

- Logic Analyzer / Oscilloscope
- Reference Platform
- Display Simulation
 - Use a Lower resolution
 - Transmitter Chips TFP410 to DVI display
 - Receiver Chips LVDS to SN75LVDS82

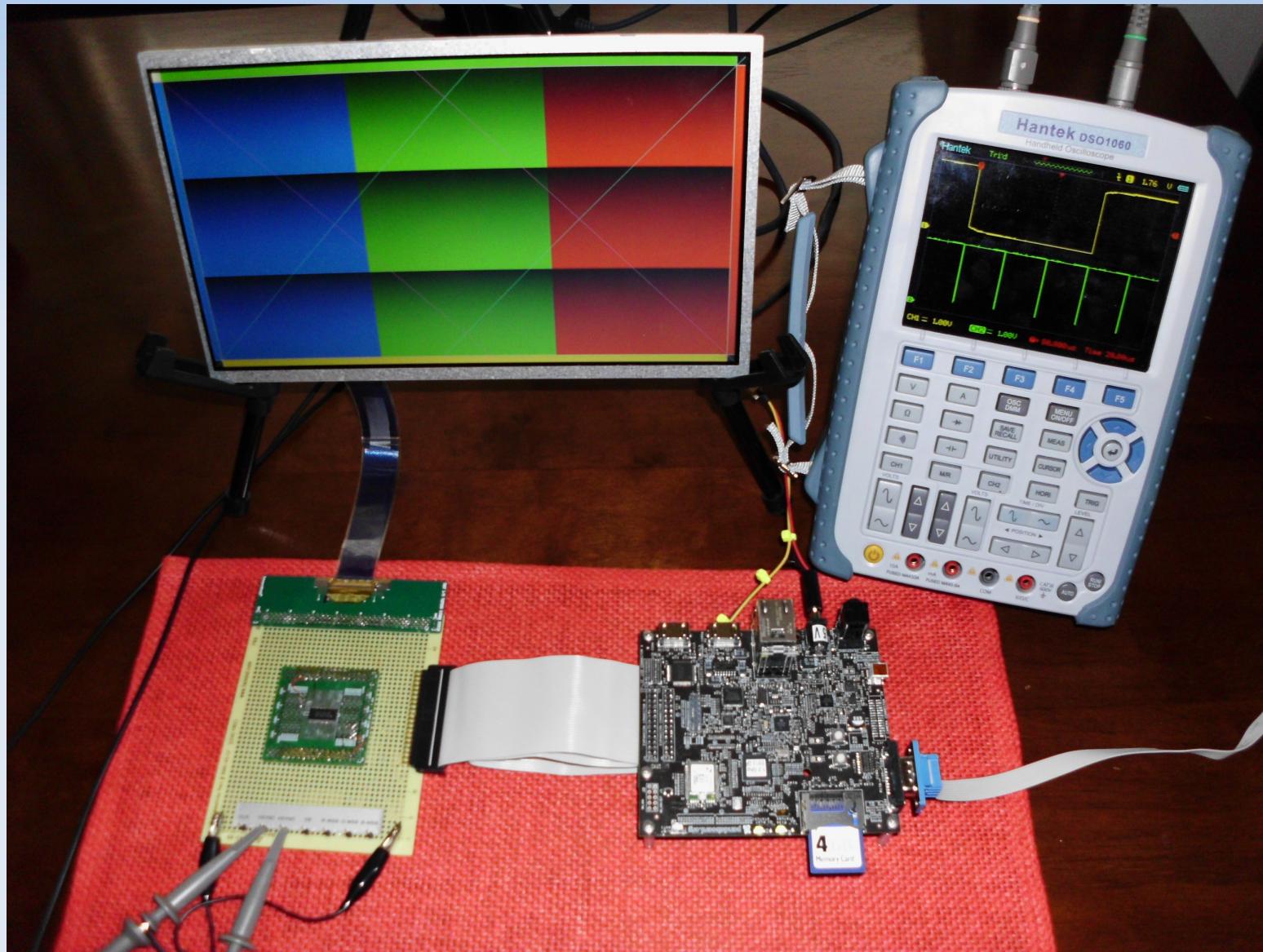


Debugging

- Logic Analyzer / Oscilloscope
- Reference Platform
- Display Simulation
 - Use a Lower resolution
 - Transmitter Chips TFP410 to DVI display
 - Receiver Chips LVDS to SN75LVDS82



Debugging



Debugging

- Logic Analyzer / Oscilloscope
- Reference Platform
- Display Simulation
- Userspace debugging

Debugging

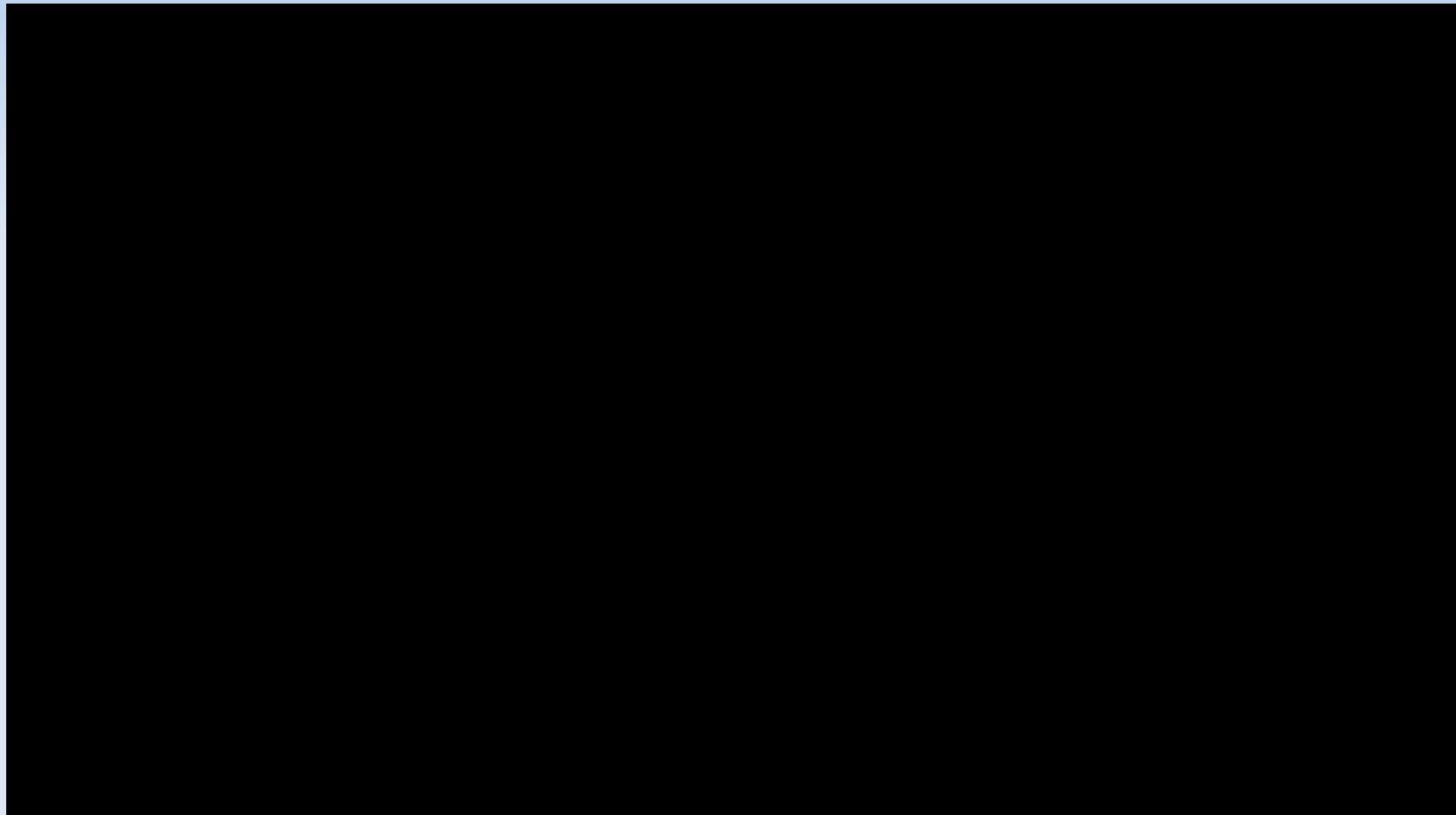
- `cat /dev/urandom > /dev/fb0`



Random Data to FrameBuffer

Debugging

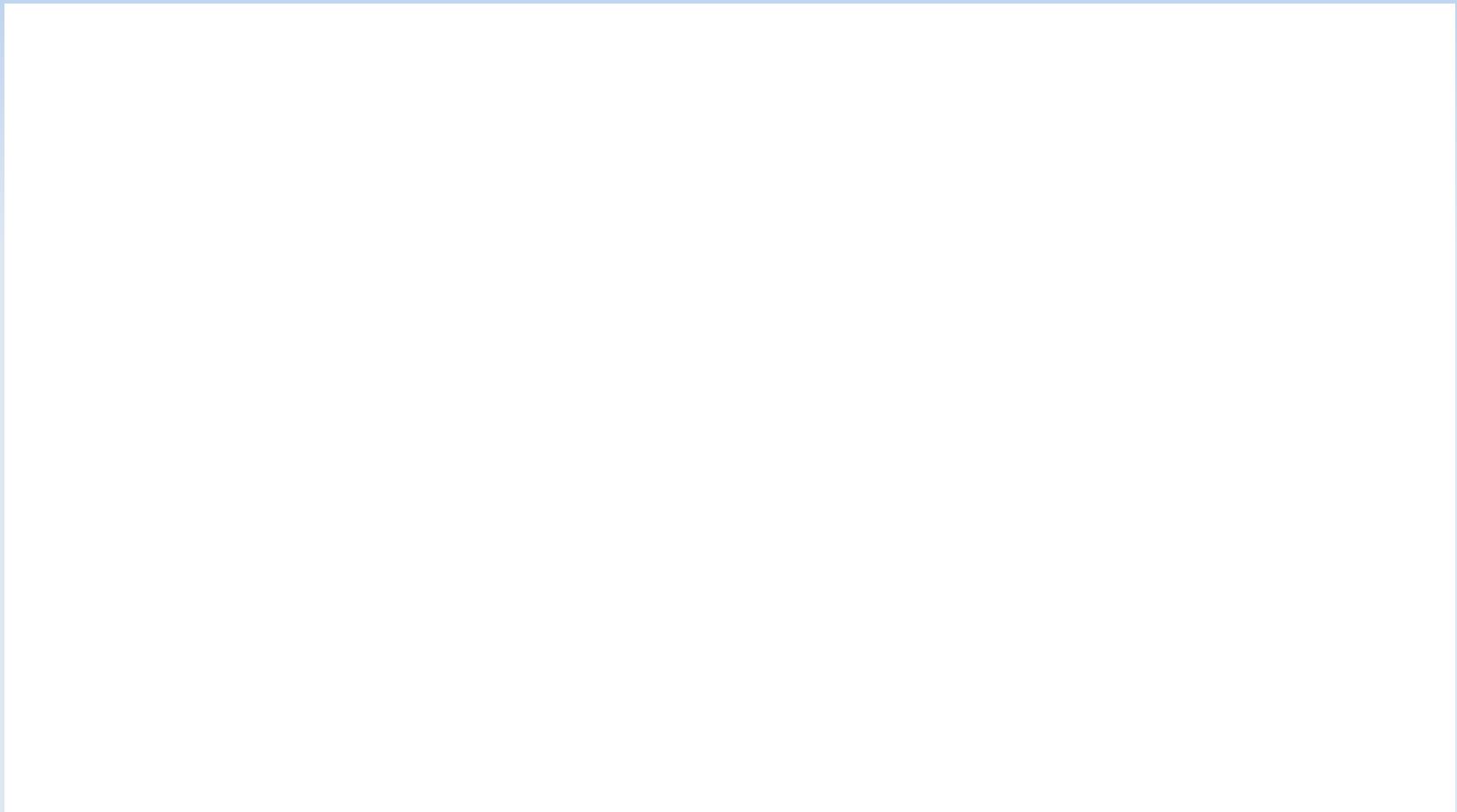
- `cat /dev/zero > /dev/fb0`



All Zeros to FrameBuffer

Debugging

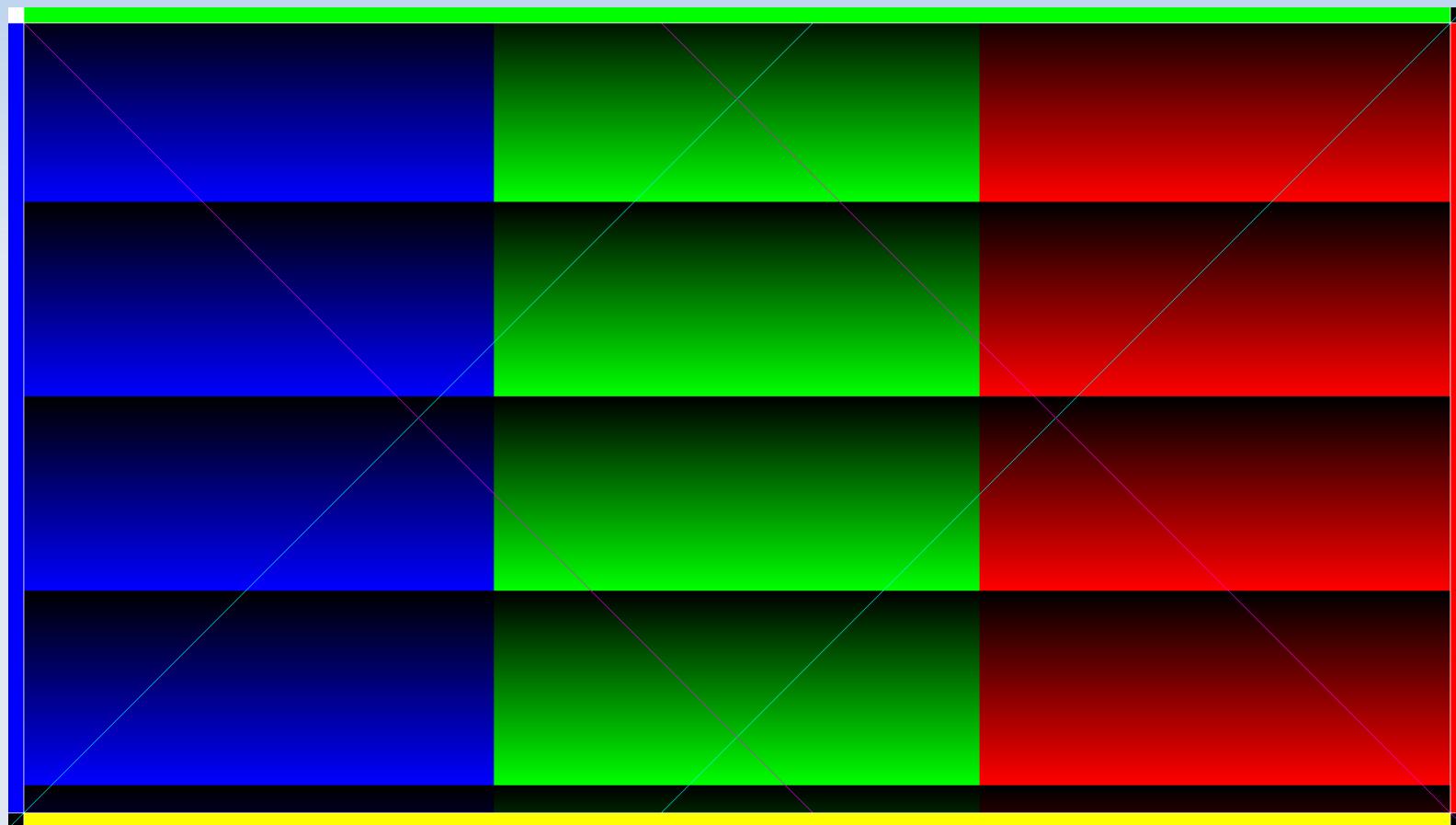
- `cat /dev/zero | tr '\000' '\377' > /dev/fb0`



All Ones to FrameBuffer

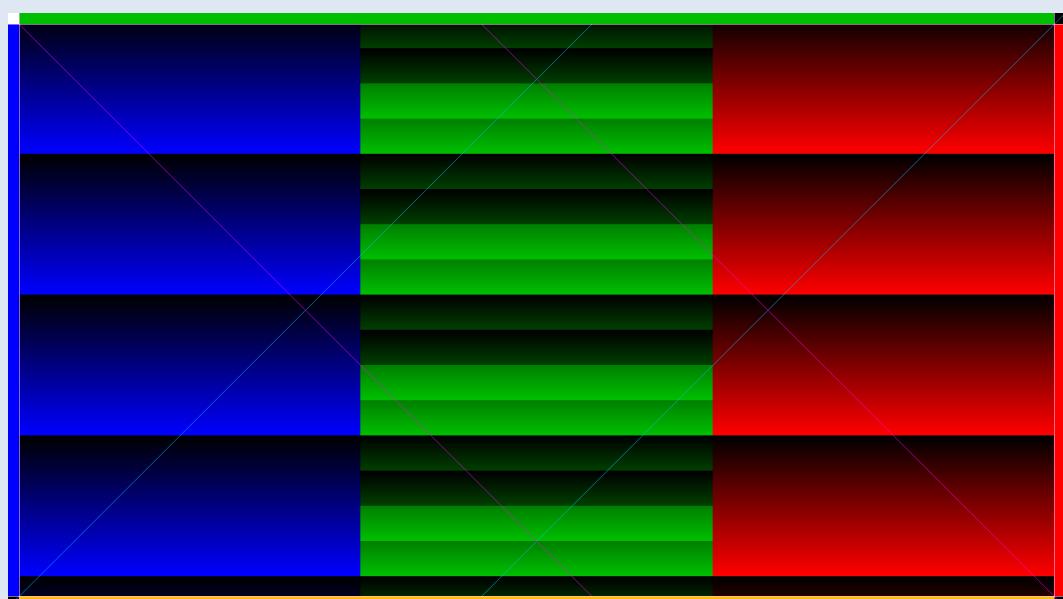
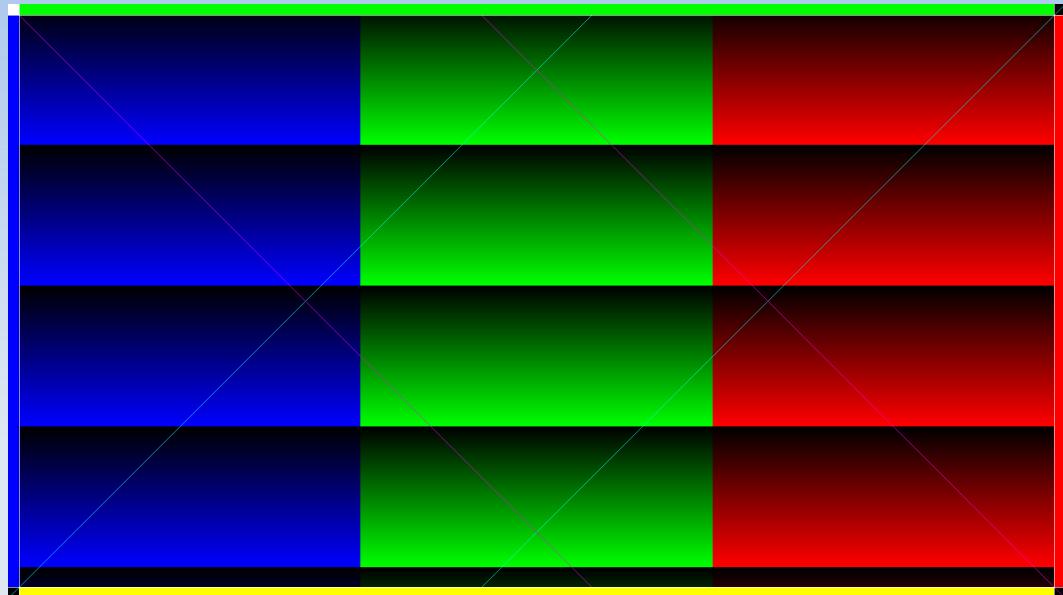
Debugging

- fb-test



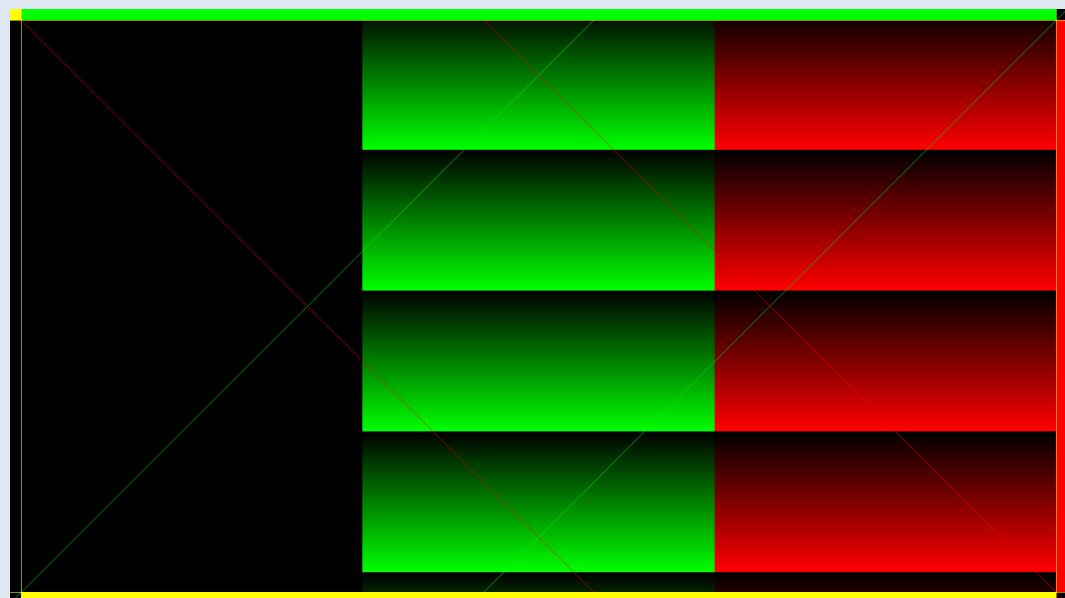
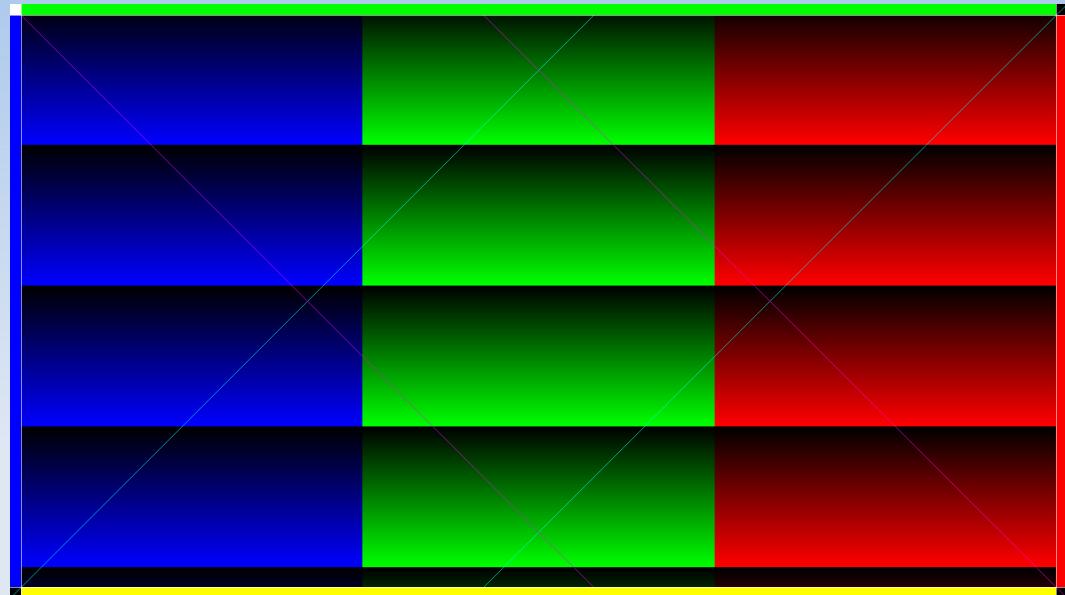
Debugging

Missing Green
Data Bit



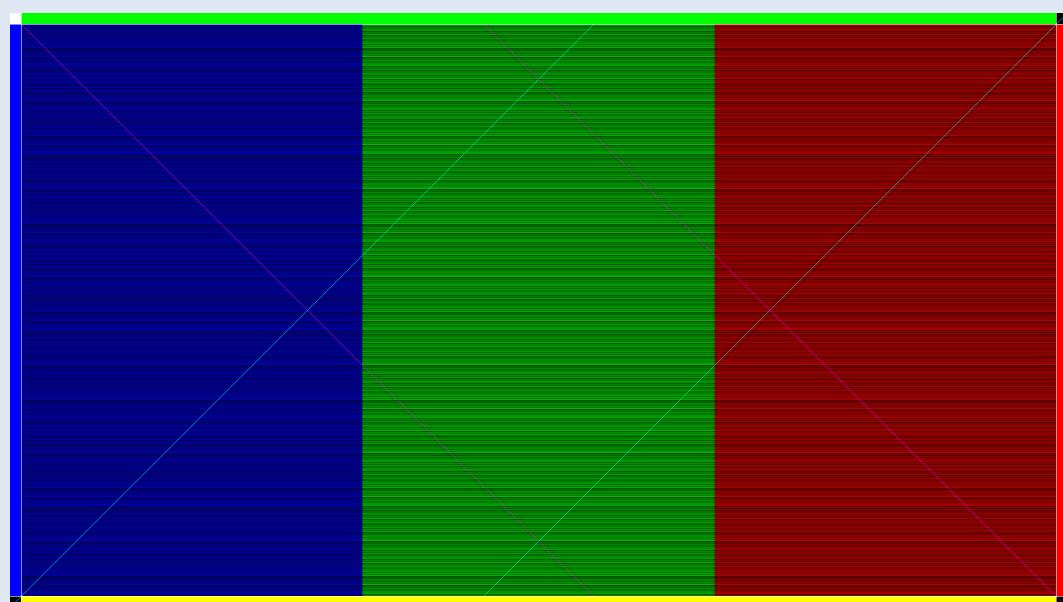
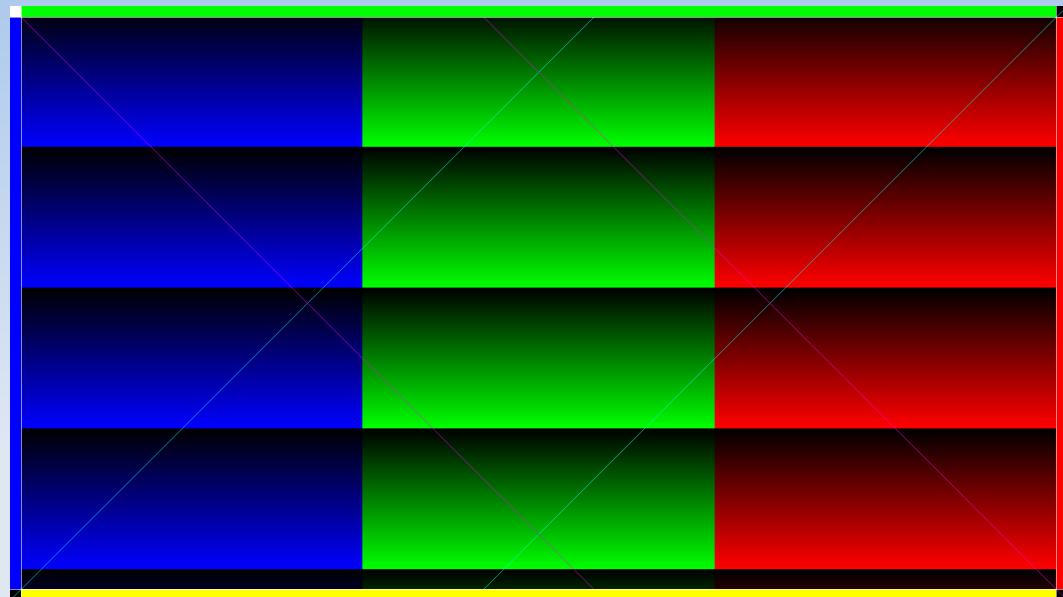
Debugging

Missing Blue
Signals



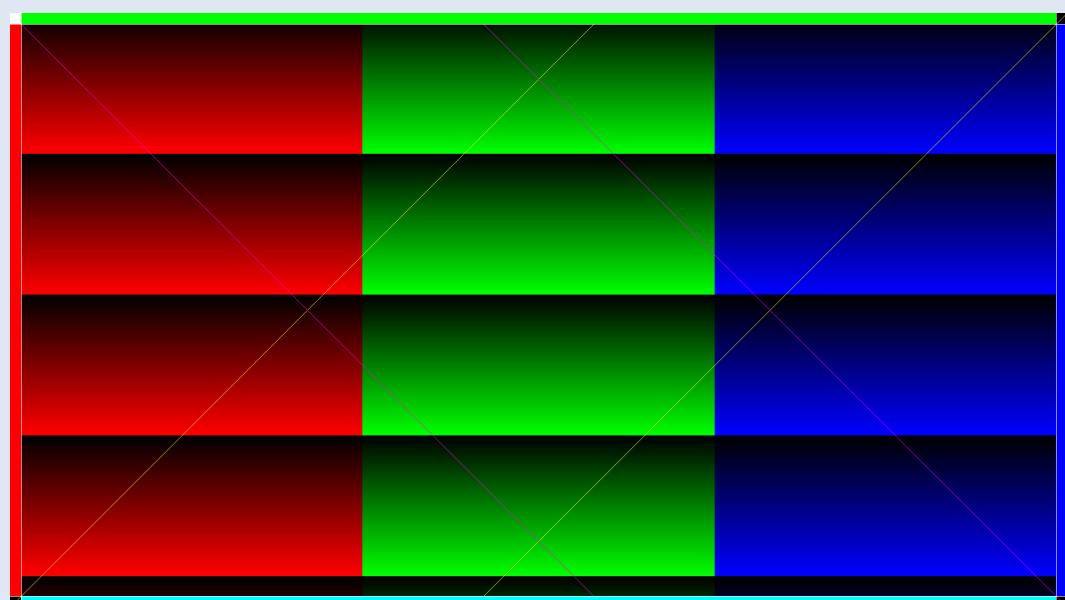
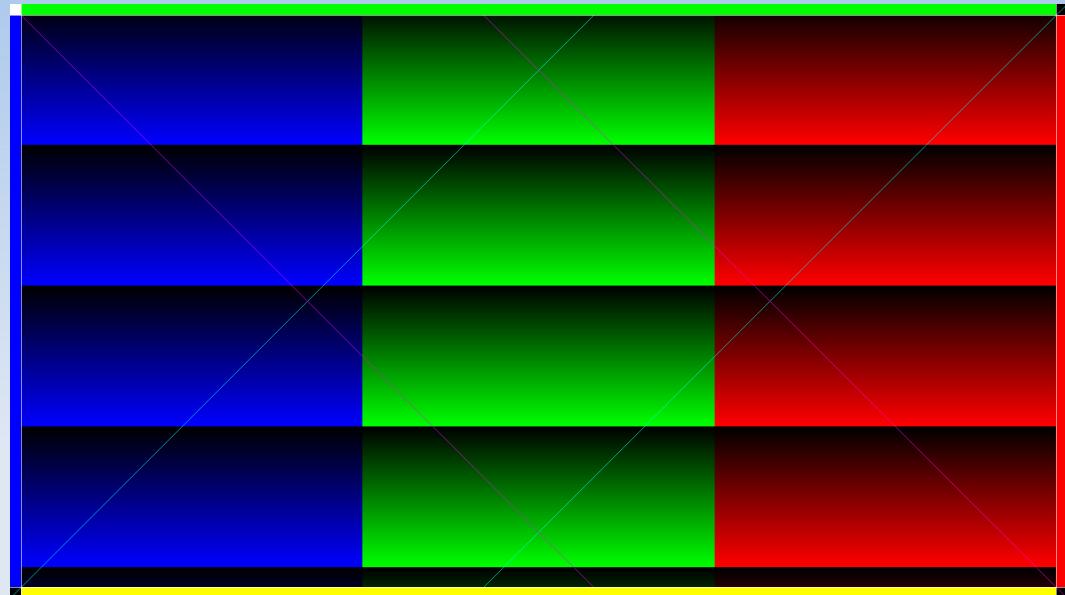
Debugging

LSB/MSB
Signal Swap



Debugging

Red/Blue
Signal Swap



Conclusion

- Summary
 - Challenges of LCD bring up
 - Interface Timings
 - Display Interfaces
 - Debugging

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- Resources
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Conclusion

Questions?

Tech Showcase @ 6:30PM