### /VI/IXI/VI

### Precision Low Voltage Micropower Operational Amplifier

#### **General Description**

The OP90 is a precision bipolar micropower operational amplifier with flexible power supply capability. Both the input voltage range and output voltage swing of the OP90 include the negative rail, allowing "ground-sensing" operation when the part is driven from a single positive voltage supply. The OP90 will accept a single power supply voltage of any value in the range +1.6V to +36V. Alternatively, the amplifier can be operated from dual power supplies in the range of  $\pm 0.8V$  to  $\pm 18V$ .

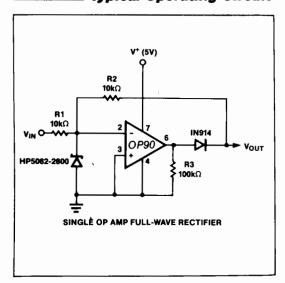
Unlike most other micropower operational amplifiers, the OP90 requires no external current setting resistor, and consumes less than  $20\mu\text{A}$  of quiescent current, allowing operation from a lithium battery of greater than 10,000 hours. Even with this minimal current consumption, the amplifier can sink or source 5mA of current into the load.

Every OP90 (A/E grade) is internally trimmed to guarantee an input offset voltage of less than  $150\mu V$ . This eliminates the need for external nulling in most applications, although null pins are provided if required. The guaranteed minimum open loop gain of 700,000 together with power supply rejection ratio of  $5.6\mu V/V$  and common-mode rejection ratio of  $100 \, \mathrm{dB}$  allow the OP90 to be used in applications requiring low power operation together with precision performance.

#### **Applications**

Precision Micropower Amplifiers Micropower Signal Processing Battery Powered Analog Circuits

### Typical Operating Circuit



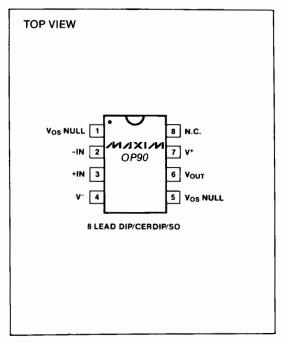
#### Features

- ♦ Single/Dual Supply Operation: +1.6V to +36V, ±0.8V to ±18V
- ♦ True Single-Supply Operation: Input and Output Voltage Ranges Include Ground
- Low Supply Current: 20μA Max
- ♦ High Output Drive: 5mA Min
- ♦ Low Input Offset Voltage: 150µV Max
- ♦ High Open Loop Gain: 700V/mV Min
- High PSRR: 5.6μV/V Max
- ♦ Standard 741 Pin Out With Nulling to V<sup>-</sup>

#### **Ordering Information**

PART	TEMP. RANGE	PACKAGE
OP90AZ	-55°C to +125°C	8 Lead CERDIP
OP90EZ	-25°C to +85°C	8 Lead CERDIP
OP90FZ	-25°C to +85°C	8 Lead CERDIP
OP90GP	0°C to +70°C	8 Lead Plastic DIP
OP90GS	0°C to +70°C	8 Lead SO
OP90GC/D	0°C to +70°C	Dice

#### Pin Configuration



### **ABSOLUTE MAXIMUM RATINGS (Note 1)**

Internal Power Dissipation	Storage Temperature Range       -65° C to +150° C         Operating Temperature Range       -55° C to +125° C         OP90A       -55° C to +85° C         OP90E, OP90F       -25° C to +85° C         OP90G       0° C to +70° C         Junction Temperature (T <sub>J</sub> )       -65° C to +160° C         Lead Temperature (Soldering, 10 sec)       +300° C
Output Short Circuit Duration Indefinite	

Note 1: Absolute maximum ratings apply to both packaged parts and Dice, unless otherwise noted.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **ELECTRICAL CHARACTERISTICS**

( $V_S = \pm 1.5V$  to  $\pm 15V$ ,  $T_A = +25$ °C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP90A/E			OP90F			OP90G			UNITS
PARAMETER	SIMBOL		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	-
Input Offset Voltage	Vos			50	150		75	250		125	450	μ٧
Input Offset Current	los	V <sub>CM</sub> = 0V		0.4	3		0.4	5		0.4	5	nA
Input Bias Current	IB	V <sub>CM</sub> = 0V		4.0	15		4.0	20		4.0	25	nA
Large Signal A <sub>VC</sub> Voltage Gain	Avo	$V_S = \pm 15V, V_O = \pm 10V$ $R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	700 350 125	1200 600 250		500 250 100	1000 500 200		400 200 100	800 400 200		V/mV
	V	$V^{+} = 5V, V^{-} = 0V,$ $1V < V_{O} < 4V$ $R_{L} = 100k\Omega$ $R_{L} = 10k\Omega$	200 100	400 180		125 75	300 140		100 70	250 140		7,
Input Voltage Range	IVR	V <sup>+</sup> = 5V, V <sup>-</sup> = 0V V <sub>S</sub> = ±15V (Note 2)	0/4 -15/13.5			0/4 -15/13.5			0/4 -15/13.5			V
	Vo	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	±14 ±11	±14.2 ±12		±14 ±11	±14.2 ±12		±14 ±11	±14.2 ±12		v
Output Voltage Swing	V <sub>OH</sub>	$V^+ = 5V, V^- = 0V$ $R_L = 2k\Omega$	4.0	4.2		4.0	4.2		4.0	4.2		V
	V <sub>OL</sub>	$V^+ = 5V$ , $V^- = 0V$ $R_L = 10k\Omega$		100	500		100	500		100	500	μ۷
Common Mode Rejection Ratio	CMRR	$V^{+} = 5V, V^{-} = 0V,$ $0V < V_{CM} < 4V$ $V_{S} = \pm 15V,$ $-15V < V_{CM} < 13.5V$	90 100	110 130		80 90	100 120		80 90	100 120		dB
Power Supply Rejection Ratio	PSRR			1.0	5.6		1.0	5.6	-	3.2	10	μ\/\
Slew Rate	SR	V <sub>S</sub> = ±15V	5	12		5	12		5	12		V/ms
Supply Current	I <sub>SY</sub>	V <sub>S</sub> = ±1.5V V <sub>S</sub> = ±15V		9 14	15 20		9 14	15 20		9 14	15 20	μΑ
Capacitive Load Stability		A <sub>V</sub> = +1 No Oscillations (Note 3)	250	650		250	650		250	650		pF

## **ELECTRICAL CHARACTERISTICS (continued)** $(V_S = \pm 1.5V \text{ to } \pm 15V, T_A = +25^{\circ}\text{C}, \text{ unless otherwise noted.})$

PARAMETER	SYMBOL	CONDITIONS	OP90A/E			OP90F			OP90G			UNITS
PARAMETER	J. INIDOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	-
Input Noise Voltage	e <sub>np-p</sub>	f <sub>O</sub> = 0.1Hz to 10Hz V <sub>S</sub> = ±15V		3			3			3		μV <sub>p-p</sub>
Input Resistance Differential Mode	R <sub>IN</sub>	V <sub>S</sub> = ±15V		30			30			30		МΩ
Input Resistance Common Mode		V <sub>S</sub> = ±15V		20			20			20		GΩ

Note 2: Guaranteed by CMRR test. Note 3: Guaranteed by design.

### **ELECTRICAL CHARACTERISTICS**

(V  $_{S}$  =  $\pm 1.5 V$  to  $\pm 15 V$ , -55° C  $\leq T_{A} \leq 125 ^{\circ} C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		OP90A				
PARAMETER	STANDOL	CONDITIONS	MIN	TYP	MAX	UNITS		
Input Offset Voltage	Vos			80	400	μ٧		
Average Input Offset Voltage Drift	TCVos			0.3	2.5	μV/°C		
Input Offset Current	los	V <sub>CM</sub> = 0V		1.5	5	nA		
Input Bias Current	IB	V <sub>CM</sub> = 0V		4.0	20	nA		
Large Signal	Avo	$\begin{split} &V_S=\pm 15 V,  V_O=\pm 10 V \\ &R_L=100 k \Omega \\ &R_L=10 k \Omega \\ &R_L=2 k \Omega \end{split}$	225 125 50	400 240 110		V/mV		
Voltage Ğain	7,40	$V^{+} = 5V, V^{-} = 0V,$ $1V < V_{O} < 4V$ $R_{L} = 100k\Omega$ $R_{L} = 10k\Omega$	100 50	200 110		\ \psi_1 \psi_2 \psi_1 \psi_2 \		
Input Voltage Range	IVR	V <sup>+</sup> = 5V, V <sup>-</sup> = 0V V <sub>S</sub> = ±15V (Note 4)	0/3.5 -15/13.5			v		
	V <sub>o</sub>	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	±13.5 ±10.5	±13.7 ±11.5		v		
Output Voltage Swing	, V <sub>OH</sub>	$V^+ = 5V$ , $V^- = 0V$ $R_L = 2k\Omega$	3.9	4.1		v		
	V <sub>OL</sub>	$V^{+} = 5V, V^{-} = 0V$ R <sub>L</sub> = $10k\Omega$		100	500	μ٧		
Common Mode Rejection Ratio	CMRR	$V^+ = 5V$ , $V^- = 0V$ , $0V < V_{CM} < 3.5V$ $V_S = \pm 15V$ , $-15V < V_{CM} < 13.5V$	85 95	105 115		dB		
Power Supply Rejection Ratio	PSRR			3.2	10	μ\/\		
Supply Current	I <sub>SY</sub>	V <sub>S</sub> = ±1.5V V <sub>S</sub> = ±15V		15 19	25 30	μΑ		

Note 4: Guaranteed by CMRR test.

PARAMETER	SYMBOL	CONDITIONS	OP90E			OP90G, unless other			OP90G			UNITS
PANAMICIEN	SIMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	34113
Input Offset Voltage	Vos			70	270		110	550		180	675	μ۷
Average Input Offset Voltage Drift	TCVos			0.3	2		0.6	5		1.2	5	μV/°C
Input Offset Current	los	V <sub>CM</sub> = 0V		0.8	3		1.0	5		1.3	7	nA
Input Bias Current	IB	V <sub>CM</sub> = 0V		4.0	15		4.0	20		4.0	25	nA
Large Signal Voltage Gain		$V_S = \pm 15V, V_O = \pm 10V$ $R_L = 100k\Omega$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	500 250 100	800 400 200		350 175 75	700 350 150		300 150 75	600 250 125		- V/mV
		$V^{+} = 5V$ , $V^{-} = 0V$ , $1V < V_{O} < 4V$ $R_{L} = 100k\Omega$ $R_{L} = 10k\Omega$	150 75	280 140		100 50	220 110		80 40	160 90		
Input Voltage Range	IVR	$V^{+} = 5V, V^{-} = 0V$ $V_{S} = \pm 15V \text{ (Note 5)}$	0/3.5 -15/13.5			0/3.5 -15/13.5			0/3.5 -15/13.5			٧
	Vo	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	±13.5 ±10.5	±14 ±11.8	•	±13.5 ±10.5	±14 ±11.8		±13.5 ±10.5	±14 ±11.8		V
Output Voltage Swing	V <sub>OH</sub>	$V^{+} = 5V, V^{-} = 0V$ $R_{L} = 2k\Omega$	3.9	4.1		3.9	4.1		3.9	4.1		V
	V <sub>OL</sub>	$V^+ = 5V$ , $V^- = 0V$ $R_L = 10k\Omega$		100	500		100	500		100	500	μV
Common Mode Rejection Ratio	CMRR	$V^{+} = 5V, V^{-} = 0V,$ $0V < V_{CM} < 3.5V$ $V_{S} = \pm 15V,$ $-15V < V_{CM} < 13.5V$	90 100	110 120		80 90	100 110		80 90	100 110		dB
Power Supply Rejection Ratio	PSRR			1.0	5.6		3.2	10		5.6	17.8	μV/V
Supply Current	I <sub>SY</sub>	V <sub>S</sub> = ±1.5V V <sub>S</sub> = ±15V		13 17	25 30		13 17	25 30		12 16	25 30	μΑ

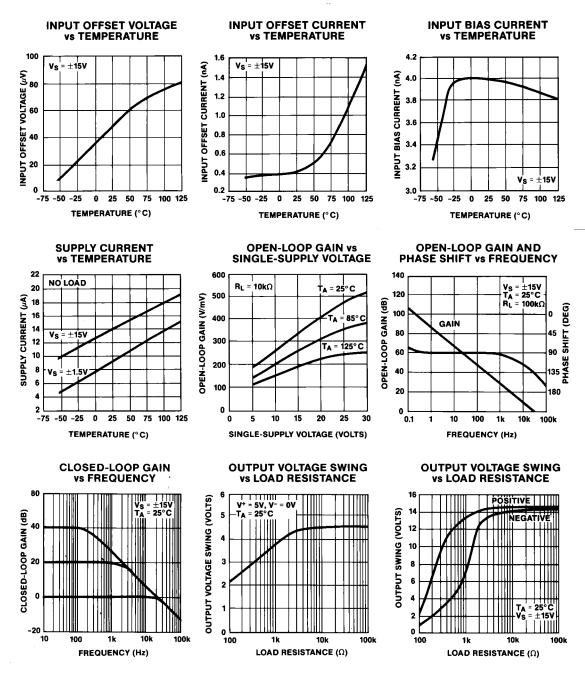
Note 5: Guaranteed by CMRR test.

**WAFER TEST LIMITS** ( $V_S = \pm 1.5V$  to  $\pm 15V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.)

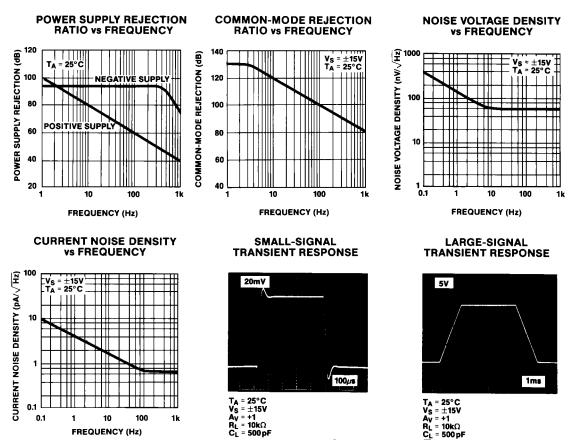
PARAMETER	SYMBOL	CONDITIONS		OP90GBC					
TATIANE LEN	0.111002	CONDITIONS	MIN	TYP	MAX	UNITS			
Input Offset Voltage	Vos				250	μV			
Input Offset Current	los	V <sub>CM</sub> = 0V			5	nA			
Input Bias Current	I <sub>B</sub>	V <sub>CM</sub> = 0V		•••	20	nA			
Large Signal	A	$V_S = \pm 15V$ , $V_O = \pm 10V$ $R_L = 100k\Omega$ $R_L = 10k\Omega$	500 250						
Voltage Gain	Avo	$V^{+} = 5V, V^{-} = 0V,$ $1V < V_{0} < 4V$ $R_{L} = 100k\Omega$	125			→ V/mV			
Input Voltage Range	IVR	V <sup>+</sup> = 5V, V <sup>-</sup> = 0V V <sub>S</sub> = ±15V (Note 6)	0/4 -15/13.5			V			
	v <sub>o</sub>	$V_S = \pm 15V$ $R_L = 10k\Omega$ $R_L = 2k\Omega$	±14 ±11		-	v			
Output Voltage Swing	V <sub>OH</sub>	$V^+ = 5V$ , $V^- = 0V$ $R_L = 2k\Omega$	4.0			v			
	V <sub>OL</sub>	$V^+ = 5V$ , $V^- = 0V$ $R_L = 10k\Omega$			500	μ٧			
Common Mode Rejection Ratio	CMRR	V <sup>+</sup> = 5V, V <sup>-</sup> = 0V, 0V <v<sub>CM&lt;4V V<sub>S</sub> = ±15V, -15V<v<sub>CM&lt;13.5V</v<sub></v<sub>	80 90			dB			
Power Supply Rejection Ratio	PSRR				10	μ\/\			
Supply Current	I <sub>SY</sub>	V <sub>S</sub> = ±15V			20	μΑ			

Note 6: Guaranteed by CMRR test.
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

### **Typical Operating Characteristics**



Typical Operating Characteristics (continued)



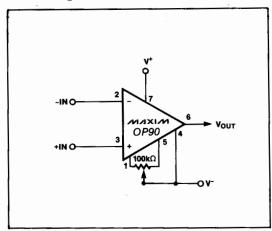


Figure 1. Offset Nulling Circuit

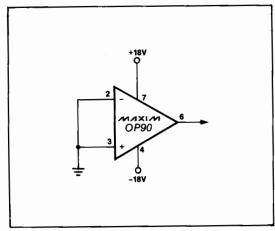
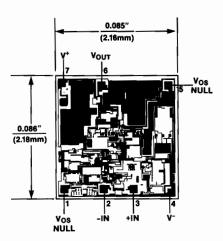


Figure 2. Burn-In Circuit

### \_\_\_Chip Topography



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