A flexible multi-channel high-resolution Time-to-Digital Converter ASIC

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Abstract

A data driven multi-channel Time-to-Digital Converter (TDC) circuit with programmable resolution (~25ps – 800ps binning) and a dynamic range of 102.4µs has been implemented in a 0.25µm CMOS technology. An on-chip PLL is used for clock multiplication up to 320MHz from an external 40MHz reference. A 32 element Delay Locked Loop (DLL) performs time interpolation down to 97.5ps. Finally, finer time interpolation is obtained using four samples of the DLL separated by 24.5ps generated by an adjustable on-chip *RC* delay line.

In the lower resolution modes of operation, 32 TDC channels are available. In the highest resolution mode eight channels are available, since four low-resolution channels are used to perform a single fine time interpolation. The TDC is capable of measuring both leading and trailing edges of the input signal.

Measurements are initially stored as time stamps in individual four-location deep asynchronous channel buffers. After proper encoding, measurements are written into four 256-deep derandomizing FIFO's shared between all channels. This TDC may be operated in a triggered or non-triggered mode. Finally, data is written into a common 256-deep read-out FIFO.

I. Introduction

The measurement of time intervals with high resolution is used extensively in High-Energy Physics experiments. Applications include particle identification in Time-of-Flight (TOF) detectors and tracking in gas based drift detectors. Future experiments have channel counts approaching 1 million, making large-scale integration essential. Data reduction at the earliest stage is also very important in order to reduce bandwidth and buffering necessary in the data acquisition system.

Different detectors require a different time resolution. A modern TOF detector may require a resolution of a few tens of pico-seconds, whereas other detectors only require nano-second resolution.

The Microelectronics group of CERN has previously developed a time interpolation architecture suitable to be used as a high channel-count, "low" resolution converter or, in a different mode of operation, as a "low" channel-count, high-resolution converter [1]. In common with several time digitization architectures described in the literature [2] [3], this architecture is based on a Delay Locked Loop (DLL). However, finer time interpolation can be obtained with a special technique, which internally uses hardware belonging to a few converter channels and an *RC* delay line.

This architecture is suitable for integration together with digital processing logic in a standard VLSI CMOS process. Therefore it is possible to perform data reduction (trigger matching) and buffering inside the TDC.

A highly flexible high-resolution multi-channel TDC implementing this architecture is presented here. It has been built in a modern 0.25µm CMOS technology. Its high flexibility enables it to be used in the future LHC's ALICE TOF detector and CMS muon drift chamber detector. The complete design containing more than 1 million transistors has been produced and shown to operate properly.

II. Architecture Overview

The TDC architecture is divided into two main functional units: A timing unit and a digital data processing and buffering unit (see Figure 1).

The timing unit performs time digitization based on a clock synchronous counter and a DLL interpolator. An adjustable *RC* delay line is used for finer time interpolation. Leading and trailing edge delay measurements can be digitized in up to 32 channels (only 8 channels in the highest resolution mode).

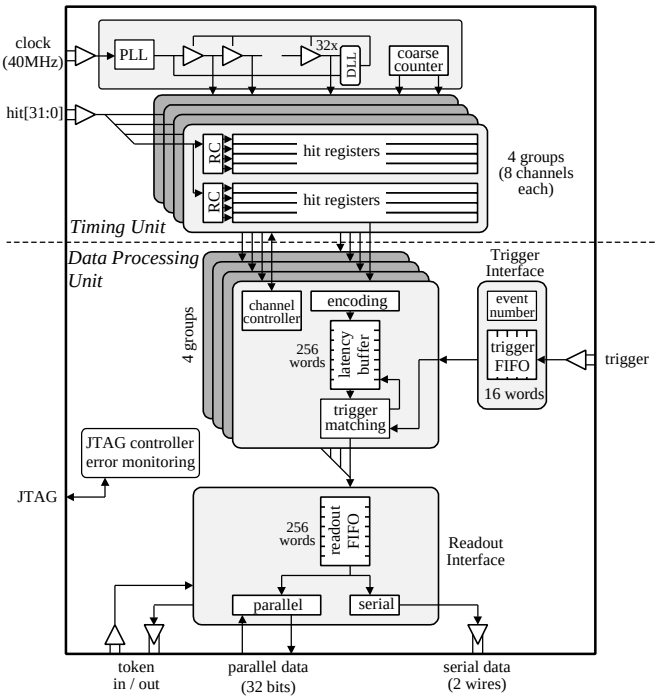

Figure 1: Block diagram of the TDC highlighting its main functionality.

The digital data processing unit encodes and stores the data previously digitized in four 256 words deep buffers. Upon receiving trigger-matching information, data filtering is

performed and only data related to the triggered event is forwarded to a readout FIFO, where it waits to be readout.

A. The Timing Unit

In the timing unit, a clock multiplying Phase Locked Loop (PLL) generates the reference clock to the time digitizer made of a clock synchronous counter, a DLL and, for the highest resolution mode, an adjustable *RC* delay line. Upon arrival of a hit in a channel, the state of the time digitizer is latched into a 4-deep pipelined channel buffer.

1) The PLL

In order to obtain different resolutions from the timing unit, the DLL must be made to lock to different clock frequencies. A PLL is used to multiply a 40MHz external reference to the frequency of the internal time reference (40, 160 or 320MHz). By choosing the frequency multiplication factor (1x, 4x, and 8x) used in the PLL, the timing unit can perform the time digitization with programmable resolution.

The PLL design was adapted from previous successful work by the authors [4]. It includes a 5 delay-cell Voltage Controlled Oscillator (VCO), a sequential Phase-Frequency Detector, a Charge-Pump, a Low Pass Filter and a clock multiplier.

The VCO permanently oscillates at 640MHz (16x factor). It's output is then divided by 2, 8, or 16. In this way it is possible to guarantee a 50% duty cycle, independently of the original duty cycle.

2) The DLL

The DLL is used to perform time interpolation within the reference clock cycle. It consists of a voltage controlled delay line with 32 delay cells, regulated by a control loop that forces it to span exactly one clock cycle. The control loop is made of a Phase Detector (PD), a Charge-Pump (CP) and a Filter Capacitor (see Figure 2). The phase detector permanently measures the phase difference across the delay chain and instructs the charge pump and filter circuit to adjust the control voltage accordingly. The delay of each delay cell is thereby maintained at a value equal to the clock period divided by 32 (781ps, 195ps or 97.7ps, depending on the frequency multiplication factor used). With the high interpolation level used, device mismatch and noise can potentially degrade the linearity and resolution attainable. A voltage controlled differential delay cell with large devices in critical parts of the circuit (for increased device matching) has been used to insure its best timing performance.

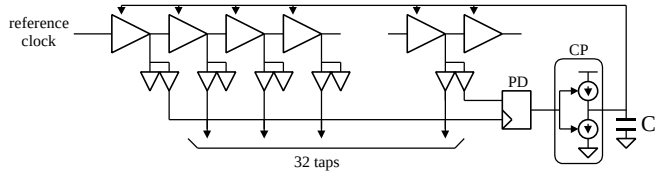

Figure 2: DLL block diagram.

The large dynamic range needed for the DLL is best obtained by dividing its locking range in two separate regions (one for the 97.7ps and 195ps modes and the other for the 781ps mode). In this way it is possible to keep the delay vs. control voltage gain low in any operating conditions. This has the advantage of reducing the sensitivity of the DLL.

The selection of the locking range is performed using differently sized tail transistors in the differential delay cells for the two modes. In this way, different tail currents are supplied, but the operating point of these transistors is always kept suitably away from its threshold voltage, therefore keeping device mismatch low.

When a hit is detected on a channel (leading and/or trailing edge) the state of the DLL is latched into a register in a channel buffer. The measurement stored reflects the time from the beginning of the clock cycle, with a resolution equal to the cell delay.

3) The clock synchronous coarse time counter

The dynamic range of the measurements is expanded beyond the reference clock cycle by using two counters synchronous to opposite phases of this clock. The state of these counters is latched, together with the DLL state, into the same register in a channel buffer. The DLL interpolation can then be used to select the correct count value and avoid ambiguities around the counter transition time.

The word obtained from the concatenation of the DLL and counter measurements reflects the time from the latest reset of the clock synchronous counter, with the resolution of the DLL measurement but a dynamic range given by the maximum count of the counter.

4) The RC delay line

An adjustable *RC* delay line spanning the "length" of a DLL delay cell is optionally used to further increase the time resolution. By storing four times the state of the DLL, at instants that are separated by a quarter of the DLL bin, as shown in Figure 3, it is possible to improve the time interpolation by a factor of four (to 24.4ps). The four sets of latches needed for this additional interpolation are taken from four low-resolution channels giving an effective channel count of eight in the high-resolution mode.

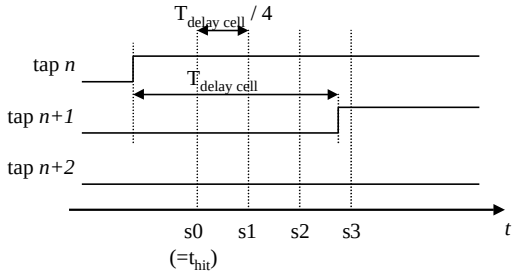

Figure 3: Improved interpolation by observing after which sample the DLL state changes (s3 ⇒ 0.25x$T_{delay\ cell}$, in the example).

The *RC* delay line is made of a non-salicided polysilicon microstrip, which is divided into four equal-delay segments, each generating the latching signal for the respective set of latches. A bank of 7 equally sized capacitors is implemented in each output tap (see Figure 4). By selecting the number of capacitors connected to the tap, it is possible to adjust the delay of each segment of the delay line.

In contrast to the PLL and the DLL, which are continuously locked to the external reference clock and

therefore are self-calibrating, the RC delay line is not part of a closed control loop. However its electrical characteristics are insensitive to the operating conditions (within +-20°C range) of the circuit. Therefore, only a start-up calibration is required to adjust the *RC* delay line against process variations. The adjustment of the *RC* line can be obtained with a simple, statistical characterization procedure (code density tests) in an iterative fashion [5].

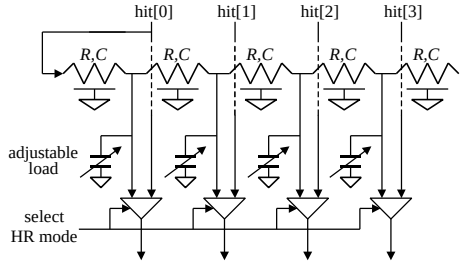

Figure 4: Adjustable *RC* delay line, with variable lumped loads and output multiplexer.

5) The channel buffers

Individual channel buffers are made as asynchronous FIFO's with four levels of latches. The channel buffers enable multiple time measurements to be made with short dead time. The digitization of individual leading and/or trailing edges (or the pairing of leading and a trailing edge) is an effective way to perform time over threshold measurements of signal amplitudes. A programmable dead time can be used to remove unwanted transitions generated from ringing in the analog front-end.

An handshaking mechanism was implemented between the four channel buffers that make up a high-resolution channel. In this way, it is possible to guarantee that the asynchronous buffer read operation does not lead to loss of synchronization between these buffers and the corruption of the *RC* time interpolation.

B. The Data Processing Unit

Time measurements stored in the channel buffers are passed to the data processing unit and, after proper encoding, they are written into four 256-deep latency buffers while waiting to be serviced by a trigger-matching unit. Having four separate buffers serviced by their individual trigger matching unit removes the potential bottleneck from the multiplexing of all the 32 channels into a single data path.

The extraction of hits related to a trigger is based on trigger time tags from an internal 16-deep trigger FIFO. Trigger matching is performed within a programmable time window (see Figure 5). Unique features of the data driven time tag based trigger matching is the fact that the trigger latency is not directly limited by the size of the latency buffers and that single hits can be matched to multiple triggers. Extracted measurements are stored in a common 256-deep readout FIFO until they are read out. After trigger matching data reduction, a single data-path can safely be used. Trigger matching can also be completely disabled whereby the latency buffers and the readout buffer work as simple FIFO's.

Accepted time measurements can be read out via a 40MHz, 32 bit parallel bus for high rate applications or alternatively via a serial link. Up to 16 TDC's can share a readout bus or serial link using a token passing mechanism.

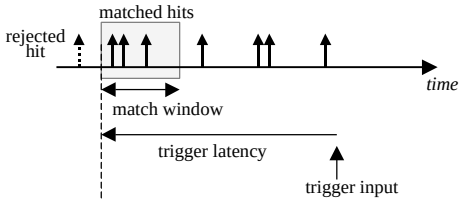

Figure 5: Window based trigger matching.

When trigger matching is used, partial event building is done locally. In this case the TDC can enclose the time measurements belonging to an event with header and trailer data packets that contain information (channel/chip number, event number, number of measurements accepted, etc) which simplify the task of the global event building in the data acquisition system.

Extensive error checking and monitoring is included in the TDC. Parity checks are applied throughout the data path to detect any malfunction caused by single event upsets. A JTAG interface is used to load programming parameters (~600bits) and access built-in test and verification features.

III. PROTOTYPE PERFORMANCE

This TDC architecture was built in a 0.25μm CMOS technology (see Figure 6). The Timing Unit is a full custom macro that was integrated together with the standard cells that implement the digital Data Processing Unit. The architecture was modeled in detail using VerilogHDL. This model was used to verify that the amount of buffering included in all the stages of the TDC is adequate for the expected conditions (hit / trigger rates, etc.) of the detectors for which it was developed [6].

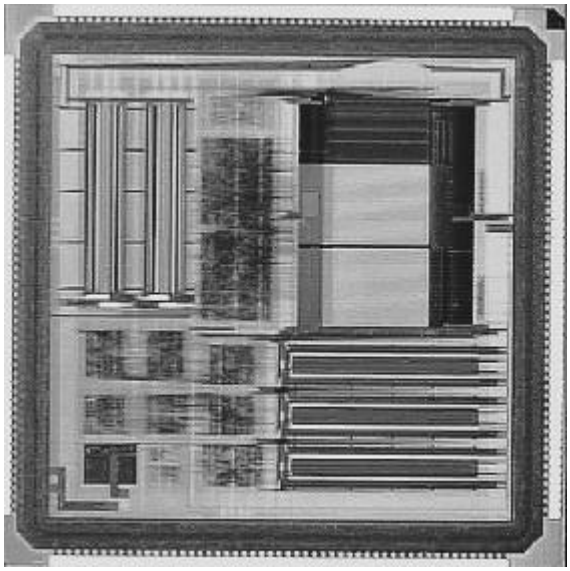

Figure 6: Photography of the prototype.

Functional testing and characterization of the prototype is proceeding at the time of writing, therefore not all the characteristics of the circuit have been verified. In this paper we will report the present status of the tests.

A. *Functional Verification*

Functional verification has performed with the help of automatic test equipment.

The main "operating modes" (combination of features) for which the chip was developed have been verified to operate correctly.

B. *Timing Characteristics*

The prototype's timing performance was measured using automatic test equipment. The main characteristics analyzed were RMS resolution, Integral and Differential Non-Linearity (INL and DNL).

Non-Linearity is measured using code density tests (CDT, or histogram tests) [5]. The RMS resolution is obtained by observing the deviation of a fixed cable delay between two channels in a large number of trials.

A coarse time sweep (time step of 100ps) over a large number of cycles is also made to verify the correctness of the dynamic range extension. A measure of the RMS resolution is also obtained.

A RMS resolution of 236ps has been measured from the linear time sweep. If the difference between the measurements in two channels is performed, its resolution is estimated to be $236ps \times \sqrt{2} = 333ps$.

The histogram in Figure 7 represents the measurement of a fixed cable delay of ~4ns length. The standard deviation of this measurement is 383ps (0.49LSB, LSB = 781ps), which is comparable with the two channel measurement estimate. However, a definitive measurement of the RMS resolution of the circuit can only be obtained by means of a fine time sweep, as in [1].

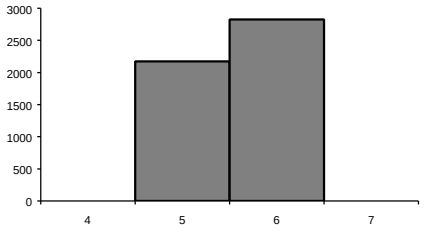

Figure 7: Measurement histogram for a fixed cable delay (low-resolution mode).

The histograms in Figures 8 and 9 reflect the Non-Linearity of the conversion. They span only a clock cycle, 25ns in this mode, since the rest of the dynamic range is a simple repetition of these bins (performed by the coarse time counter). A Differential Non-Linearity smaller than ±0.2LSB and an Integral Non-Linearity smaller than ±0.3LSB where observed.

The higher resolution modes were also characterized. The histogram in Figure 10 shows the Integral Non Linearity measured for the 320MHz mode (LSB = 97.7ps). The histogram shows an INL of ±3LSB (LSB = 97.7ps). This value should be compared with the expected ±0.5LSB.

This discrepancy has been attributed to the poor performance of the package used. Its large inductance leads to substantial noise in the power supply that is coupled to the reference clock distribution path, when the digital logic is operating.

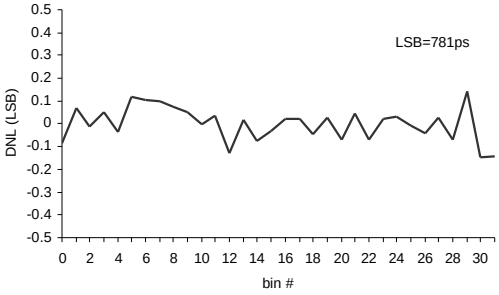

Figure 8: DNL histogram of the low-resolution mode over 25ns.

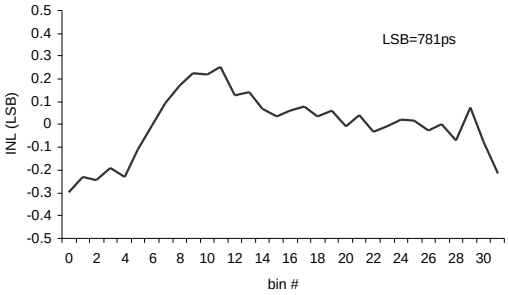

Figure 9: INL histogram of the low-resolution mode over 25ns.

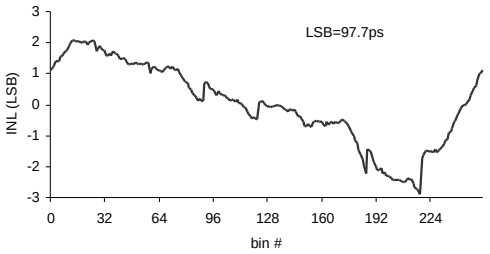

Figure 10: INL histogram of the high-resolution mode over 25ns (with on-chip crosstalk).

In Figure 11, the same histogram is repeated for the case where this source of noise is totally removed, leading to a good linearity (better than ±0.7LSB, LSB = 97.7ps). Figure 12 shows the INL histogram for the case where the *RC* interpolation is performed on chip. An INL less than ±4LSB (LSB = 24.4ps) is obtained.

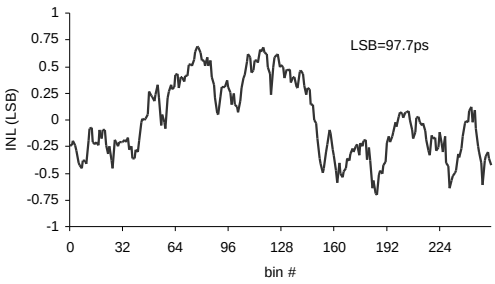

Figure 11: INL histogram of the high-resolution mode over 25ns (without on-chip crosstalk).

The fixed cable delay tests where also performed for the *RC* interpolation mode, resulting in a standard deviation of

166ps (6.79LSB) and 22.4ps (0.92LSB, LSB = 24.4ps), respectively with and without on-chip crosstalk. Following the same reasoning as before, single channel RMS resolution of 117ps is obtained with the "noisy" package and a RMS resolution of 15.8ps is obtained when the source of noise is removed.

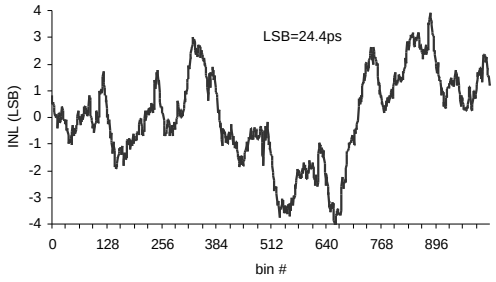

Figure 12: INL histogram of the *RC* interpolation mode over 25ns (without on-chip crosstalk).

An overall improvement of the timing performance of the high resolution modes by a factor of 2 to 3 will be obtained by using a lower inductance package and enforcing short leads to the PCB ground/power planes. Some intervention in the power distribution inside the circuit could possibly also lead to improved results.

IV. SUMMARY

A highly flexible multi-channel TDC has been fabricated in a 0.25μm CMOS technology. The ASIC has proven to be functional and its timing characteristics where analyzed.

In the low-resolution mode (LSB = 781ps), a RMS resolution of 236ps was obtained (INL = ±0.3LSB), as expected.

In the highest resolution mode (LSB = 24.4ps), a RMS resolution better than 120ps was obtained. The reasons for the discrepancy between the theoretical and the measured performance (in this mode of operation) were identified. Tests were carried out where the noise coupling was totally removed, leading to a RMS resolution better than 20ps (INL = ±4LSB). Therefore, we are confident that this ASIC can obtain the expected performance levels, when the proposed changes will be implemented.

V. REFERENCES

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