A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13 μm CMOS Technology

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***Abstract*—A 12-bit Vernier ring time-to-digital converter (TDC) with time resolution of 8 ps for digital-phase-locked-loops (DPLL) is presented. This novel Vernier ring TDC places the Vernier delay cells and arbiters in a ring format and reuses them for the measurement of the input time interval. The proposed TDC thus achieves large detectable range, fine time resolution, small die size and low power consumption simultaneously. A pre-logic unit is developed to measure both positive and negative phase errors for DPLL applications. The TDC achieves a large detectable range of 12 bits with core area of 0.75×0.35 mm^2 in a 0.13 μm CMOS technology. The total power consumption for the entire TDC chip is only 7.5 mW with a 1.5 V power supply, while operating at a clock frequency of 15 MSPS.**

***Index Terms*—Digital phase locked loop (DPLL), frequency synthesis, time and phase measurement, time-to-digital converter (TDC), Vernier.**

I. Introduction

THE time-to-digital converter (TDC) is a critical building block for emerging digital phase-locked loop (DPLL) applications [1], [2]. TDC-based DPLLs feature a high degree of integration, easy calibration and high programmability, and the DPLL can be easily scaled down to the deep-submicron CMOS process with less area and improved performance. Replacing the function of a phase detector and charge pump used in a conventional PLL, the TDC measures the phase error between the reference signal and the feedback signal in the time domain and directly outputs the phase errors in a digital format that can be processed by an on-chip digital loop filter. Due to the use of a programmable digital loop filter, the loop dynamics of a DPLL can be programmed on the fly and thus can achieve fast settling time and low phase noise simultaneously. The on-chip digital loop filter can provide accurate loop dynamics that are less sensitive to process, voltage and temperature (PVT) variations and more immune to the supply and substrate noise. In addition, the area of the DPLL can be reduced by eliminating large capacitors used in analog loop filters. Similar to other sampling circuits, a TDC inevitably generates quantization noise while digitizing the input phase error or time interval. This quantization noise associated with the finite TDC resolution limits the in-band noise of a TDC-based DPLL. In another words, the finer the TDC resolution is, the better the in-band phase noise the DPLL can achieve. On the other hand, it's desired for a TDC to have a large detectable range in order to be able to respond to large phase error during the pull-in of a phase locking process, especially in the low output frequency DPLL. DPLL can be divided into two categories: counter-assisted DPLL and divider-assisted DPLL. Large range TDC is required in divider-assisted DPLL. The TDC in counter-assisted DPLL uses the DCO period as the coarse quantization resolution which is not stable and has a large variance compared to the fine resolution of TDC. In addition, more bit number of TDC is necessary in the counter-assisted DPLL with a larger DCO period, namely a larger coarse resolution. Large dynamic range and fine resolution TDC is desired for accurate time interval measurement in physics and life science experiments, frequency and phase shift measurement and laser range measurement. Moreover, no DCO period is available to be used as the coarse resolution in these applications. However, conventional delay-line based TDCs entail the use of an extra hardware to extend the range of operation [2], which requires more area and larger power consumption. In this paper, a Vernier Ring TDC (VRTDC) architecture is proposed to improve both time resolution and detectable range [3].

An inverter-chain based TDC was employed in the first implemented DPLL for a blue-tooth radio application [4]. Since then, a variety of TDC architectures have been proposed with improved resolution and detectable range [1]–[15]. Although there are many ways to digitize the input time interval, the digital inverter-delay-line is still an appealing structure due to its digital-intensive design approach. Fig. 1(a) shows the conventional inverter-delay-line based TDC. Its time resolution is the propagation delay of each individual inverter, while its detectable range is proportional to the number of delay stages used. Its measured time interval can be expressed as $N * T_D$, where T_D is the time resolution of the TDC. Consequently, achieving fine resolution contradicts the goal of achieving large detectable range, since a TDC with finer resolution would require more delay cells in order to achieve the same detectable range. Moreover, both the time resolution and the detectable range of the TDC are very sensitive to PVT variation, which directly affects the accuracy of the measurement and thus degrades the phase noise of the DPLL.

A Vernier delay line is well known for its fine time resolution [5]. Fig. 1(b) illustrates a simplified Vernier inverter delay line TDC. It employs two inverter/buffer chains with different delays of T_S and T_F, respectively. Time resolution of the Vernier TDC now becomes the delay difference of two delay lines, namely, $T_S - T_F$. Note that the resolution is greatly improved by using

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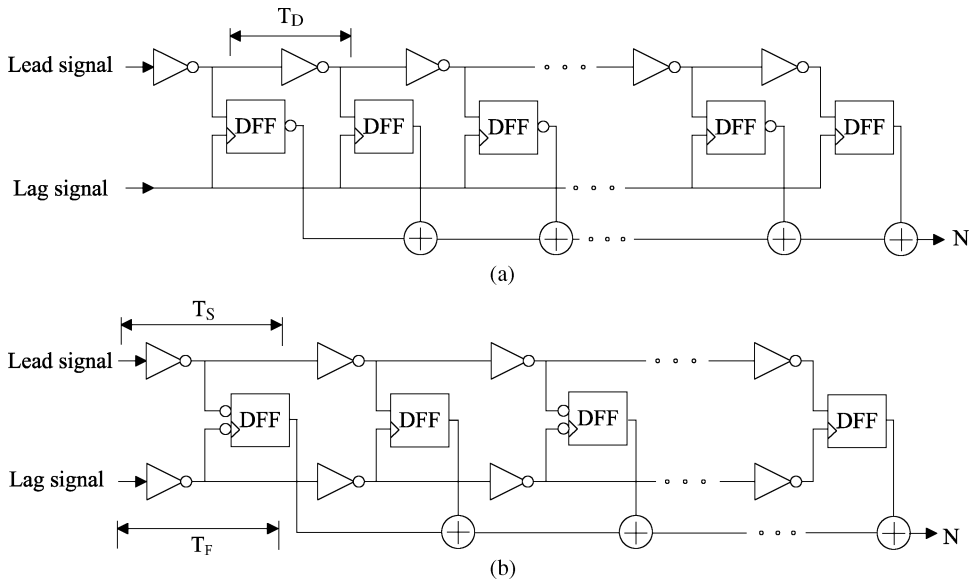

Fig. 1. (a) An inverter delay line based TDC and (b) a Vernier inverter delay line TDC.

two delay lines. In addition, the Vernier delay line architecture can tolerate first order PVT variation if the two delay lines are well matched. Nevertheless the Vernier delay line TDC struggles with reduced efficiency in measuring large time intervals for the same reason mentioned for the inverter delay line based TDC.

Recently several topologies have been explored to shrink the TDC time resolution to several picoseconds. The two-step TDC uses a delay-line TDC as a coarse TDC and a Vernier delay-line TDC as a fine TDC to achieve fine resolution and large detectable range [6], [7]. A time amplifier based TDC greatly improves the resolution and detectable range by amplifying the time residue left in a coarse TDC before quantizing it using a fine TDC [8].

A multipath gated ring oscillator (GRO) structure was proposed to improve the TDC resolution to 6 ps in a 0.13 μm technology [9]. This GRO-based TDC also achieves first order quantization noise shaping by holding the phase of the oscillator output between measurements. This GRO based TDC achieves a detectable range of 11 bits with up to 21 mW power consumption and an area of 0.04 mm^2.

A local passive interpolation TDC employs a differential delay line to obtain a coarse delay. It then interpolates this delay with a resister voltage divider and achieves a sub-gate-delay of 4.7 ps [10]. The parallel scaled delay line structure is an alternative method to improve the resolution. A two-level interpolation TDC with this parallel structure achieved a time resolution of 12.2 ps in a 0.35 um CMOS technology [11]. A pulse shrinking delay element based TDC was reported with a sub-gate-delay resolution [12]. Although there are many novel techniques developed to improve the time resolution of TDC, the Vernier delay line is still an attractive structure for the realization of a high performance TDC. A 1 ps-resolution jitter-measurement macro was implemented recently with two-step hierarchical Vernier delay line structure [13].

In this paper, a *Vernier Ring TDC* (VRTDC) is proposed that leverages the time difference between two rings of delay cells to achieve a time resolution of 8 ps. Unlike the conventional Vernier TDC, this novel TDC places the Vernier delay cells in a ring format such that the delay chains can be reused for measuring large time intervals. Digital logic monitors the number of laps the signals propagate along the rings. Arbiters are used to record the location where the lag signal catches up with the lead signal. The reuse of Vernier delay cells in a ring configuration achieves fine resolution and large detectable range simultaneously with small area and low power consumption. In the proposed Vernier ring architecture, detectable range can be increased to any large number, as long as the counter has enough space to hold the output data. In this design, a large detectable range of 12 bits has been achieved with a small area of 0.26 mm^2.

This paper is organized as follows: the architecture of the proposed Vernier ring TDC is presented in Section II. The implementation of critical building blocks of the VRTDC is discussed in Section III. The measurement results for the VRTDC chip implemented in a 0.13 μm CMOS technology are given in Section IV and conclusions are drawn in Section V.

II. Architecture Design

The proposed Vernier ring time-to-digital converter evolves from the conventional Vernial delay line TDC. Inverters were used as the delay stages to construct the VRTDC in a standard digital process. Connecting the outputs of the last delay cells of a Vernier delay line TDC to the inputs of the first pair of delay cells constructs a novel Vernier ring TDC. An odd number of delay cells (15 stages in this design) is used to form the rings. A NAND gate replaces an inverter as the first delay stage and is used to input the signals under test. The rising edge of a signal to be measured can be fed into the delay ring through one of the inputs of the NAND gate. The pair of NAND cells in the two

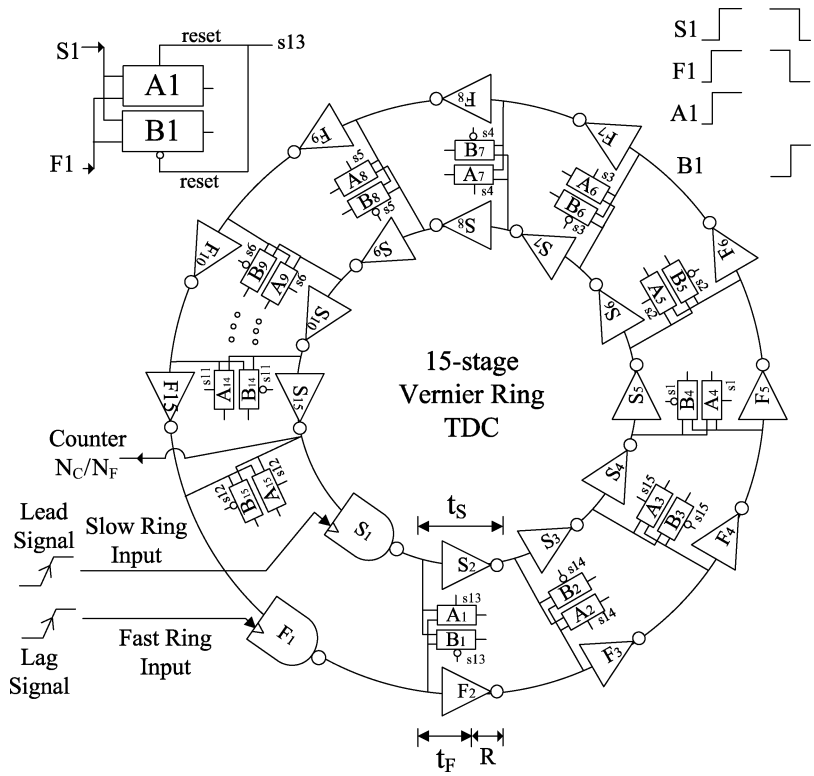

Fig. 2. Block diagram of the VRTDC core with 15 stages.

rings have the same delay difference as that of the inverter pairs in the two rings. Note that there are some subtle things that must be accounted for in order to construct a fully functional TDC using the proposed Vernier rings.

Fig. 2 illustrates the concept of the proposed VRTDC core. Two rings of inverters with slightly different delays are used to measure the input time interval. The VRTDC core consists of two chains of arbiters, which operate in odd laps and even laps, respectively. Recall that the VRTDC contains odd number of delay cells. Thus, a rising edge becomes a falling edge after one lap of propagation along the ring. The two types of arbiters are placed alternatively along the rings to compare the rising or falling edges, respectively. The VRTDC core consists of a fast ring with smaller delay, a slow ring with larger delay and 30 arbiters as shown in Fig. 2. Each ring has 15 stages of inverters with delays adjustable by external bias voltages. The propagation delay of the inverters in fast and slow rings are set to t_F and t_S, respectively. Thus, the time resolution of the proposed TDC is given by

$$R = t_S - t_F \tag{1}$$

Fig. 3 illustrates the operation of the proposed VRTDC in two successive laps, i.e., the first lap and the second lap. Two arbiter chains shown in Fig. 2 work alternatively during the measurement. To help understand the operation of the proposed VRTDC, we separate the whole VRTDC core into two Vernier delay rings shown in Fig. 3. Each ring consists of two rings of inverters and one arbiter chain. Fig. 3(a) depicts the operation of VRTDC in the first lap. Initially, slow ring and fast ring inputs are pulled down to ground (GND) before measurement starts. Two rings are latched to a stable state, where both inverter S15 and F15 output logic "1". In the first lap, the rising edges of the lead and lag signals are fed into two NAND gates to start their propagations along the fast and slow rings, respectively. Lead signal propagates to S2 after an inverter delay of t_S. Lag signal propagates to F2 after an inverter delay of t_F. Arbiter B1 compares two falling edges at S1 and F1, while the arbiter A2 compares the rising edges at S2 and F2. B1 and A2 will be reset when lead signal propagates to S13 and S14, respectively. Fig. 3(b) shows the operation of Vernier ring at the second lap. Both slow and fast ring inputs are set to logic "1" after two signals are fed into the Vernier ring until the lag signal catches up the lead signal. Setting the inputs of the rings to "1" enables two signals to propagate through the delay cells in the rings over and over again, allowing reuse of the hardware. Note that S1 and F1 toggle to logic "1" in the second lap, namely, a falling edge in the first lap becomes a rising edge in next lap. Thus, arbiter needs to compare rising edges at S1 and F1 as well as the falling edges at S2 and F2. Hence, another set of arbiters are needed to work in the second lap and the following even number of laps. This novel Vernier ring TDC is constructed by combining two set of delay rings and arbiters as illustrated in Fig. 2.

Fig. 4 shows the overall architecture of the proposed 12-bit VRTDC system. The IC chip is composed of the VRTDC core, pre-logic, control logic, thermometer decoder, a 6-bit fine counter (N_F) and a 6-bit coarse counter (N_C). The reference signal and oscillator feedback signal in a DPLL are fed into the pre-logic cell, where an arbiter judges whether the reference leads the feedback or *vice versa* and determines the sign bit of the TDC output. As shown in Fig. 4, the lead signal is steered to the slow ring by the output of the arbiter, while the lag signal

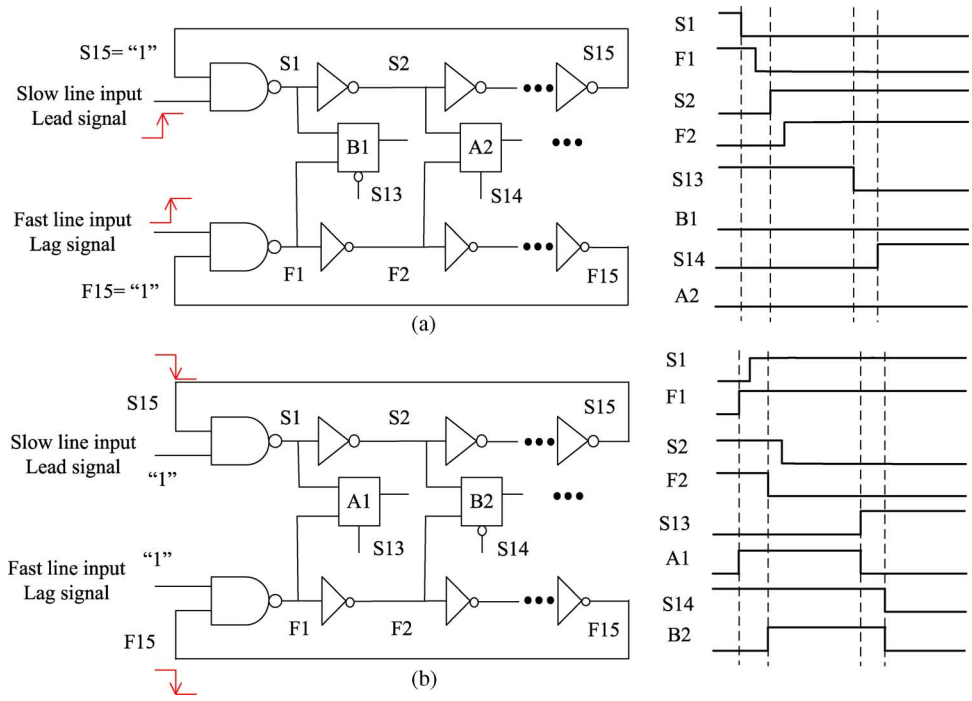

Fig. 3. Illustration of the VRTDC operation at (a) first lap, and (b) second lap.

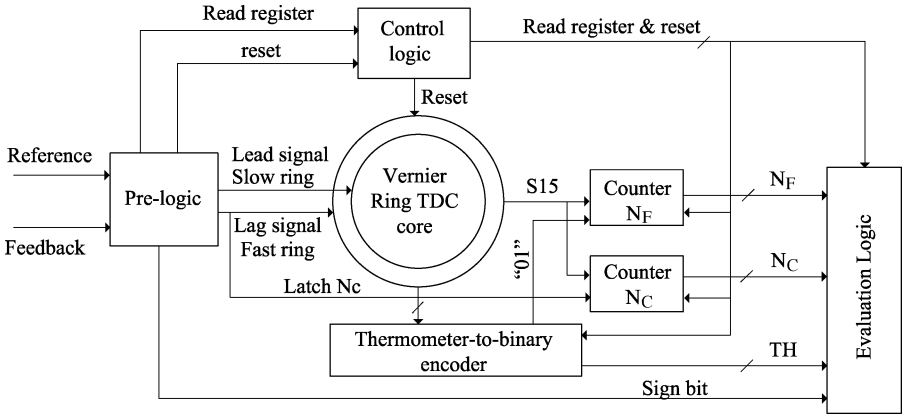

Fig. 4. Block diagram of the VRTDC system.

is fed into the fast ring. The lag signal chases the lead signal along the ring and eventually passes it after a certain amount of propagation.

The outputs of 30 arbiters are combined into a 30-bit thermometer code "TH" and are translated into a 5-bit binary code by a thermometer-to-binary encoder. TH records the location (number of delay cells) where the lag signal passes the lead signal. The fine counter (N_F) records the number of laps (odd and even) that the lead signal has propagated before the lag signal catches up the lead signal. The coarse counter (N_C) records the number of laps that the lead signal has propagated before the lag signal arrives at the input of the TDC. Therefore, the total amount of delay N consists of four elements: the sign bit, the coarse counter value N_C, the fine counter value N_F and the thermometer code TH, as shown in the timing diagram of Fig. 5. Before the lag signal enters the proposed TDC, only one signal propagates along the slow ring. Hence, the TDC operates in its coarse measurement mode, where it interpolates the input time interval with a coarse resolution of $30 \cdot t_S$. This coarse interpolation mode improves the power and area efficiency, and the measurement time as well. Once the lag signal enters the ring, the TDC automatically switches to its fine measurement mode using the Vernier principal, where the TDC interpolates the residue of the time interval under test with a fine resolution of $R = t_S - t_F$ till the lag signal catches up the lead signal. Counter N_F is used to assist the counting of the number of fine interpolations due to the limited bit count of thermometer code. The dynamic resolution adjustment of the proposed TDC differs from the *prior art* TDC architectures, where a fixed resolution were employed. Even with the conventional two-step approach, additional hardware is needed to achieve coarse and fine resolutions. The final output code of the proposed

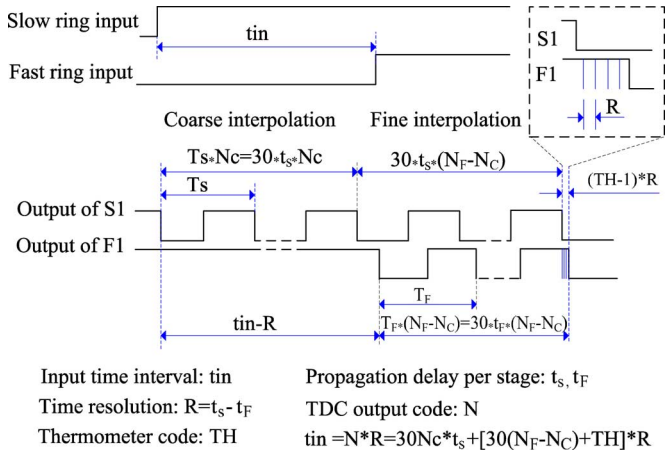

Fig. 5. Timing diagram of VRTDC.

TDC, which is the digital representation of the measured time interval, is thus given by

$$N = \pm 30(N_F - N_C) + TH + 30N_C t_S/R \tag{2}$$

where TDC resolution is given by $R = t_S - t_F$ and the polarity of N, i.e., the sign bit of the TDC output, is determined by the pre-logic as described above. This sign bit can be used to program the polarity of the phase error in a DPLL implementation. The detectable range is determined by the interpolation ratio t_S/R for a given number of bits of the coarse and fine counters because the fine interpolation code should be equal or less than the coarse resolution, namely $30(N_F - N_C) + TH \leq 30t_S/R$. The detectable range is given by the following equations:

$$\begin{aligned} |N| &\geq 30N_C t_S/R \\ &= 30\left[N_F - (N_F - N_C)\right] t_S/R \qquad (3) \\ \max(|N|) &\geq 30\left[2^6 - 1 - (N_F - N_C)\right] t_S/R \\ &\geq 30[63 - t_S/R] t_S/R \qquad (4) \end{aligned}$$

Therefore the detectable range varies with the interpolation ratio. For instance the maximum code is larger than 12 bits for the ratio $t_S/R = 4$ since $\max(|N|) \geq 30 * [63 - 4] * 4 = 7080 > 2^{12}$. It is theoretically possible that the detectable range can achieve 13 bits when the ratio is set to 8.

III. Circuit Implementation

In this section, we discuss the detailed circuit implementation of the proposed VRTDC. We present the circuits of the pre-logic unit, two types of arbiters with edge detectors, the thermometer-to-binary encoder, and two delay stages. We also explain the operation of arbiters and the correction circuit for "01" detection.

A. Pre-Logic Unit

The pre-logic unit, arbiter and delay stage are the critical building blocks of the Vernier ring TDC. The reference signal may lead or lag the oscillator feedback signal in DPLL applications. Since the two rings of inverters in the Vernier ring TDC core have different propagation delays, the lead signal should be steered to the slow ring, while the lag signal goes to the fast ring. Otherwise, the lag signal will never catch up with the lead signal and the VRTDC will not work. Therefore, the pre-logic unit is essential to the VRTDC implementation. Reference signal and the oscillator feedback signal in a DPLL are first fed into the pre-logic cell. The pre-logic unit consists of an arbiter, two symmetrical delay chains, a multiplexer (MUX) and a reset path, as shown in Fig. 6. The delay of buffer lines inserted between the input of the arbiter and MUX has sufficient delay to allow the MUX to swich the propagation path before two signals arrive. The arbiter is reset after both lead and lag signals pass by. The output of the sign bit will be "0" when the arbiter judges that the reference signal leads the feedback signal. Otherwise the sign bit is "1". This sign bit and other bits of VRTDC output will be combined into a signed value representing the positive and negative phase error in the DPLL application. The first arriving signal is used to synchronize the entire VRTDC as a global clock. Two OR gates are employed to generate the "read" and "reset" signal to control the registers where the previous measurement results are stored. The arbiters and other registers associated with the last measurement are reset as well.

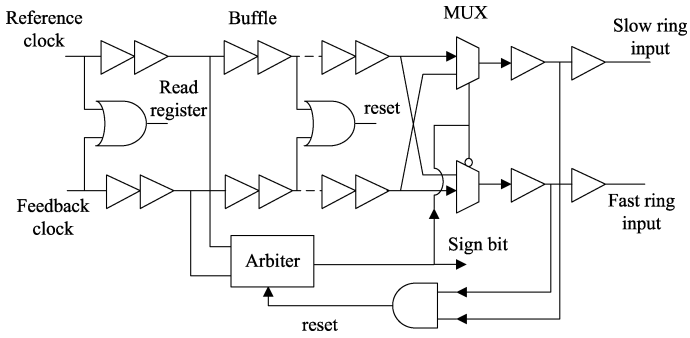

Fig. 6. Simplified circuits of the pre-logic unit.

B. Arbiter, Edge Detector and Control Logic

Similar to the operation of a Vernier delay line TDC, a comparator is needed at every stage to compare the arriving sequence of two signals propagating through the slow ring/line and fast ring/line, respectively. A D-flip-flop is often used to build this type of comparators. However, the clock propagation and data propagation paths in the conventional DFF normally do not match well such that there will be a large time offset in the DFFs characteristics [8]. This time offset is subject to the PVT variations from stage to stage and will cause a shift in the TDC output result. Therefore, an alternate arbiter architecture with symmetric topology was used in this VRTDC, where the clock path and data path match well so that the comparison is less sensitive to the PVT variation.

Fig. 7 shows the schematics of arbiters used in the proposed VRTDC. Arbiter A and B are triggered by rising and falling edges, respectively. Both arbiters consist of a pair of edge detectors, two sets of reset circuits and a core comparator. They are

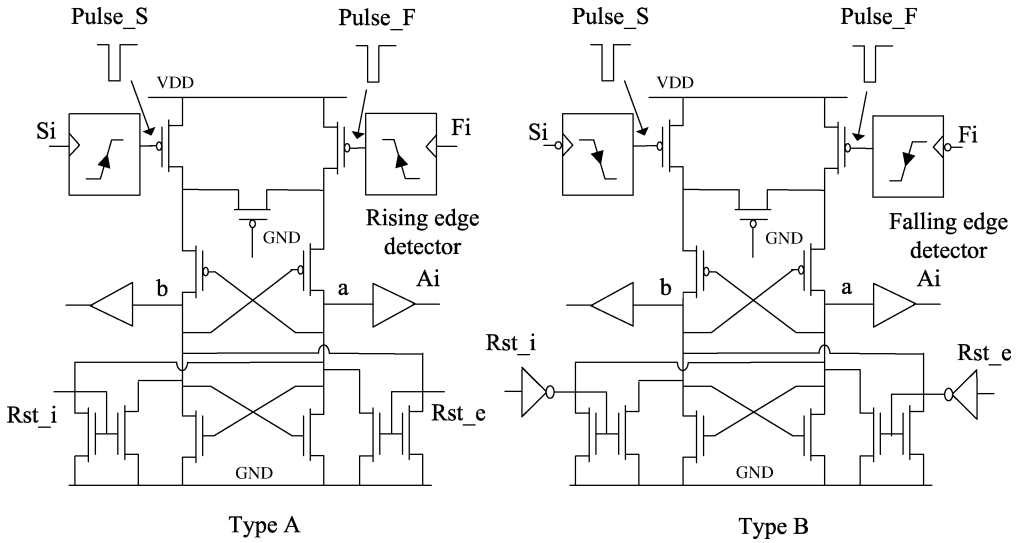

Fig. 7. Simplified circuits of arbiter A and B.

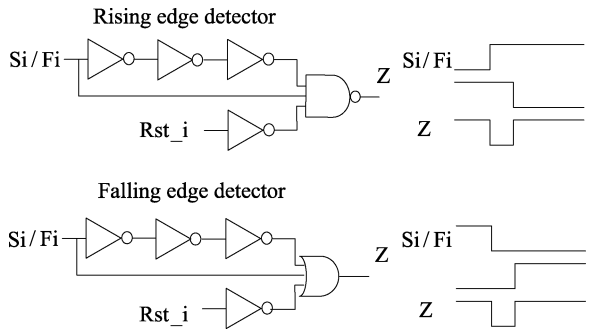

Fig. 8. Simplified circuits of rising/falling edge detector.

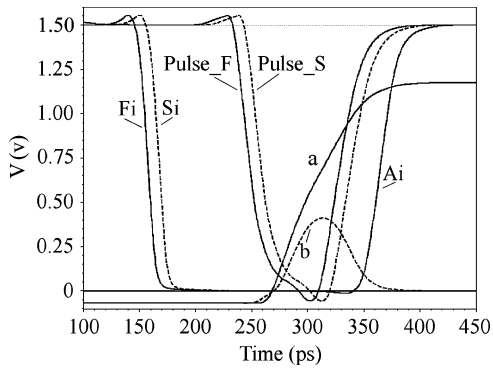

Fig. 9. Transient simulation of arbiter B with the time interval between Si and Fi setting as 2 ps.

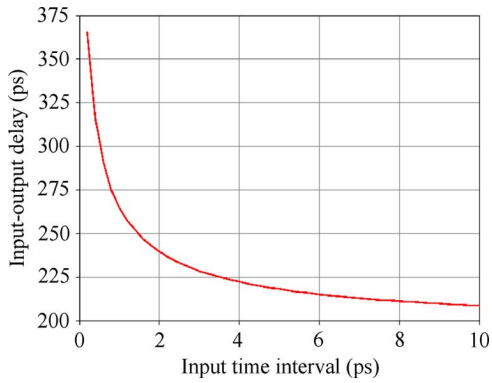

Fig. 10. Dependence of arbiter delay on the time interval between two input signals.

reset by the signal applied to Rst_i every other lap during the propagation of the lead signal in the slow ring. The reset signal coming from the control logic will reset all the arbiters through the port Rst_e before a new measurement starts. As shown in Fig. 8, the edge detector in both arbiters outputs a narrow negative pulse to set the arbiters and then release the control to the reset signals. The arbiter outputs "0" when the signal in the slow ring arrives first at Si, namely, the lag signal has not caught up to the lead signal yet. The arbiter outputs "1" when the signal in the fast ring arrives first at Fi, namely, the lag signal catches up to the lead signal. The first transition from zero to one at the arbiter output will be detected and used to latch the fine counter.

Fig. 9 shows the transient simulation of arbiter B when the time interval between Si and Fi is set to 10 ps. Pulse_F and Pulse_S start the core comparator by pulling both node a and node b to "1" so that the positive feedback loop works then the comparator settles to a stable state. In this simulation, node a settles to a higher voltage than node b which is around three fourths of $V_{\rm DD}$, representing that the signal at Fi arrives first. A set of buffers are necessary to boost the voltage to $V_{\rm DD}$. **Ai** is the output of the arbiter.

The input-output delay of the arbiter is critical to the TDC. This delay has a dependence on the time interval between two input signals, as shown in Fig. 10. The arbiter delay increases dramatically when the time interval shrinks to less 1 ps. The maximum delay of 369 ps shown in Fig. 10 is obtained at a time interval of 0.2 ps. The arbiter delay eventually settles to around 200 ps as the time interval increases.

The arbiter needs to be reset before the next comparison starts. The reset signal comes from the output of the delay stage in the slow ring three stages ahead of the current one. Thus, the arbiter is ready for comparison in a half period of the slow ring and is reset in another half period. There is always

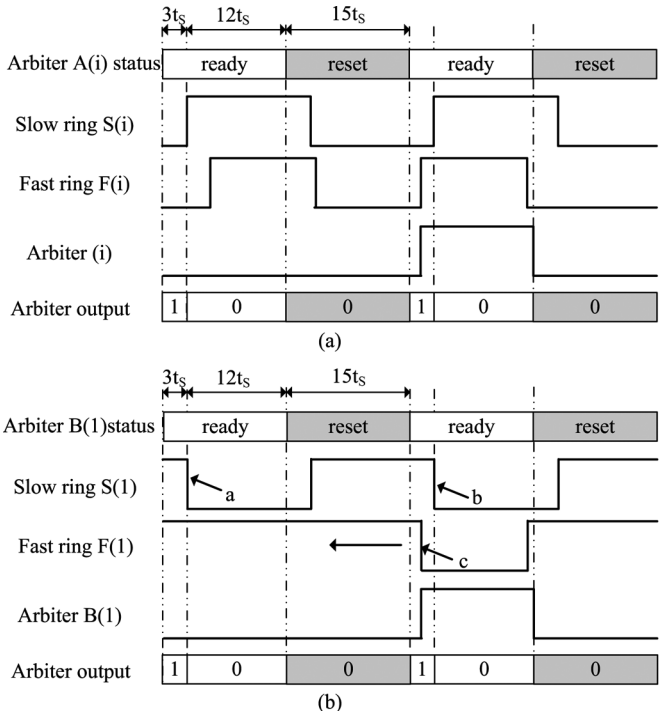

Fig. 11. Illustration of (a) the operating cycle of Arbiter A and (b) unexpected "01" transition at arbiter B(1).

a current leakage path from $V_{\rm DD}$ to ground for conventional arbiters without an edge detector during the reset half period [14], and this current leakage will waste power. In this design, two types of edge detectors shut off this current leakage path in arbiters A and B. Two types of edge detectors will block the input edge when any reset signal is applied to Rst_i. The edge detectors also make the arbiter into a genuine edge-triggered device and distinguish the arbiter A from arbiter B. The narrow negative pulse can reduce the probability of overlap of negative pulse triggered by the lag signal at Fi and reset signal in an arbiter operating cycle so that it also reduces the probability of occurrence of current leakage path. In another word, the narrower the negative pulse can be, the less dynamic power will be consumed. However the narrow negative pulse must be wide enough to set the arbiter. The width of the negative pulse can be easily adjusted through the delay of the inverter chain in the edge detector.

Fig. 11(a) shows the operating cycle of arbiter A. The first half cycle is a ready cycle in which the arbiter is ready to receive input signals and judge the arriving timing sequence of them. The following half cycle is the reset cycle, in which the arbiter is reset to zero and the input signals are screened as well. As indicated in the figure, the arbiter will output zero when the rising edge of $F(i)$ occurs in "0" zone and output one when it occurs in "1" zone. The process of the lag signal chasing the lead signal in the two rings can be viewed as the rising edge/falling edge of $F(i)$ getting closer and closer to the edge of $S(i)$ and eventually passing it. Each half period has a length of $15 * t_S$, in which the "1" zone and "0" zone have lengths of $3 * t_S$ and $12 * t_S$, respectively.

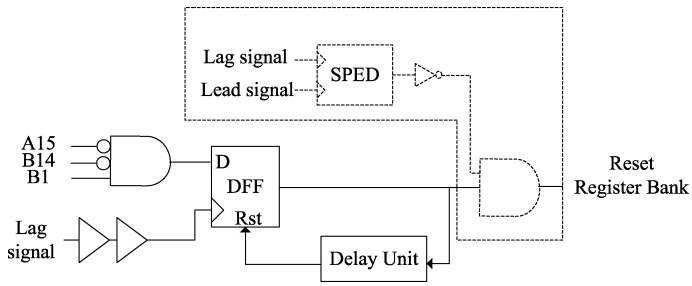

Fig. 12. Block diagram of correction circuit.

As shown in Fig. 11(b), an unexpected "01" transition is likely to occur at B(1) only when the lag signal happens to appear in the "1" zone during its first lap of propagation. Edge **c** is supposed to be compared with edge a by the arbiter B(1). Unfortunately this arbiter has been reset after it was set to zero by edge a. Therefore, the edge is going to be compared with the next falling edge b at F_1. Arbiter B(1) and the following few arbiters will be set to "1". Moreover, arbiter A15 and B14 have been set to "0" before lag signal propagates in the fast ring. A "001" transition will be erroneously detected at the least significant bit of thermometer code. The VRTDC would have mistakenly judged that the lag signal had caught up with the lead signal without proper error detection and correction circuits. This correction circuit will screen the "001" detection signal and keep edge c of the lag signal chasing edge a till the next catch-up happens. Fig. 12 illustrates the block diagram of the correction circuit. The properly delayed lag signal will sample $\overline{B}_{14}\overline{A}_{15}B_1$ as soon as it is fed into the slow fast ring. Correction circuit will reset the register bank in the thermometer-to-binary encoder if the erroneous "001" code is detected. This reset signal will remain effective untill edge c in Fig. 11(b) enters the reset area of the arbiter.

As shown in Fig. 10, the arbiter in pre-logic unit can resolve as tiny as 0.2 ps time interval between two input signals, which should be digitized as "zero" time interval in the TDC output code. This arbiter should have very little chance of erronous switching when the two input signals are so close due to phase noise. In that case the lead signal will be fed into the fast ring and set first a few arbiters to zero before its edge enters the reset zone as the edge c shown in Fig. 11(b). Similarly the correction circuit in Fig. 12 also works since the $\overline{B}_{14}\overline{A}_{15}B_1 = 1$ is sampled by the lag signal. The lead signal will run away from the lag signal untill it overpasses the lag signal the second time. Thus, the measured result is $Ts - tin \approx Ts$, which will cause a spur in the TDC output and will be filtered out by the low pass filter in DPLL applications. As shown in Fig. 12, an amendments can be made to the correction circuit to disable the reset of the register bank with an extra small phase error detectot (SPED) when input time interval is very small. SPED will be introduced in Section III-D.

Control logic in this design coordinates the entire system to work continually. Apart from the correction circuit decribed above, the control logic also sets up the timing for the read, reset and output of the measurement results in the pipeline mode. It consists of correction logic, several delay lines and clock trees.

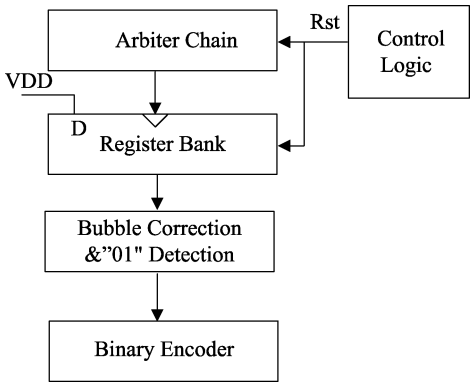

Fig. 13. Block diagram of thermal-to-binary encoder.

C. Thermometer-to-Binary Encoder

As shown in Fig. 13, the thermometer-to-binary encoder consists of a register bank, a bubble correction, a "01" detection circuit and a binary encoder. The outputs of the two arbiter chains are combined to form a 30-bit thermometer code. They are then converted to a 5-bit binary code for further processing by the evaluation unit. The outputs of the arbiters are periodical pulses with the same period as the fast ring after the lag signal catches up with the lead signal. The first "01" transition in the thermometer code will be detected by the "01"detection circuit. However there are many fake "01" transitions shown in Fig. 14 at the falling edge of the arbiter outputs which have to be removed from the output of the VRTDC. A register bank is designed to filter out those falling edges of the arbiter outputs, thus eliminating the fake "01" transitions in the thermometer code. The register bank also stores the outputs of arbiters and partly eliminates the leakage problem in the arbiters, which often screws up the measurement in many low frequency applications. In addition, the proposed arbiters are reset every other lap at a frequency of several mega-hertz during the chasing process and device leakage should be negligible during the reset interval determined by the total delay of the slow ring. The arbiter outputs will not be monitored after the first "01" is detected, which means the device leakage does not limit the minimum operating frequency of the TDC. The two rings can be stopped when two external inputs of Vernier rings are reset to "0" after the catch-up. As mentioned before, the two rings need to be stopped when the measurement is finished. The ring can be stopped without causing extra propagating edges if the external input of NAND gate is reset during the period that another input to this NAND gate is "0". The stop sequence of two rings is not of concern in this design since the arbiter outputs are screened by the register bank after the catch-up. However, the stop of two rings will be properly delayed to allow the correction circuit in Fig. 12 to complete the detection.

Bubble correction is also necessary for the encoding. "*Bubble*" means that it is possible to have an "$\ldots 00010111 \ldots$" pattern in the thermometer code due to the delay mismatch in the each arbiter or a disturbance in the circuit causing the arbiter to take more time to settle. The bubble could occur when the single stage delay of the fast and slow rings is occasionally reversed as well as the time interval input to this delay pairs is less than the reversed delay difference of this pair of stages. Therefore, the "$\ldots 00010111 \ldots$" pattern is most likely to occur

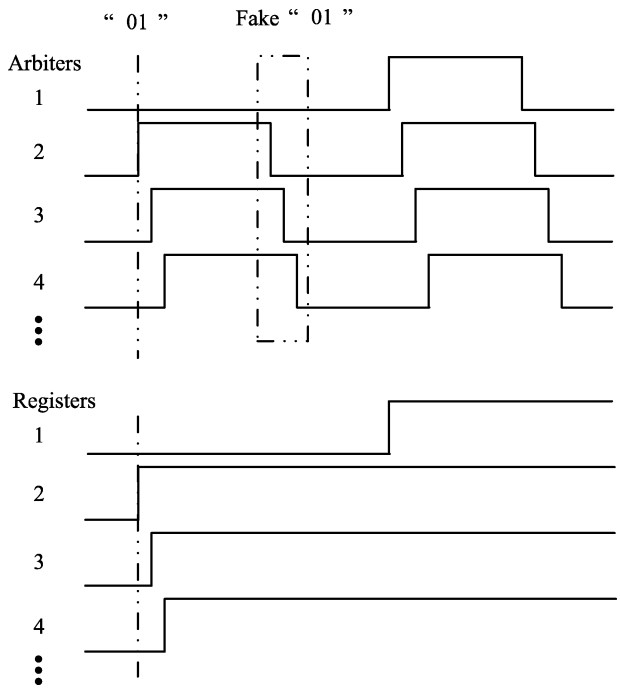

Fig. 14. Timing diagram showing that register bank filters out the fake "01" at the falling edges.

in the vicinity where the real "01" transition happens. Similar to the bubble correction circuit in ADCs, the bubble correction is helpful to get rid of the errors in the thermometer code in VRTDC and relax the demand of matching in the arbiter and interconnecting wire layout. In order to simplify the design, a "001" detection circuit is used in this design. The "001" detector can suppress the bubbles in the thermometer code to some extent.

D. Counters and Design Redundancy

Fig. 15 shows the small phase error detector (SPED) which outputs "1" if the time interval between two input signals is smaller than t_W. SPED consists of two arbiters with crossed inputs of lag signal and $S15$. Fig. 15(b) and (c) illustrate the timing diagram of SPED, in which the $Si1$, $Fi2$ and $Si2$, $Fi1$ are inversely replicated, with a delay of t_W, of S15 and the lag signal, respectively. B1 will output "1" only if the Fi1 appears in the "1" zone of $B1$ and $B2$ will output "1" only if $Fi2$ appears in the "1" zone of $B2$. As a result, Y is set to "1" only when the lag signal shows up in a small vicinity of $S15$ as shown in Fig. 15(d). Area $B1$ and $B2$ are adjacent assuming the four inverters ideally have equal delay. Fig. 15(e) shows a slight overlap of $B1$ and $B2$ achieved by a small decrease of propagation delay Δ in the inverters in $Fi1$ and $Fi2$ input paths. At least one arbiter outputs "1" when the erroneous switching occurs due to the tiny time interval between $S15$ and lag signal. The overlap in the characteristics adds the redundancy to the design.

The counters N_C and N_F are triggered by the node $S15$ in the Vernier ring as shown in Fig. 2 and Fig. 4. The missing-code may occur due to the propagation delay difference between Vernier ring to thermometer-to-binary encoder and Vernier ring to two counters, as well as delay difference between node $S15$ to coarse counter N_C and the lag signal to N_C. These delay differences vary with input time intervals and are not easy to

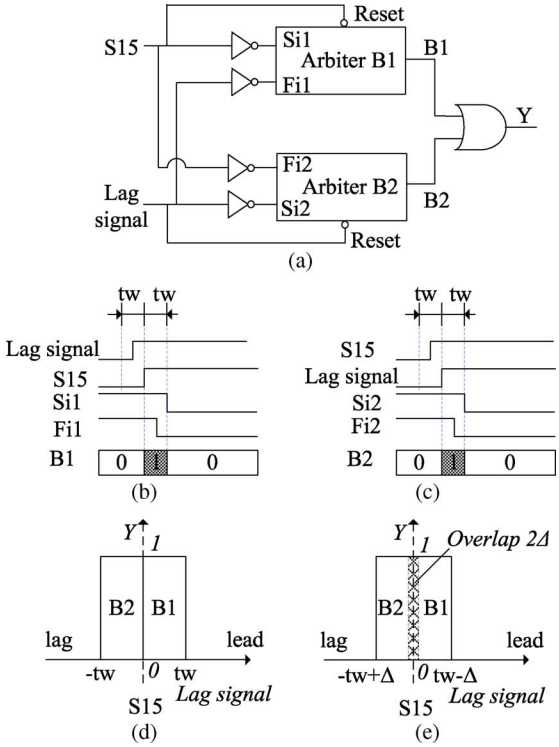

Fig. 15. (a) The circuit of small phase error detector (SPED), (b),(c) timing diagram of B1 and B2, (d),(e) characteristics of SPED without and with overlap. (Horizontal axis indicates the time interval by which the lag signal leads or lags S15.)

match. Two set of counters (N_C and N_F) have been used to tackle the missing code problem.

Fig. 16 shows the circuit diagram of the counters. $N_{C\mathrm{even}}$ and $N_{C\mathrm{odd}}$, triggered by the rising and falling edges of $S15$, are used to count the number of even and odd laps that the lead signal has propagated before the lag signal's entry into the Vernier ring. $N_{C\mathrm{even}}$ will be selected by SPED when the lag signal is not close to the $S15$. Otherwise the $N_{C\mathrm{odd}}$ minus $B1$ will be the result of N_C. $B1$ will be set to "1" only when the lag signal leads $S15$ by a small time interval and $N_{C\mathrm{odd}}$ is larger than N_C by "1". Similarly, N_{Feven} will be selected when catch-up happens in the odd laps; otherwise $N_{C\mathrm{odd}}$ minus "1" will be the output of N_F. Counting all outputs of arbiters will be simple but consumes much more power than the presented double sets of counters with redundancy.

E. Delay Stage

The design of delay stages is crucial to the performance of the VRTDC. Two identical rings are employed in this design to prevent the process variation from affecting the tiny difference in the propagation delay. In order to achieve a programmable delay difference, two different sets of bias voltages and control voltages are applied to the delay stages in the fast and slow rings, respectively. As shown in Fig. 17, the NAND and inverter also have the same topology in each ring to reduce the variation of the time resolution due to the difference in circuit topology. This delay difference between two identical rings can cancel the first order PVT variation. The simulation results shown in Fig. 18 and Fig. 19 verified this cancellation.

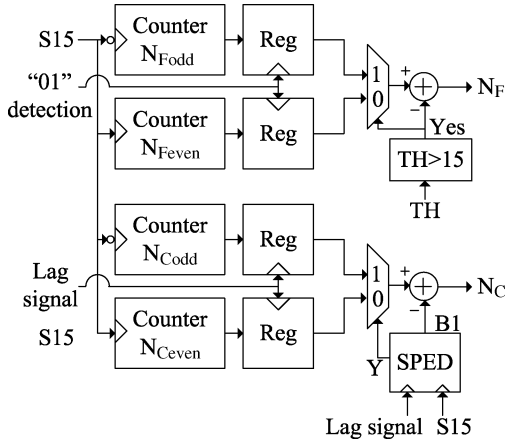

Fig. 16. Counter design for redundancy.

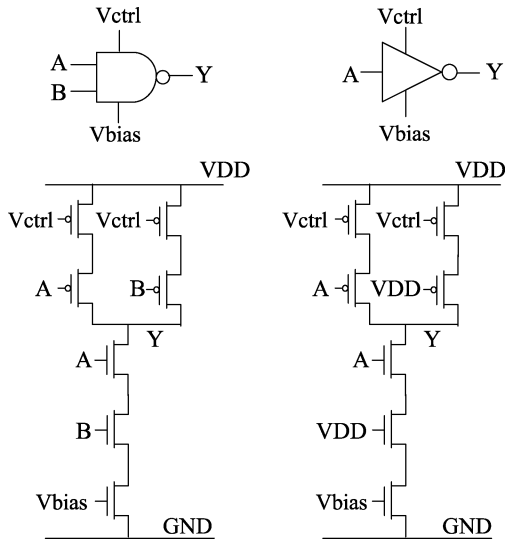

Fig. 17. Simplified circuits of NAND and inverter.

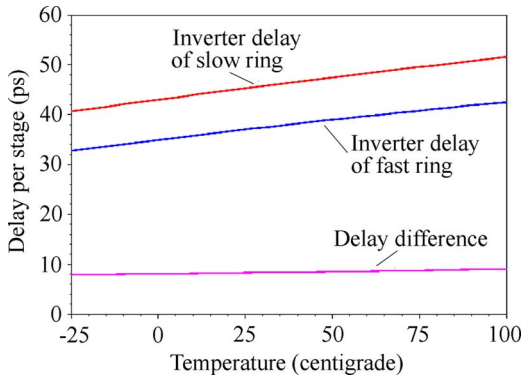

Fig. 18. Dependence of the inverter delay and delay difference on the temperature.

Fig. 18 shows the dependence of the inverter delay and delay difference on the temperature. The propagation delays of the inverters in the slow and fast ring exhibit temperature coefficients of 0.094 ps/°C and 0.08 ps/°C, respectively. The temperature coefficient of the delay difference between two inverters is reduced to 0.014 ps/°C, which is only one sixth of that of the single inverter delay.

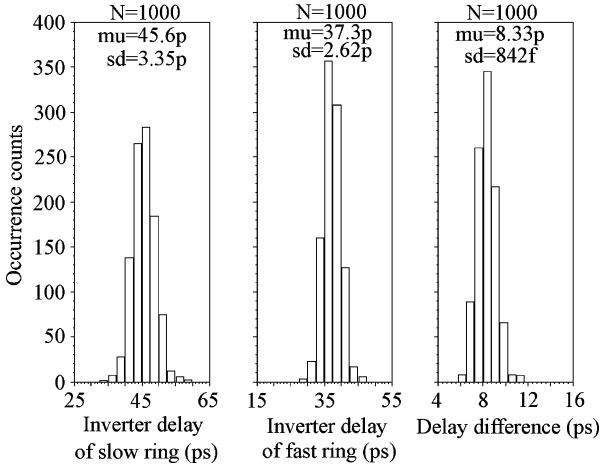

Fig. 19. Dependence of the inverter delay and delay difference on the process variation.

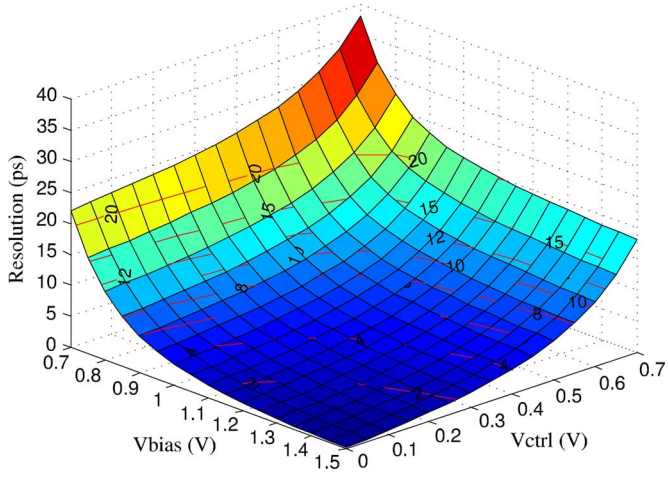

Fig. 20. Dependence of resolution on $V_{\rm bias}$ and $V_{\rm ctrl}$.

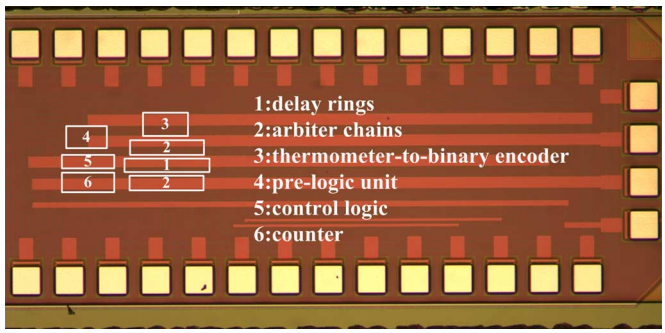

Fig. 21. Die photo of the 12-bit Vernier ring TDC in 0.13 um CMOS technology.

Fig. 19 illustrates the monte carlo analysis of the dependence of the inverter delay and delay difference on the process vialation. These two delays and delay difference are subject to Gaussian variations. The propagation delay of inverters in the slow and fast rings has a standard deviation of 3.35 ps and 2.62 ps, respectively. The standard deviation of the delay difference reduces to 0.84 ps, which is only one third of that of both inverter delays. As known, Vernier TDC gains advantages over single-delay-line based TDC for its improved resolution and immunity to device mismatch. To first order accuracy, the mismatches between the Vernier delay chains are cancelled. In our design, the delay difference is obtained through different bias voltages applied to the two delay stages. These delay stages are designed with the same structure and the parameters. Therefore, the process variations between two delay stages are correlated assuming the two stages are well matched and close enough in the layout. When two variations are totally independent, the delay difference variance can be calculated with the equation $\sqrt{\alpha^2+\beta^2}$, where α and β are the standard variation of two delays. The Monte Carlo analysis justified that the standard variation of delay difference is much smaller than that of each stage delay due to symmetry.

The mismatch of delay pair is accumulated as INL from the beginning of the delay line. INL is dependent on the variance of element delay and the length of delay line [11]. Recycling delay line can be considered to shrink the length to reduce the INL, since the INL is viewed as zero at the end of line. Reduced INL can be easily verified in the case that the frequency of two delay rings is calibrated by DLL. The delay error caused by random noise, for instance jitter and power supply noise, will be accumulated as that in the conventional delay line TDC. However, the Vernier structure can cancel out the first order mismatch and common mode noise.

The identical delay stages using different bias voltages in Vernier rings are intended to compensate the PVT variations. For testing purpose, we brought tuning voltages $V_{\rm ctrl}$ and $V_{\rm bias}$ off-chip for tunability. However, this approach suffers from noise coupling through the tuning voltages. The measured resolution was also largely degraded by the jitter performance of the test equipment. The bias condition that leads to a 2 ps resolution in simulations obtains an 8 ps resolution in measurement. In addition to noises from test equipment, PCB and package the resolution degradation is also affected by the loading effect of parasitic capacitances. In the measurement, the fine resolution smaller than 8 ps can be tuned with a higher $V_{\rm bias}$ close to $V_{\rm DD}$ and a lower $V_{\rm ctrl}$ approaching GND according to Fig. 20. However the performance under those conditions is more sensitive to noise coupling from power supply and ground.

IV. Measurement

The prototype of the VRTDC shown in the die photo (Fig. 21) was fabricated in 0.13 μm CMOS technology. The chip has an area of 1×2 mm^2 including the ESD pads and layer density filling elements. The VRTDC circuit occupies an area of only 0.75×0.35 mm^2. The VRTDC core has an area of 0.05 mm^2. The other parts of the VRTDC occupy a large portion of the circuit area for testing purpose. The area of the VRTDC can be further shrunk when embedded in a DPLL chip. The entire TDC chip consumes 7.5 mW from a 1.5 V power supply while operating at 15 MSPS. The TDC prototypes were packaged using 44 pin LCC packages and the PCB test board was developed using FR402 laminate material, which has a loss tangent of 0.015 at 1 GHz. The test setup consists of two pulse generators, an arbitrary waveform generator, an Agilent logic analyzer and a PCB test board. Two types of test setup are employed to obtain the TDC transfer curve and sinusoidal delay sweep response. Fig. 22(a) shows the test setup for measurement of the TDC transfer curve with a time interval ramp generated by two signals with a slight frequency difference at 15 MHz. A logic

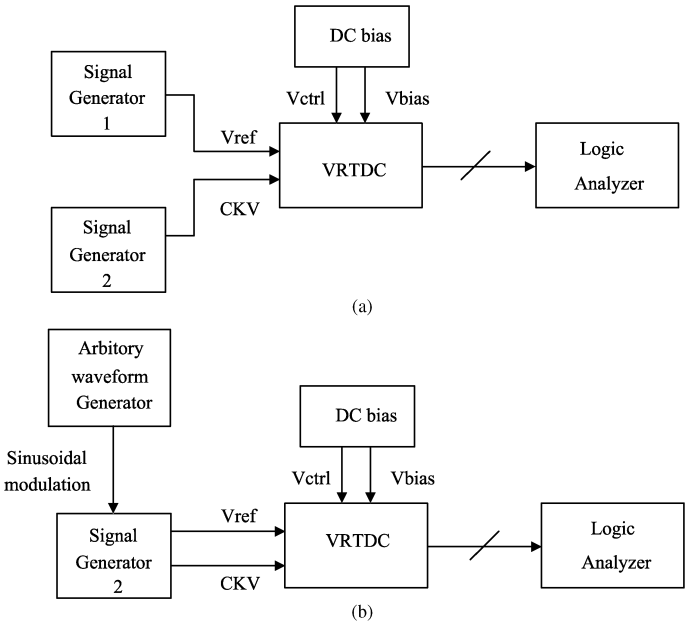

Fig. 22. (a) Time interval ramp test setup. (b) Sinusoidal modulation of time interval.

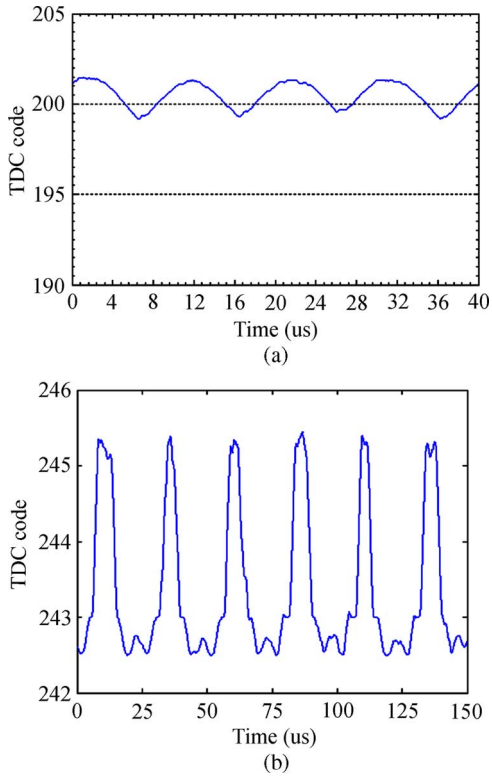

Fig. 23. Measured TDC output with sinusoidal delay sweep 20 ps (p-p): (a) 100 kHz with 2.05 ns fixed delay and (b) 40 kHz with 1.95 ns fixed delay.

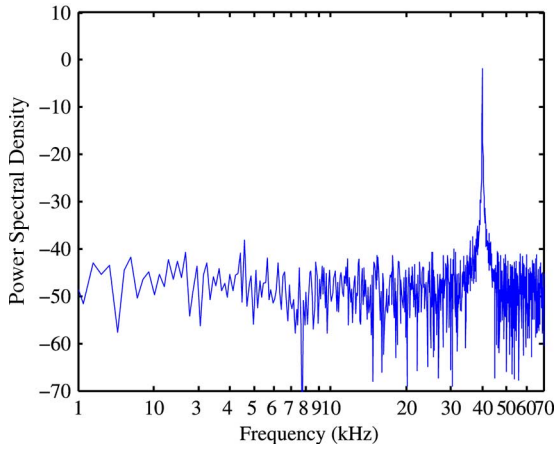

Fig. 24. The power spectrum of TDC output in Fig. 23(b).

analyzer was used to collect TDC outputs continually and display the output code for adjustment of control and bias voltage. In the test, an input time interval ramp is subject to the jitter and frequency stability of the signal source, the power supply noise and noise coupled from the PCB board and other environmental noise sources. Fig. 22(b) illustrates a sinusoidally time-varying phase difference generated by the sinusoidal modulation in one channel. An Agilent 33220A 20 MHz arbitrary waveform generator was used to provide the modulating signal of interest. The other channel was set with a fixed output delay.

Fig. 23(a) shows the TDC output measured with two inputs that have a fixed phase difference of 2.05 ns plus a sinusoidally time-varying phase difference of 20 ps peak-to-peak. The signal generator shown in Fig. 22(b) outputs a clock of 15 MHz at two channels. The output delay in one channel is modulated by a 100 kHz sinusoidal signal. The other channel has a constant delay of 2.05 ns. Sixty sequentially measured output codes were averaged to obtain the TDC output in the time domain. The measured TDC output correctly follows the input sinusoidal phase sweep when the time resolution was set to 10.2 ps. Fig. 23(b) shows the measured results of a fixed phase difference of 1.95 ns plus a 40 kHz 20 ps (p-p) sinusoidal delay sweep. The measured TDC output curve swings from 242.6 to 245.2 at a frequency of 40 kHz and demonstrates that the TDC works well at a time resolution of 7.6 ps, which was achieved by adjusting the delay difference between the two rings. The spurs in Fig. 23 are due to the harmonics of the distorted modulation signal generated by the arbitrary waveform generator or the nonlinearity of the delay modulation Fig. 24 shows the measured power spectrum of the TDC output corresponding to the conditions used in Fig. 23(b). It demonstrates that the TDC output correctly follows the input time interval with its spectral energy concentrated at a single-tone frequency of 40 kHz, which is exactly the input phase-modulation frequency.

Fig. 25 shows the measured TDC output after a median filter with 30× averaging. Two input signals with 2 Hz frequency difference at 15 MHz are applied to generate a ramp of time interval for the measurement of the TDC transfer curve. The input time interval, namely the period difference between two input signals, will increase or decrease 8.9 fs every single pulse. The slope of the transfer curve indicates an average measured time resolution of 8 ps. The measured time resolution of 8 ps was limited by the available test equipment and test setup. Noise coupling from PCB/power supply and the frequency variation of the signal generators can affect the TDC test. The simulated TDC performance achieves better than 2 ps resolution. Fig. 26 gives the measured code distribution with a constant input time interval. It indicates that the standard deviation of the TDC output is less than 1 LSB for 256,000 tests. Finally, Table I summarizes the performance comparison between the proposed work and recently reported TDCs.

TABLE I
PERFORMANCE SUMMARY AND COMPARISONS

Reference	[7]	[8]	[9]	[10]	[11]	[15]	This work
Sample Rate (MS/s)	130	10	50	180	5	26	15
Time resolution (ps)	24	1.25	6	4.7	12.2	20	8
Measuring range (bit)	8	9	11	7	14	5	12
Power Supply (V)	3-3.6	1	1.5	1.2	3.3	1.3	1.5
Power (mW)	<50	3	2.2-21	3.6	40	6.9	7.5
Technology (nm)	350	90	130	90	350	90	130
Area (mm2)	0.6	0.6	0.04	0.02	7.5	0.01	0.26

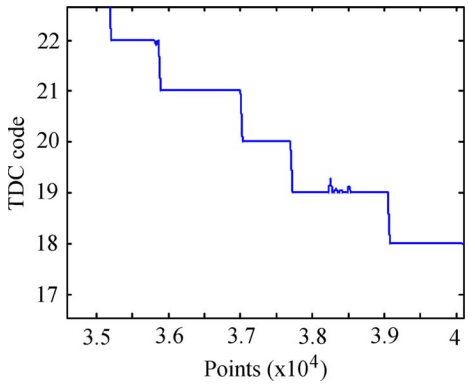

Fig. 25. Measured TDC output after median filter with 30X averaging.

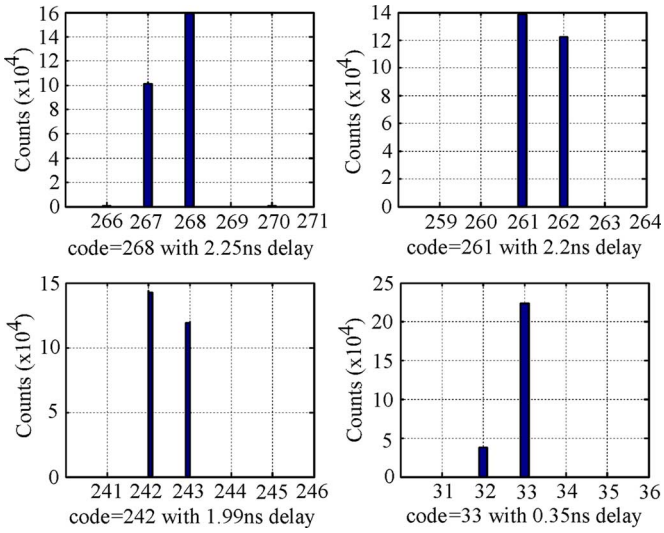

Fig. 26. Measured TDC code distributions at 4 constant delays.

V. CONCLUSION

This paper presented a novel TDC architecture that places the Vernier delay cells in a ring format such that the delay chains can be reused for measuring large time intervals. The reuse of Vernier delay cells in a ring configuration achieves fine resolution and large detectable range simultaneously with small area and low power consumption. The proposed Vernier ring TDC, featuring 12-bit measuring range and 8-ps resolution, was implemented in a 0.13 μm CMOS technology. The core of the TDC circuit occupies an area of only 0.75×0.35 mm^2. The entire TDC chip consumes 7.5 mW from a 1.5 V power supply with operation frequency of 15 MSPS.

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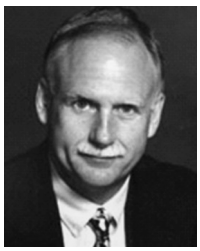

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From 1969 to 1979, he was with the IBM Corporation working on precision analog design, integrated injection logic, microprocessor architecture and low temperature MOS device and circuit behavior. He holds three patents and received two Invention Achievement Awards from the IBM Corporation. In 1979, he joined Auburn University where he is now Professor Emeritus of Electrical and Computer Engineering. He was instrumental in founding the Alabama Microelectronics Science and Technology Center in 1984 and served as its Director until 1998. From October 2001 through 2004, he was Interim Director of Auburn University's Wireless Engineering Program and led implementation of Auburn's accredited Bachelor of Wireless Engineering degrees, a joint effort between the ECE and CSSE departments. He has published over 300 technical papers and articles, served as principal investigator on more than $8 M in research contracts, and authored or co-authored six textbook editions including the Second Edition of *Introduction to Microelectronic Fabrication* (Prentice Hall, 2002), the Fourth Edition of *Microelectronic Circuit Design* (McGraw-Hill, 2010) with T. N. Blalock, and *Computerized Circuit Analysis Using SPICE Programs* (McGraw-Hill, 1997) with B. M. Wilamowski.

Dr. Jaeger received the 1998 IEEE Education Society McGraw-Hill/Jacob Millman Award for "Development of a Modern and Innovative Design-Oriented Electronic Circuits Text," and the 2004 IEEE Undergraduate Teaching Award for "Excellence In Undergraduate Teaching and Development of Outstanding Textbooks for Courses In Microelectronics." He was a member of the IEEE Solid-State Circuits Council from 1984 to 1991, serving the last two years as Council President. From 1995 to 1998 he was Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He was elected to the IEEE Solid-State Circuits Society Adcom in 1999, and served as its Vice President in 2004–2005 and President in 2006–2007. He was Program Chairman for the 1993 International Solid-State Circuits Conference, and Chairman of the 1990 VLSI Circuits Symposium. From 1980 to 1982 he served as founding Editor-in-Chief of *IEEE MICRO*, and subsequently received an Outstanding Contribution Award from the IEEE Computer Society for development of that magazine. He was selected as one of the IEEE Computer Society's "Golden Core" and received the IEEE Third Millennium Medal. Dr. Jaeger was elected Fellow of the IEEE in 1986 and was appointed to the Distinguished University Professorship by Auburn University in 1990. He received the Birdsong Merit Teaching Award from the College of Engineering in 1991. In 1993, he was chosen as the Outstanding EE Faculty Member by the undergraduate students.