Cascading delay line time-to-digital converter with 75 ps resolution and a reduced number of delay cells

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A time-to-digital converter (TDC) is described, integrated on a single field-programmable gate array device with 75 ps single-shot resolution (LSB). Multiple-shot measurement statistically improves resolution to about 5 ps. The circuit is based on a counter and a two-step cascading delay line method that uses only 24 delay cells to provide 128 LSBs in the interpolator that resolves the time interval within the reference clock cycle. The relevant calibration method is also presented to obtain the time parameters of the TDC at the current temperature and voltage. This TDC can measure time intervals from 0 to 1.3 ms and the maximum range is only limited by the range of the counter. The temperature dependence is 0.1 ps/°C. © *2005 American Institute of Physics.*
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I. INTRODUCTION

Time-to-digital converters (TDCs) with high resolution, high speed, and wide range are often required in many applications, such as testers for jitter of optical discs and laser ranging systems. The main methods used to achieve subnanosecond resolution include time-to-amplitude conversion,[1] time-stretching,[2] vernier,[3] and delay line.[4–7] Both the analog time stretching and the time-to-amplitude converter can provide about 10 ps resolution, but at the expense of significant circuit complexity and limited stability. The vernier method is also highly accurate. Unfortunately it needs a long time for a single-shot conversion, which maybe conflicts with the high repetition requirement. The delay line approach, compared to the foregoing three methods, is most advantageous because its conversion time is short and it is easy to integrate in a single chip as a fully digital technique.

More than ten different digital delay line circuits have been designed and tested by the authors thus far. However, most of them were based on single-step delay line[4,5] or parallel delay lines,[6] which mean the large amount of delay cells needed to realize a TDC. It resulted in an increase in the circuit structure and the nonlinearities of the interpolators. A smart design of the two-step interpolation TDC was presented by Mantyniemi *et al.*[7] to reduce the number of delay cells, but such TDCs are designed as ASIC chips using digital complementary metal oxide semiconductor (CMOS) technology with a complex and long design process and can be expensive, especially when produced in small quantities.

In this article another innovative two-step cascading delay line TDC is introduced, which achieves 75 ps single shot resolution and largely reduces the number of delay cells. This converter is implemented on a single field-programming gate array (FPGA) chip from the VertexII family, manufactured by Xilinx® in a 0.15 μm 8-layer metal process, so it is inexpensive and easy to be realized and modified.

II. CIRCUIT ARCHITECTURE

The conceptual timing diagram of the novel TDC developed here is shown in Fig. 1. The measured time interval T_m between the rising edges of the input START and STOP pulses is split into three parts. The first part is the integer number N_0 of the reference clock periods τ_0, measured by a 18-bit binary counter which extends the measurement range to over 1 ms with a resolution of 5 ns (at 200 MHz clock). The remaining two parts are the short intervals at the initial and the final parts within one clock period (T_{11}, T_{21} in Fig. 1), digitized by two identical two-step delay lines. The first-step delay lines measure the numbers N_{11}, N_{21} of the coarse intervals τ_1 with a resolution of ~800 ps, while the second-step delay lines continue to measure the numbers N_{12}, N_{22} of the fine intervals τ_2 at the parts within one coarse interval (T_{12}, T_{22} in Fig. 1) with a resolution better than 100 ps. Neglecting the conversion error

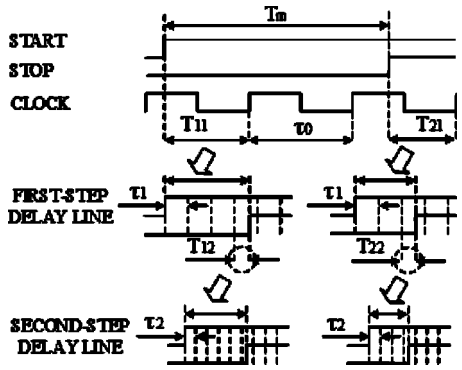

FIG. 1. Conceptual timing diagram.

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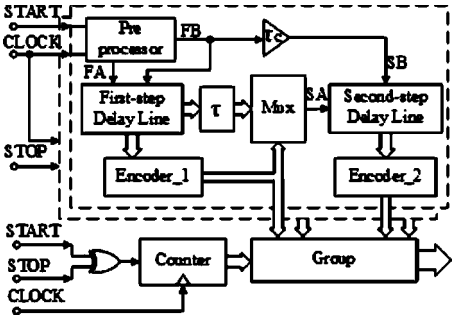

FIG. 2. Simplified block diagram.

$$T_m = N_0\tau_0 + (N_{11}\tau_1 + N_{12}\tau_2) - (N_{21}\tau_1 + N_{22}\tau_2). \quad (1)$$

The simplified circuit block diagram of the TDC is presented in Fig. 2 and the structures of the preprocessor, the first-step delay line and the second-step delay line in Figs. 3(a)–3(c), respectively. The preprocessor generates the FA and FB pulses needed for the first-step delay line. The additional flipflop A2 after the synchronizer is used to reduce the probability of the metastability, and the delay buffer τ a is to compensate the time offset and recover the initial time interval. The first-step delay line consists of eight delay cells, providing eight different offset pulses FDA [7:0] transmitted to the multiplexer. The state of the delay line is stored by the FB pulse and then coded into a 3-bit binary number working as a part of the measurement result and the control input of the multiplexer to select the proper pulse for the second-step delay line from eight FDA pulses. In order to keep synchronous, these eight FDA pulses are delayed until the control signals of the multiplexer arrive. The second-step delay line consists of 16 delay cells each of which contains two delay buffers and a D flip-flop for phase detection.[4,5] The delay

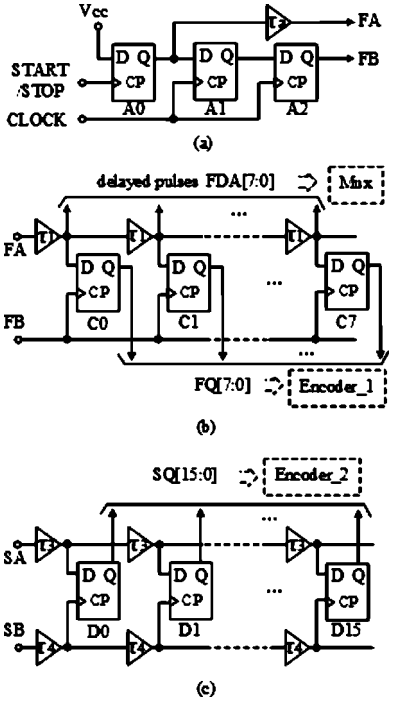

FIG. 3. Circuit structures of (a) preprocessor, (b) first-step delay line, and (c) second-step delay line.

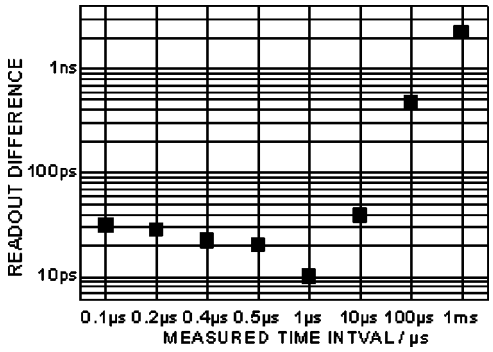

FIG. 4. Difference between measured results and ideal values.

time τ_3 is slightly longer than the delay time τ_4. The propagation delay difference $\tau_3 - \tau_4$ represents the time unit (τ_2) of the second-step delay line and the resolution of the whole TDC. To achieve resolution of 75 ps or better, τ_3 and τ_4 are carefully designed according to the architecture of the used FPGA device and some dummy loads (unused gates) are introduced when constructing the delay buffers. The measurement result is obtained by combining the results from the counter and the two cascading delay lines to be a 32-bit datum.

III. CALIBRATION

For the different propagation traces, the delay times which need to be compensated in the calculation are not identical when different FDA pulses are selected to the second-step delay line by the multiplexer. These times are difficult to be measured exactly by the apparatus, as well as the time units τ_1 and τ_2, because they are on picosecond level and change with temperature and voltage. To obtain these parameters, four standard clocks with different clock periods are used for calibration. Equation (1) is modified as

$$\sum_{i=0}^{6} \Delta a_i A_i + \sum_{j=0}^{6} \Delta b_j B_j + \tau_2(N_{12} - N_{22}) = T_m - N_0\tau_0, \quad (2)$$

where A_i and B_j are defined as follows:

$$A_i = \begin{cases} 1 & \mathrm{i} = N_{11} \\ 0 & \mathrm{i} \neq N_{11} \end{cases} \quad B_j = \begin{cases} 1 & \mathrm{j} = N_{21} \\ 0 & \mathrm{j} \neq N_{21} \end{cases}. \quad (3)$$

Δa and Δb are the compositive time parameters which contain $N_{11}/N_{21}\tau_1$ and compensated delay time. Both the first-

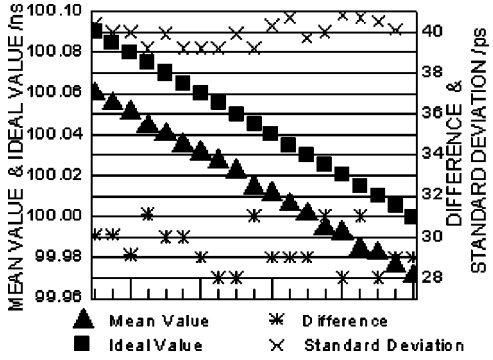

FIG. 5. The mean values and standard deviations of the measured time intervals with an increment of 5 ps.

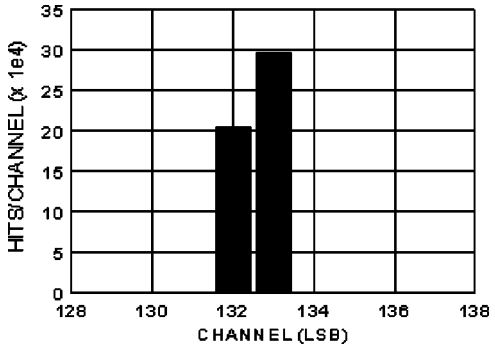

FIG. 6. Measurement result distribution.

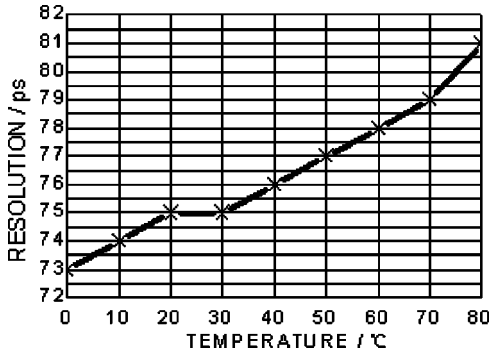

FIG. 7. Resolution of the TDC as a function of the ambient temperature.

step delay lines actually use the first seven delay cells and therefore Δa_7 and Δb_7 are not counted in. After performing 1000 successive calibration measurements of each standard clock, the linear system of equations is constructed as the form

$$MX = R, \tag{4}$$

where

$$X = [\Delta a_0, \quad ,\Delta a_6, \Delta b_0, \quad \Delta b_6, \tau_2]',$$

$$M = (A_0, \quad ,A_6, B_0, \quad B_6, N_{12} - N_{22})_{4000\times 15},$$

and $$R = (T_{CAL} - N_0\tau_0)_{4000}.$$

Because it has more equations than unknowns and is an overdetermined system, the solution that satisfies the equations might not exist, but the least square solution X can be calculated, which minimizes $\|M\|_2$. For the multiple different precision clocks used and a large number of measurements performed, the method is effective and accurate to acquire the time parameters of the TDC.

IV. TEST RESULTS

The circuit was designed in a trial-and-error process for the fine tuning of the delay lines of the TDC, because of the difference between simulation and actual result. Special attention was paid to match the propagation delays and signal slopes to ensure the validity of the delay lines and to reduce the effect of systematic errors.

The TDC was first tested at the ambient room temperature of 20 °C. To verify accuracy of the TDC a synthesized function generator HP3325B (1 μHz–10 MHz square wave, 1 μHz resolution) was used as a source of time intervals. A large sample of measurements (5000) was obtained and then the mean value was calculated for each time interval. Figure 4 shows the divergence between the measured mean values and the ideal values. For time intervals up to 10 μs the difference is lower than 40 ps. The differences appearing at 100 μs and 1 ms are mainly caused by the timebase errors of the HP3325B.

To estimate the multiple-shot resolution, another series of time intervals with an increment of 5 ps was input to the TDC and the statistical method was performed as described above. Figure 5 shows the measured mean values, the ideal values, and the differences between them. The TDC can distinguish the difference of 5 ps quite well, which means it can achieve up to 5 ps multiple-shot resolution under 5000 samples. Figure 5 also shows the standard deviation of sample for each interval. This value is caused by the signal itself and the TDC, which can be expressed as

$$\sigma_m = \sqrt{\sigma_P^2 + \sigma_S^2}, \tag{5}$$

where σ_P is the standard deviation of the constant input time intervals and σ_S is the intern jitter of the TDC. The minimum measured standard deviation is about 40 ps in Fig. 5. So the intern jitter (σ value) of the TDC is lower than 40 ps.

The stability of the measurement, affected by the metastability of the flip–flops involved in the second-step delay lines, was also examined here. In this FPGA chip the setup time of the flip–flops is about 250 ps, and therefore the metastability of the flip–flops must exist when the second-step delay lines have a resolution of 75 ps (LSB). Figure 6 shows the measurement result distribution of a measured constant time interval of about 10 ns. 99.8% of the results are distributed to two adjacent LSBs and all measurement results are distributed to four LSBs.

Finally temperature stability of the TDC was determined in the temperature range from 0 to 80 °C. Figure 7 illustrates the change of resolution of the TDC caused by the ambient temperature. The resolution increases by about 0.1 ps/°C.

ACKNOWLEDGMENT

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