A High Resolution Time-to-Digital Converter Based on Time-to-Voltage Interpolation

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Abstract - A time-to-digital converter (TDC) with a 2.5 μs input range and an accuracy of 100 ps has been designed. According to test results the single-shot resolution of the TDC is 30 ps (rms) at the clock frequency of 100 MHz. The linearity error is less than ±10 ps in the input time range 10 ns to 2.5 μs. The temperature drift of the TDC was measured to be 100 ps in the temperature range -30°C to +60 °C.

1. Introduction

Time-to-digital converters are used in applications such as laser rangefinding and instrumentation for particle physics experiments [1]. The time-to-digital converter (TDC) presented here is designed for a portable laser rangefinder where mm level measurement accuracy over the range of several hundred meters is aimed at. In time measurement 1 mm and 500 m correspond to 6.7 ps and 3 μs, respectively.

The time interval to be measured is digitized in three parts (Fig. 1). The main part T12 is synchronous with respect to the system clock and can, therefore, be digitized by counting clock pulses. With a counter and a 100 MHz clock a single-shot measurement resolution of 10 ns is achieved. Since the measurement is asynchronous with respect to the system clock, averaging can be used to improve resolution. However, the measurement time increases (typical measurement frequency is in the range 10-100 kHz), so to improve the single-shot resolution the non-synchronous parts T1 and T2 are digitized separately with interpolators. Thus, the measurement range is set by the number of bits in the counter and limited only by the stability of the system clock. An interpolating TDC has a good linearity, since during averaging the difference T1-T2 remains constant but T1 and T2 change randomly, which averages also the linearity errors of the interpolators. The resolution of the TDC is determined by the linearity and other properties of the interpolators.

One practical interpolator structure is a delay line [1]-[3]. Another approach is to use time-to-voltage converters, where a capacitor is discharged with constant current during the input time interval. Here, time-to-voltage conversion was chosen, since it has better single-shot resolution than delay lines.

2. Circuit realization

The time intervals T1, T2 and T12 are created as shown in Fig. 1. An erroneous measurement is possible due to excess delay in the flip-flop D2a (D2b) in case a start (stop) pulse occurs near the rising clock edge. To reduce this possibility, the end mark of T1 (T2) is taken not from the first but from the second clock pulse following the start (stop). Thus, if the flip-flop D2a (D2b) settles in less time than one clock period, the measurement is not affected. The linear measurement range required of the interpolators is, however, doubled from Tclk to 2Tclk, where Tclk is the period of the system clock. The start (stop) input in Fig. 1 is an output of a multiplexer which selects either the external start or the external stop. Thus, it is possible to switch the start and stop channels in every other measurement to reduce drift caused by the mismatch of the interpolators.

The principle of the interpolator based on time-to-voltage conversion is shown in Fig. 2. A capacitor (C) is discharged with a constant current (I) during the input time interval (tin). The resulting voltage change $\Delta V = (I/C) \cdot tin$ is then digitized with an N-bit A/D converter so that the LSB width of the TDC is equal to $Tclk/2^N$. A separate A/D converter IC has been used so the capacitor voltage is buffered off-chip with a CMOS buffer amplifier followed by a bipolar level shifter. The A/D converter is a 10-bit CMOS 300 kS/s RSD coded pipeline converter [4].

The gain of the time-to-voltage conversion depends on the absolute values of the capacitance and the current, so the interpolators need to be calibrated. A simple calibration logic which is enabled by an external calibration request is included. First, the calibration logic feeds a time interval equal to Tclk into both interpolators, and the output results of the interpolators are read. The same is repeated for time interval 2Tclk. From these results the gains of both interpolators can be calculated and these values can then be used during measurement. It is also possible to repeat the calibration procedure from time to time to compensate gain errors resulting from temperature changes, for example. During room temperature calibration some unused output codes should be left at both ends of the scale to prevent overflow at other temperatures.

To minimize jitter due to power supply noise and crosstalk between start and stop channels, all timing inputs (start, stop and clock) are differential signals with 400 mV amplitude, and the control/calibration logic has been implemented with ECL/CML-type differential structures. All control inputs and main counter outputs are at CMOS levels so they must be kept quiet during measurement. The first stage of the counter was implemented with a CML flip-flop so that the following CML-CMOS interface operates at half the clock frequency, and the maximum clock frequency of 100 MHz is achieved. The rest of the counter is implemented with CMOS, which reduces power consumption.

In this prototype TDC, the control and calibration logic, main counter, the two time-to-voltage conversion blocks and the following output buffers were integrated on one chip in a 1.2 μm BiCMOS process. The size of the circuit, excluding pads, is 4.4 mm^2. The A/D converter was implemented in a 0.8 μm CMOS process and the size of this circuit, excluding pads, is 1.3 mm^2. In the future, the entire TDC can be implemented on a single chip in a 0.8 μm BiCMOS process.

3. Experimental results

The clock frequency in the test system was 100 MHz. According to previous test results the A/D

converter has an effective resolution of 9.4 bits, so the theoretical LSB of the TDC is 13 ps. In both interpolators the discharging current I was set to 860 μA.
The single-shot resolution of the TDC was measured by calculating the σ–value of the distribution of the measurement results for a constant input time interval. A single output pulse was taken from a pulse generator and split into two pulses with a power splitter. One pulse was fed directly into the start input of the TDC. The other pulse was first delayed in a coaxial cable and then fed into the stop input. Thus, a nearly jitter free input time interval was created. Fifteen different time intervals ranging from 5 ns to 140 ns were created and measured. The measured worst case σ–value was 30 ps (Fig. 3a).
In the linearity measurement of the TDC the input time intervals were taken from a pulse generator. Both the start and the stop pulse were split into two pulses with a power splitter and fed simultaneously to the prototype TDC and a reference TDC. The reference TDC has been implemented with discrete ECL components and is known to have good linearity and a single-shot resolution of 30 ps (σ–value) [5]. The linearity of the prototype TDC was then calculated by comparing the measurement results of the two TDCs. An average of 1000 samples was taken to reduce measurement uncertainty to ± 8 ps (peak-to-peak). The measured linearity error over the input time interval range of 1 ns to 500 ns with an increment of 0.5 ns is shown in Fig. 3b and is below ±10 ps for input time intervals from 10 ns to 500 ns. In the total 2.5 μm measurement range the linearity error of the TDC was measured to be ± 10 ps.
The temperature drift of the TDC has an offset component and a gain component. Offset level variation without any compensation was measured to be 80 ps in the temperature range -30°C to +60 °C and is probably due to the temperature sensitivity of the buffers. Temperature dependent gain error is caused by the reference clock oscillator which is specified to have ± 10 ppm stability over 0°C to +50 °C. The total temperature drift was measured to be 150 ps in the temperature range -30°C to +60 °C. By using the switching for offset compensation, the total temperature drift can be reduced to 100 ps.

4. Conclusion

A time-to-digital converter with 100 MHz clock frequency and 2.5 μs measurement range has been implemented. According to test results the converter has a 30 ps (rms) single-shot resolution and the maximum nonlinearity is ± 10 ps.

References:

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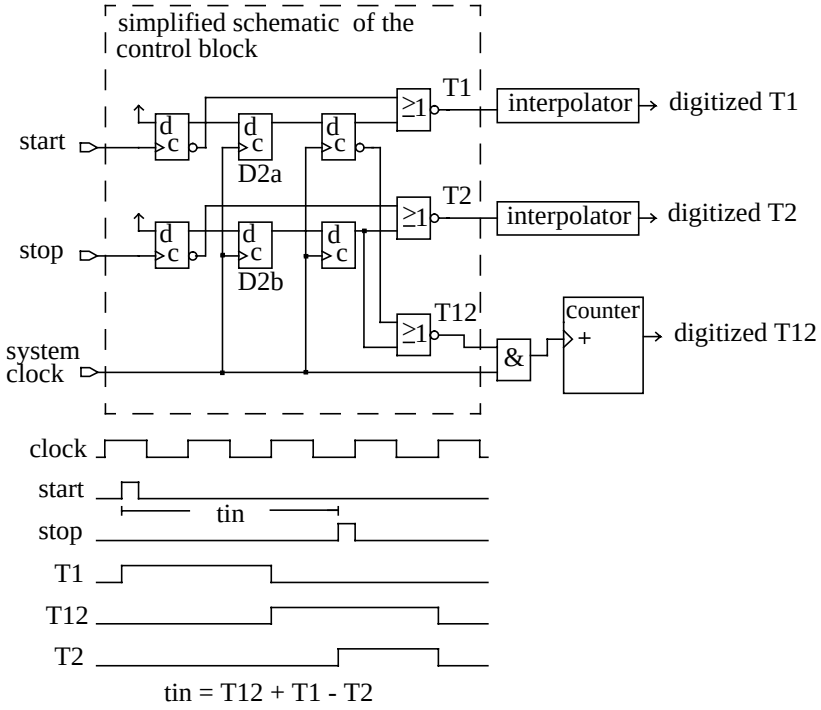

Fig. 1. Block diagram and operating principle of the TDC.

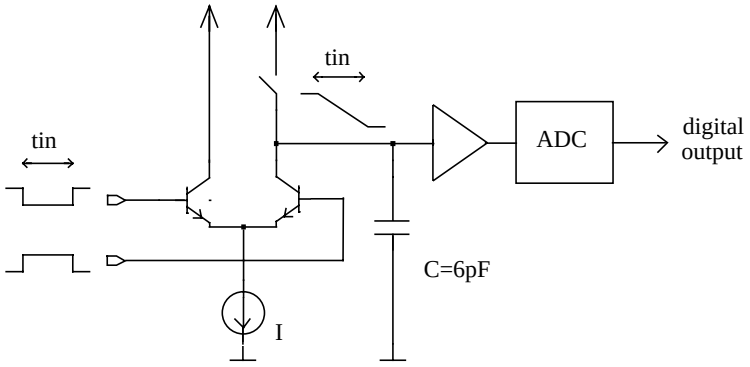

Fig. 2. Principle of the interpolator.

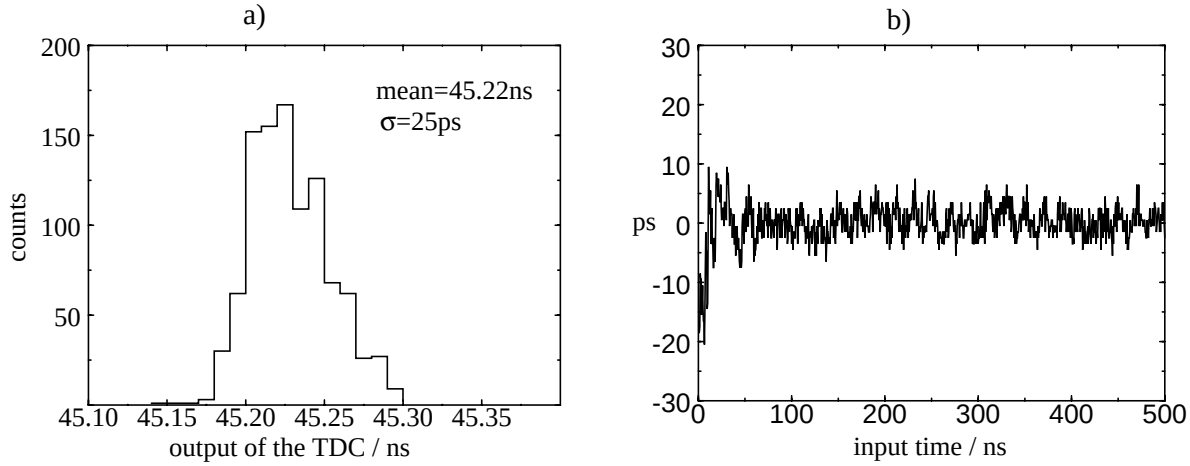

Fig. 3. a) An example of a time resolution measurement (input time 45.22ns). b) Measured linearity of the TDC.