AN INTEGRATED CMOS HIGH PRECISION TIME-TO-DIGITAL CONVERTER BASED ON STABILISED THREE-STAGE DELAY LINE INTERPOLATION

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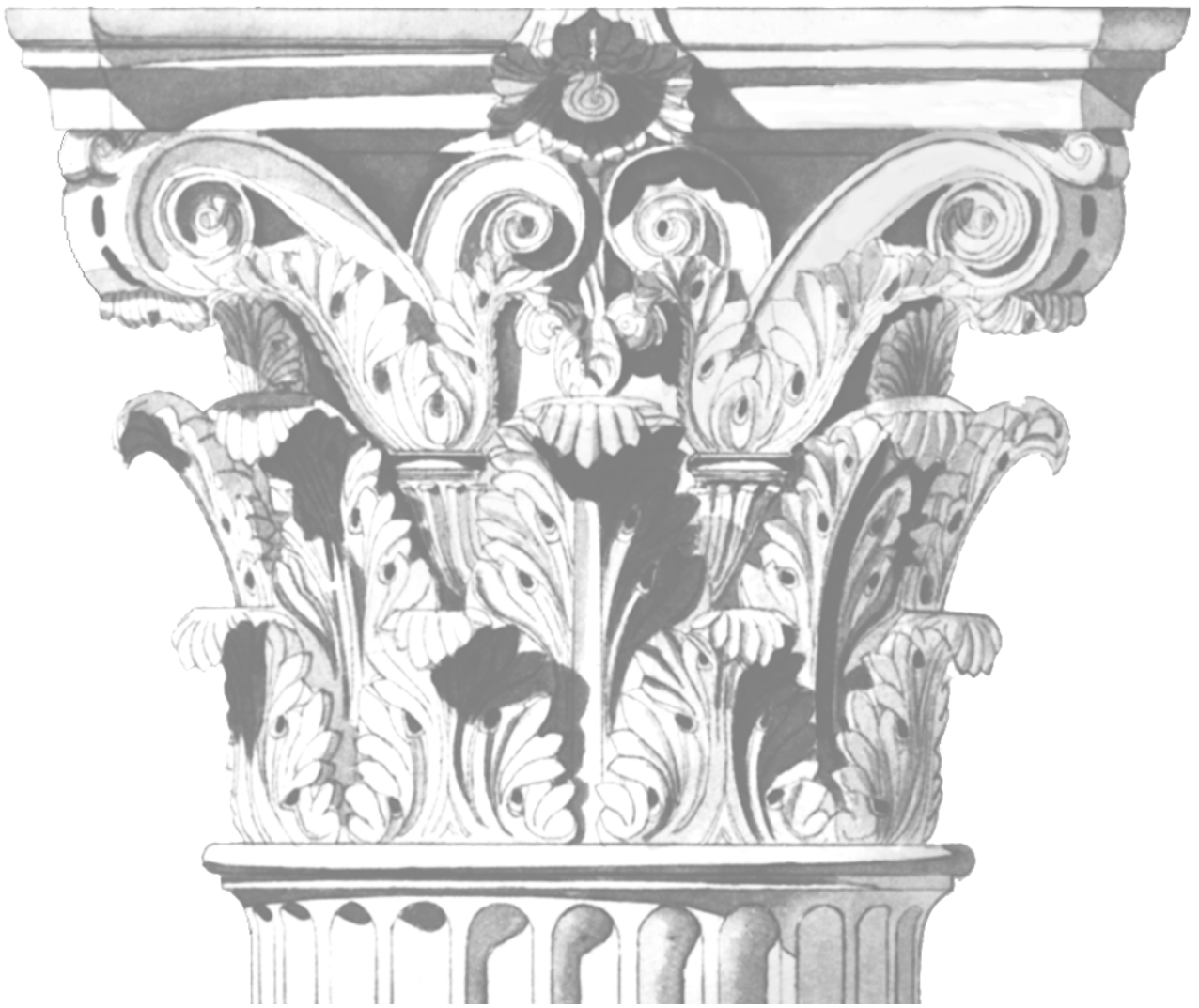

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Abstract

This thesis describes the development of a high precision time-to-digital converter (TDC) in which the conversion is based on a counter and three-stage stabilised delay line interpolation developed in this work.

The biggest design challenges in the design of a TDC are related to the fact that the arrival moment of the hit signals (start and stop) is unknown and asynchronous with respect to the reference clock edges. Yet, the time interval measurement system must provide an immediate and unambiguous measurement result over the full dynamic range. It must be made sure that the readings from the counter and the interpolators are always consistent with very high probability. Therefore, the operation of the counter is controlled with a synchronising logic that is in turn controlled with the interpolation result. Another synchronising logic makes it possible to synchronise the timing signals with multiphase time-interleaved clock signals as if the synchronising was done with a GHz-level clock, and enables multi-stage interpolation. Multi-stage interpolation reduces the number of delay cells and registers needed.

The delay line interpolators are stabilised with nested delay-locked loops, which leads to good stability and makes it possible to improve single-shot precision with a single look-up table containing the integral nonlinearities of the interpolators measured at the room temperature.

A multi-channel prototype TDC was fabricated in a 0.6 μm digital CMOS process. The prototype reaches state-of-the-art rms single-shot precision of better than 20 ps and low power consumption of 50 mW as an integrated TDC.

Keywords: CMOS integrated circuits, delay-locked loop, digital delay lines, interpolation, picosecond resolution, TDC, time interval measurement, time-to-digital converter

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List of terms, symbols and abbreviations

The terms describing the performance of the measurement equipment are defined according to the IEEE Standard Dictionary of Electrical and Electronics Terms (IEEE 1996):

accuracy is the degree of correctness with which a measured value agrees with the true value

differential nonlinearity is the difference between a specified code bin width and the average code bin width

integral nonlinearity is the maximum nonlinearity (deviation) over the specified operating range of a system

jitter is the short term deviations of the significant instants of a signal from their ideal positions in time

precision is the quality of coherence or repeatability of measurement data, customarily expressed in terms of the standard deviation of the extended set of measurement results from a well-defined (adequately specified) measurement process in a state of statistical control

random error has unknown magnitudes and directions and varies with each measurement

resolution is the least value of the measured quantity that can be distinguished

systematic error has the magnitude and direction constant throughout the calibration process

3D	three-dimensional
AD	analogue-to-digital
ADC	analogue-to-digital converter/conversion
ASIC	application specific integrated circuit
ASYNC	asynchronous
ATE	automatic test equipment
BiCMOS	bipolar-CMOS, a semiconductor process containing both bipolar and CMOS transistors
C	capacitance

CLCC	ceramic leaded chip carrier
CLK	clock
CMOS	complementary MOS, a semiconductor process containing both NMOS and PMOS transistors
CP	charge pump
CTR	counter
DA	digital-to-analogue
DDS	direct digital synthesis
DL	d latch
DLL	delay-locked loop
DNL	differential nonlinearity
ECL	emitter coupled logic
EN	enable
ESA	European Space Agency
FF	flip-flop
GaAs	gallium arsenide
INL	integral nonlinearity
LIDAR	light detection and ranging
LIN/BIN	linear to binary
LSB	least significant bit
LUT	look-up table
MEAS	measurement
MOS	metal-oxide semiconductor
NMOS	n-channel MOS
PCB	printed circuit board
PD	phase detector
PET	positron emission tomography
PLL	phase-locked loop
PMOS	p-channel MOS
RC	resistor-capacitor
REF	reference
REG	register
RF	radio frequency
rms	root mean square
SYNC	synchronous/synchronised
TAC	time-to-amplitude converter
TC	time counter
TD	time digitiser
TDC	time-to-digital converter
TIC	time interval counter
TID	time interval digitiser
TIM	time interval meter
TOF	time-of-flight
TV	television
TVC	time-to-voltage converter

Δ	offset
Φ	phase
σ	standard deviation
σ^2	variance

Contents

1 Introduction

1.1 Definition and applications of time interval measurement

An instrument used for measuring a time interval, i.e. the elapsed time between two events, is called, for example, a time counter (TC), time interval counter (TIC), time digitiser (TD), time interval digitiser (TID), time interval meter (TIM) or a time-to-digital converter (TDC), which is used in this work. The two electrical timing signals, i.e. the hit signals, determining the beginning and the end of the time interval are called start and stop, respectively. The result of the time interval measurement is a digital word as in the analogue-to-digital conversion (ADC).

There are many applications that either directly apply high resolution time interval measurement or use circuit structures that can be applied to time interval measurement. In nuclear science the flight time of particles (Porat 1973), the lifetime of positrons (Myllylä 1976, Kostamovaara 1986) and the decay time of scintillators (Moses 1993) can be measured with TDCs. Time-of-flight (TOF) laser rangefinding (Kostamovaara 1986, Ahola 1987, Määttä 1995), time-of-flight mass spectrometry (Brockhaus & Glasmachers 1992) and time-of-flight positron emission tomography (TOF-PET) (Bäck *et al.* 2002) apply time interval measurement. The jitter of a signal can be determined by time interval measurement (Wilstrup 1998, Abaskharoun & Roberts 2001). A time-to-digital converter can be used for capturing the cycle time of the incoming data in clock recovery (Park & Kim 1999). Angle modulated signals can be demodulated by measuring the cycle time of the modulated signals (Chu 1988, Rahkonen & Kostamovaara 1994). Automatic test equipment (ATE) used for characterising high-speed integrated circuits (Otsuji 1993, Brown *et al.* 1995, Chapman *et al.* 1995), digital storage oscilloscopes (Rettig & Dobos 1995, Park & Park 1999) and sampling of digital waveforms (Gray *et al.* 1994) require high resolution time interval measurement or high resolution control of signal timing. The phase difference of radio frequency (RF) signals can be determined by using a TDC (Watson *et al.* 1989). In TV applications the phase of a video signal can be measured with respect to the system clock with structures suitable for TDCs (Rothermel & Dell'ova 1993).

1.2 Historical background and goal of this work

Since the late 1970s there has been research in the area of time interval measurement at the Electronics Laboratory of the University of Oulu. The first applications were positron lifetime measurement (Myllylä 1976, Kostamovaara 1986) and time-of-flight laser rangefinding (Kostamovaara 1986, Ahola 1987, Määttä 1995). The first TDC implementations were printed circuit boards (PCB) with emitter coupled logic (ECL) components, which lead to fairly large size and high power consumption (Kostamovaara & Myllylä 1986, Määttä *et al.* 1988, Rankinen *et al.* 1991). To implement a TDC as an integrated circuit has been studied previously (Rahkonen 1993, Räisänen-Ruotsalainen 1998) and e.g. a state-of-the-art integrated TDC with ~30 ps resolution was implemented in a 0.8 μm BiCMOS process (Räisänen-Ruotsalainen *et al.* 2000).

This research work began as a co-operation between the University of Oulu, VTT Technical Research Centre of Finland, and Noptel Oy. Two prototypes of a scannerless 3D imaging LIDAR (LIght Detection And Ranging) based on time-of-flight laser rangefinding were constructed for the European Space Agency (ESA) (Myllylä *et al.* 1998, Ailisto *et al.* 2001). A 3D imaging LIDAR can measure the shape and the distance of the surface of a remote object. Examples of the applications for a 3D imaging LIDAR are found in industrial and space applications for example in docking, object identification and surface mapping. The previous 3D imaging systems use mechanical scanning for pointing the laser to the target (Ahola 1987). The new prototypes form the image without moving parts. The target surface is illuminated with a short laser pulse and viewed with a photodetector matrix. By measuring the two-way propagation delay of the laser pulse to the target and back to each detector element the distance to each pixel of the target can be calculated and the 3D image formed (Madden 1993). One of the key components of such a system is a multi-channel TDC that can simultaneously measure the time intervals between a common start signal from the laser transmitter and the multiple stop signals from the detector matrix. An integrated 9-channel CMOS TDC with a resolution of 625 ps was implemented for the LIDAR prototypes to meet the specification of 10 cm resolution (Mäntyniemi *et al.* 1997).

The development of a multi-channel TDC continued as a research to develop a TDC architecture suitable for high resolution, i.e. ps-level, measurement of multiple simultaneous time intervals. The emphasis in this work has been on developing a circuit architecture feasible to be implemented as an integrated circuit even by using a low-cost digital CMOS technology. The achievable resolution should not be dependent on the inherent propagation delay of the logic gates of the given technology. The following characteristics were set as design goals in this work. The range and resolution should be comparable with the best integrated 2-channel analogue implementations with μs-level range and ps-level resolution. A conversion principle with a short conversion time and automatic calibration to minimise the dead time between measurements enables a high measurement rate. Automatic calibration also leads to good stability and makes the TDC immune to the change in ambient conditions and process parameters. A TDC with a small area for each measurement channel enables multiple measurement channels to be integrated on the same chip, which also leads to a good matching between the channels.

Low power consumption is important e.g. in battery-operated instruments with a limited power budget.

1.3 Contribution and organisation of the thesis

A high resolution TDC architecture was developed in this work (Mäntyniemi *et al.* 2002a). The number of full clock cycles of the measured time interval is determined with a synchronous counter. The fraction of the clock cycles between the hit signals and the edges of the reference clock are determined using a three-stage stabilised delay line interpolation method developed in this work. The developed efficient architecture enables a high interpolation ratio, i.e. how many fractions the clock cycle can be digitised to, which reduces the number of delay cells and registers needed in the interpolation and makes it possible to integrate multiple measurement channels into a single chip even with a low-cost, moderate line width CMOS process. The new architecture also makes it possible to reach a high resolution with a relatively low reference clock frequency, which leads to low power consumption.

Two synchronisation methods were developed in this work to resolve the uncertainty related to the asynchronous hit signals with respect to the reference clock. The operation of the synchronous counter is controlled with a synchronising logic that is in turn controlled with the interpolation result (Mäntyniemi *et al.* 1997). Another synchronising logic makes it possible to synchronise the hit signals with multiphase time-interleaved clock signals as if the synchronising was done with a GHz-level clock and enables the multi-stage interpolation (Mäntyniemi *et al.* 2000). This makes it possible to reduce the dynamic range, power consumption and nonlinearities of the interpolators.

The three-stage interpolation is based on nested stabilised delay lines (Mäntyniemi *et al.* 1999). The first delay line is locked to the period of the reference clock. The remaining delay lines are locked to the reference provided by the first delay line. This leads to good stability and makes it possible to improve the single-shot precision with a look-up table (LUT) containing the integral nonlinearities (INL) of the interpolators (Mäntyniemi *et al.* 2002b). A one-time calibration has turned out to be sufficient to collect the INL-LUT that can be used regardless of the operating temperature.

A multi-channel prototype TDC was fabricated in a 0.6 µm digital CMOS process (Mäntyniemi *et al.* 2002a, Mäntyniemi *et al.* 2002b). The prototype reaches state-of-the-art single-shot precision and low power consumption as an integrated TDC.

Chapter 2 presents various digital and analogue TDC architectures feasible for high resolution time interval measurement. The developed TDC architecture and synchronisation methods are described in chapter 3. Chapter 4 introduces the prototype TDC. The measurements conducted with the prototype are presented in chapter 5. In chapter 6 the architecture and the measured results of the prototype TDC are compared to other published integrated TDCs. Chapter 7 summarises the results of this work.

2 High resolution TDC architectures

Various digital and analogue high resolution TDC architectures and architectures combining both digital and analogue structures have been designed and implemented as integrated circuits and by using discrete components. The measurement principles can be based on counting the cycles of one or several stable reference oscillators or on converting the time interval to be measured to an analogue voltage that can be digitised. Also the instantaneous voltages of the analogue reference signals can be sampled with the hit signals or the coincidence between the hit signals and a set of reference signals can be resolved and presented as the measurement result. The different measurement principles can also be combined.

The time interval resolving capability of a TDC is usually reported as single-shot precision, i.e. the standard deviation of the distribution of the measurement results around the mean value, when a constant time interval is measured repeatedly. The estimate of the measured time interval T can be expressed as an integral part Q and fractional part F ($0 \le F \le 1$) so that the expected value $T = T_0 \cdot (Q + F)$, where T_0 is the least significant bit (LSB) resolution of the TDC. In an ideal case there are two possible measurement results when $F \neq 0$, Q and Q + 1, the ratio of which depends on F. This is also known as the ±1 count error, and it refers to the quantisation error only. The standard deviation of the measurement results, i.e. the single-shot precision sigma-value, can be approximated with (Hewlett-Packard)

$$\sigma = T_0 \sqrt{F(1-F)} \; . \tag{1}$$

The maximum single-shot precision of $0.5 \cdot T_0$ can be measured when F = 0.5, as seen in Fig. 1, in the case of which the measurement results are evenly distributed to two LSBs. When F = 0 or F = 1 the single-shot precision is ideally zero and the measurement results are collected in one LSB. Because the single-shot precision is a function of the measured time interval, the single-shot precision performance of a TDC should be reported by determining the minimum, maximum and rms single-shot precisions with time intervals spanning from T_0 to T_0+1. Ideally the single-shot precision has an rms value of $T_0/\sqrt{6}$ obtained by integrating the variance σ^2 over one T_0 period.

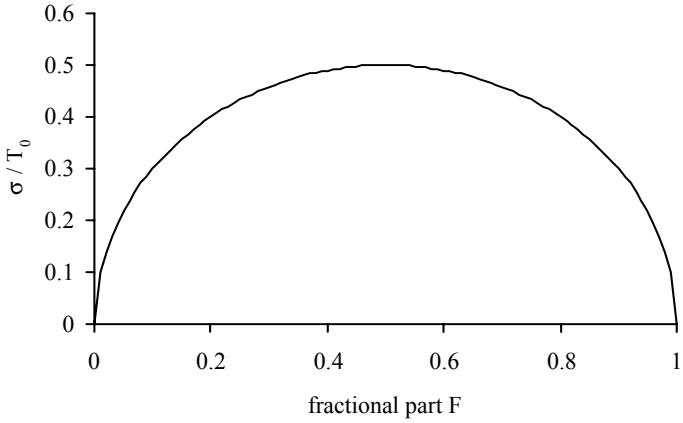

Fig. 1. Single-shot precision σ-value as a function of the fractional part F.

Even though it is possible to construct a TDC with e.g. 1 ps LSB resolution, the rms single-shot precision of the TDC is important when evaluating and comparing the performance. With high resolution TDCs the rms single-shot precision is usually worse than the ideal $T_0/\sqrt{6}$. The single-shot precision is limited by the inherent jitter of the reference clock signal, the jitter of the hit signals and the implementation loss of the TDC caused, for example, by power supply noise, device mismatch, and crosstalk.

Furthermore, in practical realisations the single-shot precision of a high resolution TDC based on a counter and interpolators, explained in section 2.6, is most likely limited by the measurement errors caused by the integral nonlinearity (INL) of the interpolators. The INLs of the interpolators make the single-shot precision vary when the time interval to be measured is swept over the period of the reference clock (T_{CLK}) and this variation repeats itself with the period of T_{CLK}. (Kalisz *et al.* 1987.) In this case the single-shot precision performance of a TDC must be determined by measuring time intervals spanning from $n \cdot T_{CLK}$ to $(n+1) \cdot T_{CLK}$. This is also apparent in the measurement results of the prototype TDC of this work, as reported in section 5.4.

The precision of the time interval measurement can be improved by averaging if the time interval to be measured is repetitive and the hit signals are uncorrelated with the time base of the measurement. However, averaging is a slow process as the improvement of the precision is proportional to $\sqrt{N}$, where N is the number of single-shot measurements averaged to each measurement result (Reed 1964, Hewlett Packard). Therefore, there has been a considerable effort in developing circuit architectures and applying faster technologies to reach a better resolution for time interval digitising. The choice of architecture can also have a significant influence on the conversion time and thus the measurement rate. If time interval averaging can be used in the application, the high resolution and high measurement rate boost the effect of averaging. Also the power consumption, layout area, required technology and processing cost of the TDC depend on the architecture. In the following paragraphs time interval measurement architectures are presented with examples of published realisations.

2.1 Counters

Time intervals of microseconds or longer are best measured with a counter that counts the oscillator clock pulses during the time interval. With a stable reference oscillator a counter can provide a moderate resolution, a large linear dynamic range and good stability (Porat 1973, Williams 1975). Also the conversion time is short, which enables a high measurement rate. A GaAs shift register counter reaches 833 ps resolution with 1.2 W power consumption (Sasaki *et al.* 1989). A resolution of 417 ps was achieved using a counter running at 2.4 GHz realised as a GaAs integrated circuit (Gao & Partridge 1991). A TDC implemented as a GaAs gate array has 1 ns resolution when both edges of the 500 MHz clock are used for clocking, but has a power consumption of about 15 W (Hazen *et al.* 1994). A 2 GHz GaAs counter as an integrated circuit has 500 ps resolution and 2.8 W power consumption (Nati & Kyles 1997). A 32-channel integrated TDC implemented in a 0.5 µm CMOS process reaches 1 ns resolution with a counter running at 1 GHz (Veneziano 1998). A very high frequency counter can be implemented using superconductive electronics. A superconductive TDC with 33 GHz clock frequency and 30 ps resolution has been implemented (Kirichenko *et al.* 2001). Due to the cooling infrastructure the applications for a superconductive TDC are limited (Tahara *et al.* 2001). The resolution can be improved by having time-interleaved counters clocked with multiphase clock signals (Rahkonen *et al.* 1989, Olsson & Nilsson 2004).

2.2 Time-to-amplitude converters (TAC)

A short, ns-level, time interval can be measured with high resolution using a time-to-amplitude converter (TAC), in which a capacitor is (dis)charged with a constant current during the measured time interval, i.e. the time between the start and stop pulses. The change in the voltage of the capacitor is proportional to the time interval. A TAC can reach a high resolution in a limited dynamic range. The dynamic range is limited by nonlinearities and drifting (Kostamovaara & Myllylä 1986, Rahkonen 1993, Kalisz *et al.* 1994). An analogue-to-digital converter (ADC) is needed for converting the voltage of the capacitor to a digital word. The conversion time is set by the speed of the ADC. An integrated CMOS realisation of a time-to-voltage converter (TVC) with a resolution of 0.5 ns and a dynamic range of 5-25 ns needs a separate ADC (Stevens *et al.* 1989). Two integrated TDCs based on a TAC and an embedded Wilkinson ADC reach a resolution and dynamic range of 107 ps and 8-24 ns (Gerds *et al.* 1994) and 200 ps and 200 ns (Simpson *et al.* 1997), respectively.

2.3 Vernier oscillators

An extension to the counter principle is the vernier oscillator principle. It is based on two startable oscillators with different cycle times, the difference of which defines the measurement resolution. The oscillators are gated on by the start and stop signals. As the

period of the stop oscillator is shorter, the phase of the stop oscillator gradually catches up with the phase of the start oscillator by one LSB in every cycle. The number of LSBs it takes the phases of the oscillators to coincide can be determined with counters (Porat 1973). The dual vernier oscillator principle has a stable reference oscillator and two startable oscillators with the same cycle time for start and stop channels, respectively. Also in this case the resolution is set by the cycle time difference between the reference and the startable oscillators (Chu *et al.* 1978). A large dynamic range and high resolution can be achieved simultaneously with vernier principles. However, the conversion time is longer than with the basic counting principle. A TDC realised in a bipolar process reaches sub-ps-level resolution, but has a power consumption of 3.2 W (Otsuji 1993). A commercial TDC instrument has a resolution of 20 ps (Chu *et al.* 1978). To shorten the measurement time of the vernier principle, a double-resolution vernier principle has been presented. The frequency difference of the oscillators is changed during the time interval measurement. At first the measurement is performed faster with a coarse resolution until a fixed phase difference between the oscillators is reached. Then the frequency difference between the oscillators is reduced and the final measurement result is resolved with a finer resolution. (Tabatabaei & Ivanov 2002.)

2.4 Sampling of sinusoidal waveforms

One method feasible for high resolution time interval measurement is based on sampling sinusoidal waveforms. As the sine and cosine outputs of an oscillator are sampled simultaneously with a hit signal, the arrival moment of the hit signal within the oscillator period can be determined. A TDC realised using ECL gates and high speed ADCs achieves an rms single-shot precision of 4 ps in the dynamic range of 100 ns, but has a power consumption of 10 W (Lampton & Raffanti 1994).

2.5 Digital delay lines

The propagation delay of a logic cell can be used in time digitising. In the simplest form the start signal propagates in a delay line made of delay cells and the stop signal stores the state of the delay line to registers (Rahkonen & Kostamovaara 1993). The resolution is defined by the propagation delay of the delay cells. As with a TAC a large dynamic range is not feasible due to the large number of delay cells needed and, consequently, due to the nonlinearities of the delay lines (Rahkonen & Kostamovaara 1993). Good stability can be achieved by locking the propagation delay of the delay line to a cycle of a stable reference oscillator by using a phase-locked loop (PLL) or a delay-locked loop (DLL) configuration with adjustable delay cells. This way the delay line provides multiple evenly spaced time-interleaved reference clock signals the state of which can be sampled by the hit signals. The conversion result is ready as soon as the registers have settled enabling a high measurement rate. This principle is analogous to the flash AD-conversion. A single DLL can be used for generating the reference signals for multiple hit signals, thus making it straightforward to construct a multi-channel TDC. An 8-channel

TDC with 64-tap DLL has a resolution of 650 ps with 24 MHz clock frequency (Chau *et al.* 1996). Another TDC based on a DLL has a resolution of 530 ps with 59 MHz clock frequency (Santos *et al.* 1996).

Several circuit architectures have been developed to circumvent the resolution limit set by the intrinsic gate delay. With vernier delay lines the difference between the propagation delays of two delay cells is used as the time unit defining the resolution. An integrated CMOS TDC based on vernier delay lines reaches a resolution of 30 ps over a dynamic range of less than 4 ns (Dudek *et al.* 2000). A single-stage vernier delay line with a resolution of 67 ps has been presented to avoid the use of long delay lines. The hit signals trigger startable ring oscillators that contain the delay cells in the feedback paths. The structure resembles the principle of vernier oscillators. (Chan & Roberts 2002.)

In the pulse shrinking delay line the time interval to be measured is converted to a pulse. The pulse then propagates in a delay line in which the pulse width shrinks by a certain amount in each delay cell, which sets the resolution. The number of delay cells it takes to lose the pulse is the conversion result (Rahkonen & Kostamovaara 1990). An integrated CMOS TDC based on delay-locked pulse shrinking delay line has a resolution of 50 ps over a dynamic range of 100 ns (Karadamoglou *et al.* 2004). In a cyclic pulse shrinking delay cell the pulse circulates in a single delay cell shrinking by a known value in each round. The number of rounds needed until the pulse vanishes is determined with a counter. An integrated TDC with a resolution of 68 ps over a dynamic range of 16 ns (Chen *et al.* 2000) and another integrated TDC with a resolution of 20 ps, a dynamic range of 18 ns and an rms single-shot precision of 76 ps (Tisa *et al.* 2003) have been reported.

2.6 Nutt method

A combination of a counter and interpolation has proven practical when a large linear dynamic range and high resolution are needed simultaneously (Nutt 1968, Kalisz 2004). The counter keeps track of the full clock cycles elapsed since the arrival of the start pulse. The counter is either halted with the stop pulse or the stop pulse stores the state of the counter. The interpolators resolve the fractional parts of the clock cycle between the arrival time of the hit pulses and the edges of the clock signal. The measurement result is obtained by combining the number of full clock cycles given by the counter and the fractional parts resolved by the interpolators. The interpolation can be done either in analogue or digital domain. As the interpolators are only used for resolving a short time interval up to a clock cycle, the limited dynamic range of for example TACs or delay lines does not restrict their use as interpolators. Furthermore, the nonlinearities of the interpolators have no effect on the linearity of the TDC in time interval averaging but induce a constant bias error to the measurement results (Kalisz *et al.* 1987, Rahkonen 1993). The conversion time may vary considerably depending on the interpolation architecture and the interpolation ratio.

2.6.1 Counter and TAC

When a TAC is used as the interpolator, the phase difference between the hit signal and the edge of the reference clock is converted to a pulse or a pulse pair, the width or phase difference of which, respectively, is determined by using the TAC. The digital word representing the interpolation result is obtained by analogue-to-digital conversion. A high interpolation ratio of 2048 reaching 9.76 ps resolution with 50 MHz clock frequency has been achieved with pulse stretching AD-conversion using discrete components (Turko 1978). A higher interpolation ratio of 5130 and better resolution of 7.8 ps with 25 MHz clock has also been presented with discrete components (Park & Park 1999). The long conversion time related to pulse stretching with a high interpolation ratio has been improved with a dual interpolation principle. The interpolation is performed in two lower ratio interpolation phases with a high combined interpolation ratio (Turko 1979, Kalisz *et al.* 1987). An extension to the dual interpolation principle is the multiple interpolation method, in which the number of interpolation phases is increased even more (Kalisz *et al.* 1986).

A resolution of 3 ps was reached with an interpolation ratio of ~3300 and 100 MHz clock using TACs and an ADC (Kalisz *et al.* 1994). Even 1 ps resolution with 100 MHz clock is possible with analogue interpolation with an interpolation ratio of 10,000 (Kalisz *et al.* 1987, Yamaguchi *et al.* 1991). A TDC built using discrete components uses TACs and fast AD-converters to reach a resolution of 10.5 ps with an interpolation ratio of 950 and clock frequency of 100 MHz (Määttä & Kostamovaara 1998). A TDC with a counter and TVCs integrated into a BiCMOS chip uses external AD-converters and has a resolution of 15 ps (Räisänen-Ruotsalainen *et al.* 1997). An integrated TDC based on a counter, TACs and pulse stretching AD-conversion with an interpolation ratio of 320, implemented in a 0.8 µm BiCMOS process, has a resolution of 32 ps, a dynamic range of 2.5 µs and a power consumption of 350 mW using 100 MHz clock (Räisänen-Ruotsalainen *et al.* 2000).

2.6.2 Counter and sampled sine and cosine

A TDC based on a counter combined with interpolators based on sampling the sine and cosine components of the 400 MHz reference oscillator reaches 9.8 ps resolution with an interpolation ratio of 255, but requires high speed and high resolution AD-converters (Berry 1993).

2.6.3 Counter and delay lines

Digital delay lines can be used as interpolators. Furthermore, the presence of a clock signal makes it natural to lock the propagation delay of the delay line to the clock cycle to achieve high stability for the interpolation. The resolution of the basic delay line interpolator is set by the propagation delay of the delay cells. In the flash principle the

delay line generates a set of evenly spaced clock signals that propagate in the delay line with a known phase difference, i.e. the resolution of the delay line. The hit signals take samples of the clock phases and store the state of the delay line in registers. The state of the registers determines the arrival moment of the hit signals within the clock period. As the propagation delay of the delay line is locked to the reference clock cycle, only a limited number of delay cells, defining the interpolation ratio, can be connected in series to form a delay line. The counter and delay line can be shared with multiple measurement channels, which make it practicable to construct a multi-channel TDC.

A ring oscillator can be built using the delay cells and phase-locked to the reference clock. An integrated CMOS TDC based on a 16-element ring oscillator running at 80 MHz has a resolution of 781 ps and a power consumption of 500 mW (Arai 2001) and an integrated BiCMOS ring oscillator running at 500 MHz has a resolution of 125 ps with a power consumption of 1.32 W (Hervé & Torki 2002). A TDC based on a counter and a free running 16-phase ring oscillator has a resolution of ~156 ps with ~400 MHz clock frequency, but a separate calibration cycle is needed between the time interval measurements (Nissinen *et al.* 2003).

An integrated 16-channel TDC based on a 16-element delay-locked delay line has a resolution of 1.56 ns (Ljuslin *et al.* 1994) and a CMOS multihit TDC with 4-element interpolation has a resolution of 750 ps with 500 mW power consumption (Kleinfelder *et al.* 1991). A multihit and multi-channel TDC with 1 ns resolution and 800 mW power consumption uses a principle in which the clock phases of a 62 MHz reference clock propagating in the 16-tap delay line are used to sample the hit signals (Andreani *et al.* 1998). A resolution of 500 ps was reached with a TDC in which the cycle of the 125 MHz reference clock was interpolated with a 16-tap delay line (Bigongiari *et al.* 1999). A variation of the theme is the 16-channel TDC with 520 ps resolution and 200 mW power consumption, in which the hit signals propagate in 32-tap delay lines and are sampled by the edge of the 60 MHz reference clock (Bailly *et al.* 1999).

Several architectures have been developed to overcome the limited resolution of a simple delay line interpolator. The coarse resolution of the ring oscillator is improved with the use of a structure that generates an output signal the timing of which is based on the weighted sum of the two input signals. A resolution of 15.625 ps is achieved as an integrated circuit in a bipolar process. However, the power consumption of the circuit is 5.7 W. (Knotts *et al.* 1994.) An architecture, in which the propagation delay of the delay-locked loop is locked to a subharmonic of the reference clock, reaches 47 ps resolution, while using 64 delay cells with a propagation delay of 516 ps locked to 5.5 cycles of a clock frequency of 166.66 MHz (Gorbics *et al.* 1997). In that architecture the number of delay cells in the delay-locked delay line and the reference clock frequency can be increased. A TDC with vernier delay lines used as interpolators has a resolution of 100 ps and a dynamic range of 43 s (Szplet *et al.* 2000). Even the high resolution of 50 ps of a superconductive counter has been improved to 5 ps with interpolation (Kaplan *et al.* 2001). An array of delay lines working together in a time-interleaved mode has an effective resolution of 89 ps, even though the propagation delays of the delay cells used are 446 ps and 357 ps (Mota & Christiansen 1998). One way to improve the timing resolution is to split the hit signals, i.e. start and stop, to several phases with a resolution finer than used in the delay line (Mota & Christiansen 1999). As the clock signals propagating in the delay line are sampled with these multiple time-interleaved hit signals,

an improved resolution is achieved. The resolution of 130 ps of a CMOS ring oscillator was improved to 65 ps with a 2-phase input signal (Braun *et al.* 1999, Fischer *et al.* 2002). The resolution of 95.7 ps of a delay-locked loop of a multi-channel TDC implemented in a 0.25 µm CMOS process was improved to 24.4 ps by splitting the hit signals with 4-tap integrated RC delay lines (Mota *et al.* 2000).

The Nutt method with interpolators based on stabilised delay lines has proven a workable concept for multi-channel integrated TDCs used in the high energy physics experiments in which a large number of measurement channels and high measurement rate are needed (Christiansen 1996, Mota *et al.* 2000, Arai 2001). The use of CMOS technology makes it possible to integrate digital functions such as filtering, buffering and post-processing of data into a single chip to reduce the size and cost of the overall system.

2.7 Conclusion

At an early stage of this work analogue interpolation methods had already proven feasible for integrated high resolution TDCs (Räisänen-Ruotsalainen *et al.* 1997, Räisänen-Ruotsalainen 1998). However, BiCMOS technology was required for the implementation leading to high power consumption. Also the conversion time of TDCs based on analogue interpolation can be in the order of µs.

The achievable resolution set by the propagation delay of the adjustable delay cells used in the delay line interpolators has improved concurrently with the evolving CMOS technologies from the ns-level of 1.0 µm CMOS processes (Ljuslin *et al.* 1994, Andreani *et al.* 1998) to around 100 ps of the 0.25 µm CMOS processes (Mota *et al.* 2000). Even faster improvement has been gained with architectural design. The inherent propagation delay of a logic cell has been circumvented in many ways to reach a resolution of dozens of picoseconds even with moderate line width CMOS processes (Gorbics *et al.* 1997, Mota & Christiansen 1998, Braun *et al.* 1999, Mota & Christiansen 1999, Dudek *et al.* 2000, Szplet *et al.* 2000, Chan & Roberts 2002, Tisa *et al.* 2003, Karadamoglou *et al.* 2004).

The objectives of this work are in many ways similar to the challenges of the TDC design related to the high energy physics experiments. Therefore, the Nutt method with flash delay line interpolation was selected as the starting point for the development of the TDC architecture.

There are many ways to improve the resolution of a TDC based on flash delay lines. With architectural design the clock frequency, the number of delay cells and effectively the number of reference clock phases within the clock period can be increased (Gorbics 1997). An array of delay lines can be used for increasing the number of reference signals within the clock period (Mota & Christiansen 1998). The reference clock phases can be sampled with multiple time-interleaved hit signals, which significantly reduces the number of delay cells required to generate the reference clock phases (Mota & Christiansen 1999).

In general, in a single-stage flash delay line interpolation the interpolation result is obtained by storing the coincidence of the hit signal(s) and the time-interleaved reference

signals provided with the delay line(s). As the arrival moment of the hit signal is uncorrelated and unknown with respect to the reference signals, there is no prior knowledge of the arrival moment. Therefore, registers have to be reserved for storing every possible combination of the coincidence, i.e. the number of registers for each hit signal equals the interpolation ratio.

In this work the TDC architecture based on three-stage interpolation has been developed to reduce the number of delay cells and especially the number of registers. The coarse interpolator first resolves the arrival moment of the hit signal within the phases of the delay line. Using this information a new reference signal is generated. The coincidence of the new reference signal and the delayed hit signal is registered with a fine interpolator with improved resolution. This architecture enables a higher interpolation ratio with less delay cells and registers and makes it possible to reach a high resolution with a relatively low reference clock frequency.

3 A TDC architecture utilising a multiphase clock and three-stage interpolation

3.1 Introduction

The general architecture of the TDC developed in this work is based on the classic Nutt method (Nutt 1968). A counter provides a large linear dynamic range and interpolation enables high resolution. The developed three-stage interpolation method provides a high interpolation ratio and makes it possible to reach a high resolution with a relatively low reference clock frequency. The low clock frequency and the new interpolation method that reduces the number of delay cells and registers, i.e. switching nodes, help to reach low power consumption and also decrease the crosstalk between measurement channels in a multi-channel TDC, and make it feasible to implement a multi-channel and high resolution TDC as a single chip. The efficient architecture also leads to a small layout area, thus lowering the processing cost.

The extensive use of stabilised delay lines in the interpolation provides good temperature stability, automatic calibration and a stable resolution. With automatic calibration the measurement rate is not limited by separate calibration cycles. The flash operating principle in which the coincidence of the hit and reference signals is determined also provides a high measurement rate.

The biggest design challenges in the design of a TDC are related to the fact that the arrival moment of the hit signals (start and stop) is unknown and asynchronous with respect to the reference clock edges. Yet, the time interval measurement system must provide an immediate and unambiguous measurement result over the full dynamic range (Chance 1949). This is especially true with the systems using the Nutt method. It must be made sure that the readings from the counter and the interpolators are always consistent with very high probability. Two synchronisation schemes were developed in this work. The first synchronisation circuit is for controlling the operation of the counter, as explained in section 3.4. The second synchronisation circuit generates the difference signal for the fine interpolation, as explained in section 3.6.2.

3.2 Architecture and operating principle

The time interval measurement is divided in three stages in the developed architecture. The operating principle is presented in Fig. 2 as a conceptual timing diagram and the general architecture of the TDC is presented in the block diagram of Fig. 3. A more detailed block diagram is presented in Fig. 17 in section 4.1. In the first stage the integer number of the cycles of the reference clock (ref_clk in Fig. 2) of the measured time interval (T_{meas} in Fig. 2) is determined with a synchronous counter (T_{ctr} in Fig. 2 and Fig. 3). The control signals for the counter are obtained by synchronising the hit signals (start and stops) to the rising and falling edges of the reference clock with the block counter sync in Fig. 3 using the dual-edge synchronisation method developed in this work and described in section 3.4. The synchronisation is controlled with a feedback signal from the interpolation (clk_sel in Fig. 3) to ensure the consistency between the readings from the counter and the interpolators. The counter is enabled (ctr_en in Fig. 3) with the start signal and the state of the counter is stored (store_ctr in Fig. 3) with the stop signals without disabling the counter.

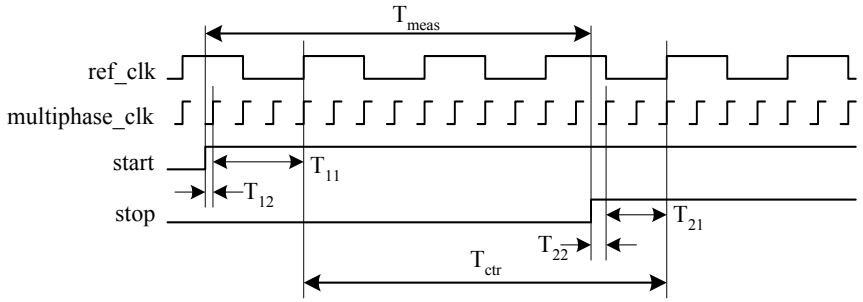

Fig. 2. Conceptual timing diagram.

In the second stage the resolution is improved by a factor of N by using a coarse N-tap stabilised multiphase clock (multiphase_clk in Fig. 2 and Fig. 3) common to all measurement channels. The multiphase clock signal has N time-interleaved phases of the reference clock signal evenly distributed within the clock cycle. This first, coarse interpolation stage works as a flash converter. No actual residue is formed. The coincidence of the asynchronous hit signals and the multiphase clock is stored in N registers (coarse interpolation reg and synchronisation in Fig. 3) the states of which (T_{11} and T_{21} in Fig. 2 and Fig. 3) directly represent the arrival moment of the hit signals within the clock period T_{clk} with the resolution of T_{clk}/N.

In the third stage the phase difference between the hit signals and the edges of the multiphase clock (T_{12} and T_{22} in Fig. 2 and Fig. 3) is measured with stabilised fine interpolators in two stages with an interpolation ratio of M, as explained in section 3.7. The combined interpolation ratio after the three interpolation stages is thus N·M. To be able to use a single fine interpolator structure for each hit signal for digitising the arrival

moment of the hit signal within any of the multiple clock phases, a difference signal or a residue proportional to the arrival moment of the hit signal with respect to the N clock phases is needed. The difference signal is the phase difference between the asynchronous hit signal and the hit signal synchronised to the phases of the multiphase clock (e.g. start_async and start_sync in Fig. 3), as explained in section 3.6.2. The nature of this fine interpolation is analogous to the principle used e.g. with TACs, pulse shrinking delay lines or vernier delay lines.

The dynamic range of the fine interpolator is controlled with a bias signal ($bias_2$ in Fig. 3) generated by the fine interpolation reference that receives the time base from the multiphase clock, as explained in section 3.9. Also the bias signal ($bias_1$ in Fig. 3) generated for stabilising the multiphase clock is needed in the fine interpolator structure for controlling the offset delay of the different propagation paths, as explained in section 3.8. In fact, the architecture contains two nested stabilising loops. The outer loop is the stabilised delay line for generating the multiphase clock. The inner loop is the fine interpolation reference. The principle of nested stabilised loops developed in this work (Mäntyniemi *et al.* 1999) was also utilised as a delay generator in a direct digital synthesis (DDS) clock generator (Heiskanen *et al.* 2001).

The main difference between the TDC architecture developed in this work and the previous TDC architectures based on flash delay line sampling is that in this work also the edges of the multiphase clock generated by the delay line for the coarse interpolation are utilised to generate new timing signals needed in the fine interpolation. This makes the multi-stage interpolation possible and significantly reduces the amount of hardware, especially registers, needed to reach a high interpolation ratio. The edges of the multiphase clock are also used as reference signals to stabilise the dynamic range of the fine interpolation structure.

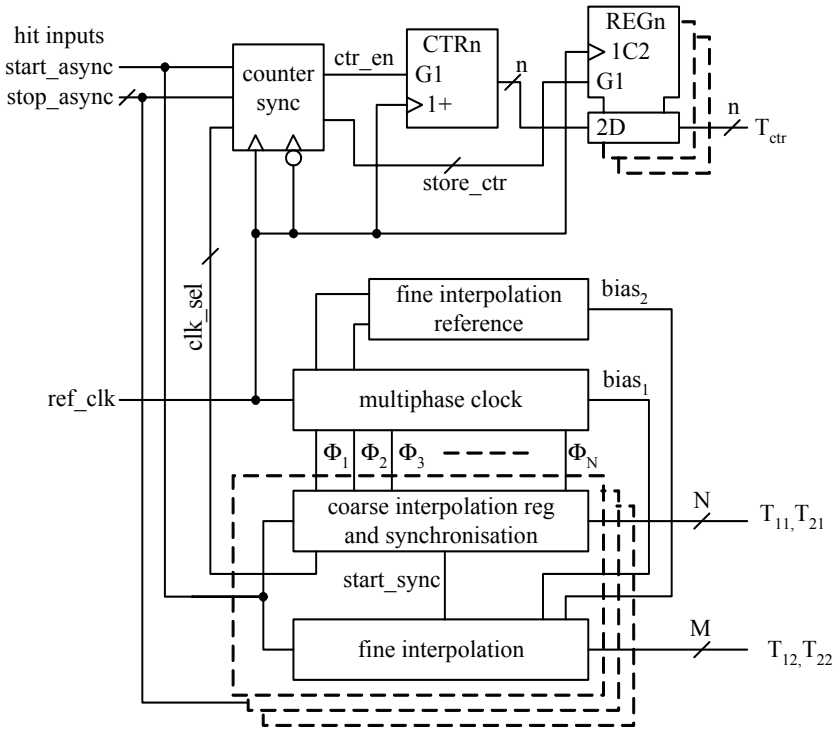

Fig. 3. Block diagram of the TDC architecture.

3.3 Counter and hit signal synchronisation

The operation of the counter has to be synchronised carefully. The counter must be enabled with the start signal and disabled or sampled with the stop signal in a controlled manner regardless of the random arrival moment of the start and stop signals. The counter cannot just be asynchronously sampled on the fly. The sampling moment could well take place while the counter is in transition, which would make the reading unreliable. Also the readings of the counter and the interpolators must be co-ordinated so that the measurement result is always correct regardless of the arrival time of the hit signals.

The problem with a counter and a delay line interpolator with a simple two flip-flop synchroniser of Fig. 4 is illustrated in the timing diagram of Fig. 5. There is no particular control for the synchronisation. The start hit signal is first synchronised to the reference clock (ref_clk in Fig. 4 and Fig. 5) with two flip-flops producing the signal q2, which is used as the enable signal for the counter. In case one the hit signal arrives just before the rising edge of the clock signal but is detected by the first flip-flop. Due to the synchronising delay the counter (ctr in Fig. 5) starts to run two clock cycles after the

arrival moment of the hit signal. In case two the hit signal arrives only a bit later. The sample of the multiphase clock, i.e. the result from the interpolation, is thus the same as in case one. Only this time the timing margins of the first flip-flop are not met and the synchronisation is delayed by one clock cycle. Consequently, the counter is started one clock cycle later compared to case one. Thus, there is an uncertainty of one clock cycle in the measurement result. The same uncertainty also exists with the synchronisation of the stop signal. The synchronised stop signal to sample the state of the counter or to stop the counter can be one clock cycle late. Therefore, it is not sufficient to have the hit signals just synchronised, rather they must be synchronised to the correct edge of the reference clock consistently.

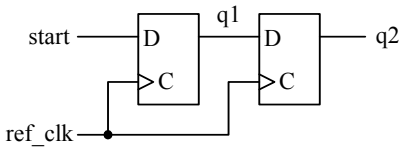

Fig. 4. Two flip-flop synchroniser.

In the prior art, the synchronisation problem related to a counter and flash delay line interpolation has been solved for example by having two separate counters running with opposite phases of the clock signal. The hit signals store the states of the counters into two registers. In this way at least one of the counters has a stable and correct state while being sampled. Based on the reading from the interpolators the register with the valid counter data is read (Knotts *et al.* 1994, Mota & Christiansen 1998). In the case of a multi-channel TDC with many stop channels two counters are needed as well as two registers for each stop signal. With long counters the overhead caused by the additional counter and the registers can be substantial.

In one of the former TDC realisations a single counter is clocked with both edges of the reference clock. Effectively the most significant bit of the interpolator is redundant with the least significant bit of the counter, which makes it possible to correct the counter data with the interpolator data during the readout of the results. (Gorbics *et al.* 1997.) Only one additional bit is needed in the counter and in the registers for the stop signals to reach the same dynamic range, but the clock frequency of the counter is doubled.

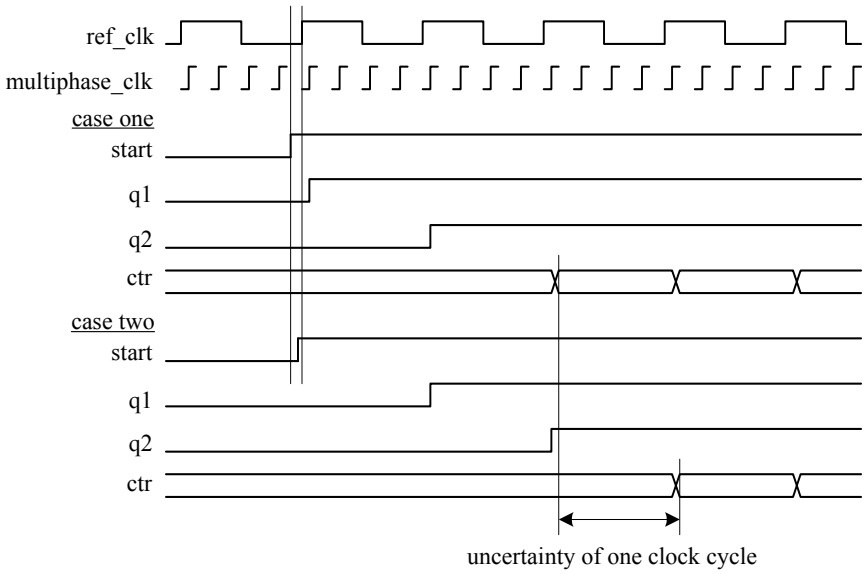

Fig. 5. Uncertainty with the operation of the counter.

3.4 Dual-edge synchronisation method

In this work a dual-edge synchronisation method for the control signals of the counter was designed (Mäntyniemi *et al.* 1997). The major improvement is the need for only one common counter running at the reference clock frequency and one register for each stop signal to store the state of the counter on the fly. Instead of using the interpolator data for selecting which of the two counter registers contains the correct data, the state of the multiphase clock at the arrival moment of the hit signal is used for selecting whether it is safe and whether the hit signals should be synchronised to the rising or falling edge of the reference clock (ref_clk) to co-ordinate the operation of the counter and the interpolators.

The logic diagram of the synchroniser is presented in Fig. 6. Actually only the state of the first phase (Φ_1) of the multiphase clock is needed to give the required information with the registered signal (clk_sel in Fig. 6). This tells whether the interpolation result is larger or smaller than $T_{CLK}/2$. Controlling the operation of the counter with the feedback from the interpolation guarantees that the readings from the counter and interpolators are consistent with very high probability.

The counter (CTRn) is synchronously enabled with the start signal (ctren in Fig. 6) and storing the state of the counter to the register (REGn) is synchronously enabled during one clock cycle with the signal storectr of Fig. 6. The final synchronised signal, whether it is the start signal to enable the counter or the stop signal sampling the state of the counter, is always synchronous to the rising edge of the clock. Any pipeline delay due

to the synchronisation is cancelled out since all the hit signals are treated the same way. This synchronisation method has also been adopted in a 4-channel TDC implemented in BiCMOS (Hervé & Torki 2002).

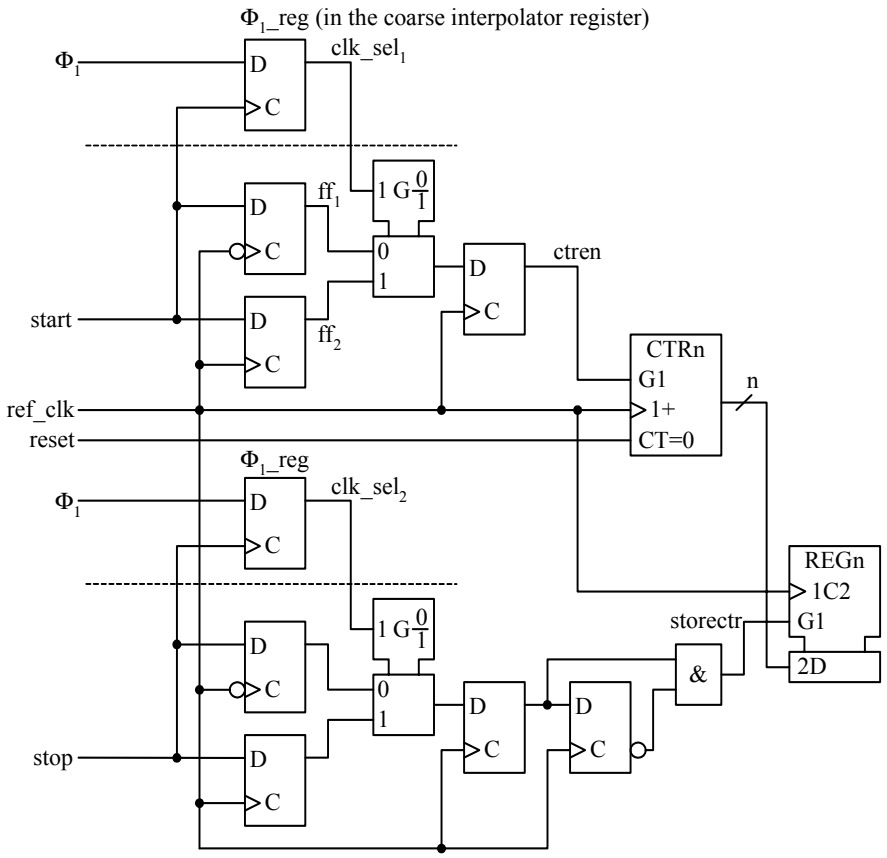

Fig. 6. Logic diagram of the dual-edge synchroniser.

Fig. 7 illustrates the operation of the dual-edge synchroniser in three different cases. The interpolation is performed with an 8-tap multiphase clock delay line, i.e. the LSB of the measurement is $T_{CLK}/8$. The delay difference between the start and stop signals is 7 LSBs. The possible interpolation results are presented as the distance to the next rising edge of the phase Φ_1 of the multiphase clock (multiphase_clk states in Fig. 7).

In case one the start signal appears just before the rising edge of the phase Φ_1 of the multiphase clock. The state of the register (Φ_1_reg in Fig. 6) storing the state of Φ_1 (clk_sel$_1$ in Fig. 6) is zero. It means that a rising edge of the reference clock could be close to the edge of the hit signal. Therefore, it is not safe to synchronise to the rising edge of the clock signal because the hit signal could violate the timing margins of the corresponding flip-flop. Therefore, in case one the enable signal for the counter (ctren) is obtained by synchronising the start signal first to the falling edge and then to the rising

edge of the reference clock. Clearly the timing margins of the flip-flop synchronising the start signal to the falling edge are not violated. Thus, synchronising first to the falling edge is reliable. The stop signal is synchronised in the same way as the start signal.

In case two the start signal appears just after the rising edge of the phase Φ_1 of the multiphase clock. The state of the register storing the state of Φ_1 (clk_sel_1 in Fig. 6) is therefore one. Now the falling edge of the reference clock could be close to the edge of the start signal. Therefore, the start signal is first synchronised to the rising edge of the reference clock. The enable signal for the counter is delayed by one clock cycle as compared to case one. Consequently, the state of the counter when stored by the synchronised stop signal is smaller by one. However, this is compensated for by the start interpolator the result of which at the same time jumped from the minimum to the maximum and is added to the measurement result. The stop signal is synchronised in the same way as in case one.

In case three the synchronisation of the start signal is carried out in the same way as in case two. However, the stop signal arrives just after the rising edge of the phase Φ_1 of the multiphase clock. Therefore, the stop signal is first synchronised to the rising edge of the reference clock. Compared to cases one and two the signal storing the state of the counter is delayed by one clock cycle and the state of the register containing the reading from the counter is increased by one as compared to case two. This is compensated for by the stop interpolator the result of which jumped from the minimum to the maximum and is subtracted from the measurement result.

In general, if the result of the interpolation for a hit signal $< T_{CLK}/2$, the synchronisation delay varies between $\sim T_{CLK}$ and $\sim 1.5T_{CLK}$, depending on the arrival moment of the hit signal. If the result of the interpolation for a hit signal $\geq T_{CLK}/2$, the synchronisation delay varies between $\sim 1.5T_{CLK}$ and $\sim 2T_{CLK}$. A smaller result of the interpolation leads to a shorter delay of synchronisation.

Therefore, if the interpolation result for the start signal $< T_{CLK}/2$, the counter is enabled earlier compared to the situation in which the interpolation result for the start signal $\geq T_{CLK}/2$. As the counter is enabled earlier, the state of the counter stored by the stop signal is larger. However, the result of the interpolation for the start signal added to the measurement result is smaller. With the stop signal a smaller result of interpolation leads to storing the state of the counter sooner, which means that the stored state of the counter is smaller. However, the result of the interpolation for the stop signal subtracted from the measurement result is also smaller and the consistency between the readings from the counter and the interpolators is ensured.

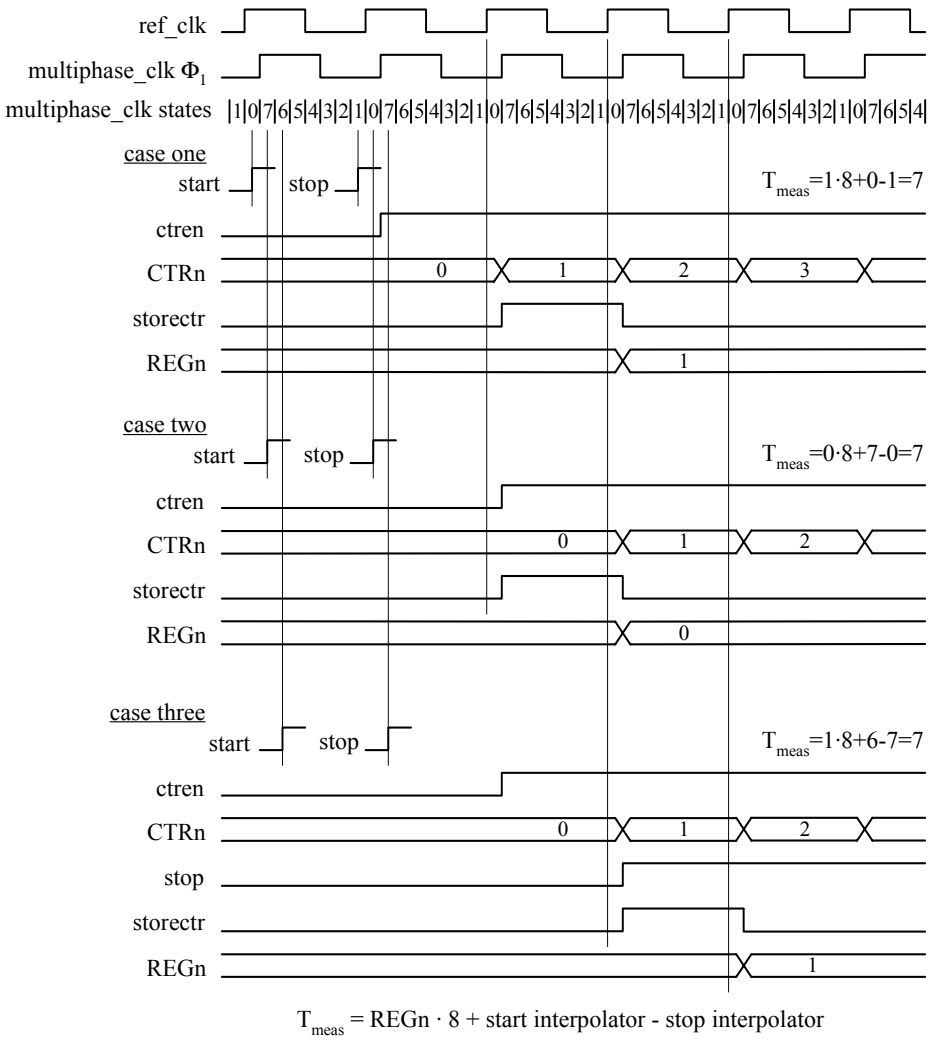

Fig. 7. Timing examples of the operation of the dual-edge synchroniser.

The limitation of this synchronisation method is that the register, Φ_1_reg in Fig. 6, storing the state of the first delay phase Φ_1 of the multiphase clock must resolve its state in less than a clock cycle to control the synchronisation reliably, because no redundant counter data is stored, as opposed to the previous art (Knotts *et al.* 1994, Gorbics *et al.* 1997, Mota & Christiansen 1998). This limits the maximum operating frequency. The timing of the most critical situation is illustrated in Fig. 8 for the start signal of Fig. 6. The start signal arrives just after the rising edge of the Φ_1 of the multiphase clock. However, the timing margins of the register storing the state of Φ_1 are not met and the signal clk_sel$_1$ of Fig. 6 eventually settles to state zero after a possible metastable state, as shown in Fig. 8.

This selects the hit signal to be synchronised to the falling edge and then resynchronised to the following rising edge which is less than a clock cycle away. When the time available for the signal clk_sel_1 to resolve its state is estimated, it has to be taken into account that Φ_1 is delayed from the reference clock and the hit signal arrives about a setup time of the register later than the rising edge of Φ_1. The state of the register must be stable before the next rising edge of the clock minus the delay of the multiplexer (t_{pmux}) and the setup time of the synchronising flip-flop (t_{sFF}), as shown in Fig. 8.

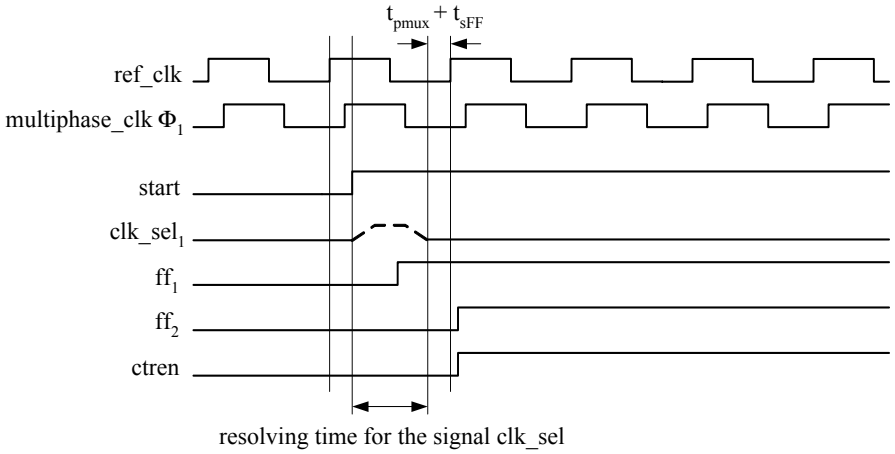

Fig. 8. Most critical timing of the dual-edge synchroniser.

Even though an ideal 50/50 duty cycle is assumed for the clock signals, the only effect the non-ideal duty cycle has on the operation of the synchroniser logic is that the timing margins are reduced, which limits the maximum operating frequency. However, the synchroniser can be adapted to a higher clock frequency by inserting additional synchronising flip-flops, as shown in Fig. 9 for one hit signal. This way the sample of the delay line has an additional clock cycle to recover to increase reliability. This has been tested with a TDC prototype based on a counter and a ring oscillator interpolator running at ~400 MHz (Nissinen *et al.* 2003). Even more flip-flops can be cascaded to further increase the settling time.

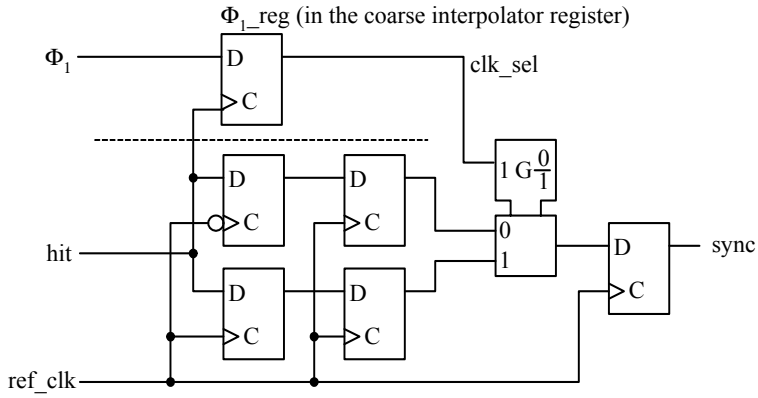

Fig. 9. Logic diagram of the dual-edge synchroniser with increased settling time.

3.5 Multiphase clock with stabilised delay line

The multiphase clock can be generated, for example, with a stabilised delay line configured as a delay-locked loop (DLL) or as a ring oscillator configured as a phase-locked loop (PLL). The reference clock frequency and the number of delay cells in the delay line have a strong effect on the power consumption because the delay line operates continuously. Also the expected maximum integral nonlinearity (INL) increases as the number of delay cells in the delay line is increased. In the proposed architecture with three-stage interpolation the length of the delay line can be limited to reduce power consumption and nonlinearity. The actual high resolution is reached with the fine interpolation structure that is activated and thus consumes power only when the hit signals arrive.

3.6 Coarse interpolation with synchronisation of hit signals

The block that determines the coincidence of the hit signals and the multiphase clock and provides the coarse interpolation result (coarse interpolation reg and synchronisation in Fig. 3) is the key building block to reduce the number of delay cells and especially the registers, as it also provides the synchronised signal used for generating the residue for the fine interpolation.

3.6.1 Generating a linear residue for interpolation

A common practice to generate the signals for the interpolators and for the counter with interpolators based on TACs, vernier delay lines and pulse shrinking delay lines is to use a time-to-pulse-length or a time-to-pulse-pair synchroniser built of two synchronising flip-flops for each hit signal, as shown in Fig. 10. The first flip-flop (ff0) is used as a hit register to store the arrival of a possibly short hit signal. The residue for the interpolation is the phase difference between the asynchronous hit signal d and the synchronised output q2 of the second synchronising flip-flop (Kostamovaara & Myllylä 1986, Määttä *et al.* 1988, Määttä & Kostamovaara 1998, Park & Park 1999, Räisänen-Ruotsalainen *et al.* 2000).

Two synchronising flip-flops are needed because of the inevitable violation of the timing margins of the first flip-flop (ff1), which increases the delay of the first flip-flop and makes the residue nonlinear if the output q1 of the first flip-flop is directly used for the residue. The first synchronising flip-flop can even enter a metastable state.

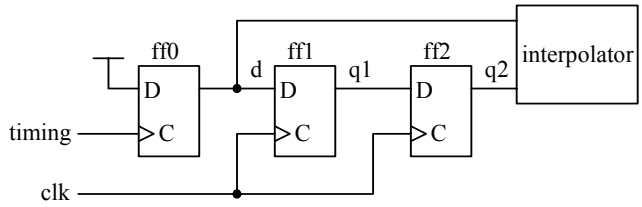

Fig. 10. Two flip-flop synchroniser for the generation of the interpolator residue.

The way to deal with the metastability is to wait until the first flip-flop has recovered from the metastable state with a high probability (Kleeman & Cantoni 1987, Horstmann *et al.* 1989, Philips 1989, Gabara *et al.* 1992, Shear 1992, Cypress 1997). Thus, the output of the first synchronising flip-flop is not sampled with the second flip-flop (ff2) until the output of the first flip-flop has settled. Adding the second flip-flop gives the first flip-flop a clock cycle minus the setup time of the second flip-flop to resolve its state before the output is synchronised with the second flip-flop. As a result, the residue, i.e. the delay between d and q2, is linear with a high probability, but the offset of one clock cycle has to be taken into account in the interpolator. The minimum period of the reference clock is limited by the minimum required settling time for the first synchronising flip-flop and the setup time of the second flip-flop.

The simulated propagation delay of the flip-flops of the synchronisation logic of Fig. 10 is shown in Fig. 11 as a function of the arrival time of the hit signal with respect to the cycle of the reference clock T_{clk}. The nonlinearity of the delay from the clock input clk to the output q1 of the first synchronising flip-flop ff1, t_{cq1} in Fig. 11, is translated into a nonlinear delay from the input d to the output q1, t_{dq1} in Fig. 11. The linear delay from input d to the output q2 of the second synchronising flip-flop ff2, t_{dq2} in Fig. 11, is the linear residue to be interpolated.

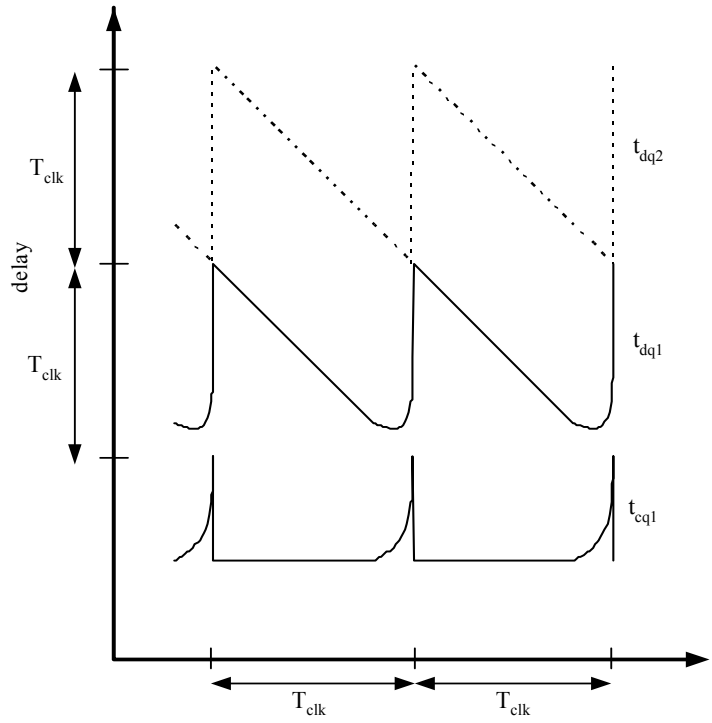

Fig. 11. Nonlinear propagation delay of the first flip-flop (t_{cq1}), nonlinearity of the residue with violated timing margins (t_{dq1}) and the linear residue obtained with a two flip-flop synchroniser (t_{dq2}).

3.6.2 Synchronising to a multiphase clock

The synchronising method developed in this work is an extension of the synchroniser with two flip-flops. The synchronising clock signal used here is the multiphase clock signal. Fig. 12 presents a possible logic diagram of the multiphase clock synchroniser. N parallel two flip-flop synchronisers sample the arrival moment of the hit signal with clock phases Φ_1-Φ_N with a cycle of T_{CLK}. The states of the first flip-flops (ff_{10}-ff_{N0}) are the coarse interpolation result. The hit signal is assumed to be a rising edge and to remain a logic one until a new measurement is initiated. The second flip-flops (ff_{11}-ff_{N1}) generate N time-interleaved synchronised signals ($sync_1$-$sync_N$). The delays between the arrival moment of the hit signal and the N synchronised signals represent N time-interleaved difference signals with the amplitude and period of T_{CLK} and the offset of ~T_{CLK}, as shown in Fig. 13, which shows the result when synchronising to the clock phases of a multiphase clock with four phases.

To generate a cyclic difference signal with an amplitude and period of T_{clk}/N, shown in Fig. 13 with N = 4, the outputs of the N flip-flops are combined with an N-input OR gate, as shown in Fig. 12. The first of the N synchronised outputs always triggers the OR gate output. The difference signal for the fine interpolation is the delay difference between the hit signal and the output of the OR gate. Effectively the hit signal is synchronised with a GHz-level clock signal, even though such a high frequency real clock signal never has to be generated in this architecture. Actually the operation of the synchroniser is analogous to the operation of the time-interleaved AD/DA-converters.

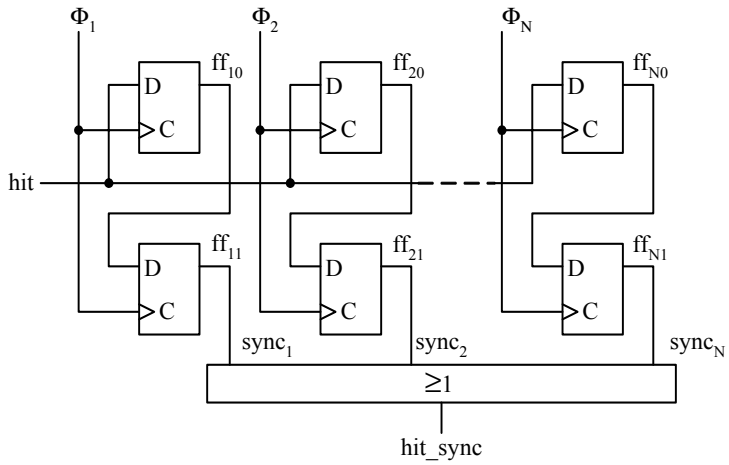

Fig. 12. Logic diagram of the multiphase clock synchroniser.

Synchronising the hit signal to a certain clock phase takes place if the hit signal arrives early enough before that clock edge, as seen in Fig. 14, in which the output of the first flip-flop ff_{10} eventually settles to a logic one and the second flip-flop ff_{11} generates the synchronised signal because the hit signal arrived before phase Φ_1. The drawback of this method is the offset of the difference signal, also visible in Fig. 13. The offset of $\sim T_{clk}$ guarantees that the first flip-flop has settled and the setup time of the second flip-flop is not violated to keep the delay of the second flip-flop constant. If no residue is generated for the fine interpolation, as is the case for example with the TDC by Mota & Christiansen (1999), in which the multiphase clock is sampled with multiple time-interleaved hit signals, there is no offset to be taken into account. However, in that case the number of registers to store the interpolation result equals the interpolation ratio.

As the state of all the first flip-flops is set to one after a clock cycle, the information about the arrival moment of the hit pulse is lost unless the contents of the first flip-flops is stored to an additional set of registers, as is done in a multihit TDC (Andreani *et al.* 1998). A simple local feedback logic can also be used to retain and decode the timing information without the use of additional registers (Kalisz *et al.* 1997a, Kalisz *et al.* 1997b, Szplet *et al.* 2000).

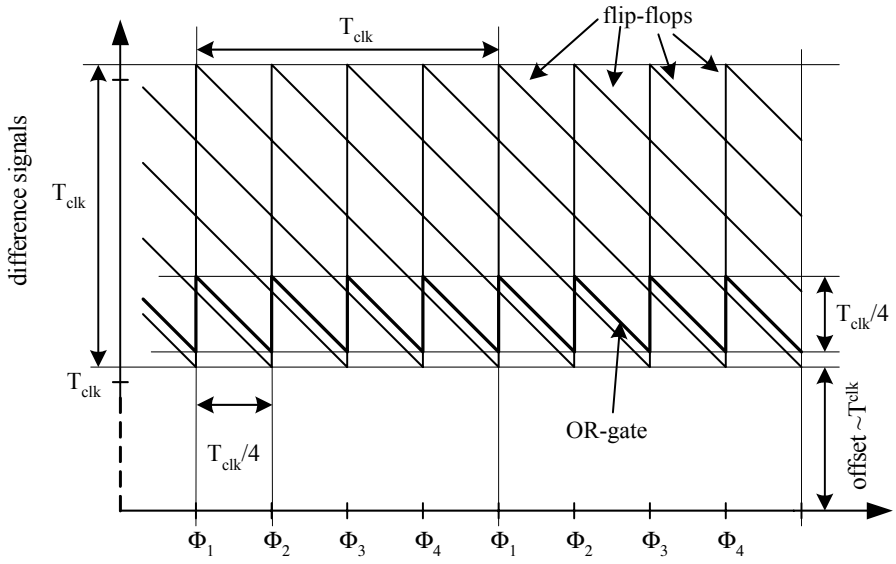

Fig. 13. Difference signals generated by the synchronising logic.

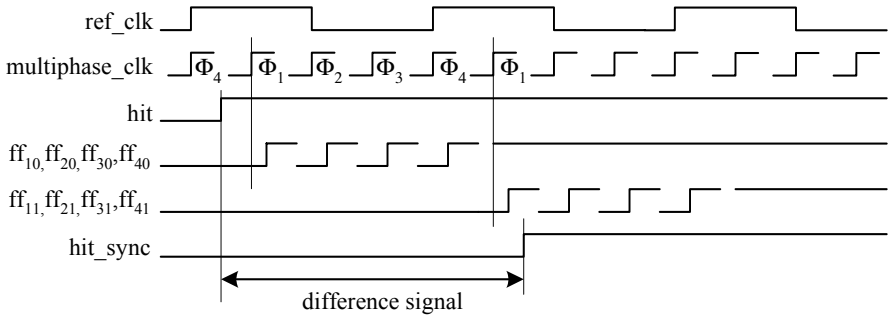

Fig. 14. Timing diagram of the synchronising logic with a 4-tap multiphase clock.

The offset of ~T_{clk} of the logic of Fig. 12 can be reduced by shifting the clock signal phases connected to the second flip-flops, as shown in Fig. 15. As the timing characteristics of the flip-flops are known, it can be estimated how long the first flip-flops must be allowed to settle before they are synchronised with the second flip-flops. If it turns out that a reliable synchronisation can be achieved with a settling time shorter than a full clock cycle, it can easily be realised by rearranging the clock signals to the second flip-flops. The synchronising offset can be varied from T_{clk}/N to T_{clk} with different values of the offset K in Fig. 15. The notation (N+K)modN containing the modulo-operation

means that the clock phase Φ_{N+1} following Φ_N is Φ_1 of the next clock cycle etc. However, the synchronising logic generates a linear residue only if the timing margins of the second flip-flop are not violated.

The loss of data in the first flip-flops can also be prevented by swapping the role of the data and clock signals of the first flip-flop, also shown in Fig. 15. This way the flip-flops store a snapshot of the states of the delay line clock phases connected to the data inputs when the hit signal arrives to the clock inputs. The snapshot determines the arrival moment of the hit signal within the clock cycle with a resolution of T_{clk}/N. However, the interpretation of the timing diagram of Fig. 14 is slightly different. With the same timing between the hit signal and the multiphase clock phases propagating in the delay line the output of the first flip-flop settles to logic zero because now the clock signal of the first flip-flop ff_{10} arrived just before the data signal, being a logic zero at that time. Since the second flip-flop should be allowed to synchronise also in this case to keep the synchronising identical with the logic of Fig. 12, the zero output of the first flip-flop must be inverted to a logic one by using the inverted outputs of the first flip-flops, as seen in Fig. 15.

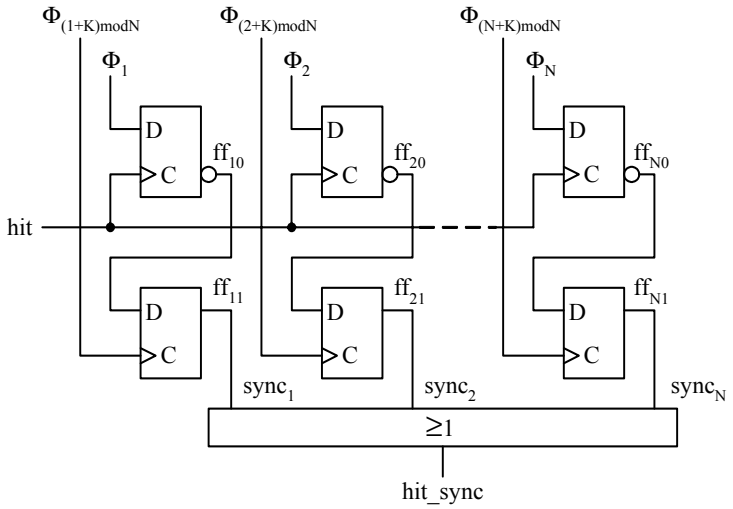

Fig. 15. Multiphase clock synchroniser with shifted clock phases and swapped data and clock signals of the first flip-flop.

3.7 Fine interpolation

The final high resolution is achieved with the fine interpolator. There are several possibilities for realising the fine interpolator, because the dynamic range of T_{CLK}/N of the fine interpolator is only a fraction of the reference clock cycle and a small interpolation ratio is adequate to achieve high resolution. But due to the attainable high

resolution the absolute gate propagation delay cannot be used as the digitising unit. An interpolator structure in which the resolution is based on the delay difference between delay cells can be used. Vernier delay lines or pulse shrinking delay lines are feasible with low dynamic range. To reach a short conversion time and to reduce the number of delay cells, a different approach was selected in this work.

At a conceptual level either the asynchronous hit signal or the synchronised signal of the residue could be split to M multiple equally spaced phases with a delay difference of $T_{clk}/N/M$. The offset needed in the synchronising would be compensated for with an additional propagation delay equal to the synchronising delay in the propagation path of the asynchronous hit signal. The coincidence of the M multiphase signals and the other signal of the residue would be stored to M registers.

To reduce the number of delay cells the fine interpolation ratio of M can be obtained by splitting both signals of the fine interpolation residue. By splitting the synchronised signal to M_1 and the asynchronous hit signal to M_2 phases, an effective fine interpolation ratio of $M = M_1 \cdot M_2$ can be achieved with M_1+M_2 signal phases. The delay difference between the phases of the synchronised signal equals $T_{clk}/N/M_1$ and the delay difference between the phases of the asynchronous hit signal equals $T_{clk}/N/M_1/M_2$. The overall combined interpolation ratio including the coarse interpolation is thus $N \cdot M_1 \cdot M_2$ and this TDC architecture combines, in fact, three interpolation stages. The implementation of the fine interpolator is explained in section 4.4.

The operation of the fine interpolation method is illustrated in Fig. 16 with a multiphase clock with four phases. Both the synchronised signal (hit_sync) and the asynchronous hit signal (hit_async) are split to four phases ($M_1=M_2=4$). The coincidence of the synchronised signals and the asynchronous hit signals is shown in three cases. The synchronisation offset is $T_{clk}/2$, i.e. K in Fig. 15 is N/2. The operation of the fine interpolator at the wrap-around point of the cyclic residue is particularly important, as shown in Fig. 16 b) and in Fig. 16 c), because this shows that the readings of the coarse and fine interpolators are consistent.

Fig. 16 a) shows the earliest possible arrival moment within the clock cycle for the hit signal to be synchronised to phase Φ_3 of the multiphase clock. This generates the maximum residue, i.e. the maximum delay difference between the hit signal and the synchronised signal. The offset is adjusted so that all the M_2 phases of the asynchronous hit signal (M_2_hit_async) arrive just before the phases of the synchronised signal (M_1_hit_sync).

In Fig. 16 b) is shown the latest possible arrival moment of the hit signal that can be synchronised with the clock phase Φ_3. With this minimum residue only the first phase of the M_2 hit signals arrives before the last phase of the M_1 synchronised signals. Thus, if the synchronised signal is split to M_1 phases and the asynchronous hit signal is split to M_2 phases, there are $M_1 \cdot M_2$ possible combinations of the coincidence of these signals depending on the arrival moment of the hit signal within the phases of the multiphase clock.

In Fig. 16 c) the hit signal arrives a bit later than in Fig. 16 b). Therefore the synchronisation is carried out by the clock phase Φ_4. The reading of the coarse interpolation would be smaller by T_{clk}/N, if the reading from the coarse interpolation is interpreted as the distance to the next rising edge of the reference clock signal. However, at the same time the residue and thus the fine interpolation result jumps from the

minimum to the maximum. The overall interpolation result of that hit signal changes only by an LSB and the results from the coarse and fine interpolation are consistent.

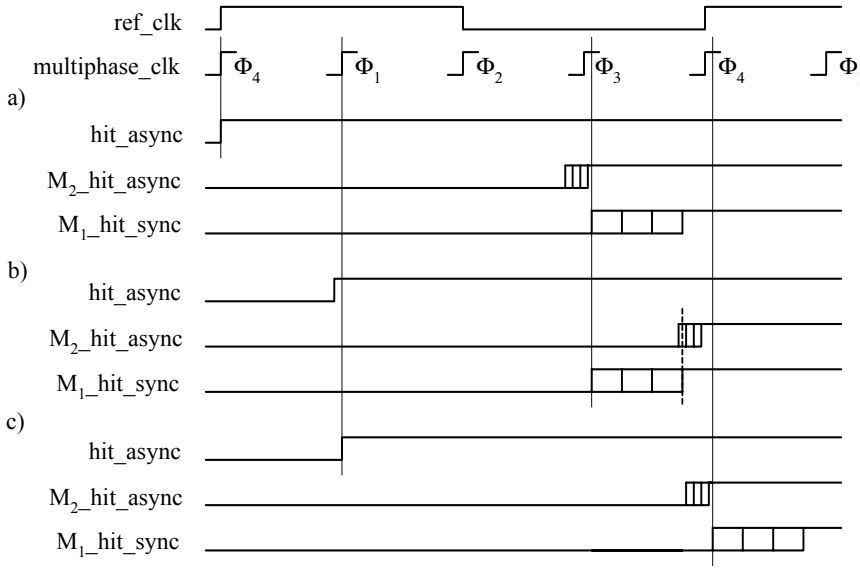

Fig. 16. Timing diagram of the fine interpolation method with a) the earliest arrival moment of the hit signal to be synchronised to Φ_3 b) the latest arrival moment of the hit signal to be synchronised to Φ_3 and c) the earliest arrival moment of the hit signal to be synchronised to Φ_4.

3.8 Offset compensation

There are three major sources of propagation delay offset in the fine interpolator structure. Firstly, the synchronisation offset needed in the logic generating the residue for the fine interpolator depends on the recovery time allowed for the first synchronising registers to settle. This offset can be compensated for by adding delay cells identical to those used in the coarse delay line and stabilised with the same bias signal to the propagation path of the asynchronous hit signal. Secondly, the propagation delay difference between the structures to generate the M_1 synchronised and M_2 asynchronous signals of the fine interpolation residue must also be compensated for. Thirdly, also any other difference of logic gates between the synchronous and asynchronous propagation paths can be compensated for by adding dummy logic gates. Any logic gate that is specific to one path is added also to the other path.

3.9 Fine interpolation reference

The dynamic range of the fine interpolator equals the delay difference between the edges of the multiphase clock. The operating point of the delay cells used in the fine interpolator is stabilised by using a pair of reference signals from the multiphase clock delay line, instead of just adjusting the operating point by a control voltage without any feedback (Chapman *et al.* 1995). This way also the fine interpolator structure has automatic calibration. The delay cells in the reference delay line must be identical to those used in the fine interpolator structure.

4 Prototype TDC

4.1 Architecture

The feasibility of the architecture presented in the previous chapter was verified with a prototype circuit with ten measurement channels implemented as a full-custom application specific integrated circuit (ASIC) in a 0.6 μm single-poly, double metal digital CMOS process. The architecture of the prototype is presented in Fig. 17. The circuit measures the time intervals between a common start signal and nine independent stop signals (stop(1:9)).

The hit signals are synchronised to the rising and falling edges of the reference clock to control the operation of the 15-bit counter (CTR15) using the method presented in section 3.4. The synchronisation of each hit signal is controlled separately by the control signals clk_sel(0:9) of Fig. 17. The counter is enabled with the start signal (ctr_en) and the state of the counter is synchronously stored (store_ctr) to nine 15-bit registers (REG15) with the stop signals.

A 16-tap voltage-controlled ($bias_1$) delay line connected as a delay-locked loop (DLL_1 in Fig. 17) is used as the timing core to produce the 16-phase multiphase clock (Φ_1-Φ_{16}). The DLL_1 is presented in more detail in section 4.2. The coarse interpolation result is stored in a 16-bit register (REG16), i.e. the coarse interpolation ratio N is 16, and the hit signals are synchronised to the phases of the multiphase clock to provide the residue for the fine interpolation (coarse interpolation REG16 and synchronisation block), as explained in section 4.3.

The synchronised signal of the residue (hit_sync) is split to four ($M_1(1:4)$) and the asynchronous hit signal of the residue (hit_async) to eight phases ($M_2(1:8)$) to produce a fine interpolation ratio M of 32. The fine interpolation results are stored in 32-bit registers (REG32). The overall interpolation ratio is thus $16 \cdot 32 = 512$. The structure of the fine interpolator is explained in more detail in section 4.4.

The DLL_1 also provides a reference signal pair for stabilising the fine interpolator structures with the fine interpolator reference (DLL_2 in Fig. 17) that generates the bias voltage $bias_2$, as explained in section 4.6.

As the results of the interpolations are stored in a thermometer code, a linear to binary coder (lin/bin) is needed in the data interface. The propagation delay offset between the synchronous and asynchronous paths of the signals forming the residue for the fine interpolation is adjusted with the blocks ΔT_1 and ΔT_2, explained in section 4.5. Section 4.7 presents the ways to calibrate the TDC to improve the single-shot precision otherwise limited by the INLs of the interpolators. A single-channel multihit operation mode was included in the prototype TDC, as explained in section 4.8. The layout of the prototype chip is presented in section 4.9.

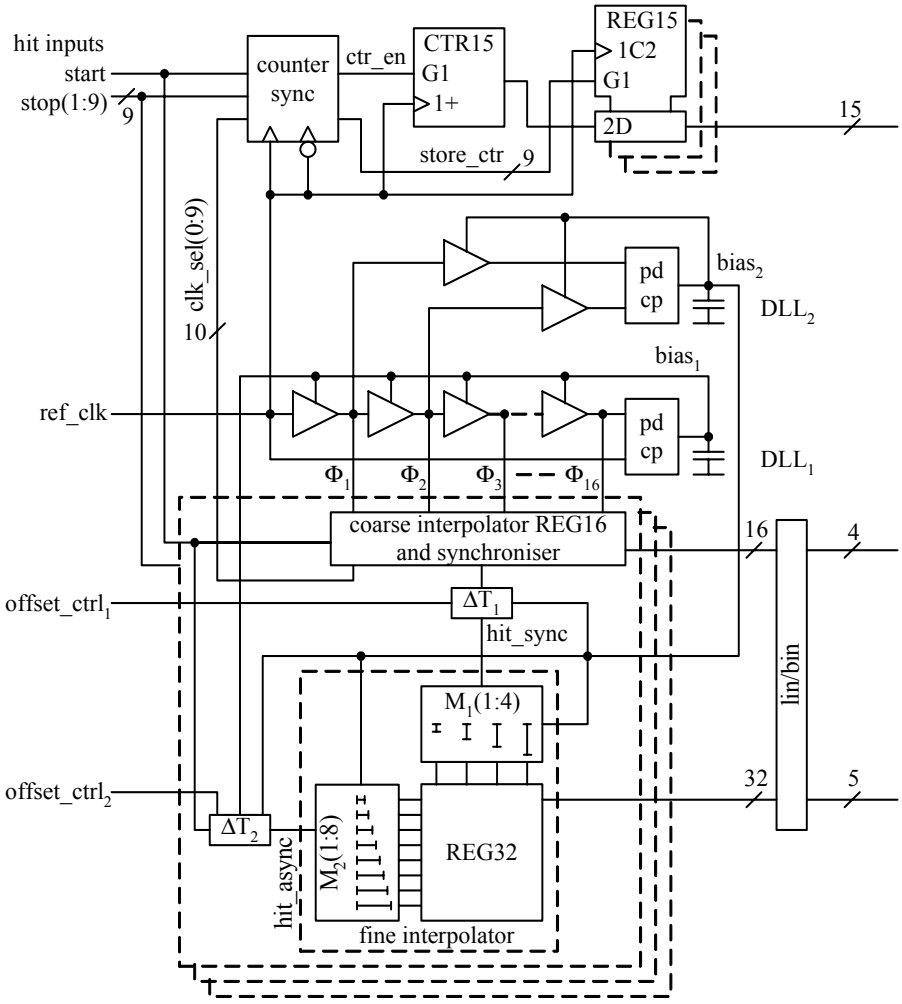

Fig. 17. Block diagram of the prototype TDC.

4.2 DLL_1

The propagation delay of the coarse delay line is locked to the reference clock cycle with a DLL, as shown in Fig. 18. The output of each delay cell is connected to the input of the next delay cell and buffered to provide the multiple clock phases (Φ_1-Φ_{16}) and the reference for the fine interpolator ($fine\_ref_1$ and $fine\_ref_2$). An identical buffering tree is connected to all delay cells to have equal loading and thus equal propagation delay in all branches. A phase detector (pd) compares the rising edges of a buffered reference clock and the buffered output of the last delay cell and controls the charge pump (cp) so that the voltage of the loop filter capacitor ($bias_1$) sets the propagation delay of the delay line equal to a clock cycle. The gate-to-channel capacitance of an nmos transistor is used as the loop filter with a capacitance of ~100 pF. An additional dummy delay cell is connected as a load to the last actual delay cell and the reference clock is fed to the delay line using a delay cell so that the inputs and outputs of the delay cells providing the multiple clock have equal signal slopes.

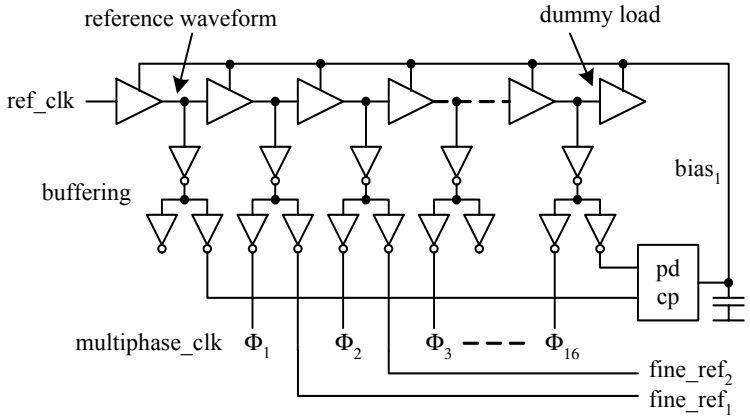

Fig. 18. Circuit diagram of the DLL_1.

The delay cell consists of two identical current starved inverters. The schematic diagram of a delay cell is shown in Fig. 19 a) and the delay as a function of the bias voltage with 3.3 V power supply voltage is shown in Fig. 19 b). The delay cell was characterised with fast process parameters at -40 °C, with typical parameters at +20 °C and with slow parameters at +60 °C. The delay cell was dimensioned so that a 16-tap delay line can be locked to ~66 MHz clock frequency with any given process parameters in the temperature range of -40 - +60 °C. A moderate resolution of about 1 ns is adequate as the actual high resolution of ~30 ps is reached with the fine interpolation structure.

In principle the delay cell retains the duty cycle of the input signal because both the rising and falling edges of the input signal are adjusted similarly. However, due to the buffering tree used in the DLL_1 the second inverter of the delay cell has a larger load than the first inverter. Therefore, the slope of the falling edge in the output of the delay cell is slower than the slope of the rising edge, and the pulses propagating in the DLL_1 are

slightly stretched. According to the simulations this stretching is less than 1 ns in the whole delay line and has no impact on the performance of the TDC, because only the rising edges of the multiphase clock are used as reference signals in the time interval measurement.

The other objective in the design of the delay cell was adequate matching between the propagation delays of the delay cells. Ideally the DLL provides as many evenly spaced clock signals within the clock cycle as there are delay cells in the delay line. However, the variation of the propagation delay of the delay cells caused by device mismatch due to the variation of process parameters appears as nonlinearity of the delay line structures. Also the power supply noise caused by the bonding wires and wiring resistances introduce delay variation in the delay cells.

The expected maximum INL caused by random variation appears in the middle of the DLL with the variance of $N\sigma_1^2/4$, where σ_1 is the standard deviation of the propagation delay of the delay cells and N is the number of delay cells in the delay-locked delay line (Toifl *et al.* 1999). The timing error at the input and output of a DLL is ideally zero. The nonlinearity caused by the random variation between delay cells can be minimised at circuit level by good device matching and by restricting the number of delay cells in the delay line at the architecture level.

Monte Carlo simulations showed a standard deviation of < 5 ps between the propagation delays of the delay cells in the same chip with the selected transistor dimensions, which corresponds to better than 0.5% matching with ~1 ns unit delay. With a 16-tap delay-locked delay line the expected maximum INL due to random variation would be $2\sigma_1$, which is less than 10 ps, i.e. one third of an LSB with the nominal LSB of ~30 ps. The random variation of the propagation delays between different process runs is compensated for with the bias voltage of the DLL.

The target unit delay and the number of delay cells of the DLL_1 were also limited to keep the reference clock frequency low to reduce power consumption. The DLL_1 operates continuously and is likely to dominate the power consumption of the TDC (Mota & Christiansen 1999). Also the overhead caused by the synchronisation logic generating the difference signal for the fine interpolation and the offset compensation delay line can be kept smaller with a shorter DLL. The cumulative jitter in the DLL can also be reduced by limiting the number of delay cells (van de Beek *et al.* 2002).

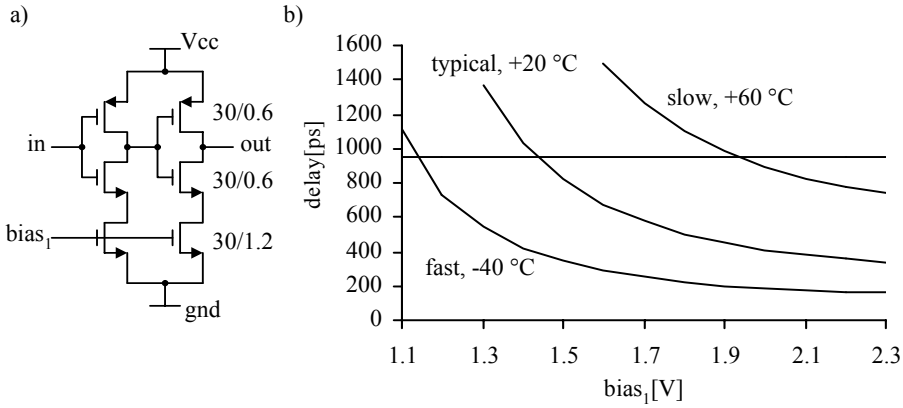

Fig. 19. a) Schematic diagram of the coarse delay cell and b) propagation delay of the coarse delay cell as a function of bias voltage.

DLLs can be used in applications in which the control of the signal timing is important, such as clock synthesis (Bazes *et al.* 1996, Birru 1998, Chien & Gray 2000, Aguiar & Santos 2001, Foley *et al.* 2001, Kim *et al.* 2002), clock alignment or deskewing (Efendovich *et al.* 1994, Christiansen 1996, Geannopoulos & Dai 1998, Garlepp *et al.* 1999), timing control in SDRAM circuits (Hatakeyama *et al.* 1997), direct digital synthesis (DDS) (Heiskanen *et al.* 2001), maximising timing margins (Horowitz *et al.* 1998), clock recovery (Kim & Horowitz 2002) and data retiming (Sonntag & Leonowich 1990). There are time-interleaved applications, such as high-speed analogue-to-digital or digital-to-analogue converters, in which a DLL can provide the multiphase clock signals needed (Wu & Black 2001, Yang *et al.* 2001, Poulton *et al.* 2002).

4.3 Coarse interpolation with synchronisation of hit signal

In the prototype TDC the first edge-active flip-flops of the multiphase clock synchroniser storing the coarse interpolation result were replaced with level active latches to save layout area. Fig. 20 shows the modified logic diagram with latches (dl) and synchronising flip-flops (ff). The clock phases between the latches and flip-flops are shifted by eight phases, i.e. half a clock cycle to reduce the synchronising offset to $\sim T_{clk}/2$. Therefore, the time available for the latch to resolve its state is half a clock cycle minus the setup time of the flip-flop. The 16-input OR-gate was realised as a pseudo-nmos gate to provide equal propagation delay from any of the OR-gate inputs to the synchronised output (hit_sync).

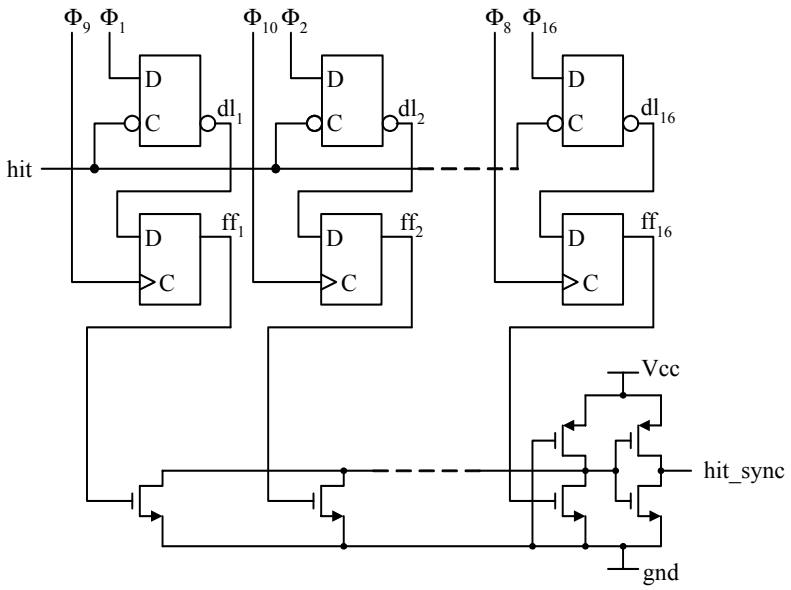

Fig. 20. Logic diagram of the multiphase clock synchroniser of the prototype TDC.

4.4 Fine interpolation

The two main advantages of using the fine interpolation method developed in this work are that a single fine interpolation structure can be used in each measurement channel for digitising the arrival moment of the hit signal within any of the multiple clock phases, which reduces the number of delay cells and registers needed, and that the fine interpolators consume dynamic power only when the hit signals arrive. At that moment the fine interpolator structures are activated and generate two sets of multiphase signals that propagate in the delay cells, one from the asynchronous and the other from the synchronised hit signal. The coincidence of the multiphase signals in the different paths is stored as the interpolation result and the structure becomes idle again.

The duty cycle of the pulses propagating in the fine interpolator structures is not important because only the coincidence of the rising edges of the signals is used in digitising. Therefore, the adjustment of the propagation delay in the delay cell of the fine interpolator can be simpler than in the delay cell of the DLL_1 of the coarse interpolator. Identical delay cells are used for generating the delayed versions of the synchronised and asynchronous hit signals and in the fine interpolation reference (DLL_2) providing the bias voltage ($bias_2$) that stabilises the delay difference between the delay cells. The attainable resolution with the fine interpolators is much better than the attainable propagation delay of the adjustable logic gates. Therefore, it is the delay difference between the logic gates that is used as the time unit defining the resolution of the fine interpolator.

The schematic diagram of the fine delay cell is shown in Fig. 21 a) and the delay difference between two delay cells with one and two load capacitances is shown as a function of the bias voltage in Fig. 21 b). The propagation delay of the delay cell can be adjusted with the bias voltage and by scaling the load capacitance. The bias voltage provided by the fine interpolation reference block sets the overall delay, whereas the capacitive loading scales the propagation delay difference between the delay cells. In addition to the bias voltage and the difference of the load capacitance, also the threshold voltage of the inverter following the capacitively loaded node has an influence on the delay difference between adjacent delay cells as shown by Δt_1 and Δt_2 in Fig. 22. The higher the threshold voltage of the following inverter the smaller is the delay difference or the larger unit capacitance can be used for the same delay difference.

The gate-to-channel capacitance of an nmos transistor with drain, source and bulk connected to the ground is used as the load capacitance. This way a single-poly standard digital CMOS process can be used. The current starved inverter, the unit capacitance and the logic threshold of the inverter following the capacitively loaded node were dimensioned so that a delay difference of ~30 ps, i.e. $T_{CLK}/16/32$, can be achieved with any given process parameters in the temperature range of -40 - +60 °C. The absolute propagation delay of the delay cells varies from ~460 ps to ~670 ps with typical process parameters at room temperature depending on the number of load capacitors. According to the simulation, the capacitance of a single unit capacitance is ~10 fF. Two buffered outputs (out_1 and out_2) are needed for the structure to generate the M_1 phases of the synchronised hit signal, as shown in Fig. 25, in which some of the delay cells have two inputs as a load. Leaving the other output floating has a negligible effect on the propagation delay of the other branch.

The gate-to-channel capacitance (moscap) decreases nonlinearly as the gate-to-source voltage approaches the threshold voltage of the nmos transistor, which explains the difference between the slopes of the nodes load_cap7 and load_cap8 loaded with seven and eight ideal and moscap capacitors, as shown in Fig. 22. However, the output of the inverter following the capacitively loaded node, q7 and q8 in Fig. 22, changes its state before the nonlinear region is reached and the nonlinearity of the capacitor is negligible.

In addition to scaling the capacitive load (Chapman *et al.* 1995, Bazes *et al.* 1996, Geannopoulos & Dai 1998, Andreani *et al.* 1999) another way to realise the delay difference between logic gates with high resolution is to use scaled current starving transistors to control the pull-up and pull-down strength of the delay cells (Dunning *et al.* 1995). It would also be possible to use so called phase blenders to generate new signal phases between existing signals (Sidiropoulos & Horowitz 1997, Garlepp *et al.* 1999, Weinlader *et al.* 2000). Schmitt trigger gates with scalable logic threshold voltage (Minami *et al.* 2000) and passive integrated RC-delay lines (Gogaert & Steyaert 1995, Mota & Christiansen 1999, Mota *et al.* 2000) have also been used.

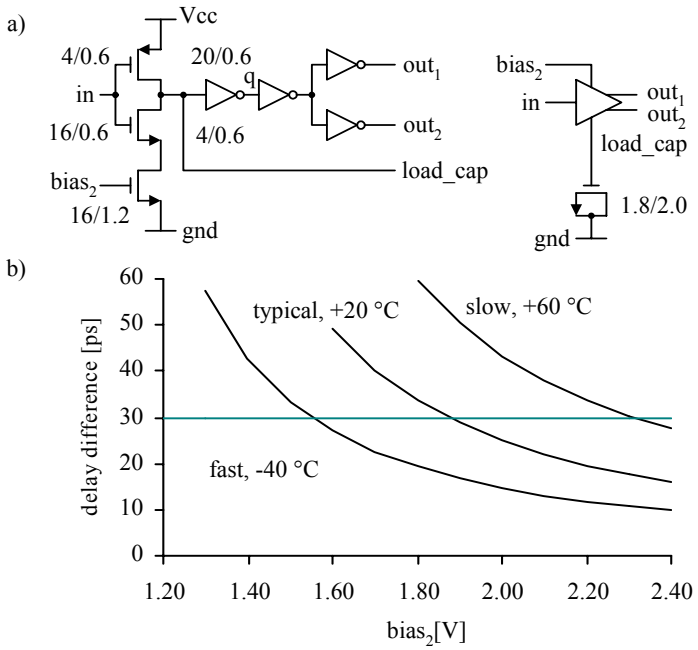

Fig. 21. a) Schematic diagram of the fine delay cell and b) propagation delay difference between the fine delay cells as a function of bias voltage.

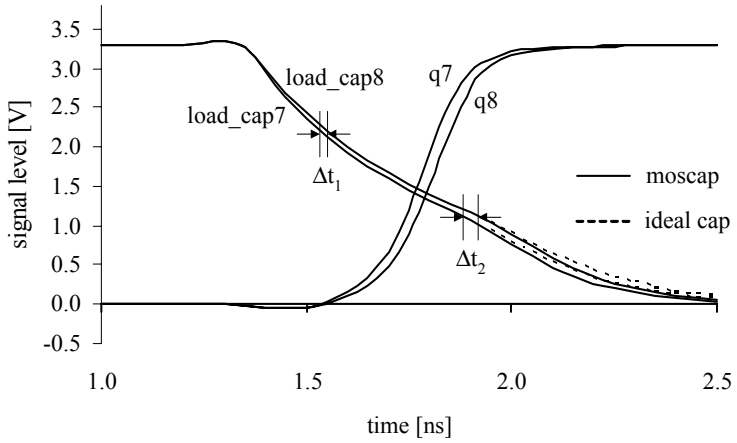

Fig. 22. Nonlinearity of the moscap capacitor and the delay difference depending on the logic threshold.

The M_2 phases of the asynchronous hit signal can be generated with eight delay cells sharing a common input signal. The first delay cell has one capacitor as a load, the second one has two and the last one has eight load capacitances, as shown in Fig. 23. The delay difference between the adjacent delay cells equals one LSB in the stabilised operating point. There is no cumulative nonlinearity with parallel delay cells with a common input as opposed to the delay-locked delay line of Fig. 18 with delay cells connected in series. However, the slope of the capacitively loaded node slows down as the load capacitance is increased. At the same time the propagation delay of the following inverter increases, which partly compensates for the reduced delay difference. Fig. 24 shows the simulated behaviour of 8-, 16- and 32-tap parallel delay generators. The dynamic range of the different structures has been adjusted so that the delay difference between delay cells with 1 and 9 load capacitances equals $T_{CLK}/16/4 = 237$ ps, the delay difference between delay cells with 1 and 17 delay cells equals $T_{CLK}/16/2 = 473$ ps and the delay difference between delay cells with 1 and 33 delay cells equals $T_{CLK}/16 = 947$ ps.

The delay difference between adjacent delay cells decreases systematically as the number of load capacitors is increased, as seen in the differential nonlinearity (DNL) plot of Fig. 24 a), which leads to the systematic integral nonlinearity (INL) shown in Fig. 24 b). The systematic INL of the 32-tap structure is about one third of an LSB. From the nonlinearity point of view the 16-tap structure would be feasible. However, the number of M_2 phases with the delay difference of an LSB was limited to eight to restrict the dynamic range and thus the nonlinearity of the structure and also to reduce the number of delay cells and load capacitances. The 32-tap structure requires 528 capacitors and the 16-tap requires 136 capacitors, whereas the 8-tap structure requires only 36 capacitors, which decreases the layout area required by the capacitances and simplifies the layout design.

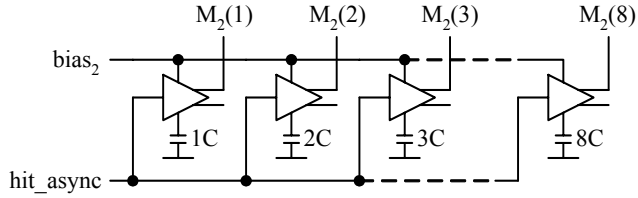

Fig. 23. Structure to generate M_2 signals with a delay difference of an LSB.

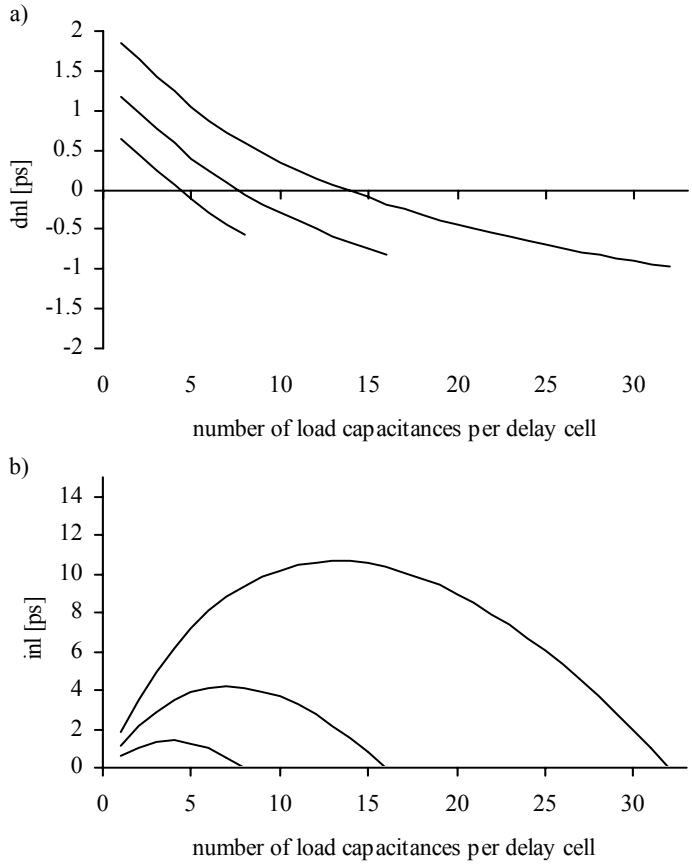

Fig. 24. Simulated a) differential and b) integral nonlinearities of 8-, 16- and 32-tap capacitively loaded delay generators.

The M_1 phases of the synchronised signal with a nominal delay difference of $T_{CLK}/16/4=237$ ps are generated with the structure shown in Fig. 25 by utilising the delay difference between the different propagation paths (Moyer *et al.* 1996). Also here the target resolution is better than the attainable propagation delay of a logic gate. The first delay cell provides a reference waveform to the subsequent delay cells. The delay difference between the different propagation paths is scaled with load capacitances. Each of the subsequent propagation paths has eight load capacitances more than the previous one. The delay difference between the adjacent outputs is thus eight LSBs in the stabilised operating point. The simulated delay difference provided by the structure of Fig. 25 is shown in Fig. 26 with the delay difference between the first and second outputs. The error in the delay difference between the adjacent outputs of Fig. 25 was simulated to be < 1 ps, which causes negligible systematic integral nonlinearity.

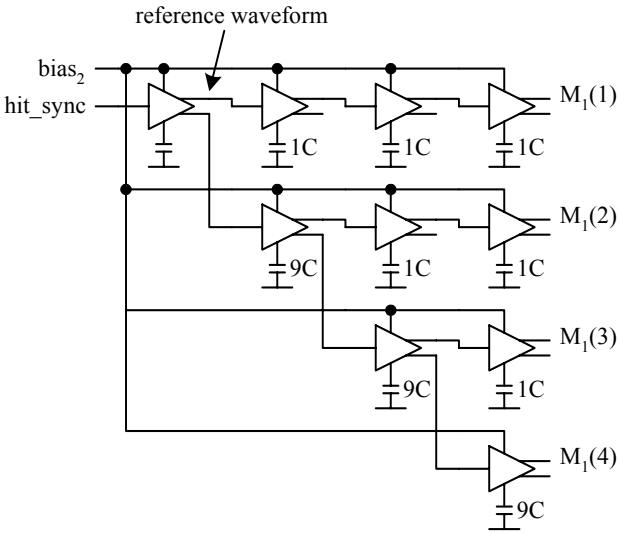

Fig. 25. Structure to generate M_1 signals with a delay difference of eight LSBs.

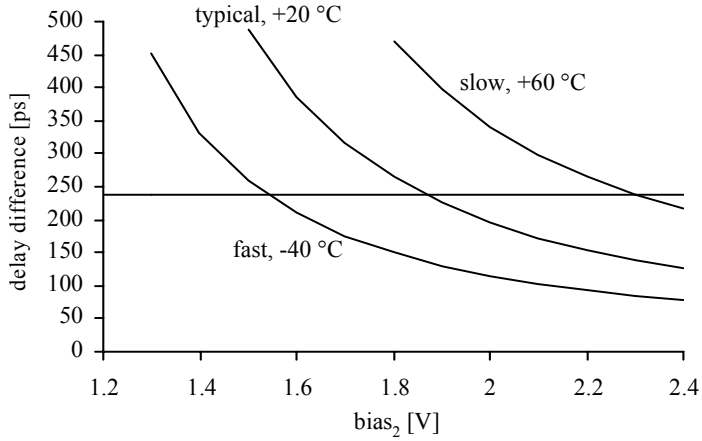

Fig. 26. Propagation delay difference between the M_1 outputs as a function of bias voltage.

The fine interpolator structures used for time interval digitising are not controlled in a closed loop as is done in the coarse DLL_1. Stabilising the fine delay structures relies on matching between the delay cells of the fine interpolation reference (DLL_2) and the fine interpolators. The maximum delay variance appears at the end of the fine interpolator structures with the variance of $N\sigma_2^2$, where σ_2 is the standard deviation between the propagation delays of the fine delay cells and N is the number of delay cells connected in

series (Toifl *et al.* 1999). The standard deviation of the propagation delays of the fine delay cells was simulated to be 1.5 ps with one load capacitance and 2.4 ps with nine load capacitances. The expected standard deviation of the propagation delay of the delay cells of the parallel structure generating the M_2 phases of the asynchronous hit signals with a resolution of an LSB is σ_2 because N is one. The worst case standard deviation of the propagation delay between the delay cells with seven and eight load capacitances is < 4 ps.

There are four delay cells in series in the structure generating the four M_1 phases of the synchronous signal, as seen in Fig. 25. The biggest difference is between the first ($M_1(1)$) and the last ($M_1(4)$) branches. As the branches share a common reference, the number of delay cells in each branch is three. The standard deviation of the propagation delays of the first and the last branches are $\sim\sqrt{3}\cdot 1.5$ ps ≈ 2.6 ps and $\sim\sqrt{3}\cdot 2.4 \approx 4.2$ ps, respectively. The expected maximum standard deviation between the propagation delays of the delays of these two branches is < 5 ps.

The expected maximum timing error of the interpolation due to random variation is less than half an LSB when the expected maximum INL of <10 ps of the coarse DLL_1 is combined with the standard deviation of the propagation delays of the fine interpolator structures.

4.5 Offset compensation

The synchronisation offset needed in the logic generating the residue for the fine interpolator equals $8\cdot T_{CLK}/16$ which was implemented with eight delay cells identical to those used in the coarse DLL_1 and adjusted with the same bias voltage. The propagation delay difference between the structures to generate the M_1 synchronised and M_2 asynchronous signals of the fine interpolation residue was compensated for by adding three fine delay cells to the propagation paths of the asynchronous signals. Also any other difference of logic gates between the synchronous and asynchronous propagation paths was compensated for by adding dummy logic gates so that any logic gate that was specific to one path was also added to the other path.

The propagation delay paths can be matched to a certain degree by design, but due to the device mismatch caused by variation of the process parameters the delay difference between the apparently similar paths can vary notably, at least compared to the sought-after resolution of ~30 ps of the TDC. Therefore, in addition to carefully matching the two propagation delays with identical signal paths, an external control was added to enable calibration of the propagation delays to minimise any offset error.

The variation of the propagation delays of the offset delay paths between the measurement channels on the same chip due to process variation can be compensated for by digital control. Each delay cell in the prototype TDC contains a one bit register that controls the additional load capacitance connected to the delay cell. The gate of an nmos transistor is connected as a capacitive load to a delay cell and the source and drain are connected to the output of a control register. In this way the propagation delay of each delay cell can be adjusted by ~10 ps by controlling the value of the load capacitance with the control data of the register (Bazes *et al.* 1996). In addition, adjustable delay cells with

external analogue control voltages (offset_ctrl$_1$, offset_ctrl$_2$ in Fig. 17) were added to both the synchronous and asynchronous propagation paths of the fine interpolators to be on the safe side if the dynamic range of the digital control appears to be insufficient. The delay cells with external bias voltages provide a common control to all measurement channels. These can also be used to compensate for the differences between the TDC chips from different process runs. However, TDCs from the same process run can use the same analogue offset control voltages.

The offset can be adjusted during a one-time calibration in which the number of hits to the bins of the fine interpolators, i.e. a histogram, is collected. With an ideal offset between the asynchronous and synchronous propagation paths of the fine interpolator the number of hits to each bin of the fine interpolator should be identical if the interpolators are otherwise ideal. If there is error in the offset, the number of hits to the bins of the fine interpolator is no longer uniform, rather there are more hits collected to one end of the interpolator. At the same time there are hits missing from the other end of the interpolator. This information can be used for adjusting the offset.

The effect of the offset error on the single-shot precision of the TDC can be calculated by determining the INL of the interpolator with an offset error. This INL represents the error caused by nonlinearity, and the standard deviation of the INL values of the interpolator defines the effect the nonlinear interpolator has on the single-shot precision.

Fig. 27 shows the effect of the offset error only on the single-shot precision of the TDC implemented in this work. With the LSB of ~30 ps the ideal single-shot precision set by the quantisation error is ~12 ps. The lower curve presents the effect of the offset error if both the start and stop signals are assumed to have equal offset errors. As seen in Fig. 27, an offset error of one LSB in both measurement channels deteriorates the total rms single-shot precision only by ~2 ps. The INL caused by the offset error also causes a systematic offset error in the measurement results, which can be calibrated if it remains constant.

The register used for storing the coincidence between the asynchronous and synchronous signals in the fine interpolator must have zero setup and hold times, i.e. the register must operate as an arbiter that detects which of the inputs to the register arrived first. Therefore an SR-latch composed of two cross-coupled NAND-gates was used (Rabaey *et al.* 2003). A register with non-zero timing margins would produce an offset drifting as a function of temperature.

In the first prototype TDC with two-stage interpolation the dynamic range of the fine interpolation equalled two units of the coarse DLL (Mäntyniemi *et al.* 2000). The offset was compensated for by careful design. Only half of the 16 phases of the hit signal in the fine interpolator were used for the actual time digitisation. The rest of the signal phases were used for compensating for the propagation delay drift and random variation in the synchronous and asynchronous propagation paths. The benefit of that structure was that the offset did not need to be calibrated. However, the drawback was that effectively one bit of resolution was lost for the compensation compared to a situation in which the dynamic range of the same number of delay cells equals one timing unit of the coarse DLL. The measurement results of the first prototype showed that the drift of the propagation delays between the synchronous and asynchronous signal paths was only ~20 ps in the temperature range of -40 to +60 °C. This led to the idea of utilising all the

delay cells for reaching a higher resolution by adjusting the offset during initial calibration.

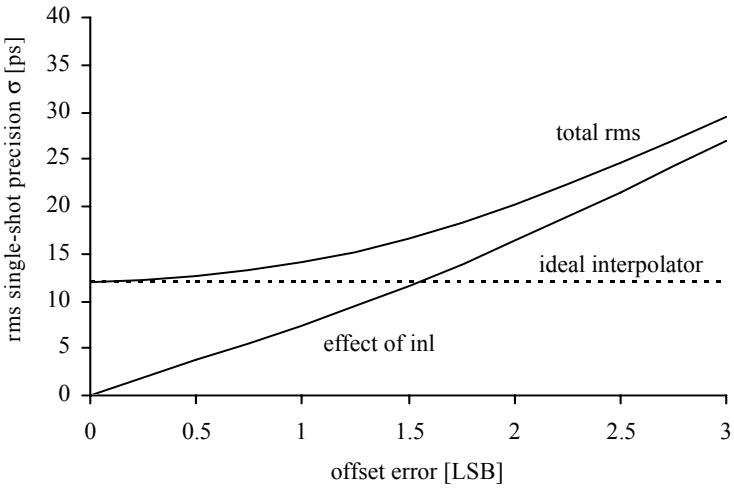

Fig. 27. The effect of the offset error of the fine interpolator on the rms single-shot precision.

4.6 Fine interpolation reference DLL_2

The delay line structures of the fine interpolator use one to nine load capacitances to scale the delay difference between the delay cells so that the delay difference between the delay cells with one and nine load capacitances equals $T_{CLK}/16/4 = 8 \cdot LSB$. However, the delay difference between the reference signals available from the coarse DLL_1 is $T_{CLK}/16$, i.e. 32 LSBs. Therefore the fine reference structure shown in Fig. 28 is used. Four pairs of delay cells with one and nine load capacitances are connected in series to realise a delay difference of 32 LSBs in the locked operating point. Also due to the nonlinear characteristics of the capacitively scaled delay cells the fine reference should use about the same number of capacitances as loads as are used in the fine interpolator structures to minimise systematic errors. The delay cells in the reference delay line are identical to those used in the fine interpolator.

In the locked operating point there is a delay difference of $T_{clk}/16$ between the input signals. The reference signal arriving first ($fine\_ref_1$) is connected to the slower reference delay line and the reference signal arriving later ($fine\_ref_2$) is connected to the faster reference delay line. As the bias voltage, $bias_2$ in Fig. 28, of the reference delay lines is adjusted so that the outputs of the delay lines are in phase, the propagation delay difference scaled by 32 capacitors is $T_{clk}/16 = 947$ ps with a nominal clock frequency of 66 MHz. The simulated delay difference of the two propagation paths of the fine interpolation reference as a function of the bias voltage is shown in Fig. 29. The gate-to-

channel capacitance of an nmos transistor is used as the loop filter with a capacitance of ~100 pF.

The fine interpolation reference only provides the bias voltage for the fine interpolator structures. The timing signals generated by this block are not used for digitising. Therefore, the update rate of the bias voltage can be slower than the reference clock frequency to save power. In the prototype TDC the fine interpolator bias voltage is updated, i.e. the fine interpolation reference delay lines are activated at every fourth clock cycle.

Also the fine interpolation reference suffers from device mismatch. Using a single pair of signals from the delay-locked delay line of the first interpolator as a reference is not an optimal solution for locking the delay of the fine interpolation delay cells. There could well be an offset in the reference signal pair due to the random mismatch of the delay cells and power supply noise, which would lead to a false adjustment of the dynamic range of the fine interpolators. Also the propagation delay mismatch between the two propagation delay paths of the fine interpolation reference can cause offset in the bias voltage of the fine interpolator. The digital control of the propagation delay of the delay cells can be used for improving the matching between the propagation paths.

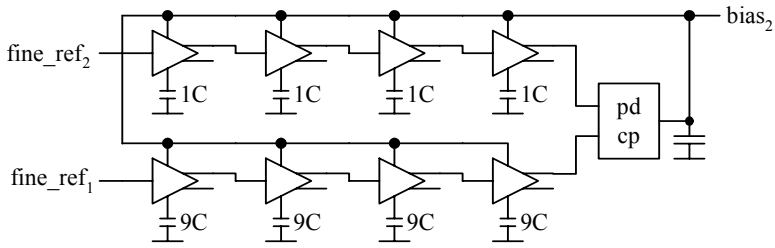

Fig. 28. Schematic diagram of the fine interpolation reference DLL_2.

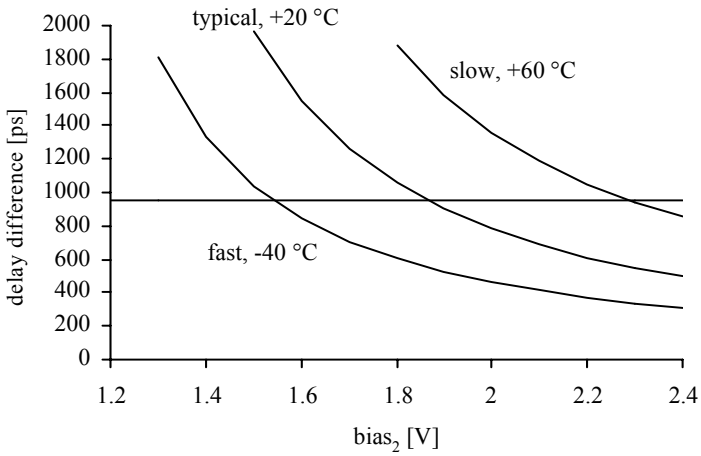

Fig. 29. Propagation delay difference between the reference delay lines as a function of bias voltage.

4.7 Calibration of the integral nonlinearity of the interpolators

The effect of the integral nonlinearity of the delay line interpolators on the single-shot precision of a TDC can be reduced by utilising delay adjustment structures, which allow individual control of the propagation delay of the delay cells. The bias voltage of each delay cell not only follows the common control voltage set by the stabilising loop but also in each delay cell the voltage can be tuned to reach a better matching (Abaskharoun & Roberts 2001, Park *et al.* 2001, Wu & Black 2001). The adjustment of a single delay cell can also be done by controlling the load capacitances of the delay cells (Mota & Christiansen 1999, Mota *et al.* 2000, Fanucci *et al.* 2001) or by scaling the current starving strength of the delay cell (Weinlader *et al.* 2000). The propagation delay change to the delay line caused by an adjustment made to a single delay cell is corrected by the stabilising loop so that the overall delay of the delay line equals the clock period.

If the nonlinearity characteristics of the interpolators are known, they can be used for improving the single-shot precision (Kalisz *et al.* 1994, Pelka *et al.* 1997, Bigongiari *et al.* 1999, Baronti *et al.* 2001). For example, the INLs of the interpolators are stored in a look-up table (LUT) that represents the error of the interpolation in each LSB of the interpolators. Each measurement result is then corrected using the INL-LUT (Mäntyniemi *et al.* 2002b). The correction table can be collected during a one-time calibration cycle in which a large number of measurements with hit signals asynchronous with respect to the reference clock are made (Kalisz *et al.* 1987). The hits to each LSB are collected and the INL of the interpolators is calculated and the INL-LUT is stored.

To make the nonlinearity correction efficient and practical it would be preferable if a single correction table could be used for a circuit in any ambient temperature without having to measure the operating conditions or readjusting the correction parameters. The requirement to be able to use a single correction table is that the characteristics of the interpolators are virtually constant over the whole temperature range. This can be adequately guaranteed if the interpolation is based on stabilised delay lines and the propagation delays of the signal paths in the interpolators are controlled and kept equal regardless of the operating temperature, i.e. the gain and offset of the interpolators must remain constant. The effect of the INL-LUT correction is presented with measurement results in section 5.4.

If stabilising is not used in the interpolators, additional delay cells must be included in the interpolators to allow for the drift caused by the random variation of the delay cells and the propagation delay change due to changes in the operating temperature. As the temperature changes, also the delay cells used for interpolation and consequently the INLs of the interpolators change. Thus, a correction table collected in one temperature becomes inefficient if there is a significant change in temperature (Szplet *et al.* 2000). This problem could be minimised e.g. by adaptive calibration if the operation conditions change (Kalisz *et al.* 1994).

In addition to limiting the single-shot precision, the INL of the interpolators result as constant offset error to the averaged results. The magnitude of this systematic error is the difference between the mean values of the INLs of the start and stop interpolators. As the offset error does not depend on the measured time interval it also does not have an effect on the linearity of the measurement, only on the accuracy (Kalisz *et al.* 1987, Rahkonen 1993). However, if the nonlinearity of the interpolators changes as a function of temperature it also makes the offset error drift, deteriorates the stability of the TDC and makes the measurement accuracy dependent on temperature. This can happen if the dynamic range of the interpolators is not locked to the reference clock cycle, rather the dynamic range of the interpolators is larger than the clock cycle with room for temperature drift, as is done e.g. with analogue TACs. Also the nonlinearity of a single flip-flop synchroniser, explained in section 3.6.1, is a function of temperature. Therefore, a single flip-flop synchroniser should not be used for generating the residue for interpolation. The use of stabilised delay lines automatically stabilises the interpolators and reduces the offset drift.

4.8 Option for single channel multihit operation

The prototype TDC has two operating modes. It can either be used as a multi-channel TDC with a common start and nine independent stop channels or as a single-channel multihit TDC with ten hits in a single measurement channel with a typical double-pulse resolution of 2 ns. The multihit operation mode was custom designed for a fibre-optic time-of-flight radar for the measurement of integral strain (Lyöri *et al.* 2003).

In the multihit operation mode all measurement channels are utilised for measuring the arrival times of the rising edges of a pulse train. A mode select logic, shown in Fig. 30, distributes the hit signals to the measurement channels. In the multi-channel mode

(mode=0) the multiplexers select the start signal hit flip-flop to enable all stop channels, thus preventing the stop signals from appearing before the start signal. In the multihit mode (mode=1) the arrival moment of the first rising edge of the pulse train is measured in the start channel and each following pulse after that is treated as a stop pulse one by one, as shown in Fig. 31. The start signal enables only the first stop channel, which in turn enables the next stop channel and so on. The double-pulse resolution of 2 ns is limited by the propagation delays of the flip-flop and multiplexer and the setup time of the flip-flop.

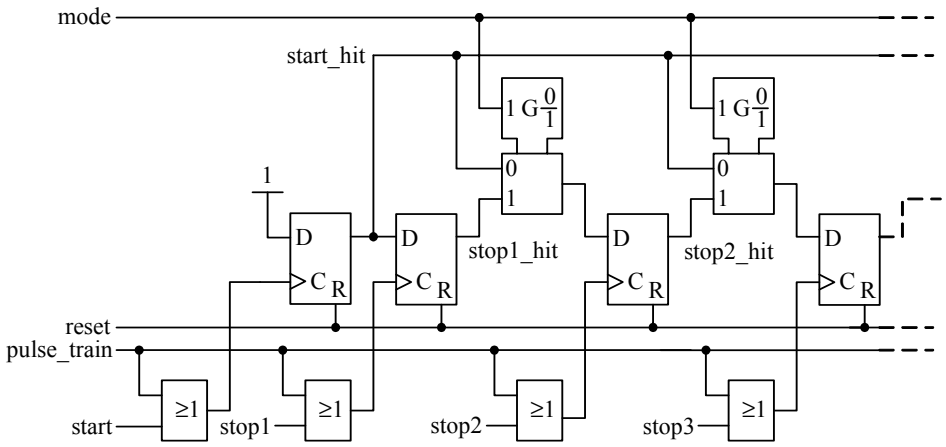

Fig. 30. Logic diagram of the mode select logic.

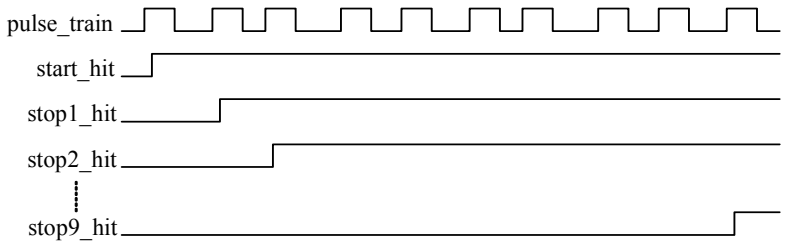

Fig. 31. Timing diagram of the mode select logic with multihit operation.

4.9 Layout of the prototype TDC

The prototype TDC was fabricated in a 0.6 μm single-poly, double metal digital CMOS process. The photomicrograph of the chip is presented in Fig. 32. The layout area is 3.5x3.9 mm including pads. The DLLs, the interpolation structures for each hit signal and

the digital logic including the counter and registers storing the state of the counter were each provided with their own separate power supply pads to reduce crosstalk between different functional blocks and measurement channels, and especially to isolate the DLLs from the digital blocks. A total of 32 of the 68 pads are used for the power supply and 4 pads are used for external bias signals.

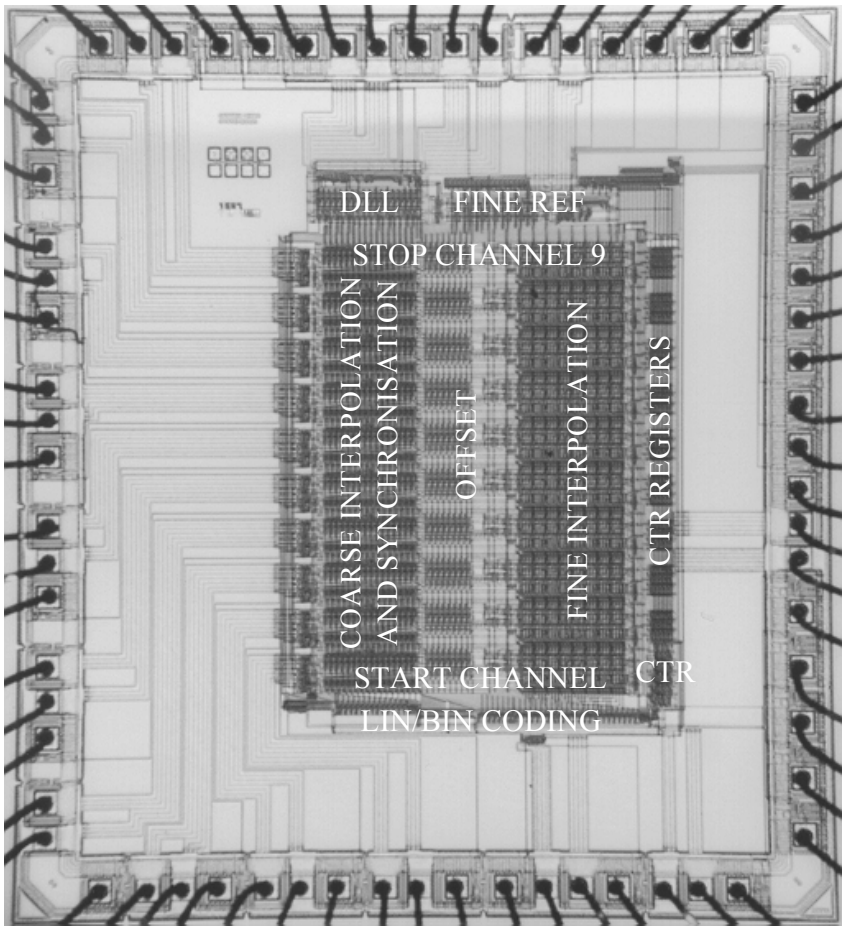

Fig. 32. Photomicrograph of the TDC prototype chip.

5 Measured results

5.1 Measurement setup

The performance of the prototype TDC was characterised with measurements. Initial measurements with a TDC in a ceramic CLCC-68(J)-package, shown in Fig. 33 a), installed into a socket showed that the power supply noise caused by the long bonding wires and the leads of the package and the socket limited the attainable single-shot precision. Therefore, the measurements were conducted with a hybrid printed circuit board (PCB) in which the TDC chip is bonded directly onto the PCB to minimise the parasitic inductances of the package and to locate the power supply bypass capacitors closer to the chip, as shown in Fig. 33 b). The size of the hybrid is 28·28 mm.

The functionality of the TDC was checked with the power supply voltages of 2.7 - 5.0 V and with reference clock frequencies from 40 - 80 MHz. The initial measurements showed that the single-shot precision saturates to ~15 ps with the reference clock frequency of 66 MHz. The measurements characterising the performance were carried out with 3.3 V power supply and clock frequency of 66 MHz also to limit the power consumption and power supply noise. A Marconi Instruments 2024 signal generator was used as the reference clock source. The rms jitter of the reference clock was measured to be ~5 ps. With the clock frequency of 66 MHz the nominal unit delay of the delay cells of the coarse DLL_1 is ~947 ps, the delay difference between the M_1 phases of the synchronised signals of the fine interpolator is ~237 ps and the delay difference between M_2 phases of the asynchronous hit signals setting the LSB resolution of the TDC is ~29.6 ps.

The hit signals, i.e. start and stops, were asynchronous with respect to the reference clock and 3.3 V CMOS signal levels were used for the hit signals. The offsets of the delay paths of the fine interpolators were adjusted at +20 °C. The measurements were controlled with a Labview software running in a portable PC. The measurement rate was limited to ~1.6 kHz by the execution speed of the software. The time intervals to be measured were generated using an Avtech AVPP1-C pulse generator, a power splitter and coaxial cables and coaxial cable switch boxes. The typical rms jitter of the measured time intervals combining the rms jitter of the start and stop signals was measured to be ~5 ps.

a) b)

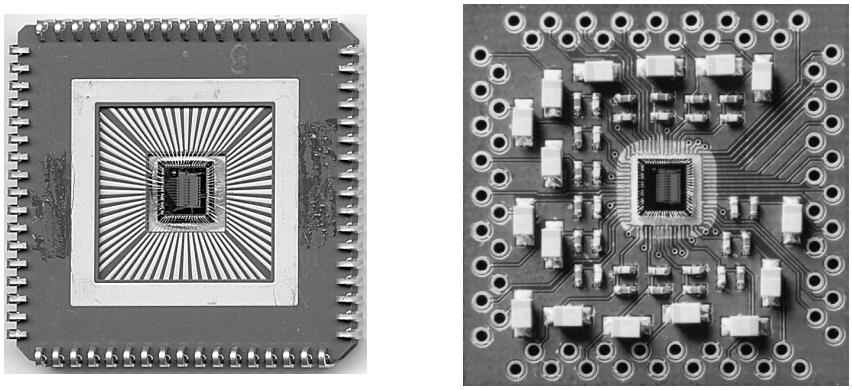

Fig. 33. Photograph of the TDC a) in CLCC-package and b) in hybrid.

5.2 Performance characteristics

The performance of the prototype TDC is summarised in Table 1. The nonlinearity of the interpolators, single-shot precision without crosstalk and linearity error are explained in more detail in the following chapters.

The maximum measured temperature drift of the hybrid and the twenty engineering samples in CLCC-packages was ~20 ps in the temperature range of -40 °C to +60 °C. Any delay difference between the propagation paths of the start and stop hit signals drifts as a function of temperature. Also any change in the mean values of the INLs of the interpolators as a function of temperature changes the measurement result. The use of the INL-LUT causes a constant offset in the measurement results but has no effect on the temperature stability.

The worst-case crosstalk error between the measurement channels was determined by measuring a constant time interval in one stop channel while the time interval of the other eight stop channels was swept over the constant delay. The maximum measurement error caused by crosstalk was 150 ps peak-to-peak and the worst case single-shot precision 85 ps. The crosstalk error is mainly caused by the change in the bias voltage of the coarse DLL_1 due to crosstalk through the bias nmos transistors of the delay cells of the offset delay paths as the hit signals propagate in the offset delay cells. The other error mechanism is the change of the load the coarse DLL_1 sees when the latches storing the state of the DLL_1 are clocked by the hit signals. When the latches are clocked with the hit signals, the input capacitance of the latches changes and there is delay offset in the buffered outputs of the coarse delay cells.

The crosstalk error could be reduced by increasing the loop filter capacitance and by isolating the bias voltages of different measurement channels by buffering the bias

voltages. Also buffering should be used between the outputs of the DLL_1 and the inputs of the latches of the measurement channels.

Table 1. Performance characteristics.

Parameter	Value
Technology	0.6 µm CMOS (single poly, double metal)
Layout area, including pads	3.5 · 3.9 mm
Power supply voltage	3.3 V
Reference clock frequency	66 MHz
Typical power consumption	50 mW
LSB resolution	29.59 ps
Measurement range	496 µs
Measurement channels	1 start + 9 stops
Single-shot precision w/o crosstalk @ -40 °C	min 19.6 ps, max 34.5 ps, rms 29.9 ps
Single-shot precision w/o crosstalk @ +20 °C	min 16.7 ps, max 32.9 ps, rms 28.8 ps
Single-shot precision w/o crosstalk @ +60 °C	min 20.1 ps, max 34.8 ps, rms 30.7 ps
Single-shot precision w/o crosstalk @ -40 °C, INL-LUT	min 16.9 ps, max 20.9 ps, rms 19.9 ps
Single-shot precision w/o crosstalk @ +20 °C, INL-LUT	min 15.0 ps, max 16.9 ps, rms 16.2 ps
Single-shot precision w/o crosstalk @ +60 °C, INL-LUT	min 16.6 ps, max 19.5 ps, rms 18.4 ps
Worst-case single-shot precision with crosstalk	85 ps
Worst-case error due to crosstalk	150 ps p-p
Linearity error without crosstalk, 5 ns < T_{meas} ≤ 20 ns	± 20 ps
Linearity error without crosstalk, T_{meas} > 20 ns	± 6 ps
Temperature drift	< 0.2 ps/°C

5.3 Nonlinearity of the interpolators

The nonlinearity characteristics of the interpolators were determined with the statistical code density test in which ten million asynchronous hits to the bins of the interpolators were collected.

Fig. 34 a) shows the INLs of the 16-bin coarse interpolators of the start channel and one stop channel. The INLs are almost identical because a common delay-locked delay line is used in the coarse interpolation in each measurement channel. The differences come from the random variation of the timing parameters of the registers storing the state of the delay line. Fig. 34 b) shows the INL of the coarse interpolator of the start channel at temperatures of -40 °C, +20 °C and +60 °C. The offset of the INL is a function of temperature, whereas the shape of the INL remains almost constant.

The standard deviation of the DNLs of the coarse interpolators of the hybrid TDC is ~13 ps, i.e. the matching between the delay cells is ~1.4%, which is more than double compared to the Monte Carlo simulations. The standard deviations of the coarse interpolators of TDCs in a CLCC-package were ~25 ps, which indicate that the power supply noise was the main reason for the worse matching.

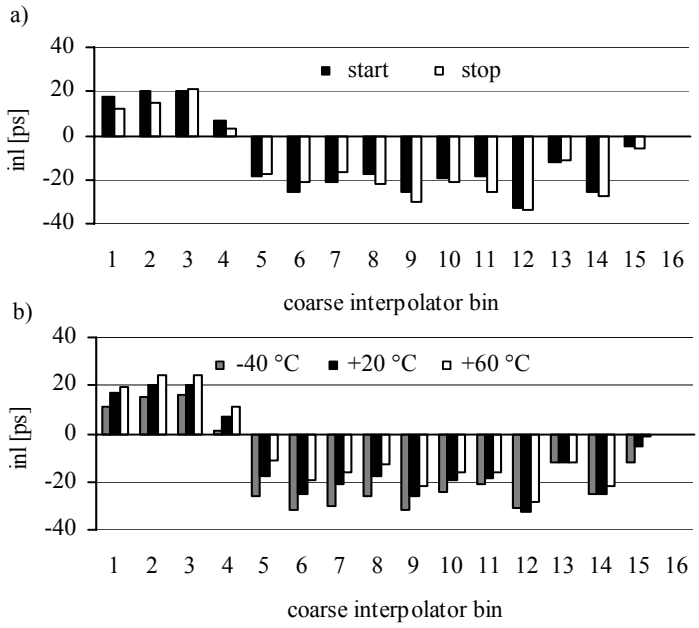

Fig. 34. a) INLs of the start and stop coarse interpolators and b) INL of the start coarse interpolator at temperatures of -40 °C, +20 °C and +60 °C.

Fig. 35 a) shows the DNLs of the 32-bin fine interpolators of the start channel and one stop channel. The two DNLs are different because separate delay line structures perform the fine interpolation in each measurement channel. The standard deviations of the DNLs of the fine interpolators are ~5 ps. Fig. 35 b) shows the DNL of the fine interpolator of the start channel at temperatures of -40 °C, +20 °C and +60 °C. The distribution of the hits to the fine interpolator moves as a function of temperature. The changes are apparent in the first and last bins of the interpolator, whereas the change of the widths of the other bins is negligible. The main reason is that the offset between the two delay paths of the fine interpolator drifts as a function of temperature. This causes offset to the INL of the fine interpolators, as seen in Fig. 35 c).

Fig. 36 a) presents the DNL of the 512-bin combined interpolator of the start channel as an example. The DNL exceeds the LSB of ~30 ps indicating that there are missing codes. The standard deviation of the DNL is ~8 ps. Fig. 36 b) shows the INLs of the combined 512-bin interpolators of the start channel and one stop channel. The shape of the INL of the 32-bin fine interpolator repeats itself sixteen times in the INL of the combined interpolator because the same fine interpolator is used for interpolating between the phases of the 16-tap coarse delay line interpolator. The INLs of the start and stop interpolators are different, but follow the same trend set by the common coarse interpolator. Fig. 36 c) shows the INL of the start channel at temperatures of -40 °C, +20 °C and +60 °C. The shapes of the three curves are practically identical, whereas the

offset, i.e. the mean value of the INLs, changes as a function of temperature. The difference between the mean values of the start and stop interpolators changes ~15 ps in the temperature range of 100 °C. This is the main source of temperature drift in the measurement results. The INLs exceed ±LSB and will limit the attainable single-shot precision.

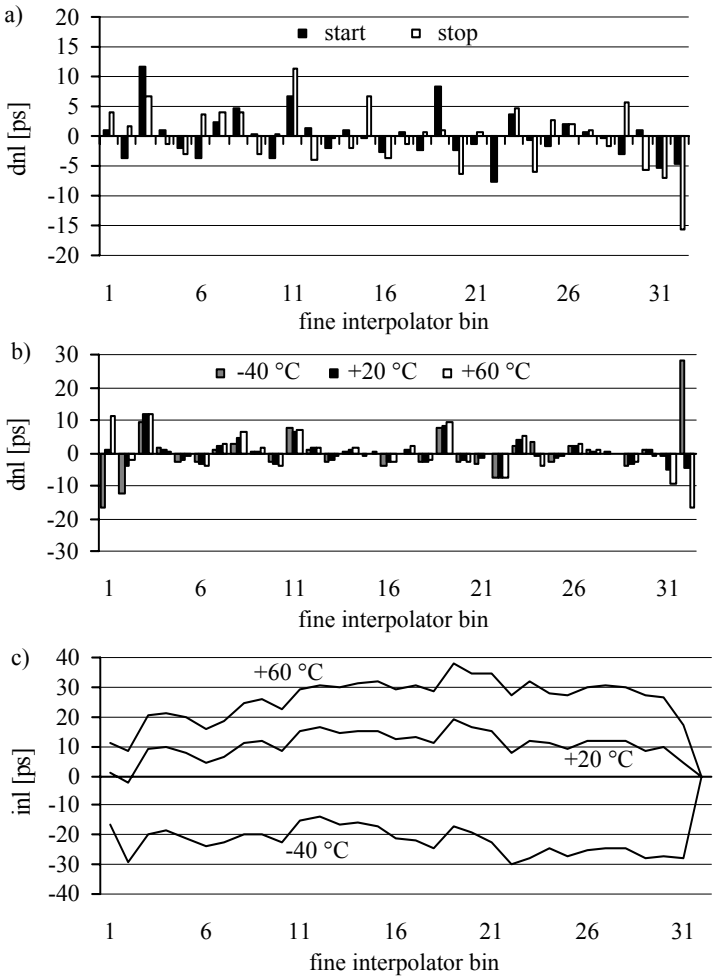

Fig. 35. a) DNLs of the fine interpolators of the start and one stop channel b) DNLs of the start fine interpolator at temperatures of -40 °C, +20 °C and +60 °C c) INLs of the start fine interpolator at temperatures of -40 °C, +20 °C and +60 °C.

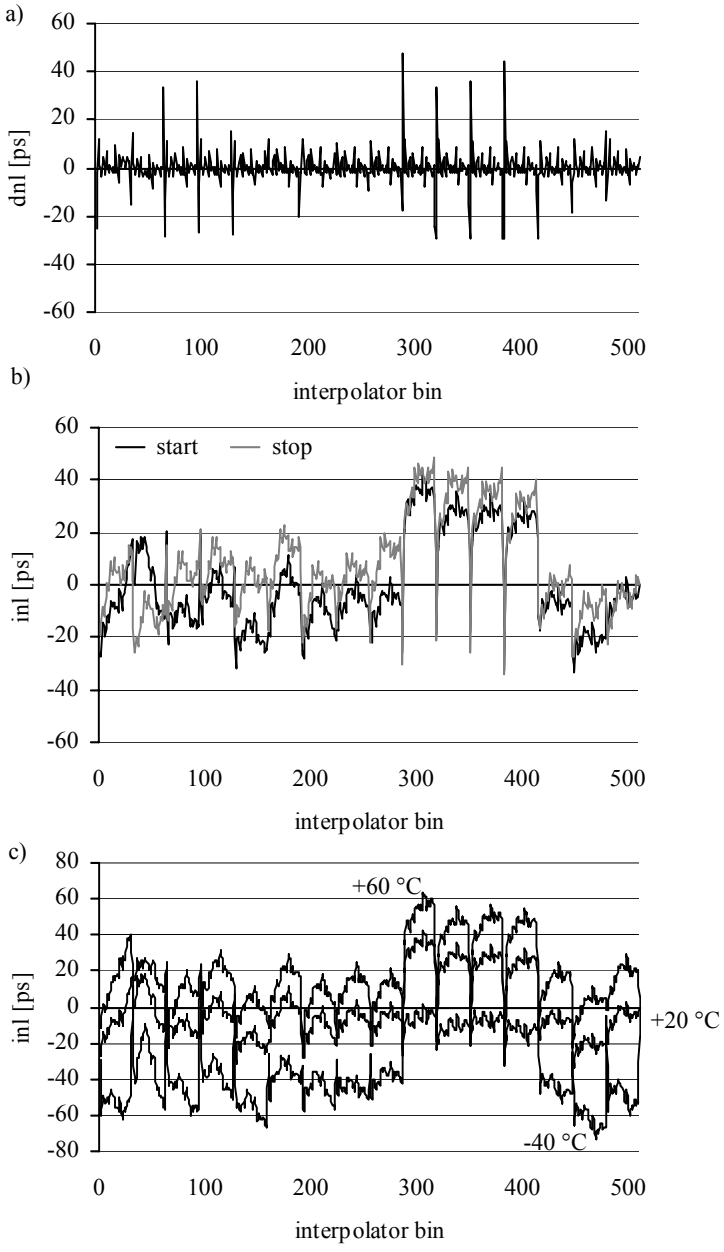

Fig. 36. a) DNL of the 512-bin combined interpolator of the start channel b) INLs of the 512-bin combined interpolators of the start and one stop channel and c) INLs of the 512-bin combined start interpolator at temperatures of -40 °C, +20 °C and +60 °C.

5.4 Single-shot precision without crosstalk

The INLs of the start and stop channels can be used to estimate the single-shot precision of the TDC. The standard deviations of the INLs represent the typical measurement errors due to the INL of the interpolators. The maximum difference between the values of the INLs of the interpolators of the start and stop channels sets the maximum interpolation error due to the INL in a single measurement. The rms single-shot precision σ_{rms} of a TDC based on a counter and interpolation, with the measured time intervals extending over one clock period, can be estimated with

$$\sigma_{rms} = \sqrt{\sigma_q^{\,2} + \sigma_{st}^{\,2} + \sigma_{sp}^{\,2} + \sigma_{clk}^{\,2} + \sigma_{tdc}^{\,2} + \sigma_{stinl}^{\,2} + \sigma_{spinl}^{\,2}}\,, \tag{2}$$

where σ_q is the rms quantisation error, σ_{st} and σ_{sp} are the rms jitter of the start (st) and stop (sp) signals, σ_{clk} is the rms jitter of reference clock, σ_{tdc} is the inherent rms jitter of the signals within the TDC, and σ_{stinl} and σ_{spinl} are the standard deviations of the INLs of the start (stinl) and stop (spinl) interpolators. For example, the standard deviation of the INL of the start channel is 17.7 ps and 17.5 ps in one stop channel of the hybrid TDC at the temperature of +20 °C. Therefore, the total expected rms single-shot precision including the rms quantisation error of 12.08 ps of the ideal TDC with an LSB of 29.6 ps can be estimated to be 27.7 ps without the jitter being taken into account.

Fig. 37 presents the calculated single-shot precision of the TDC as a function of the measured time interval. The measured time interval is swept over one clock cycle in the calculation and a calculated time interval measurement is performed with all possible combinations of the start and stop interpolation values. The single-shot precision for each time interval measurement result is then calculated. The rms single-shot precision is equal to the predicted value of 27.7 ps. The single-shot precision reaches the minimum when the time interval is a multiple of the reference clock cycle. In that case the difference between the INLs of the start and stop interpolators is the smallest, as seen in Fig. 36 b). The offset in the time interval to clock cycle ratio was selected to match the measurement results shown in Fig. 38. The single-shot precision curve is cyclic and repeats itself with the cycle of the reference clock (Kalisz *et al.* 1987).

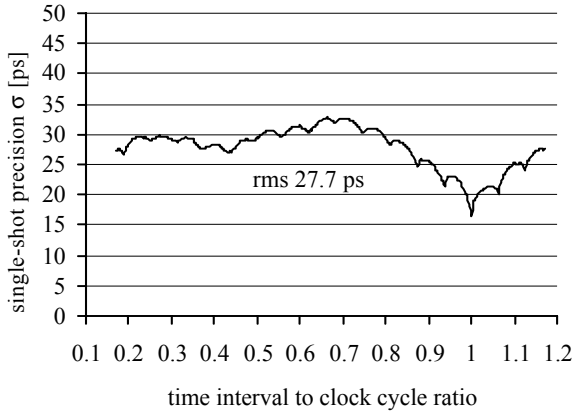

Fig. 37. Calculated variation of the single-shot precision as a function of time interval to clock cycle ratio.

The single-shot precision was measured with time intervals spanning over one cycle of the reference clock. The measured time interval was stepped over one clock cycle with steps of ~250 ps using a Canberra 2058 coaxial cable switch box with 500 ps delay resolution and an additional 250 ps delay cable. 10,000 single-shot measurements were averaged to each result to reduce statistical variation. The measured single-shot precision as a function time interval to clock cycle ratio is presented in Fig. 38 with and without the INL look-up table (INL-LUT) correction. Without the INL correction the single-shot precision sigma varies between 18.4 - 34.8 ps depending on the measured time interval and the temperature. This variation has a cycle of the period of the reference clock and is clearly caused by the INL of the interpolators, as can be seen by comparing Fig. 38 to Fig. 37. The best single-shot precision was measured when the time interval was a multiple of a clock cycle. The rms single-shot precision is 28.8 ps at +20 °C, 30.7 ps at +60 °C and 29.9 ps at -40 °C. The single-shot precision is slightly worse at -40 °C and at +60 °C because the offsets of the fine interpolator structures have been calibrated at +20 °C. The difference between the calculated and measured rms single-shot precision is ~1.1 ps at +20 °C. This is caused by the combined rms jitter of <10 ps of the hit signals, reference clock and the TDC itself. When the INLs of the interpolators measured at the temperature of +20 °C are utilised as a correction INL-LUT to minimise the errors caused by the nonlinearities of the interpolators (σ_{stinl} and σ_{spinl} in equation (2)), the single-shot precision is < 21 ps with rms values of 16.2 ps at +20 °C, 18.4 ps at +60 °C and 19.9 ps at -40 °C. The best possible single-shot precision of 15 ps was determined by adjusting the measured time interval to be an exact multiple of the cycle of the reference clock.

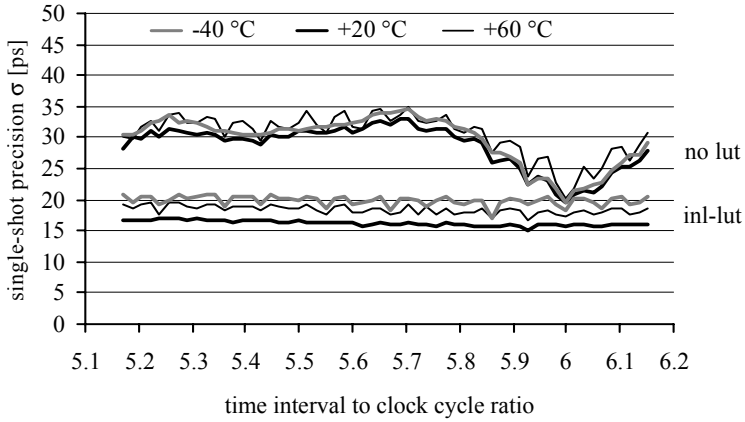

Fig. 38. Measured single-shot precision at temperatures of -40 °C, +20 °C and +60 °C as a function of time interval to clock cycle ratio.

5.5 Linearity error without crosstalk

The linearity of the prototype TDC was measured over periods of 5 ns - 25 ns with a time step of 200 ps and from 10 ns to 1000 ns with a step of 10 ns. Stanford Research DG535 delay generator was used as a time interval source. The results were verified using a TDC made of discrete components (Määttä *et al.* 1988). That TDC has a typical single-shot precision of 30 ps and good linearity determined in a laser rangefinding system. 10,000 single-shot measurements were averaged to each result to reduce statistical variation. With short input time intervals of less than 25 ns the linearity error is about ± 20 ps, as seen in Fig. 39 a). With longer time intervals the linearity error is ± 6 ps, as seen in Fig. 39 b). The nonlinearity measurement results include the nonlinearity of the reference TDC and the statistical variation of the measurement results of the two TDCs. Also here the reason for the nonlinearity is likely the change in the bias voltages and the change in the load seen by the coarse DLL_1 after the start signal has arrived.

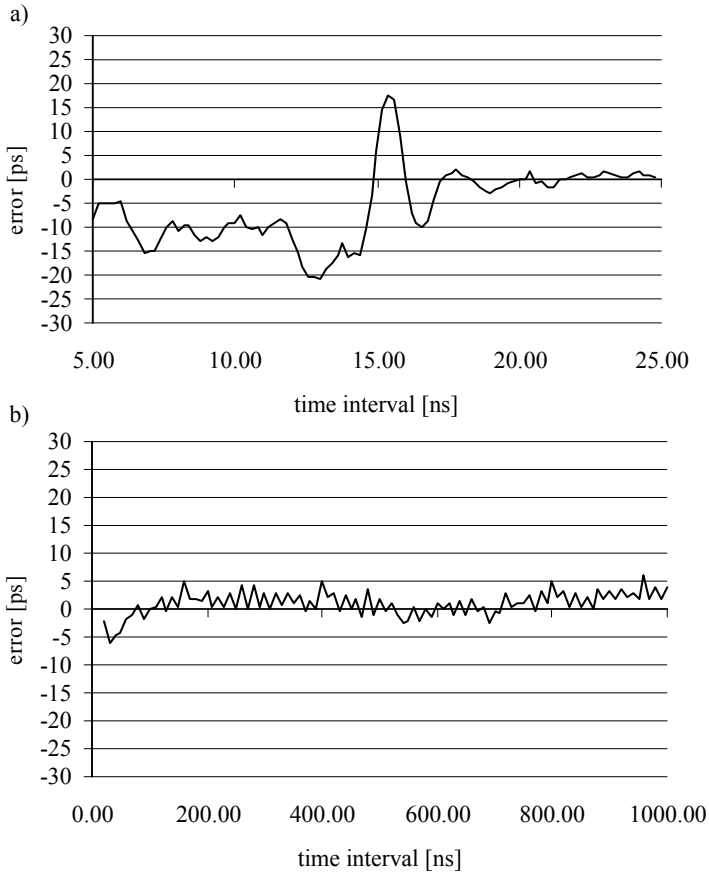

Fig. 39. Linearity error with a) short and b) long time intervals.

6 Discussion

The result of this work is an architecture that enables the realisation of multi-channel time interval measurement system with ps-level resolution as an integrated circuit. The architecture was verified with a prototype TDC with ten measurement channels implemented in a low-cost 0.6 µm single-poly, double metal digital CMOS process. The measurements of the prototype showed that low power consumption and picosecond level resolution are reachable simultaneously with an integrated TDC. In the following both the architecture and performance of the prototype TDC developed in this work are compared to other published TDCs with a comparable resolution.

6.1 Comparison of architectures

Table 2 summarises integrated high resolution TDCs from the architecture point of view. The reference clock frequency, interpolation ratio, LSB resolution, the number of delay cells and registers needed to reach the interpolation ratio, and an estimate of the conversion time are included in the comparison. If the number of delay cells or registers is dependent on the number of measurement channels, the variable N is included in the formulas.

Three of the presented TDCs directly measure the delay difference between the start and stop hit signals (Chen *et al.* 2000, Dudek *et al.* 2000, Karadamoglou *et al.* 2004). Additional synchronisers with two flip-flops for each hit signal would be needed to generate the residues to be interpolated if the Nutt method was to be applied with these three architectures. Also the offset of a clock cycle of the residue should be compensated for by using propagation delay paths with the length of a clock cycle. The other TDCs, including the TDC developed in this work, apply the Nutt method and use flash delay line interpolators to resolve the delay difference between the hit signals and the edges of the reference clock signal, which leads to shorter conversion time.

Two of the earlier presented TDCs reached a higher interpolation ratio than the number of delay cells used by utilising both edges of the reference clock (Gorbics *et al.* 1997) or by using the propagation delay of an inverter as the timing unit (Braun *et al.*

1999, Fischer *et al.* 2002). The TDC by Chen *et al.* (2000) based on cyclic pulse shrinking has a compact architecture but suffers from the long conversion time.

The architecture developed in this work makes it possible to reach a high interpolation ratio and thus high LSB resolution while using a relatively low reference clock frequency. The three-stage interpolation method utilising the edges of the multiphase clock provided by the stabilised delay line substantially reduces the number of registers because a single fine interpolation structure in each measurement channel can be used for digitising the arrival moment of the hit signal within any of the phases of the multiphase clock. Only 64 registers in each measurement channel are needed to reach the interpolation ratio of 512. The fact that dedicated delay cells are needed in each measurement channel for the fine interpolation increases the number of delay cells compared, for example, to the TDC by Gorbics *et al.* (1997). However, only 16 delay cells in the DLL_1 are active all the time, whereas the delay cells needed in the fine interpolators are activated only when the hit signals arrive. The other architectures that can cope with a smaller number of delay cells require a much higher reference clock frequency or more registers to reach the same LSB resolution.

Table 2. Comparison of architectures with N-channel TDCs.

Circuit	Clock freq [MHz]	Interpol. ratio	LSB [ps]	Delay cells	Registers	Conversion time
Gorbics *et al.* 1997	166.66 uses both edges	128	46.9	64	N·64	~T_{clk}
Mota & Christiansen 1998	80	140	89.3	140+28	N·140	~T_{clk}
Braun *et al.* 1999, Fischer *et al.* 2002	202.43	76	65	19+N·2	N·38	~T_{clk}
Dudek *et al.* 2000	260	128	30	N·2·128 + offset delay	N·128	> T_{clk}
Chen *et al.* 2000	No reference clock used	200	68	N·43 + offset delay	N·8	>>> T_{clk}
Mota *et al.* 2000	320	128	24.4	32+N·4	N·128	~T_{clk}
Karadamoglou *et al.* 2004	10	2048	48.8	N·2048 + offset delay	N·2048	>> T_{clk}
This work	66	512	29.59	16+N(18+11)[a] = 16+N·29	N·(16+16+32)[b] = N·64	~T_{clk}

a) coarse DLL_1 16, fine interpolators 10+8, offset compensation 8+3=11.

b) multiphase clock synchroniser 16+16, fine interpolator 32.

6.2 Comparison of performance

Table 3 summarises integrated high resolution TDCs from the performance point of view. In addition to the TDC examples compared in the previous chapter, six other TDCs are included. The TDC by Knotts *et al.* (1994) reaches a state-of-the-art resolution with bipolar technology but suffers from high power consumption. The TDC by Mota & Christiansen (1999) introduced the use of RC-delay lines but does not contain a counter to expand the dynamic range. Räisänen-Ruotsalainen *et al.* (2000) use BiCMOS technology to implement a TDC with a counter and TACs. The use of a CMOS FPGA device is demonstrated by Szplet *et al.* (2000). The TDC by Tisa *et al.* (2003) uses the cyclic pulse shrinking delay line introduced by Chen *et al.* (2000). Nissinen *et al.* (2003) have a counter and a free running ring oscillator implemented using CMOS technology. The processing technology, clock frequency, LSB resolution, the best measured rms single-shot precision, measurement range, number of measurement channels, power consumption per measurement channel and chip area are compared. The features included in different TDCs can differ. Some TDCs have special buffering for fast readout of data, etc. The measurement rate at which the circuits were tested can be different. However, the comparison gives an idea of the differences between the performance characteristics of the TDCs.

A moderate line width CMOS technology was used for implementing the prototype TDC in this work. The clock frequency of the TDC of this work is one of the lowest and the LSB resolution is one of the best. These result from the high interpolation ratio enabled by the three-stage interpolation method developed in this work. The measurement range of the TDCs based on the Nutt method using a counter and interpolation is typically on the microsecond level, whereas the TDCs without a counter reach a dynamic range of a few dozen nanoseconds.

The power consumption per measurement channel of the TDC developed in this work is only a fraction of the other TDCs based on the Nutt method with delay line interpolation. The power consumption is dominated by the coarse DLL_1. As the DLL_1 is shared with multiple measurement channels, the power consumption per channel is reduced. The fine interpolation structures providing the high resolution are activated only when the hit signals arrive, which reduces the power consumption. The rms single-shot precision of 29 ps is clearly limited by the integral nonlinearity of the interpolators, as expected. However, the extensive use of delay-locked delay lines makes the interpolation structures very stable. Therefore the rms single-shot precision could be improved to < 20 ps by using a single correction look-up table (LUT) collected at room temperature during a one-time calibration cycle.

Owing to the extensive use of stabilised delay lines in the interpolation the maximum measured temperature drift of the prototype TDCs is 0.2 ps/°C, which is e.g. one fourth of the temperature drift of an integrated analogue realisation (Räisänen-Ruotsalainen *et al.* 2000). The worst case single-shot precision of 85 ps and the 150 ps peak-to-peak measurement error of the prototype TDC of this work caused by crosstalk need to be improved to reach the same performance regardless of the arrival moment of the hit signals in the other measurement channels. For comparison, a four channel TDC based on an array of delay-locked delay lines with 89.9 ps resolution has a maximum crosstalk

error of ±179 ps (Mota & Christiansen 1998) and the single-shot precision of 22.4 ps is deteriorated to 166 ps due to crosstalk (Mota *et al.* 2000).

Table 3. Comparison of performance.

Circuit and architecture	Tech [µm]	Clock [MHz]	LSB [ps]	rms [ps]	Range [µs]	Meas chan	P/chan [mW]	Area [mm^2]
Knotts *et al.* 1994, counter and ring osc.	Bipolar	4000	15.6	±11[a]	0.016	1	5700	16
Gorbics *et al.* 1997, counter and delay line	0.8 CMOS	166.66 (333.3)	46.9	40	10	2	NA	NA
Mota & Christiansen 1998, counter and delay lines	0.7 CMOS	80	89.3	34.3[b]	3.2	4	200	23
Mota & Christiansen 1999, delay line	0.7 CMOS	160	48.8	21.5[b]	0.0063	2	110	10.7
Braun *et al.* 1999, Fischer *et al.* 2002, counter and ring osc.	0.6 CMOS	202.43	65	NA	4.2	4	125	NA
Räisänen-Ruotsalainen *et al.* 2000, counter and TAC	0.8 Bi-CMOS	100	32	<25	2.5	2	175	11.9
Chen *et al.* 2000, Cyclic pulse shrinking	0.35 CMOS	NA	68	54	0.016	1	1.2	0.032[c]
Dudek *et al.* 2000, vernier delay lines	0.7 CMOS	260	30	20	0.004	2	NA	10
Mota *et al.* 2000, counter and delay lines	0.25 CMOS	320	24.4	22.4	12.8	8	NA	42.25
Szplet *et al.* 2000, counter and vernier delay lines	CMOS FPGA	100	110	70[d]	45e6	2	70	NA
Nissinen *et al.* 2003, counter and ring osc.	0.35 CMOS	398	157	<78.5	2.57	2	36	NA
Tisa *et al.* 2003, cyclic pulse shrinking	0.8 CMOS	NA	20	76	0.018	1	NA	2
Karadamoglou *et al.* 2004, pulse shrinking	0.8 CMOS	10	48.8	NA	0.1	2	5	33.64
This work, counter and delay lines	0.6 CMOS	66	29.6	29 16[d]	496	10	5	14

a) peak-to-peak.

b) for one hit signal only.

c) only core excluding pads.

d) with INL-LUT.

7 Summary

The goal of this work was to develop a time-to-digital converter architecture with a high resolution, large dynamic range, low power consumption, fast conversion, automatic calibration, good stability, low cost and with feasibility for multi-channel implementation as an integrated circuit.

As the result, a new TDC architecture based on the Nutt method was developed. The number of full clock cycles of the measured time interval is determined with a synchronous counter. The fraction of the clock cycles between the hit signals and the edges of the reference clock are determined using the three-stage stabilised delay line interpolation method developed in this work. The developed architecture enables a high interpolation ratio, which reduces the number of delay cells and registers needed in the interpolation and makes it possible to integrate multiple measurement channels into a single chip even with a low-cost, moderate line width CMOS process. The efficient architecture also makes it possible to reach a high resolution with a relatively low reference clock frequency, which leads to low power consumption.

Two synchronisation methods were developed in this work to resolve the uncertainty related to the asynchronous hit signals with respect to the reference clock. The operation of the counter is controlled with a synchronising logic that is, in turn, controlled with the interpolation results. As a result, a single counter clocked with the reference clock can be used instead of either two counters with opposite clock phases and with two storage registers or a single counter running at twice the reference clock frequency.

Another synchronising logic makes it possible to synchronise the hit signals with multiphase time-interleaved clock signals as if the synchronising was done with a GHz-level clock. This makes it possible to reduce the dynamic range, power consumption and nonlinearities of the interpolators, and to use a single fine interpolator in each measurement channel.

The three-stage interpolation is based on nested stabilised delay lines. The first delay line is locked to the period of the reference clock. The remaining delay lines are locked to the reference provided by the first delay line. This leads to good stability and makes it possible to improve the single-shot precision with a look-up table (LUT) containing the integral nonlinearities (INL) of the interpolators. A one-time calibration has turned out to

be sufficient for collecting the INL-LUT that can be used regardless of the operating temperature.

The feasibility of the developed architecture was demonstrated with a ten-channel prototype TDC circuit implemented as a full-custom application specific integrated circuit (ASIC) in a 0.6 µm single-poly, double metal digital CMOS process. A high resolution of ~30 ps was reached with a relatively low reference clock frequency of 66 MHz due to the high interpolation ratio of 512. The state-of-the-art low power consumption of 50 mW or 5 mW per measurement channel results from the low clock frequency and the architecture in which the fine interpolation structures are activated, and thus consume power only when the hit signals arrive.

The rms single-shot precision of the prototype TDC is ~29 ps without crosstalk at room temperature. The single-shot precision is clearly limited by the INL of the interpolators. However, with the use of a single LUT containing the measured INLs of the interpolators the prototype TDC reaches a state-of-the-art rms single-shot precision of better than 20 ps regardless of the measured time interval or the measurement temperature in the temperature range of -40 °C to +60 °C.

Owing to the extensive use of stabilised delay lines in the interpolation the maximum measured temperature drift of the prototype TDCs is 0.2 ps/°C, which is markedly better than what has been reached with analogue realisations.

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