A 16ps-Resolution Random Equivalent Sampling Circuit for TDR Utilizing a Vernier Time Delay Generation

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Abstract-- **A Random Equivalent Sampling (RES) circuit that has 16ps sampling resolution has been developed for a high-resolution Time-Domain Reflectometer (TDR). The high-resolution TDR uses an expensive programmable delay chip or a complex Time-to-Digital Converter (TDC) circuit to capture the waveform with very fine time interval. The Vernier time delay generation technique using two crystal oscillators of slightly different frequency is proposed, which is simpler and more cost-effective and provides subpicosecond time resolution. One of the two clocks is used for the reference time to generate incident periodic pulses, and another clock is used for the sampling.**

The implemented RES circuit consists of the Vernier clock generator, the pulse generator and the control logic for pulse generation, interface and high-speed memory control. Using the ADC of relatively low sampling rate, the periodic pulse waveform is reconstructed with tens of GSPS high equivalent sampling rate by the repetitive sampling utilizing the incremental Vernier time delay.

The performance of RES circuit is measured through the operation of TDR. The resolution of the RES circuit is 16.8ps equal to 59.5GSPS sampling rate, which means that the signal waveform in the 66.7%VOP RG58C/U cable can be sampled by 1.6mm interval.

I. Introduction

RANDOM Equivalent Sampling (RES) method is one of the equivalent sampling methods to achieve a high-speed sampling. RES circuits are used in devices that should obtain the waveform of the periodic signal with the subpicosecond interval. The resolution and accuracy of RES circuits are very important for instrument devices that require the high sampling rate, such as a Digital Storage Oscilloscope (DSO) or a Time Domain Reflectometer (TDR). Especially, in the case of TDR, the performance of RES circuits determines the horizontal resolution of TDR, which determines the fault location of circuits like opens and shorts and measures the characteristic impedance of transmission lines accurately. For example, RES circuits should be able to obtain the waveform of the incident and reflected pulse signal with at least 10ps interval to determine the location of opens and shorts with 1mm distance because the velocity of propagation (VOP) in transmission lines is about 66.7% of the velocity of light (3×10^8m/s).

There are several methods to realize high-speed RES circuits: the method using a programmable delay chip and the method using a TDC circuit. A digitally programmable delay has a 10ps incremental delay resolution at the minimum 2.5ns full-scale range [7]. Although the resolution is very fine enough to obtain 1mm horizontal resolution, 2.5ns full-scale range limits the horizontal measurement range of only 250mm transmission line. Moreover, more delay chips and additional sequential logic circuits are required in order to extend the measurement range. TDCs can measure very short time interval because they have high resolution from tens of ps to hundreds of ps [1], [2]. However, a lot of analog components are required for the implementation and time-consuming tuning process is required for the reliable performance.

RES circuits should have tens of ps sampling resolution for a submillimeter horizontal resolution of TDR. Therefore, the real-time sampling using only high-speed ADC cannot be applied to the TDR because the sampling rate of the fastest high-speed ADC produced currently is 1.5GSPS that can sample the analog signal with 667ps interval [8]. The methods above are mostly used to capture periodic signal with very fine interval utilizing the equivalent sampling method. However, they are complex and expensive for the realization, and have disadvantages that explained above. We present cost-effective and higher performance method to implement RES circuits.

The RES circuit presented in this paper utilizes an analog delay scheme named a *Vernier time delay generation technique* for TDR. This scheme uses two clocks with slightly different frequencies. The time difference between two clocks makes it possible to generate very fine time delay between the sampling time and the signal reference time. The Vernier method can achieve theoretically very high resolution below 1ps and more cost-effective than the other methods.

Because the designed horizontal resolution of TDR is 16.8ps for submillimeter determination, the RES circuit with 16ps sampling interval was implemented with the presented method. We made Vernier clock generator circuit for generating fine time delay, control logic for the periodic pulse generation and fast memory control, and pulse generator circuit for steep pulse edge and driving long cable with high bandwidth.

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The construction and performance characteristics of the RES circuit and TDR with very high resolution are presented in this paper. The principles of operation utilizing a Vernier time delay generation technique and random equivalent sampling method are presented in Section II, a detailed circuit description of the individual stages is presented in Section III, and a discussion on the performance testing of RES circuit is presented in Section IV.

II. PRINCIPLES OF OPERATION

A. Random equivalent sampling

The sampling process converts a signal waveform into discrete electrical values for the purpose of the storage, processing and display, etc. Especially for instrument devices such as TDR and DSO, the very fast and precise sampling is indispensably required for their reliable performance. According to the Nyquist sampling theorem, a sampling rate should be at least twice as higher as a signal bandwidth to reconstruct the signal waveform accurately by interpolation and to avoid aliasing. In mathematical terms of the Nyquist sampling theorem, $f_s \geq 2f_c$ where f_s is the sampling rate and f_c is the signal bandwidth (the highest frequency contained in the signal).

There are two kinds of mostly used sampling methods: the real-time sampling method and the equivalent sampling method [3], [5]. The real-time sampling is required in most high-speed designs to capture nonperiodic and random events occurred over a single time window. To capture a nonperiodic signal as numerously as possible for capturing instant events, an ADC should have large bandwidth and high sampling rate. For example, if we want to capture random instant events of 1GHz bandwidth, a high-speed ADC must operate with at least 2 GSPS sampling rate. As the event bandwidth becomes larger, the required sampling rate should be faster.

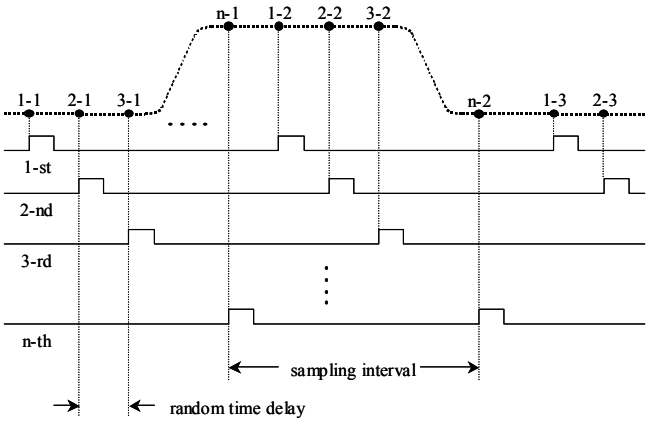

Figure 1. Random equivalent sampling method

Although currently used CMOS technology is able to make high-speed flash ADC, the maximum sampling rate is up to 1.5GSPS [8]. That is too slow to capture events with subpicosecond interval. Therefore, the real-time sampling method cannot be applied for a TDR of submillimeter horizontal resolution.

The equivalent sampling method overcomes the limitation of sampling resolution by piecing together samples from different timing of a periodic waveform. The sample points are taken at slightly different time intervals so that sufficiently dense points are obtained to reconstruct the waveform adequately as shown in Figure 1. This method can achieve tens or hundreds of times faster sampling rate for the periodic signal than the real-time sampling. In addition, even using and relatively low-speed ADC can obtain high sampling rate [2].

There are various methods to realize high-speed RES circuits such as using a programmable delay chip and using a TDC circuit. The method using a programmable delay chip or a TDC circuit is mostly used to implement equivalent sampling circuits with very fine interval. AD9501, which is a digitally programmable 8bit delay device of Analog Devices, has a 10ps incremental delay resolution at the minimum 2.5ns full-scale range. Although the resolution is very fine enough to obtain 1mm horizontal resolution, 2.5ns full-scale range can realize measurement range of only 250mm transmission line. Moreover, more delay chips and additional sequential logic circuits are required in order to extend the measurement range.

TDCs using the pulse stretching method have 20ps resolution and those utilizing a Vernier delay line have 30ps to 250ps resolution [1], [2]. Although TDCs can measure very short time interval, their pulse stretching circuit consists of a lot of analog components and is tuned for the precise operation. Vernier delay line should be made to CMOS chip, so the flexibility is low. Above methods are complex and expensive, then we use the Vernier time delay generation technique, which overcomes above disadvantages and has higher resolution, to generate fine delay for RES circuits.

B. Vernier time delay generation

The Vernier principle can be understood by the Vernier calipers, which is the tool of measuring the fine physical length with two jaws that slide closed over an object to be measured. Two jaws have slightly different scale and we can measure the fine length according to the matching point that two scales meet exactly.

The Vernier time delay generation is the electrical application of the Vernier calipers. Using two oscillators with slightly different frequencies, we can generate the fine time delay that makes slightly different sampling points and realizes the fine measurements of the cable length and transmission line anomalies by acquiring more narrow samples.

$$k = \frac{T_1}{T_1 - T_2} = \frac{T_1}{\Delta T} = \frac{f_2}{f_2 - f_1} = \frac{f_2}{\Delta f} \qquad (1)$$

T_1 and T_2 are each periods of the lower oscillator and the higher. f_1 and f_1 are their frequencies. Their period difference ΔT added to the time difference of their rising edge every clock. The coincidence between rising edges of two clocks happens after every k clocks [6].

The timing diagram for Vernier time delay generation is illustrated in Figure 2. Two jaws of Vernier calipers are equal to two different clocks. 16.000312MHz clock is

reference of PULSE_OUT for generating pulse and 8.000000MHz is sampling clock to ADC. At the first rising edge of PULSE_OUT, Pulse waveform on the cable is sampled at the rising edge of 8.000000MHz clock. At the next pulse, the sampling position is delayed as the amount of the Vernier time delay about $10\times\Delta T$ in Figure 2. A set of samples delayed automatically is obtained every pulse generation. Samples at slightly different time are pieced together sequentially. Then, the reconstructed waveform that is similar to that sampled with very high-speed ADC of theoretically high sampling rate is obtained.

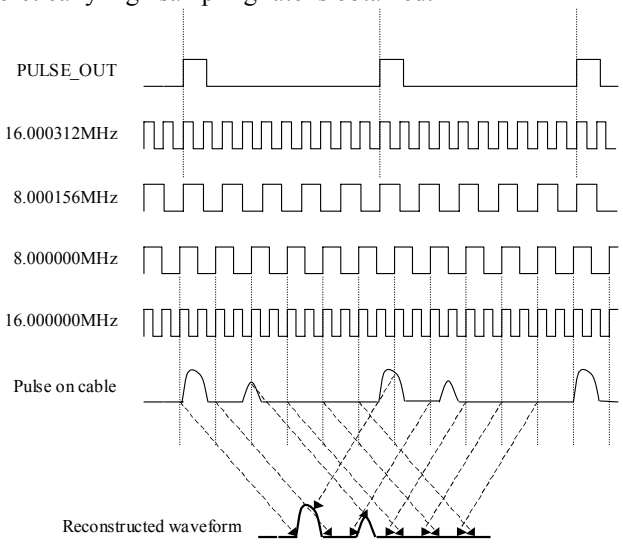

Figure 2. Timing diagram of Vernier time delay generation

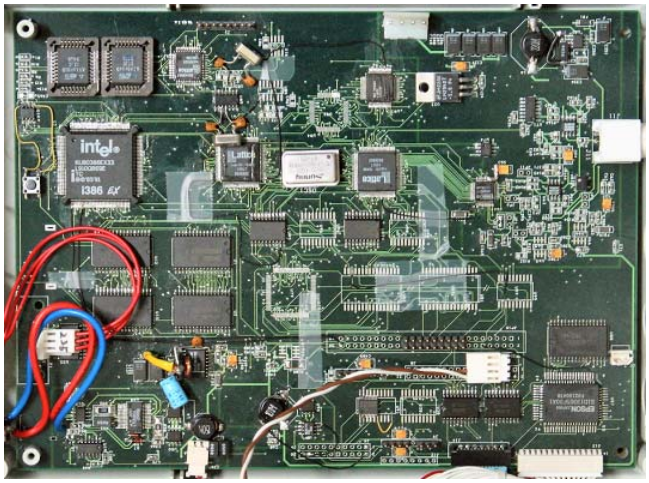

Figure 3. A photograph of the TDR board

III. CIRCUIT DESCRIPTION

The RES circuit is one pare of the TDR circuit that consists of Vernier clock generator, control logic and pulse generator. A photograph of the TDR developed is shown in Figure 3. Detailed descriptions of each stage will follow.

A. Vernier clock generator

The Vernier clock generator circuit generates two system clocks for pulse generating reference and sampling, which consists of two crystal oscillators and inverters. 16.000000MHz clock is used for sampling and logic operation and 16.000312MHz clock for pulse generating reference.

The commercial crystal oscillator pairs that have slightly different frequency and subpicosecond time differences are listed in Table I. It shows that the minimum time differences between two clocks are various as which crystal pairs of different frequency are selected. Time differences are all ones of ps and the third pair has remarkable 0.24ps time difference.

It is theoretically possible to make infinitely small time difference, if we can make the crystal frequency much close. The sampling resolution improved when the time difference is small. However, it has practical limitation to improve sampling resolution because the portion of uncertainty grows as the time difference becomes smaller. Uncertainty of the pairs are 50ppm and 2~6ps.

TABLE I
CRYSTAL OSCILLATOR PAIR

Crystal frequency	Period	Uncertainty	Difference
8.000000 MHz 8.000156 MHz	125000 ps 124997.56 ps	6.25 ps 6.25 ps	2.4 ps
16.000000 MHz 16.000312 MHz	62500 ps 62499.86 ps	3.125 ps 3.125 ps	1.2 ps
24.000000 MHz 24.000014 MHz	41666.66 ps 41666.42 ps	2.09 ps 2.09 ps	0.24 ps

According to Table I, the minimum time difference is smaller as the crystal frequency is faster. However, the time difference is not related to how fast the frequency of crystal is, but how long the periods of two crystals are different.

We determined the second pair crystal oscillators in consideration of sampling resolution, sampling rate of ADC and the speed of logic operation. For the case of our implementation, designed sampling resolution is 16.8ps, the speed of logic operation 10MHz or more and ADC has 10MSPS maximum sampling rate. The first pair is too slow for the logic operation and the third pair has excessively small time difference comparing to design specification.

The second pair satisfies the sampling resolution and operating speed. The 16.8ps sampling resolution is satisfied by 14 times 1.2ps time difference. Logic operates with 16MHz frequency and ADC with 8MSPS sampling rate.

B. Control logic

PLD performs as the control logic circuit for pulse generation, CPU interface and ADC and FIFO control. Each functional description will follow.

1) Pulse generation

Pulse generation part consists of a counter and a D-flipflop, which controls incident pulse timing and generate pulse signal for the pulse generator circuit.

In order to generate incident pulse periodically, control logic count pulse generating reference clock with the counter synchronized to 16.000312MHz as shown in Figure 4. If the internal start signal, SYNC1_START, is generated, counter starts. After all measurements TDC_END is generated, then pulse generation is stopped. When the counting number is 14, the PLD output pulse is generated. Because the output of D-

flipflop is connected to its CLR, it is reset after internal time delay. This makes very short pulse.

The output pulse after 14 clock has 16.8ps increment time delay with sampling clock. 14 clocks take 874.98ns, which is the time that the pulse propagates 87.5m through the cable. It is enough for the designed measurement range, 40m containing reverse propagating time.

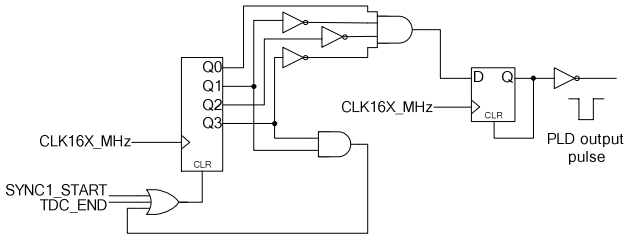

Figure 4. Schematic of pulse generation control logic

2) CPU interface

CPU is used for data processing and supervising entire operation of TDR. The data bus is shared with CPU, FIFO and ADC. The right to use the data bus should be controlled sequentially, otherwise data collision occurs.

The timing diagram of sequence to share data bus is described in Figure 5. When the measurements begin, START_IN signal goes low (A). PLD requests the bus right to CPU with low HOLD (B) and CPU acknowledges the request with low HLDA (C). Then, PLD gets the bus right and store the measured data from ADC to FIFO (C-D). When the measurements and the storing data process are complete, PLD generates high TDC_END and high HOLD signal (D). CPU gets the bus right again (E) and completes the measurements with high START_IN (F).

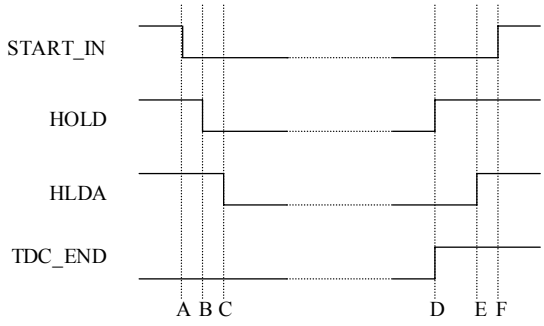

Figure 5. Timing diagram of bus sharing sequence

3) ADC and FIFO control

ADC and FIFO control part supervises write and read operation of the FIFO memory device and ADC output. The clock frequency of ADC is 8MHz dividing 16MHz clock with a T-flipflop. 8MHz clock is also used for the WCLK of FIFO. ADC output data passes 6 D-flipflops because ADC puts out valid data after 7 clocks.

FIFO_WEN signal for writing enable is generated every 14 clocks of 16MHz, which makes it possible not to rearrange sampling data in FIFO by storing one sample data during one pulse (14 clocks). Sampling time is sequentially delayed by the Vernier time difference equal to 14 clocks. Sampling data is stored from head to tail. Storing one sample per one pulse shot is faster than storing several samples because the rearrange process of CPU takes long time comparing to transfer data from FIFO to CPU.

C. Pulse generator

Pulse generator circuit is shown in the Figure 6, which consists of a Schmitt triggered inverter and current feedback amplifier. It operated with the function that load the pulse generated from the PLD to the cable after two signal conditioning stages of steep edge and cable driving.

Steep edge of the pulse is obtained through 74ACT14 Schmitt triggered inverter. ACT logic family has 1ns risetime and falltime according to the Motorola FACT Data DL138 Rev 3., so it can be enough to generate the steep rising edge with about 2ns and short pulsewidth. The PLD output pulse is negative pulse in order to utilize fast Schmitt trigger.

Amplifier stage with AD8009 current feedback amplifier drives capacitive loads with hundreds of MHz bandwidth pulse. Cable driving amplifier, AD8009 has about 5,500V/us slew rate and 440MHz large signal bandwidth at gain 2. It is enough to preserve the 2ns steep pulse with 4V amplitude.

According to the measurements, the pulse risetime was 2.03ns and the pulsewidth 3.44ns.

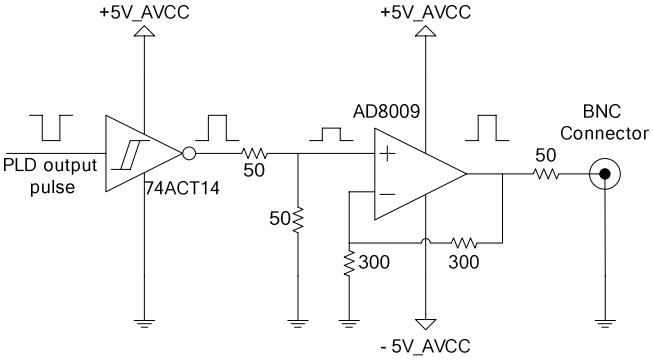

Figure 6. Schematic of pulse generator circuit

IV. PERFORMANCE

The performance of the RES circuit was obtained from TDR measurements because the implemented RES circuit is part of TDR. The horizontal resolution of TDR is equal to the sampling resolution of RES circuit. So we measure the cables with TDR and obtained the sampling interval.

We measured the RG58C/U coaxial cables of known-length and 66.7%VOP in order to verify the performance of the RES circuit. The length of cable is various from 2m to 40m and their terminations are open state. The incident pulse reflected at the fault location because of impedance mismatching. In the open state like our case, the incident pulse and reflected pulse have same positive voltage. Then we can obtain the length of cable by finding the starting points of two pulses. The number of points between two starting points represents the length of cable.

TABLE II
MEASUREMENTS RESULT

Cable length (m)	Incident pulse to reflected pulse (pt)	Distance per sample (mm)	Sampling time resolution (ps)
2.012	1274	1.5793	15.81
3.016	1813	1.6635	16.65
4.020	2448	1.6422	16.43
5.015	2996	1.6739	16.75
7.010	4395	1.5950	15.96
9.011	5517	1.6333	16.35
11.010	7106	1.5494	15.51
13.010	7842	1.6590	16.60
25.004	14950	1.6725	16.74
30.005	17890	1.6772	16.79
35.008	20757	1.6866	16.88
40.017	23661	1.6913	16.93
	Average	1.6436	**16.45**
	Standard deviation	0.0458	0.46

Table II represents the result of the experiment, which shows length of cable, the number of sample points between two pulse starts and sampling time resolution. Cable length presents the reference length of the RG58C/U cable. The incident pulse to the reflected pulse means the number of sampling points between incidents pulse and reflected pulse, which can be the length of cable. The distance per sample is obtained by dividing the cable length by the number of points between two pulses. Finally, the sampling time resolution is obtained from the distance per sample converted to the time that the pulse propagates through the cable of the distance per sample.

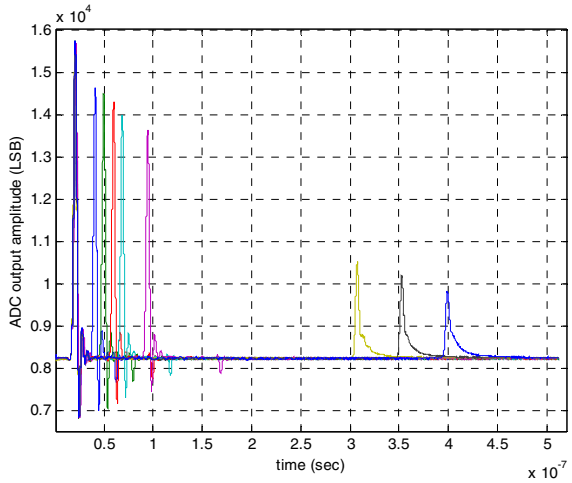

Figure 7. TDR waveforms of various length cables with incident pulse and reflected pulse

Sampling time resolution was 16.45ps that is matched with intended specification 16.8ps approximately. There exists some variation due to a kind of jitter or nonlinearity such as clock uncertainty and clock drift in relatively long duration. The real waveform of TDR is shown as Figure 7, which has waveforms of the eight different length cables, and Figure 8 that combined the reflected pulses arranged to the pulse starting point. As shown in Figure 8, the amplitude of the reflected pulse become smaller as the cable length is longer due to the cable nonlinearity like attenuation loss and nonuniform impedance.

The error due to the cable nonlinearity is compensated using software fitting. The detailed compensation methods will be introduced in the other study.

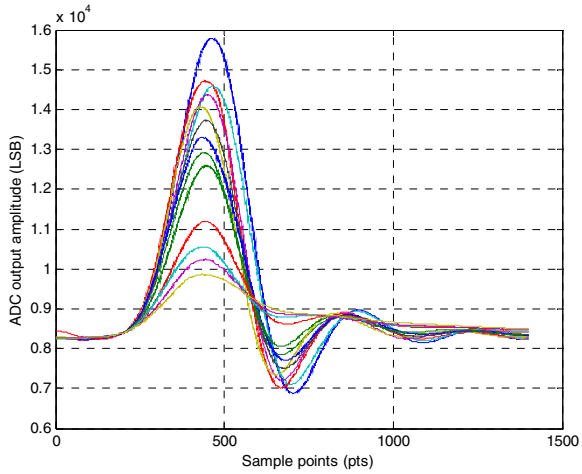

Figure 8. TDR waveforms of reflected pulses with various length cables arranged to the starting points.

V. Conclusion

We have implemented a Random equivalent sampling circuit utilizing Vernier time delay generation technique for the high-resolution TDR, which can sample waveform with 16.8ps interval equal to 59.5GSPS sampling rate. The circuit design and implementation were presented, and the performance of implemented circuit was measured.

VI. References

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