A Jitter Characterization System Using a Component-Invariant Vernier Delay Line

Antonio H. Chan, *Member, IEEE,* and Gordon W. Roberts, *Fellow, IEEE*

***Abstract*—Jitter characterization has become significantly more important for systems running at multigigahertz data rates. Time and frequency domain characterization of jitter is thus a crucial element for system specification testing. Time domain jitter measurement on a data signal with subgate timing resolution can be achieved using two delay chains feeding into the clock and datalines of a series of *D*-latches known as a Vernier delay line (VDL). An important drawback to the VDL structure is that its measurement accuracy depends on the matching of the various delay elements. Although careful layout techniques can help to minimize these mismatches, it cannot eliminate them completely. As well, due to the nature of the design, a relatively large silicon area is required for silicon implementation. In this paper, a novel technique is developed which reduces the silicon area requirements by two orders of magnitude, as well enables the measurement device to be synthesized from a register transfer level (RTL) description. A custom IC was designed and fabricated in a 0.18-μm CMOS process as a first proof of concept. The design requires a silicon area of 0.12 mm^2 and measured results indicate a timing resolution of 19 ps. The synthesizable nature of the design is demonstrated using an field-programmable gate-array implementation. As test time is an important consideration for a production test, an extension to the component-invariant VDL technique is provided that reduces test time at the expense of more hardware. Finally, a method for obtaining the frequency domain characteristics of the jitter using the VDL will also be given.**

***Index Terms*—Characterization, component-invariant, frequency, jitter, measurement, register transfer level (RTL), synthesizable, time, vernier delay line (VDL).**

I. Introduction

TIMING accuracy is an important criteria for high-speed data communication systems operating at multigigahertz data rates. An important loss of timing accuracy is attributed to noise coupling into the system from both on-chip and off-chip sources. These noise sources introduce uncertainty in the timing edge of the signal, known as jitter. Due to the statistical nature of jitter, various measures are used to describe its impact on the timing accuracy of the system. In order to perform such characterization, specialized bench-top instrumentation is often used, typically located several feet away from the device-under-test (DUT). With such large separation distances, the impact of off-chip noise sources on the timing accuracy is greatly enhanced due to increases in inductive and capacitive pickup, and increases in cable resistance.

In recent years, researchers have devised various schemes in which to perform on-chip jitter measurements, such as a time-to-digital converter (TDC) using a delay-locked-loop (DLL) technique [1], a Vernier delay line (VDL) technique [2] and a technique that involves the many phases of a ring oscillator [3], [4]. For a jitter measurement, in particular, an on-chip circuit consisting of a ring oscillator and a calibration circuit was reported in [5] capable of measuring timing jitter with a resolution as low as a single gate delay in the given process technology. Moreover, the circuit was fully synthesizable from an RTL description, as the design did not depend on the matching of delay elements. In fact, due to the scalability of digital circuits and turn-over rate of synthesizable circuits, the design in [5] was considered a major step forward in the evolution of embeddable test circuits. Subsequently, a jitter measurement device was reported in [6] that was capable of measuring timing with a resolution below a single gate delay. In this case, the timing resolution was derived from the difference of two gate delays. However, in this particular design, the timing resolution was strongly dependent on the matching of pairs of delay elements [7]. Moreover, the design required a large number of counter circuits to collect the statistical data necessary for jitter characterization, resulting in a large silicon area penalty. In this paper, we shall present a new VDL design that eliminates the matching requirement and reduces the number counter circuits required to a single one. At the center of this new design is a component-invariant VDL structure consisting of a single VDL stage.

A description of the paper is as follows. In Section II, we shall describe the fundamental principles of a jitter measurement and some of its related statistics. In Section III, we shall introduce the design details of our component-invariant VDL, calibration and test time issues, and a novel method for reducing test time. In this same section, we shall also demonstrate how the component-invariant VDL circuit can also be used to deduce the frequency-domain behavior of jitter. In Section IV, we shall provide some experimental results obtain from a field-programmable gate-array (FPGA) and IC implementation of the component-invariant VDL circuit. Finally, conclusions are provided in Section V.

II. Background

A. Jitter Statistics and Characterization

To illustrate the basic principle of a jitter measurement, consider uniformly sampling a noiseless clock signal with, say for

Manuscript received October 29, 2002; revised February 17, 2003. This work was supported in part by the National Sciences and Engineering Research Council of Canada, and in part by the Canadian Microelectronics Corporation.

A. H. Chan was with the Microelectronics and Computer Systems Laboratory, McGill University, Montreal, Canada. He is now with DFT Microsystems, Inc., Montreal, QC, H3B 1A7 Canada (e-mail: antoniochan@ieee.org).

G. W. Roberts is with the Microelectronics and Computer Systems Laboratory, McGill University, Montreal, QC H3A 2A7 Canada (e-mail: roberts@ece.mcgill.ca).

Digital Object Identifier 10.1109/TVLSI.2003.820531

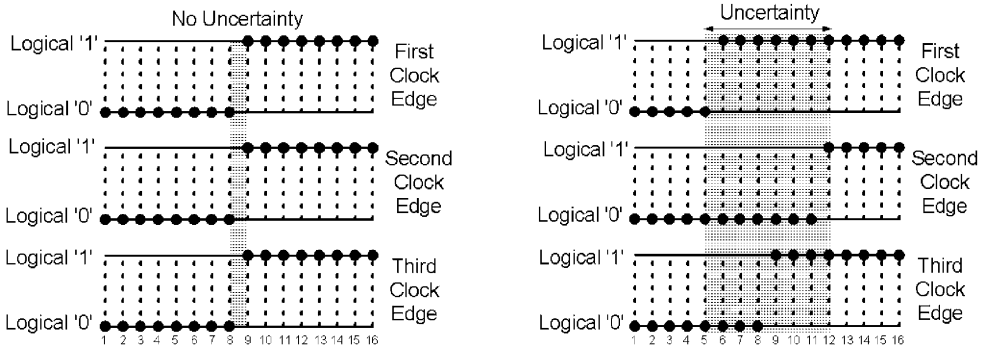


Fig. 1. Sampling instances of (a) jitter-free signal (b) jittery signal.

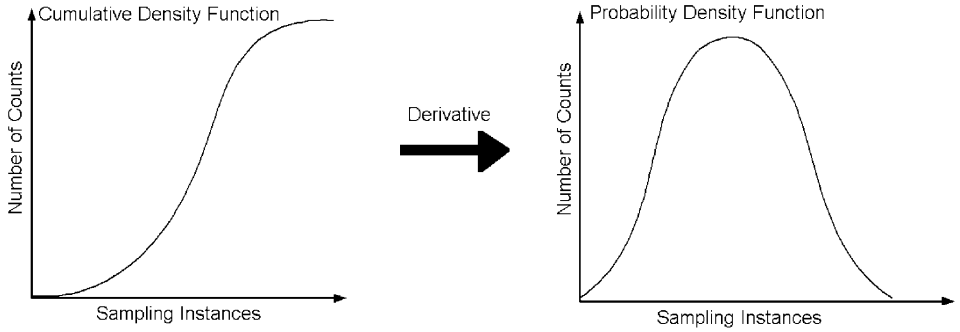


Fig. 2. Jitter CDF and PDF.

sake of explanation, 16 points per period. Next, stack consecutive periods of this sampled clock signal one above the other as shown in Fig. 1(a), taking care to line up each sampling point relative to the start of each clock cycle. As expected for a noiseless clock signal, in all three cases shown, the transition from logical low to logical high occurs at the same point, somewhere between sampling instances 8 and 9. However, if the clock signal is jittery, as shown in Fig. 1(b), the rising edge of the clock signal will vary over the period of the clock. Statistically, we can characterize this variation by computing the Cumulative Density Function (CDF) of the jittery clock signal. This is simply done by counting the number of times the clock signal is logically high at each sampling instance. For the 3-period example given in Fig. 1(b), at the first sampling instance the count is 0. The count remains at 0 for the next three sampling instances then increases to 1 at the 6th sampling instance, remains at 1 until the 9th sampling instance where it increases to 2. The count remains at 2 until the 11th sampling instance and then increases to 3 at the 12th sampling instance. The count remains at 3 for the remaining four sampling instances. Although the granularity of this particular example is rather coarse, a smoother positive-increasing monotonic function would result if a larger number of clock periods are used in the calculation. The resulting CDF would then take on a shape similar to that shown in Fig. 2(a). Interesting enough, if the derivative of the CDF is computed, then one would obtain the probability density function (PDF) or histogram of the jittery clock signal as shown in Fig. 2(b) [8]. Subsequently, we can extract familiar statistical measures of the jitter, such as the RMS and Peak-to-Peak values, based on these results.

B. Unit Gate Delay Resolution

The algorithm described above can be implemented using the circuit shown in Fig. 3(a) consisting of a series of N D-type flip-flops or *D*-latches, counters and a delay line with N taps. The signal under test, herein referred to as the data signal, is simultaneously applied to the input of each *D*-latch whose clock inputs are delayed slightly with respect to one another to correspond to the appropriate sampling instance described in Section II-A. The clock signals for the various *D*-latch are generated by passing a master clock signal through a chain of buffers, delaying the clock by τ second as is shown Fig. 3(b). Assuming that the master clock signal is jitter-free, the size of the delay τ establishes the timing resolution of the measurement. If the data signal is leading a particular clock signal, the output of the corresponding flip-flop will go high and cause the counter connected to its output to increment its content by 1. However, if the data signal is lagging the clock signal, the flip-flop will latch to a logic low value and the counter will maintain its current value. For example, consider the timing relationship between data, Clock_1, Clock_2 and Clock_3 shown in Fig. 3(b). In this case, the data signal is sampled by three delayed version of the same clock signal simultaneously. Counter_1 keeps its current value while Counter_2 and Counter_3 increment their contents by 1. This process is repeated for a large number of clock cycles. The values stored in the counters are then processed to obtained a CDF and, in turn, a PDF [8].

C. Subgate Delay Resolution Circuit

It should be obvious that a smaller unit delay in the delay chain will result in a finer-timing resolution in which to collect

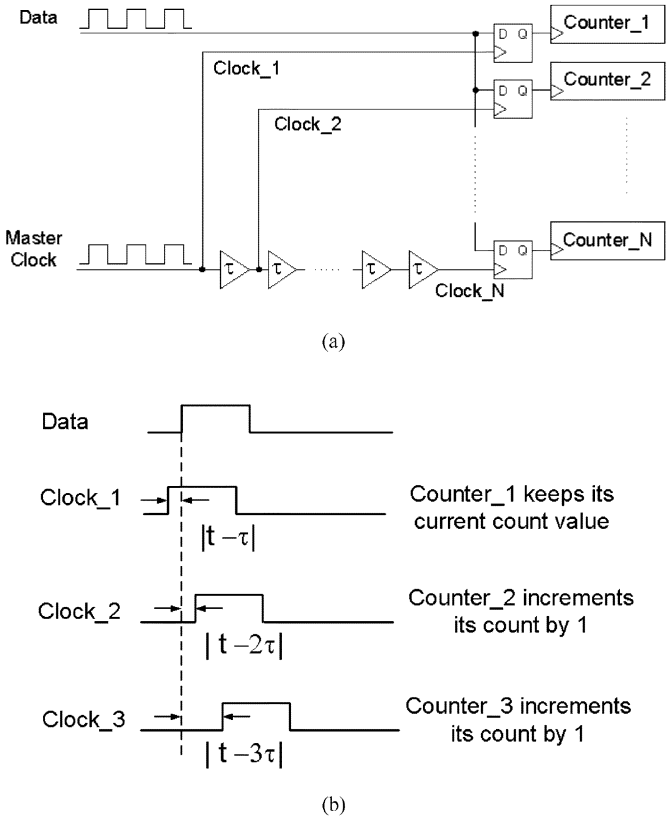


Fig. 3. Timing measurement with unit gate resolution implementation. (a) Circuit diagram. (b) Timing diagram.

the signal statistics. However, the smallest gate delay available is technology dependent, as summarized in Table I.

To circumvent this limitation, an additional delay chain can be added to the datapath as shown in Fig. 4(a). The resolution is no longer dependent on the intrinsic gate delay, but rather the delay difference between two gates. If the gates delays are made slightly different, subgate timing resolution is possible. Such a structure has come to be known as a VDL. Here it is assumed that the clock signal is jitter-free. The symbols τ_f and τ_s are the respective propagation delays of the buffers interconnecting each stage of the VDL. As the propagation delays of the clock and datapaths differ by an amount $\Delta t = \tau_s - \tau_f$, the time difference between the rising edges of the data and clock signals will decrease by Δt after each stage of the VDL. The phase relationship between these two rising edges after each stage is detected and recorded by a corresponding *D*-latch. A logical low output will result when the clock signal leads the data signal, whereas a logical high output will result when the data signal leads the clock signal. The output of the *D*-latch is passed to a counter circuit, which simply counts the number of times the data signal leads the clock signal (i.e., the number of logical 1's) with a delay difference set by its position in the VDL.

By design, the data signal will be made to always lead the clock signal at the input of the VDL by placing an additional delay block in series with the clock input. Subsequently, as the clock input signal propagates along the VDL, it comes to a point where the data signal will go from a leading to lagging situation that is detectable. This will result in all the *D*-latches prior to this point to register logical high levels, whereas all *D*-latches

TABLE I
INTRINSIC DELAY OF DIFFERENT CMOS TECHNOLOGY

Technology	Buffer Delay
0.35 μm	52.3 ps
0.18 μm	25.1 ps

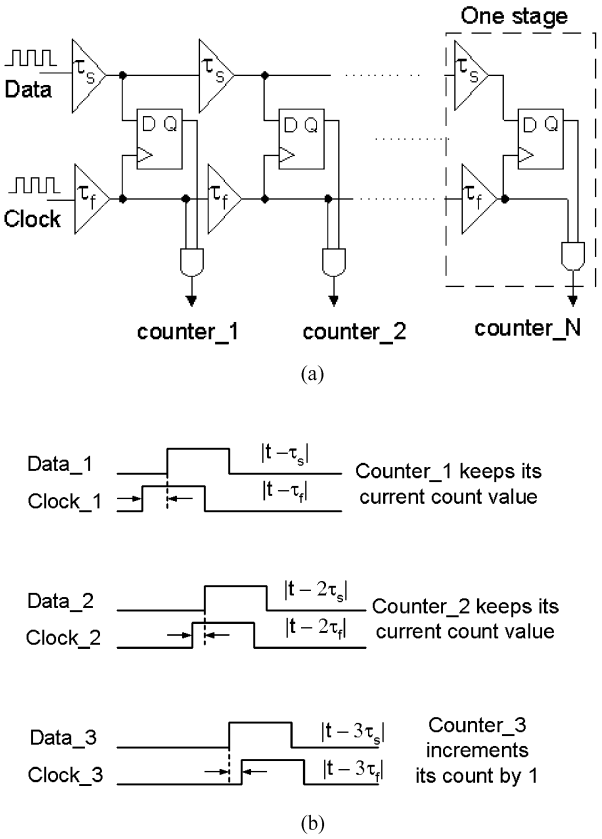


Fig. 4. VDL with subgate timing resolution. (a) Circuit diagram. (b) Timing diagram.

after this point will register logical low levels. The counter in each stage then registers the corresponding state of each *D*-latch. As the phase between the data and clock signals at the input of the VDL is a random variable, each time the measurement is performed, a different set of *D*-latches are set to a logical high level and the corresponding counters begin to register different values. In the case of the first counter, its count value reflects the number of times the rising edge of the data signal is ahead of the rising edge of the clock signal with a delay greater than Δt. Likewise, the counter in the next stage will correspond to the number of times the rising edge of the data signal leads the rising edge of the clock signal with a delay greater than $2\Delta t$. Subsequently, the following stages correspond to the number of times the data signal leads the clock signal by $3\Delta t$, $4\Delta t$, and so forth. As an example, the timing relationship between the data and clock signal is shown in Fig. 4(b). In this case, three delayed version of the data signal is sampled simultaneously by three delayed version of the clock signal, resulting in subgate timing resolution. Statistically, the various count values can be

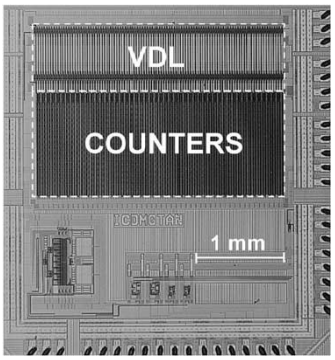


Fig. 5. VDL in 0.35-μm CMOS technology.

TABLE II
SILICON AREA FOR VDL IN CMOS-0.35 μm

Component	Area occupied
VDL	2.4 mm^2
Counter	3.1 mm^2

collected and used to create a CDF of the jitter riding on the data signal. Subsequently, a PDF can then be obtained.

D. Drawbacks

To see the drawback of this design, let us take a look at the design implemented previously in [6]. This design was implemented in a 0.35-μm CMOS technology consisting of 101 buffer stages in the VDL. The chip micrograph taken from [6] is shown in Fig. 5. The respective sizes of the VDL and the counter is summarized in Table II. An important drawback of this design is large number of counters it requires. Not only is size a drawback to this design, the measurement accuracy of this VDL structure is dependent on the matching of delay elements in the various stages, as symbolically illustrated in Fig. 6. These mismatch errors lead to differential nonlinearity timing errors. Although careful layout techniques can help to minimize these mismatches, it cannot eliminate them completely.

III. A COMPONENT-INVARIANT VDL STRUCTURE

First, let us take a look at how to overcome the number of counters required. If one assumes that the period of the data and clock signal, denoted as T, is larger than the total propagation delay through an M-stage VDL, then the outputs of all the *D*-latches can be combined into one bit-stream whose total count of logical high levels represents the actual time difference between the edge of the data and clock signal taken at a particular instant in time. This is easily achieved by ORing the outputs of all the *D*-latches together and counting the number of logical high levels over the time period T, as shown in Fig. 7. Repeating the measurement *N* times enables a histogram of the jitter signal to be constructed. This eliminates the problem of having to use a large number of counters.

As noted previously, the original VDL design is sensitive to component mismatches in the delay elements. However, by utilizing the same delay elements in each stage, mismatches can be

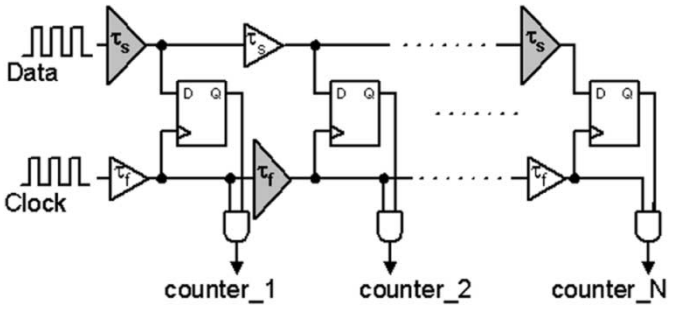


Fig. 6. VDL with mismatched elements.

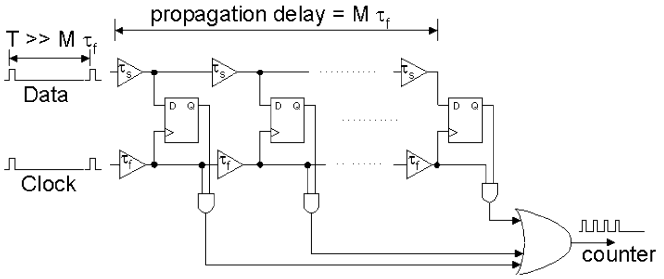


Fig. 7. Obtaining a timing measurement directly from a VDL.

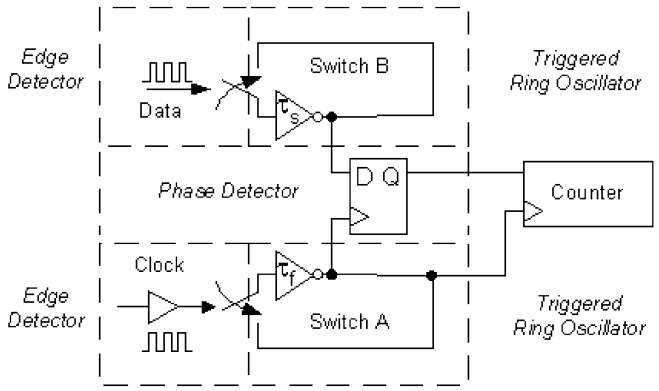


Fig. 8. Replacing VDL by a component-invariant VDL structure.

completely eliminated. Such an approach is achieved by modifying the circuit in Fig. 7 to obtain the component-invariant VDL structure shown in Fig. 8 [9]. This novel circuit is the main focus of this paper and will be discussed in some detail in Section III-A. In this circuit, inverters instead of buffers are used to create the delay difference between the data and clock input signals to the *D*-latches. In addition, the output of each inverter is fed back to its corresponding input, depending on the state of the switch in its feedback path. When the switches are closed, the inverters are configured with regenerative feedback, hence will oscillate with a period of $2\tau_s$ or $2\tau_f$ s, depending on the propagation delay of the inverter in the feedback loop. More importantly, each inverter circuit will delay the leading edge of the data signal with respect to the leading edge of the clock signal by an amount $2(\tau_s - \tau_f)$ or $2\Delta t$ s every cycle of the input clock signal. Alternatively, one can envision this to be equivalent to having two ring oscillators running simultaneously with different frequencies to produce a constant delay difference during every cycle of oscillation.

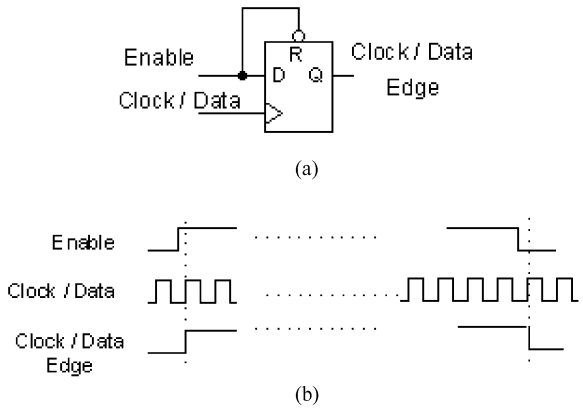


Fig. 9. Edge detector. (a) Circuit diagram. (b) Timing diagram.

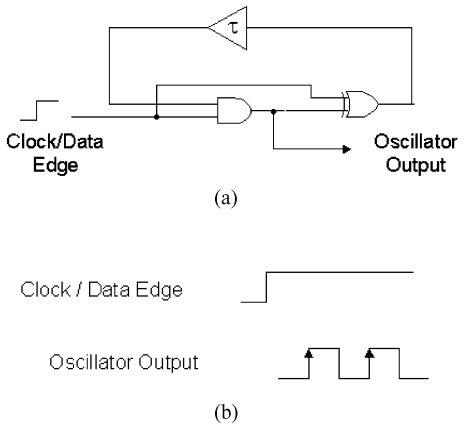


Fig. 10. Triggered ring oscillator. (a) Circuit diagram. (b) Timing diagram.

To ensure an accurate time measurement, switch A in the feedback path of the inverter controlling the clock of the *D*-latch shown in Fig. 8 must be closed on the rising edge of the clock signal, whereas switch B must be closed on the rising edge of the data signal. Simultaneously, the output of the single *D*-latch is passed to a counter, which simply determines how many clock cycles the *D*-latch remains in the high state. Once the edge of the data signal goes from a leading to lagging situation with respect to the clock signal (or vice versa), the counter is stopped. The time difference between the data and clock edges can then be computed. The process is then repeated and a histogram of the jitter is derived.

A. Circuit Implementation

In this Section, we shall describe the circuit details of the three main circuit components of the component-invariant VDL circuit: the edge detector, the triggered ring oscillator and the phase detector. We shall also outline the calibration and measurement process, and the time it takes to complete a single measurement.

1) Edge Detector: The main function of the edge detector is to catch the rising edge of the data or clock signal. This can be implemented using a single D-type flip-flop with the D and reset inputs connected together as shown in Fig. 9(a). With the enable signal set high, the D-type flip-flop output will latch its output high on the subsequent rising edge of the clock or data signal. The D-type flip-flop will be reset when the enable input is set low and another clock or data edge occurs. These two situations are illustrated in Fig. 9(b).

2) Triggered Ring Oscillator Circuits: At the heart of the component-invariant VDL are the two triggered ring-oscillator circuits highlighted in Fig. 8. Note that τ_f and τ_s are the respective propagation delays around the loop of each ring oscillator. In order to maintain a predictable phase relationship for detection, τ_s is set to be greater than τ_f. (Here, the subscript "s" indicates a slow oscillation and "f" for a fast oscillation.) This in turn, establishes the ring oscillator triggered by the clock signal to run at a higher frequency than the oscillator triggered by the data signal. To trigger each oscillator on a logical high level, the circuit of Fig. 10 was chosen. The delay in the ring oscillator circuit can be designed to be tunable using the voltage-controlled delay cell [7] shown in Fig. 11 or as a fixed-delay buffer using several inverter circuits in cascade.

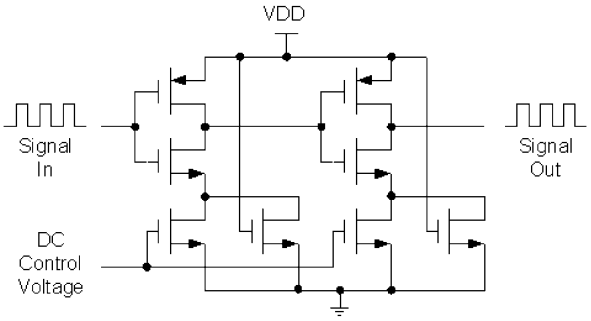


Fig. 11. Voltage-controlled delay circuit.

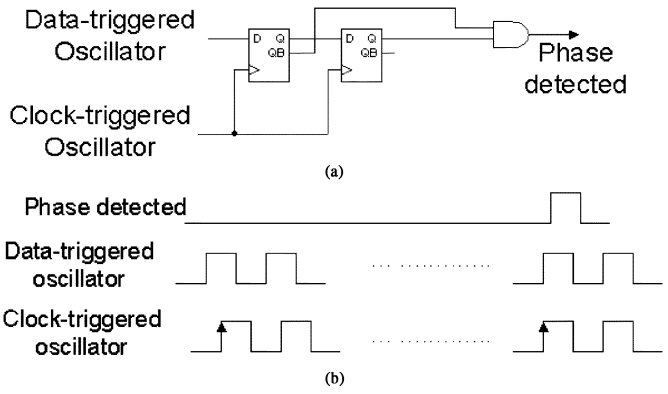


Fig. 12. Phase detector (a) circuit diagram (b) timing diagram.

3) Phase Detector: The phase detector circuit is used to keep track of the history of the phase difference between the two oscillators, thus providing information on a phase change. As mentioned in Section II, by design, the edge of the data signal is always set to lead the clock signal at the start of the measurement process. It is when the data signal begins to lag the clock signal that the measurement process will stop. To accomplish this, the phase detector is implemented using the two *D*-latches shown in Fig. 12(a). The output of the AND gate will switch from a logical low level to logical high level when an input sequence of "10" is detected as shown in Fig. 12(b).

4) Complete Circuit: By combining the edge and phase detectors, the two triggered oscillators and the counter circuit, the complete component-invariant VDL circuit is shown in Fig. 13.

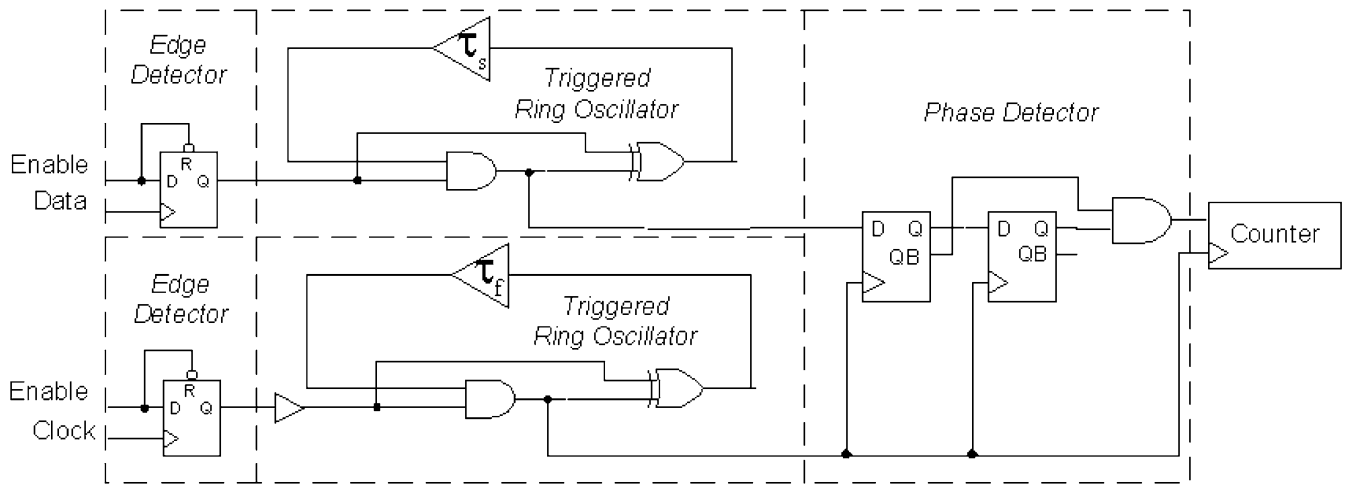


Fig. 13. The circuit implementation of the component invariant VDL structure.

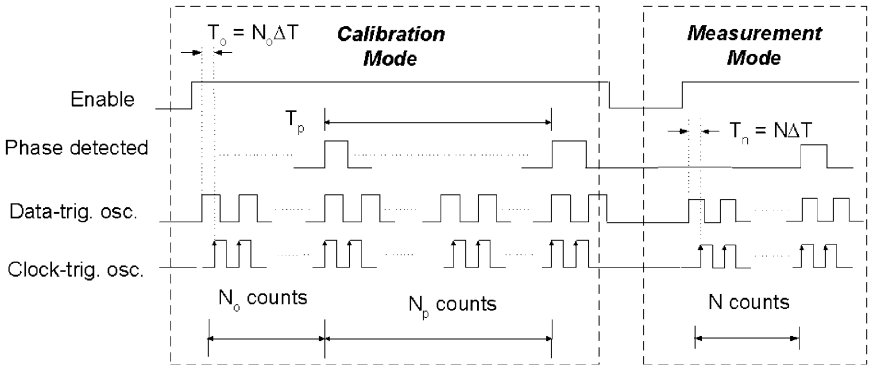


Fig. 14. Timing diagram for the calibration and measurement modes of operation.

It is interesting to note that this circuit can be synthesized using entirely digital logic.

B. Calibration and Measurement Processes

There is an intrinsic delay difference between the signal path of the clock and the datalines, which includes the intentional delay added between the clock-triggered oscillator and the edge detector, the setup time and propagation delay difference between the *D*-latches in the two edge detectors, as well as that of the XOR gate in the ring oscillators. Since all these delays are process sensitive, the measured delay will be different from the actual delay difference between the clock and the data edges. Also, note that the difference in oscillation frequencies determines the measurement resolution, which also becomes process sensitive due to the unpredictable delay of each loop in the ring oscillator. Therefore, in order to make the design fully synthesizable, i.e., no element matching is required, a calibration sequence is necessary to determine the frequency of oscillations and the difference between the delay path of the data and clock signal.

To achieve a calibration, the clock and datalines are first connected together to determine the delay difference between the two signal paths. Because the two inputs are tied together, jitter on the input calibration signal will have little effect. As the enable signal goes high, the two oscillators start to oscillate and the counter starts to record the number of clock cycles that the rising edge of the clock signal is leading the data signal. Once the clock signal lags the data signal, the counter will have counted to a value of N_o corresponding to a time delay of T_o as shown in Fig. 14.

After a certain period of time T_p, the rising edge of the clock-triggered oscillator will move across one complete cycle of the data-triggered oscillator, corresponding to N_p counts as also shown in Fig. 14. The timing resolution, ΔT is defined as

$$\Delta T = T_s - T_f \tag{1}$$

where T_s is the oscillation period of the data-triggered oscillator and T_f is the oscillation period of the clock-triggered oscillator. T_f is related to T_p and N_p according to

$$T_f = \frac{T_p}{N_p}. \tag{2}$$

As the clock-triggered oscillator completes N_p cycles in the time T_p, the data-triggered oscillator must complete $N_p - 1$ cycles. Hence, the fundamental relationship that governs the coherence of this design is

$$T_p = N_p \cdot T_f = (N_p - 1) \cdot T_s. \tag{3}$$

We shall refer to T_p as the coherency period. By rearranging (3), the period of the data-triggered oscillator can be then determined in terms of the measured data as follows:

$$T_s = \frac{T_p}{N_p - 1}. \tag{4}$$

Finally, the timing resolution ΔT can be determined by substituting (2) and (4) into (1), to obtain

$$\Delta T = \frac{T_p}{N_p \cdot (N_p - 1)}. \tag{5}$$

The time value of T_p is usually very large compared to T_f, thus, depending on measurement equipment, measuring an accurate T_p may be difficult, especially in the case of a small time step over a large measurement range. An alternative approach is to measure T_f indirectly through the counter output. As shown previously in Fig. 13, the counter is used to count the number of the clock-triggered oscillator cycles during calibration and during a phase measurement. Therefore, when the oscillator is running, T_f can be obtained by measuring the cycling time of one bit of the counter. Thus, T_f is related as follows:

$$T_f = \left(\frac{1}{2}\right)^n \cdot T_c \tag{6}$$

where n is the bit position with respect to the least significant bit of the counter and T_c is the cycling time of the nth counter bit. Therefore, T_p can be determined from (3) as follows:

$$T_p = T_f \cdot N_p = \left(\frac{1}{2}\right)^n \cdot T_c \cdot N_p. \tag{7}$$

Of course, once T_p is known, T_s can be calculated using (4).

Now that the calibration phase is complete, we are ready to perform a time measurement. Assuming that the calibration and measurement modes experience the same intrinsic delay along the clock and datapaths, we can compute the measured phase difference by subtracting off the intrinsic delay T_o according to

$$T_o = \Delta T \cdot N_o. \tag{8}$$

Similarly, denoting the counter output during the measurement mode as N (shown in Fig. 14), the total measured time T_n is given by

$$T_n = \Delta T \cdot N. \tag{9}$$

Since this time includes the intrinsic delay T_o, the actual time difference between the data and clock signal is given by

$$T_m = T_n - T_o. \tag{10}$$

Substituting (8) and (9) into (10), T_m can be written more directly in terms of the measured parameters as follows

$$T_m = \Delta T \cdot (N - N_o). \tag{11}$$

The accuracy of our measured time interval T_m is directly dependent on the accuracy of the calibration factors, T_p and the counts, N_o and N_p. To a first-order approximation and assuming, the relative accuracy of Tm can be expressed as

$$\frac{\Delta T_m}{T_m} \approx \frac{\Delta T_p}{T_p} - 2\frac{\Delta N_p}{N_p} - \frac{\Delta N_o}{N - N_o}. \tag{12}$$

With count errors of ± 1 count, the accuracy of the time measurement becomes

$$\frac{\Delta T_m}{T_m} \approx \frac{\Delta T_p}{T_p} \mp 2\frac{1}{N_p} - \frac{1}{N - N_o}. \tag{13}$$

Here we clearly see that N_p, $N - N_o$, and T_p should be as large as possible in all situations to maximize the relative accuracy of the measurement. Of course, $N - N_o$ is outside of our direct control, as it varies with each measurement. However, as evident from (3), in order for T_p and N_p to be maximized, the periods of both the data and clock triggered oscillators (i.e., T_f and T_s) must be maximized. In general, to increase the oscillation period of a ring oscillator requires additional delay stages to be added in the feedback loop of the oscillator. However, incorporating additional delay stages increase the noise introduced into the circuit and adds to the randomness in any particular measurement. Nonetheless, measurement averaging can be exploited to reduce this variation at the expense of more test time.

C. Test Time Comparison

Since test time is one of the criteria to quantify the performance of a measurement device, the required test time of the component-invariant VDL is compared with the original VDL circuit shown in Fig. 4. For the VDL circuit of Fig. 4, the test time to collect all the CDF data is roughly equal to

$$T_{\text{test}} \approx T_{\text{clk}} \cdot N_{\text{sample}} \tag{14}$$

where T_{test} is the total test time, T_{clk} is the clock period and N_{sample} is the total number of samples taken. For clock period of $T_{\text{clk}} = 1$ ns and 5000 samples collected, the total test time would be approximately $T_{\text{test}} \approx 5\ \mu$s.

For the component-invariant VDL, assuming jitter is uncorrelated with the clock signal, the average test time per sample can be estimated by taking the mean of the maximum and minimum test time per sample. Test time per sample is at a maximum when the clock and data signal is different by almost one clock cycle T_f. This is determined during the calibration phase to be equal to T_p. Test time per sample is at a minimum when the data and clock signal is aligned such that it only requires one oscillation cycle to obtain a phase change. Hence, the maximum test time per sample is estimated to be

$$T_{\text{max-test-per-sample}} \approx T_p. \tag{15}$$

Therefore, the average test time per sample is

$$T_{\text{test-per-sample}} \approx \frac{T_p}{2} \tag{16}$$

and the average overall test time becomes

$$T_{\text{test}} \approx \frac{T_p}{2} \cdot N_{\text{sample}} \tag{17}$$

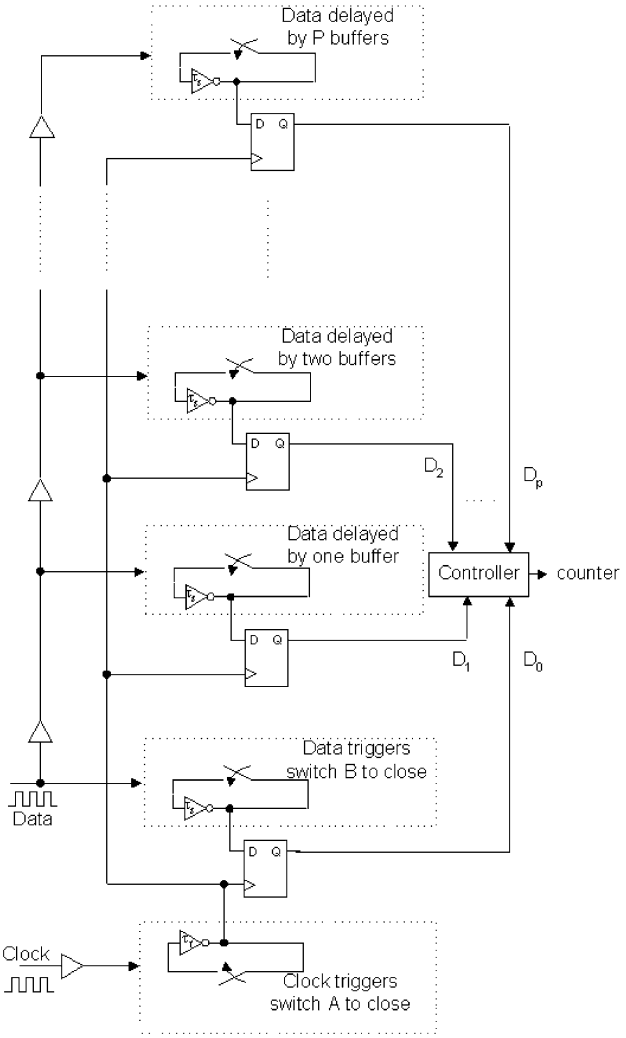


Fig. 15. An array of component-invariant VDLs.

where N_{sample} is the total number of samples collected. Note that the emphasis on test time comparison between the original VDL and component-invairant VDL is on hardware processing time and does not include software processing time to obtain RMS and peak-to-peak jitter in both cases, since software processing time is not the bottleneck of overall test time during production test.

With 5000 samples collected, a timing resolution of 10 ps, a result of clock and data oscillators having periods of 2 ns and 2.01 ns, respectively, and a coherency time T_p of 402 ns, we find from above that the average test time is expected to be $T_{\text{test}} \approx 1$ ms.

The component-invariant approach typically requires longer test times than the original VDL approach of Fig. 4. One way to reduce the test time is through the application of additional component-invariant VDL stages.

D. Reducing Test Time Using a Spatial Arrangement of Component-Invariant VDLs

An array of component-invariant VDLs can be configured as shown in Fig. 15. Here a single clock-triggered ring oscillator is shown driving the clock input of each D flip-flop. All

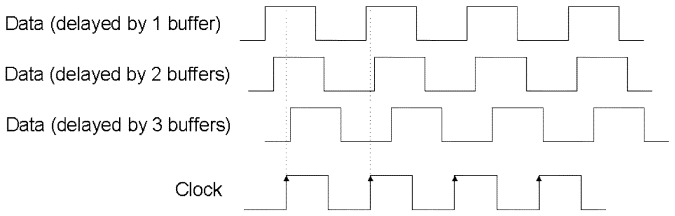


Fig. 16. Timing relationship for VDL array.

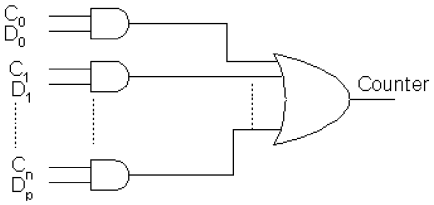


Fig. 17. Controller for VDL array structure.

the data-triggered ring oscillators are designed to have the same nominal oscillation frequency but all are triggered by a progressively increasing one-gate delayed data signal. With the data-trigger oscillation frequency set below the clock-triggered oscillation frequency, a time-grid of data-triggered oscillation will result as shown in Fig. 16. Therefore, as soon as the rising edge of the clock-triggered oscillator passes through any one of the rising edges of the data-triggered oscillators, the result will be known. For jitter measurement applications, this structure has the advantage that the measurement time is significantly reduced. Since jitter is assumed to be random and, hence, does not correlate with the time that the sample is taken, a nonuniform sampling of data will also lead to a good estimation of the jitter statistics.

Note that the phase difference between any data-triggered oscillator does not have to be matched, since calibration can be performed on each component-invariant VDL circuit. For the same reasons, the frequency of oscillations of these data-triggered oscillators does not have to be made exactly equal.

Since there are multiple phase detectors, a controller will be required to select the earliest phase detection. This can be easily implemented using some simple combinational logic such as that shown in Fig. 17. The calibration process is exactly the same as the single component-invariant structure, provided one calibrates each data-triggered oscillator with respect to the clock-triggered oscillator. During calibration mode, the control signal C_i will be set to a logical high level to enable the ith data-triggered oscillator, and all other C_j's $(i \neq j)$ will be set to a logical low level to disable the other data-triggered oscillators. During measurement mode, all C's will be set to a logical high level.

Since the efficiency of the time reduction depends on the time grid location, if P component-invariant VDLs are added to provide the optimal time grid, the average test time per sample is now reduced to

$$T_{\text{test-per-sample}} \approx \frac{T_p}{2 \cdot P}. \tag{18}$$

Therefore, the total test time becomes

$$T_{\text{test}} \approx \frac{T_p}{2 \cdot P} \cdot N_{\text{sample}} \tag{19}$$

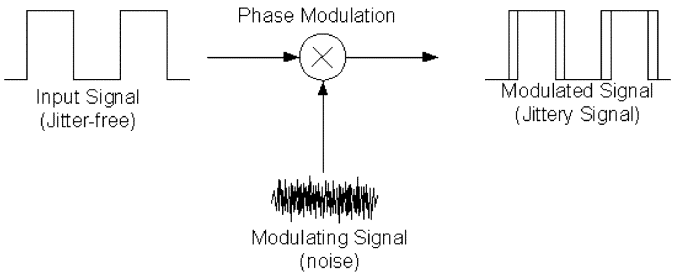


Fig. 18. Phase modulation by noise.

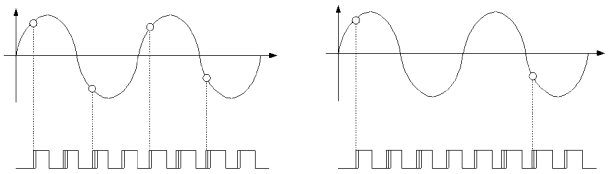


Fig. 19. Effect of sampling rates. (a) Higher sampling rate and (b) lower sampling rate.

where N_{sample} is the number of samples collected over the test period.

For a VDL with four additional oscillators (each with an oscillation period of $T_f = 2.01$ ns), 5000 samples collected over the test time and a timing resolution of $\Delta T = 10$ ps, the expected test time becomes 500 μs (compared to 1 ms in the single oscillator VDL case).

Note that an OR gate with a large number of inputs is necessary if a large number of data-triggered oscillators are used. Practically speaking, however, only a few are required to produce a "time grid" fine enough to reduce the test time significantly. In addition, circuitry for decoding which data-trigger oscillator is responsible for the phase detect must also be added. This is necessary to know which calibration factors should be used to compute the appropriate measurement time. Latching the state of the outputs of each phase detect at the time of the first phase detect will enable the user to know which oscillator is taking part in the time measurement.

E. Frequency Characterization of Jitter

Another way of characterizing jitter is to describe its frequency distribution. Jitter timing can be modeled as a noise signal phase-modulating a perfect digital signal as shown in Fig. 18. Here a single sinusoidal signal is seen modulating a jitter-free digital signal. The deviation of the edge position of the digital signal from its ideal position is based on the instantaneous value of the modulating signal. In other words, samples of the modulating waveform give rise to the phase modulated or jittery signal. Assuming that the average test time per sample is $T_{\text{test-per-sample}}$, as described by (16), the component-invariant VDL can sample the input signal at a frequency of $F_s \approx 1/T_{\text{test-per-sample}}$. Further assume that the highest frequency component in the jitter signal is less than $F_s/2$, then a fast Fourier transform (FFT) of the jitter signal can be used to approximate the frequency spectrum of the jitter. As shown in Fig. 19(a), the sampling rate is high enough so that no frequency aliasing will occur. However, if this condition is not met as shown in Fig. 19(b), aliasing effects will occur and distort the spectral distribution. It is therefore important to have some idea of the spectral distribution of the jitter in order for this approach to be effective.

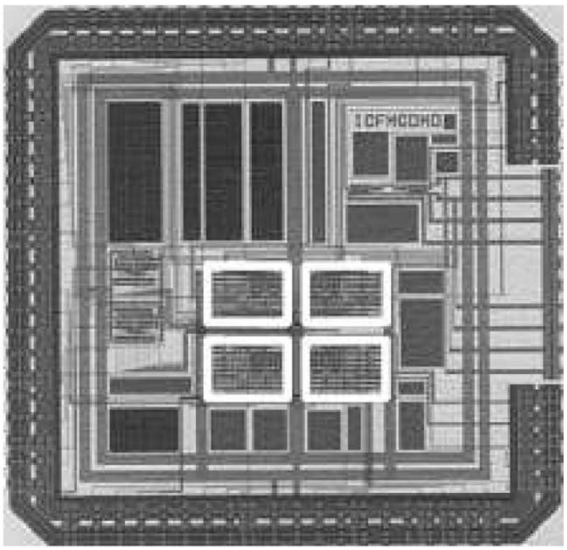


Fig. 20. A chip monograph of component-invariant VDL implemented in a 0.18-μm CMOS process. The boxed region illustrates one component-invariant VDL circuit consuming approximately 0.12 mm^2 of silicon area.

IV. Experimental Results

A. CMOS Implementation of a Component-Invariant VDL

In this section, we shall describe the experimental results of a single-stage component-invariant VDL implemented in a 0.18-μm CMOS process. The schematic of the circuit that was used is shown in Fig. 13, with the addition of two 12-b shift registers. These two registers were included for scanning digital data off the chip. The buffers in the feedback path of the two triggered oscillators was implemented using the voltage-controlled delay circuit shown in Fig. 11 with the dc control node of each delay cell brought off the chip for external control. The layout of the experimental chip is shown in Fig. 20. In the center of the chip monograph are four white boxes containing four component-invariant VDLs. Each cell occupies an area of 0.12 mm^2.

Several experiments were run using the experimental setup shown in Fig. 21. This setup consists of a Teradyne A567 mixed-signal tester configured as a pseudo jittery clock stimulus and a Wavecrest DTS-2770 jitter analyzer for comparing the results of the VDL. Through a mathematical analysis in MATLAB, the edges of the jittery clock signal were assigned a specific statistical distribution and stored in the memory of the Teradyne A567 tester. The jittery clock signal was then applied simultaneously to the VDL and the Wavecrest instrument from which the actual phase error of the test signal relative to a reference clock signal could be measured.

With the dc control voltage of the two delay cells set to 0.68 and 1.8 V, respectively, the VDL was calibrated using 2000 samples of a 1.56-MHz clock. Specifically, T_p was measured to be 345 ns, N_p was measured to be 80.1 counts and N_o was found to be 23.05 counts. Subsequently, according to (2) and (4), the oscillation frequency of the clock-triggered oscillator, T_f, was calculated to be 4.307 ns which corresponds to a frequency of

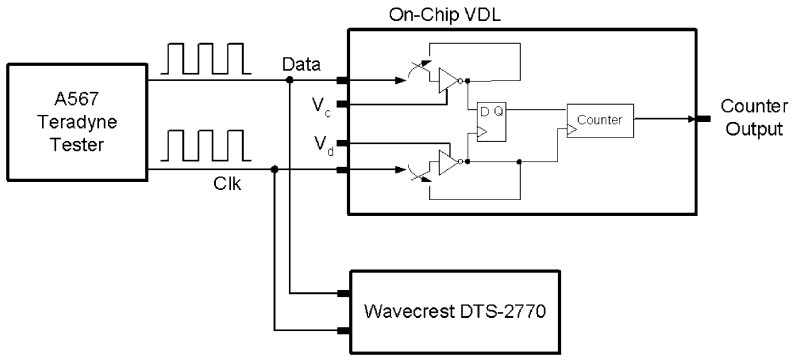
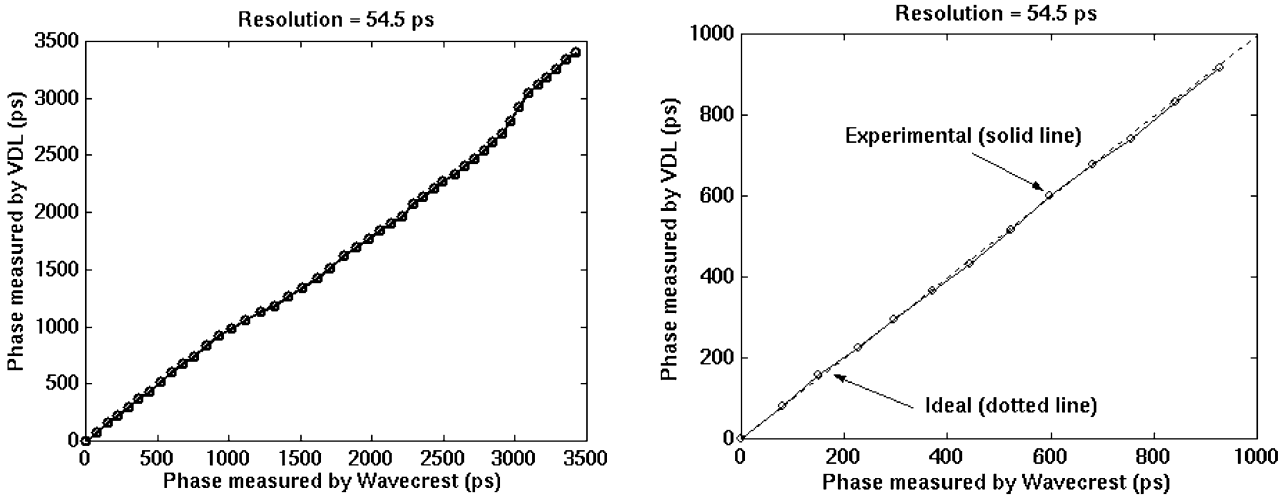


Fig. 21. Experimental setup.



(a) (b)

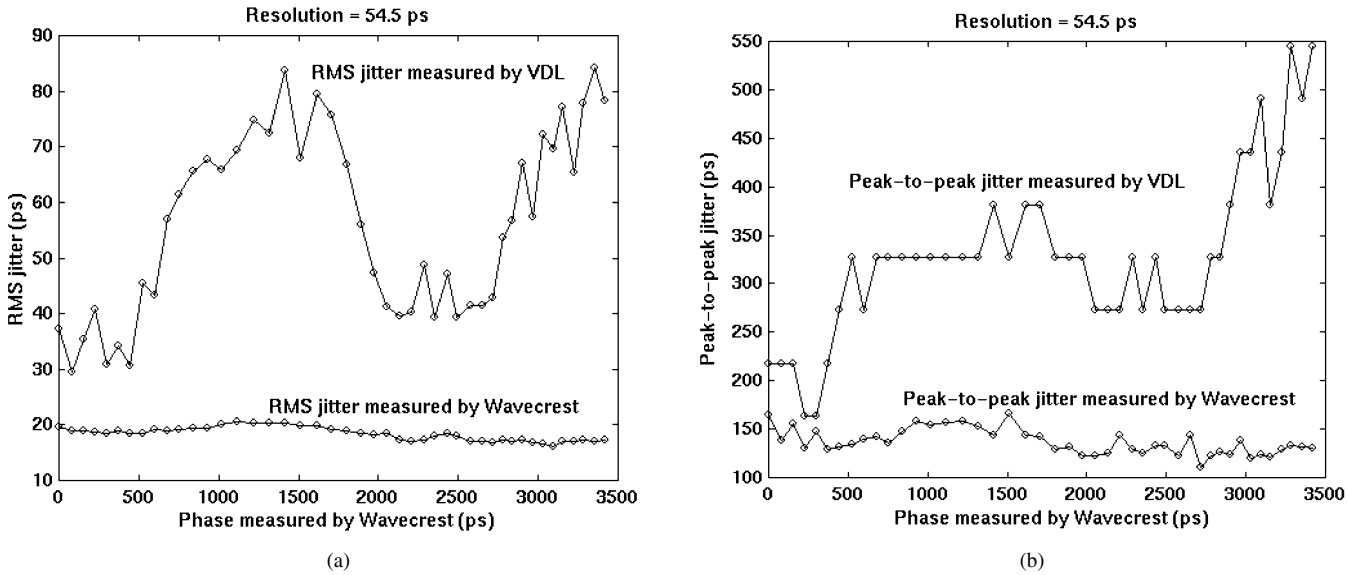
Fig. 22. Phase measurement of VDL set to the 54.5 ps timing resolution. (a) Full view and (b) zoom view.

232 MHz and T_s was calculated to be 4.362 ns which corresponds to a frequency of 229 MHz. Therefore, according to (5), a timing resolution of 54.5 ps was achieved.

The VDL circuit was then characterized by sweeping its input with a 1.56-MHz clock signal whose phase was linearly varied over its clock period. Simultaneously, the same signal was sampled by the Wavecrest DTS-2770 jitter analyzer which has 0.8 ps hardware timing resolution, ± 25 ps single-shot accuracy and ± 10 ps average accuracy [11]. 5000 samples of the input signal was measured. The results are displayed in Fig. 22(a) with the VDL results plotted as a function of the Wavecrest results. As is clearly evident, there is a strong linear correlation between the two results. In the phase range 0–1000 ps, the correlation is nearly perfect as evident from the expanded view shown in Fig. 22(b). Above this level, the measurement correlation seems to decrease. We believe this deviation is due to excessive noise induced on the power supply by the triggered oscillator pair and the counter. Since the delay cells and the counter share a common power supply and that the ring oscillator pair draws different amount of current from the power supply—depending on the relative position of the rising edges of the ring oscillator pair—the power supply level varies with the input signal conditions. This is more evident from Fig. 23 whereby the measured RMS and peak-to-peak values deviate from that of the Wavecrest for phase range higher than 1000 ps. Better layout and improved on-chip power supply decoupling is expected to improve this situation. Note also from Fig. 23 that the measured RMS value from the VDL agrees closely to that of the Wavecrest within the timing resolution of the VDL.

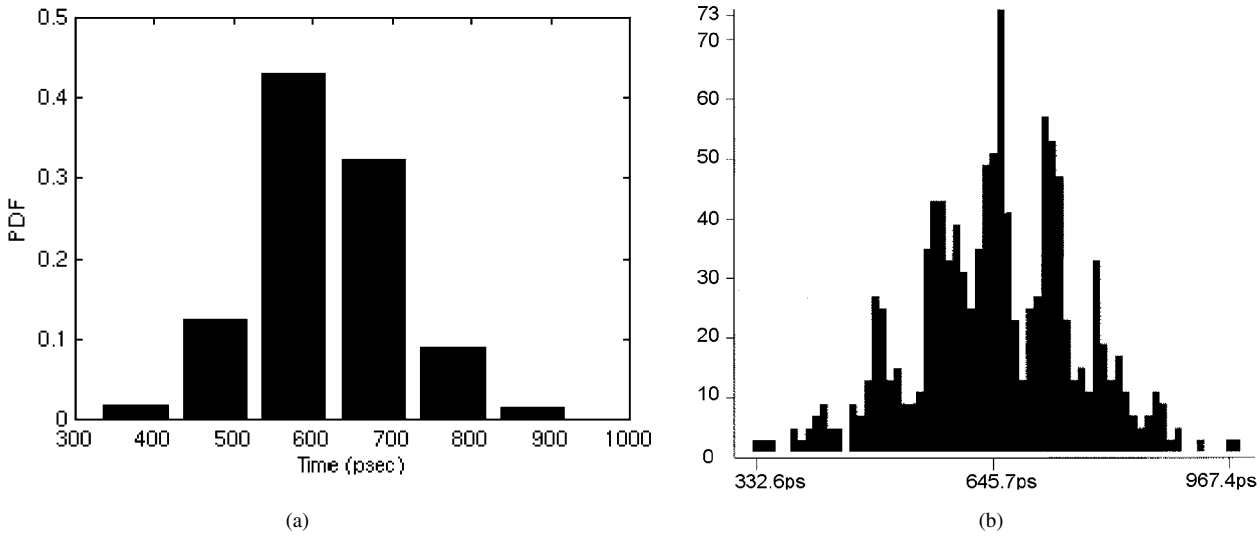
The next experiment was one that involved generating a 1.56 MHz clock signal with a jitter component having Gaussian statistics. The jitter variation was made to stay within the linear range of the VDL (i.e., <1000 ps). The dc control voltages of the VDL circuit were adjusted to 0.68 and 1.8 V, respectively, whereby a 54.5-ps timing resolution was achieved. Two thousand samples were simultaneously collected by the VDL and Wavecrest instrument. The captured histograms are shown in Fig. 24(a) and (b), respectively. The resolution is clearly higher with the Wavecrest instrument (finer line widths), however, the overall shape has very similar behavior. The RMS and peak-to-peak values of the two distributions are summarized in Table III. The two sets of statistics show excellent correlation.

Another experiment was run in a manner similar to that just described, however, this time a 1.56 MHz clock signal with a jitter component having a sinusoidal distribution was created and applied to the VDL and Wavecrest instrument simultaneously. The captured histograms are shown in Fig. 25(a) and (b). The RMS and peak-to-peak values of the two distributions are summarized in Table III. As is evident, the two sets of statistics show very good correlation.



(a) (b)

Fig. 23. (a) RMS and (b) peak-to-peak measurements of VDL set to the 54.5-ps timing resolution.



(a) (b)

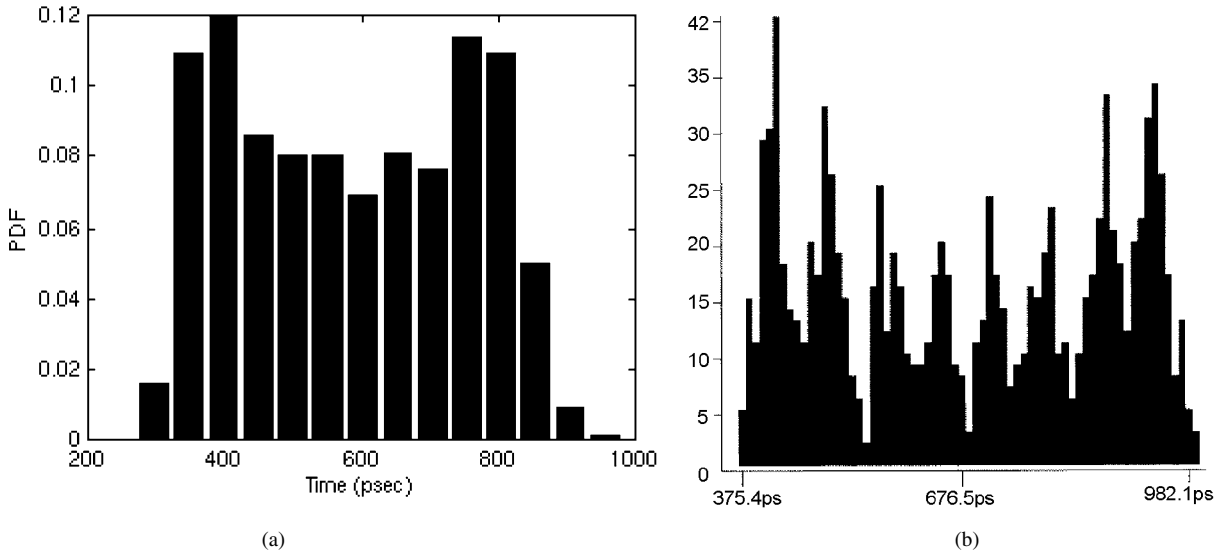
Fig. 24. Histograms for Gaussian distributed jitter from: (a) VDL and (b) Wavecrest.

TABLE III
JITTER MEASURED USING 54.5 PS TIMING RESOLUTION VDL

Jitter Distribution	Measurement Type	VDL (54.5 ps timing resolution)	Wavecrest (as reference)
Gaussian	RMS	92.8 ps	98.79 ps
Gaussian	Peak to peak	599 ps	634.8 ps
Sinusoidal	RMS	168.3 ps	185.6 ps
Sinusoidal	Peak to peak	707.9 ps	606.6 ps

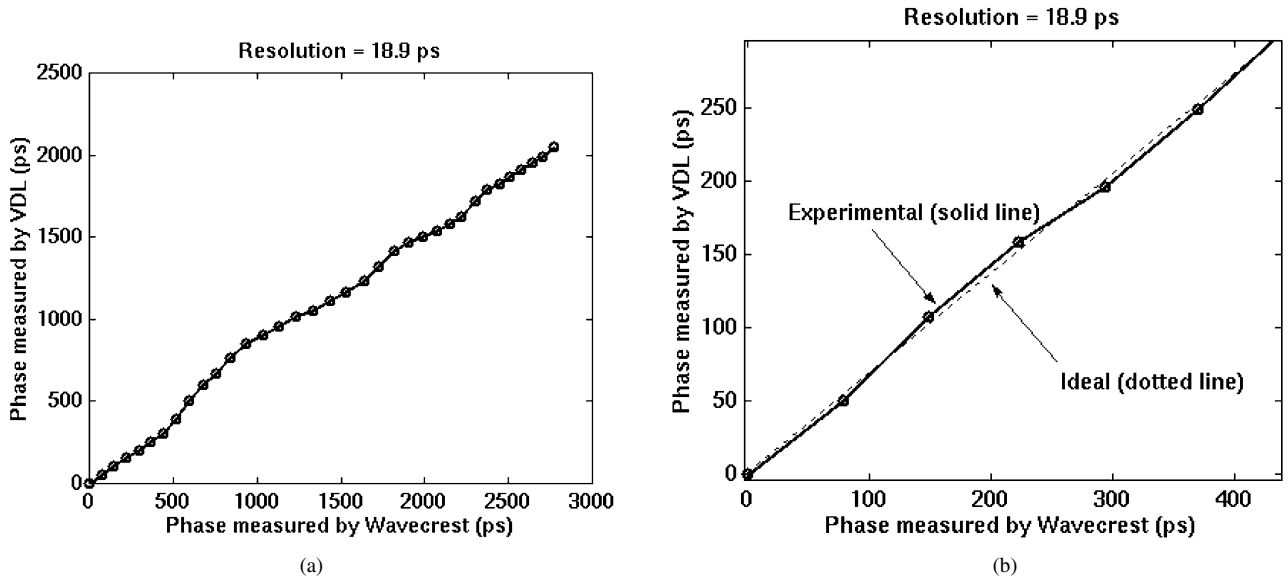
By adjusting the control voltages associated with the two delay blocks inside the VDL circuit, we were able to fine-tune the time resolution of the component-invariant VDL to 18.9 ps. The histogram results for both a Gaussian and sinusoidal jitter distribution for both the VDL and the Wavecrest instrument are shown in Figs. 26–29. Furthermore, Table IV summarize the statistics of each these experiments. Note also from Fig. 27 that the measured RMS value from the VDL agrees closely to that of the Wavecrest within the timing resolution of the VDL. Once again, we conclude that the results of the VDL correlate very well with the Wavecrest instrument.

Finally, in Fig. 30 we compare the spectral distribution of a sinusoidal phase-modulated clock signal synthesized by a Teradyne A567 mixed-signal tester and sampled with a component-invariant VDL circuit with its ideal spectral distribution. Specifically, a 1.56 MHz clock signal was generated from the tester with an equivalent phase modulation from a 90.3069-Hz sinusoidal signal having a 1-V amplitude. The resulting spectrum $X(n)$ is shown with a dotted line in Fig. 30 as a function of the FFT bin index. This signal was then synthesized using the A567 tester and applied to the input of a component-invariant VDL tuned to a time resolution of 18.9 ps. Subsequently, 4096 samples were captured at an effective sampling rate of 16.0825 kHz and an FFT was then performed on the sample set. The resulting spectrum Y(n) represented by a solid line is also shown in Fig. 30. As is evident, the results agree reasonably well. The difference between the actual and expected outputs is due to the jitter contributed by the tester and the on-chip VDL.



(a) (b)

Fig. 25. Histograms for sinusoidal distributed jitter from (a) VDL and (b) Wavecrest.



(a) (b)

Fig. 26. Phase measurement comparison between Wavecrest and VDL (set to a 18.9-ps timing resolution). (a) Full view and (b) zoom view.

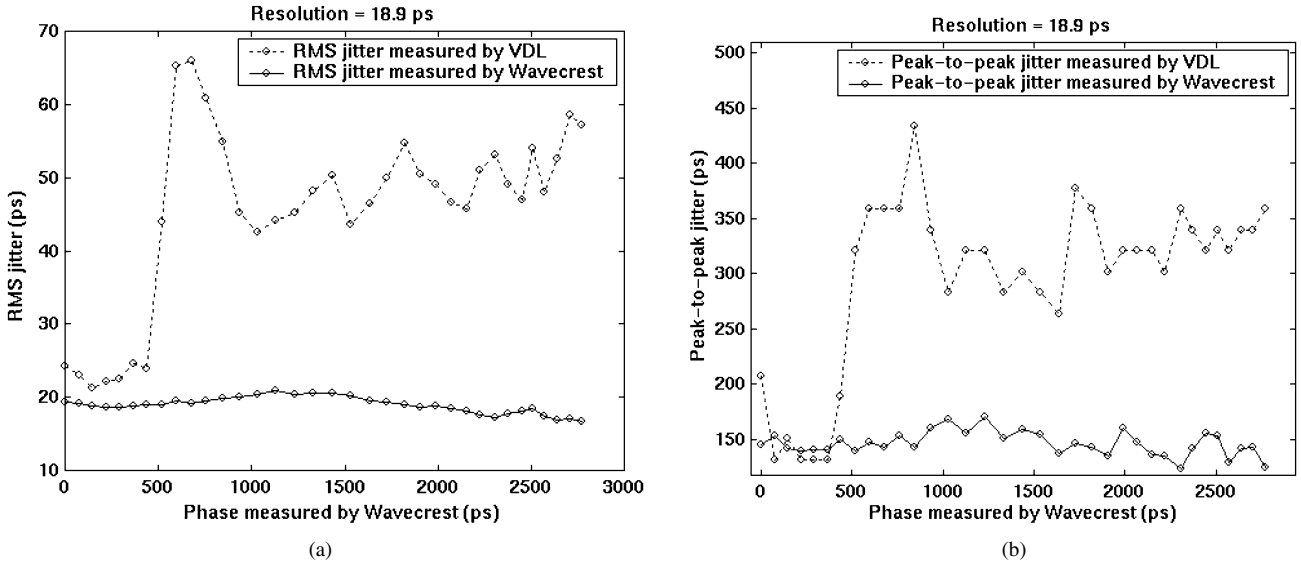
B. Three-Oscillator Component-Invariant VDL in an FPGA

To demonstrate the synthesizable nature of the proposed design, in this section we shall implement a three-oscillator component-invariant VDL circuit using an FPGA. This section will also demonstrate the test time saving of the multiple array approach.

A three-oscillator component-invariant VDL structure was implemented on an Altera FPGA as a first proof of concept of the synthesizable nature of the VDL design. The entire design was capable of fitting into a 128 macrocell FPGA. The circuit was calibrated by collecting 1500 samples, resulting in the following parameters: $N_{p1} = 143.2$ counts, $N_{o1} = 57.4$ counts, $N_{p2} = 66.1$ counts, and $N_{o2} = 99.2$ counts. In this design, the oscillation period of the clock-triggered oscillator was found to be 81.6 ns, corresponding to a frequency of 12.3 MHz, which is deduced from the cycling time of one bit of the counter. In this situation, the oscillation period of the clock is larger than that of the data. This is a result of our inability to precisely control the location of our cells. As a result, the clock-triggered oscillator completes N_f cycles in the time T_p while the data-triggered oscillator completes N_f+1 cycles. Hence, the coherency equation becomes

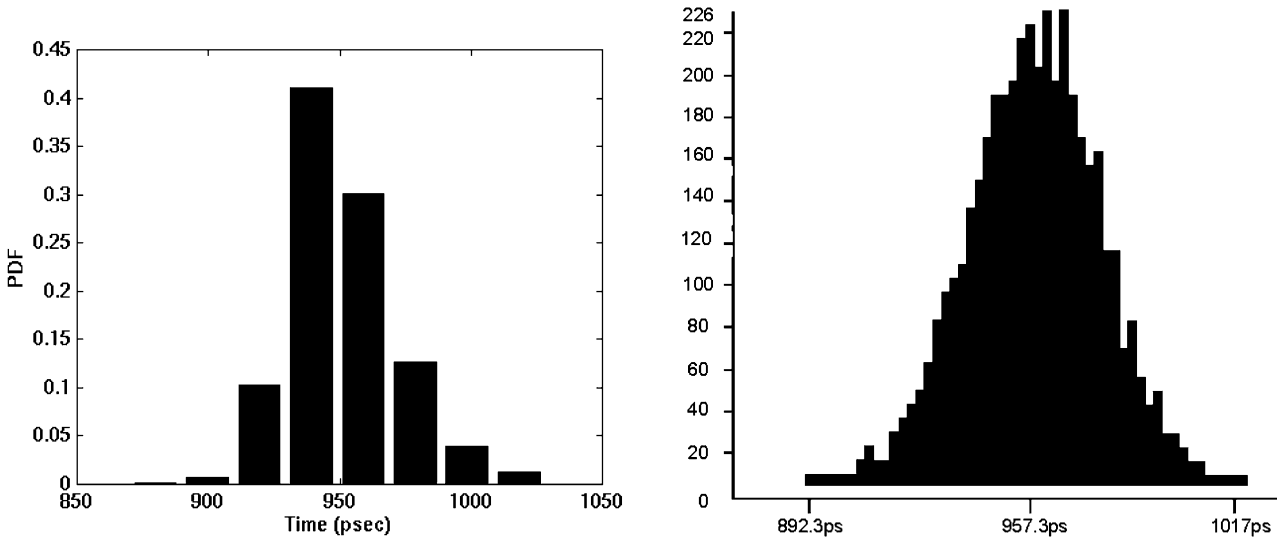
$$T_p = N_p \cdot T_f = (N_p + 1) \cdot T_s. \tag{20}$$

This is slightly different than what we saw before in (3). Consequently, the formulas for T_s and ΔT in (4) and (5) are slightly modified by replacing $N_p - 1$ by $N_p + 1$. Subsequently, the oscillation periods of the two data-triggered oscillators were calculated to be 81.03 and 80.38 ns, giving rise to timing resolution of 0.566 ns in one case and 1.22 ns in the other. Although the measured timing resolutions are not comparable to that obtained in custom IC, this experiment does serve the purpose of demonstrating the ability for the circuit to be synthesized using RTL description. These particular timing resolutions obtained in this experiment are strongly dependent on the physical location of the macrocells in the FPGA. If



(a) (b)

Fig. 27. (a) RMS and (b) peak -to-peak measurements of VDL set to the 18.9 ps timing resolution.



(a) (b)

Fig. 28. Histograms for Gaussian distributed jitter from (a) VDL and (b) Wavecrest.

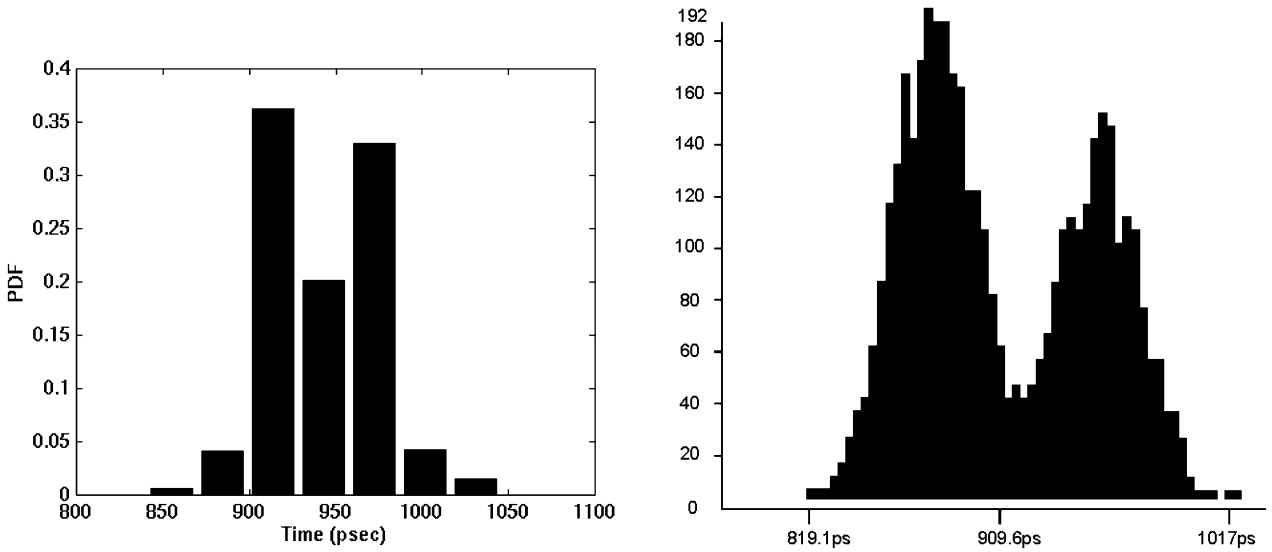
one were to exercise greater control over the cell placement, then we would expect a higher timing resolution.

To test this circuit, we made use of a Teradyne A567 mixed-signal tester to generate a 2 MHz repetitive data signal with a jitter component having Gaussian statistics. The experimental setup is shown in Fig. 31. Subsequently, the RMS and peak-to-peak values of the histogram are derived. The jittery signal was designed to have zero mean, an RMS value of 1.03 ns and an 8-ns peak-to-peak value. The theoretical histogram is shown in Fig. 32(a). The component-invariant VDL with a 0.566 ns timing resolution was then used to measure the characteristics of this signal with 1500 samples. The resulting histogram is displayed in Fig. 32(b). Here the RMS value was found to be 1.27 ns and the peak-to-peak value was found to be 9.05 ns. In the case of the RMS value, the experimental error was 0.24 ns, which is within the timing resolution of the VDL, i.e., 0.566 ns.

A second test was run, but this time we made use of the component-invariant VDL that had a 1.22 ns timing resolution. In this case, the jitter was designed to have an RMS value of 2.06 ns and a 16 ns peak-to-peak value. The histogram of the Jitter input is shown in Fig. 33(a). Fifteen hundred samples of this jitter were then gather by the VDL and the results are shown in Fig. 33(b). The measured distribution has an RMS value of 2.64 ns and a 19.8-ns peak-to-peak value. In the case of the RMS value, the experimental error was 0.58 ns which is again within the timing resolution of the VDL, i.e., 1.22 ns.

Deviations of the experimental results from the theoretical are speculated to be caused by the internal jitter of the tester and by the jitter generated by the VDL. Nonetheless, the measurements correlate very well with each other.

To illustrate the test time reduction that is possible when an array of VDL are utilized, we summarize in Table V the test time required for two VDLs tuned to a 0.5466 and 1.22 ns timing



(a) (b)

Fig. 29. Histograms for sinusoidal distributed jitter from (a) VDL and (b) Wavecrest.

TABLE IV
JITTER MEASURED USING 18.9 PS TIMING RESOLUTION VDL

Jitter Distribution	Measurement Type	VDL (18.9 ps timing resolution)	Wavecrest (as reference)
Gaussian	RMS	21.1 ps	18.68 ps
Gaussian	Peak to peak	158.2 ps	124.5 ps
Sinusoidal	RMS	32.5 ps	41.94 ps
Sinusoidal	Peak to peak	234.5 ps	197.8 ps

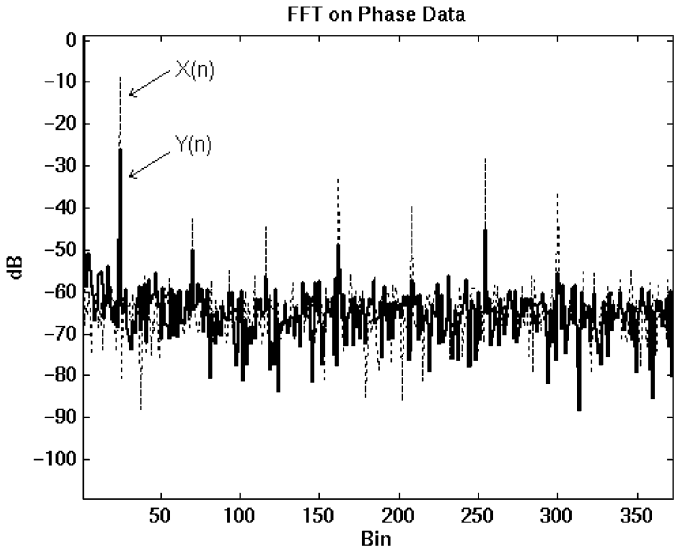


Fig. 30. A comparison of the frequency spectrum of a sinusoidal distributed jitter before and after the VDL.

resolution, and when both are utilize during the time measurement. As is clearly evident in the case cited, when the two VDLs are combined, a significant reduction in test time is achieved. Since the efficiency of the time reduction depends on the time grid location of the VDLs, if one were to exercise greater control over the cell placement, then we would expect even a greater improvement in test time reduction.

C. Limiting Factors

Although very high-timing resolution can be obtained by tuning the oscillation periods of the clock and data delay lines, the maximum resolution is limited by some basic characteristics of the VDL circuit. In the design of this paper, we saw significant detection errors when the timing resolution was driven below 15 ps. Hence, we limited our timing resolution to be no less than 18.9 ps. Below are several reasons for this error.

1) Metastability in the D-Latches: As resolution increases, the probability that the setup time between clock and data signals in the phase detector is violated becomes higher. This results in exponentially increasing propagation delay and may drive the circuit into a metastable state. This is similar to the case of a traditional or standard open loop vernier design which uses D flip-flops to latch signals. If the *D*-latches do not have enough bandwidth to latch small time difference signals, metastability will occur in any one of the latches in the delay line that experiences a small time difference. Although, careful design and layout of the *D*-latches can be used to minimize this effect, it cannot be eliminated entirely [12]. The probability of failure is usually characterized by a mean-time-between failure (MTBF) measure which can be approximated in terms of the VDL design parameters as follows:

$$\text{MTBF} \approx \frac{T_f \cdot e^{(T_f - t_{su} - t_d)/\tau}}{2 \cdot R \cdot T_w}. \tag{21}$$

Here, T_f is the period of the clock triggered oscillator, τ, t_d, and t_{su} is the time constant, maximum propagation delay and setup time of the *D*-latch, respectively, *R* is the rate at which the data changes and T_w is the metastability window parameter expressed in seconds [13], [14]. Here, T_w is defined as the minimum time difference between the rising edge of the clock and data signals such that no metastability effect occur. In the case

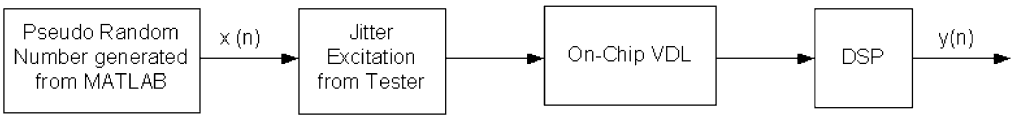
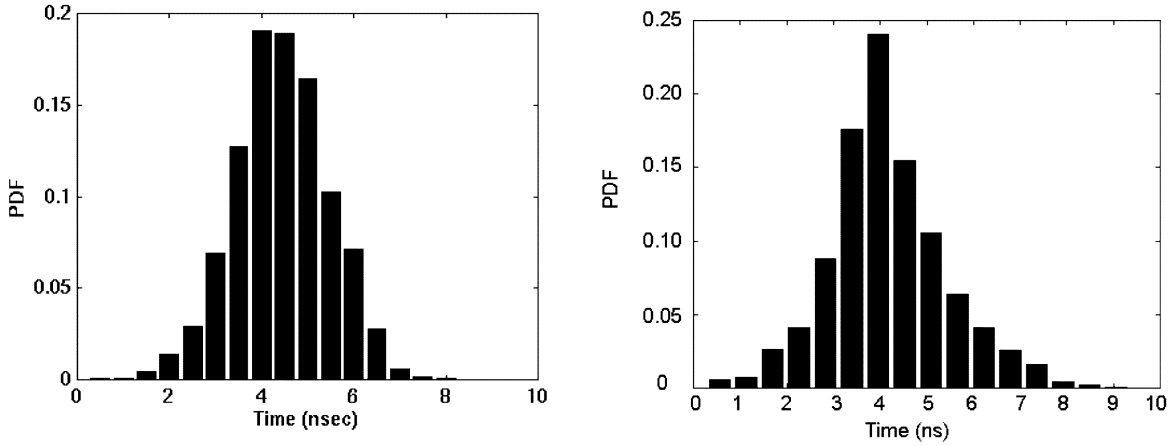
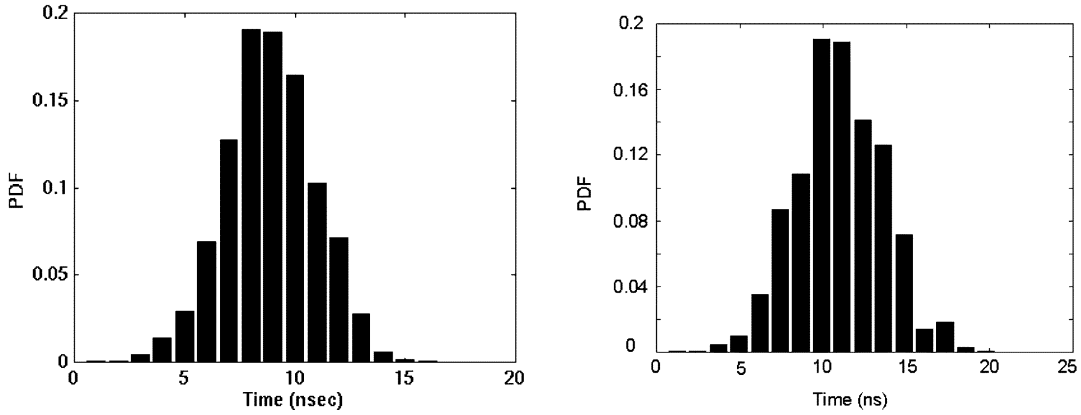


Fig. 31. Test setup.



(a) (b)

Fig. 32. Histograms for 0.566-ns VDL. (a) Theoretical. (b) Experimental.



(a) (b)

Fig. 33. Histograms for 1.22-ns VDL. (a) Theoretical. (b) Experimental.

TABLE V
TEST TIME REDUCTION (PEAK-TO-PEAK JITTER OF 45 ns)

VDL Used	Test Time
0.566 ns-resolution VDL	196635 clock cycle
1.22 ns-resolution VDL	96235 clock cycles
Both VDLs	81960 clock cycles

of our component-invariant VDL, R can be expressed as $1/\Delta T$ since the metastability event can only occur within the time ΔT. Therefore, (21) can be written as

$$\text{MTBF} \approx \frac{T_f \cdot \Delta T \cdot e^{(T_f - t_{su} - t_d)/\tau}}{2 \cdot T_w}. \tag{22}$$

One can observe from (21), that the MTBF will improve with a larger T_f and smaller metastability window T_w. Unfortunately, the MTBF decreases with finer timing resolution ΔT.

As a first-order approximation, the change in MTBF can be expressed as

$$\left|\frac{\delta(\text{MTBF})}{\text{MTBF}}\right| \approx \frac{\delta(\Delta T)}{\Delta T}. \tag{23}$$

For a change of $\Delta T = 20$ ps to $\Delta T = 15$ ps, we expect to see $|\delta(\text{MTBF})/\text{MTBF}| \approx 25\%$. This supports, at the very least, what we have experimentally observed.

In addition, the metastability effect of the front-end flip-flop in the edge detector can be a source of measurement inaccuracy. As long as the flip-flop can latch the edge of the signal being measured, the measurement can be processed. However, when the enable signal falls very near the limits of the setup time of the flip-flop, a metastability condition can arise resulting in a measurement error. In general, all the flip-flops used in the circuit need to have high bandwidth in order to minimize the chances of metastability occurring.

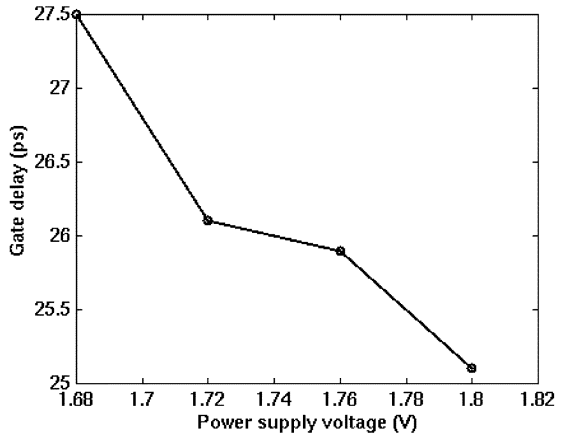


Fig. 34. Delay versus power supply.

2) Resolution Limited by Noise: Another limiting factor is the internal noise from the power supply and substrate that couples in from the analog and digital grounds of the circuit [16]. The variation in the delay for a single buffer due to a change in power supply is summarized in Fig. 34. Although, the sensitivity of a single delay cell to a power supply variation is quite small, this error will accumulate as more stages are incorporated into the design. In particular, due to the nature of VDL, noise from the ring oscillator in this VDL will be additive which degrades the accuracy of measurements. This effect is similar to a traditional VDL where noise from each stage of the delay line will be additive. Effectively, if there are N stages in a traditional VDL and if each stage has Gaussian distributed noise with standard deviation of σ, the Nth stage will have Gaussian distributed noise with standard deviation of $\sqrt{N} \cdot \sigma$ [17]. In the case of the component-invariant VDL described in this paper, it will have similar noise property as the traditional VDL, since each oscillation cycle of the oscillator in this new VDL effectively corresponds to one stage of the traditional VDL. However, if the oscillators are free running, noise accumulated within the oscillator will be passed on from one measurement to the next. Therefore, it is imperative that the oscillators are reset after each measurement so that the noise does not accumulate. So in conclusion, the accuracy of the component-invariant VDL is degraded by circuit noise in the exact same manner as a traditional VDL. In practice, it is clear that a clean power supply for the component-invariant VDL is essential in order to isolate power supply noise coupled from circuits other than the DUT on the same IC. However, the substrate of the component-invariant VDL will still be quite noisy due to common substrate in most CMOS technology. Clearly in order to obtain high resolution, a fully differential structure can be used to reject signal that are common to both delay lines of the component-invariant VDL.

3) Noise-Free Clock: Although this design does not require a jitter-free clock during calibration, it does require a relatively clean clock in order to perform a measurement during its measurement phase. This is a fundamental constraint of this design.

V. Conclusion

A high-resolution timing measurement circuit based on a component-invariant or single-stage VDL structure is developed. This circuit is synthesizable whereby precise element matching is not required. The design was implemented on an FPGA as well as a custom IC as a first proof of concept. Experimental results confirm the validity of this approach. In the case of the FPGA implementation, the design requires about 128 macrocells. In the case of an IC implementation in a 0.18-μm CMOS process, the circuit occupies a total silicon area of 0.12 mm^2, while achieving a 18.9 ps timing resolution. Although, the measured timing resolutions from the FPGA are not comparable to that obtained from the custom IC, the FPGA experiment does serve the purpose of demonstrating the ability of the circuit to be synthesized using a RTL description. The component-invariant approach resulted in a significant IC hardware savings when compared to the original VDL circuit, while maintaining similar timing resolution. Although the design is not limited by precise element matching, the frequency characteristics of the D-type flip-flop limits the maximum timing resolution achievable.

References

[1] M. Mota and J. Christiansen, "A four-channel self-calibrating high-resolution time to digital converter," in *Proc. IEEE Int. Conf. Electronics, Circuits, Systems*, 1998, pp. 409–412.

[2] M. S. Gorbics, J. Kelly, K. M. Roberts, and R. L. Sumner, "A high resolution multihit time to digital converter integrated circuit," *IEEE Trans. Nuclear Sci.*, vol. 44, pp. 379–384, Mar. 1997.

[3] Y. Arai, M. Ikeno, M. Sagara, and T. Emura, "Time memory cell VLSI for the phenix drift chamber," *IEEE Trans. Nuclear Sci.*, vol. 45, no. 3, pp. 735–739, Mar. 1998.

[4] E. Raisanen-Rnotsalainen, T. Rahkonen, and J. Kostamovaara, "Time interval digitization with an integrated 32-phase oscillator," in *Proc. IEEE Int. Symp. Circuits Systems*, vol. 5, 1994, pp. 673–676.

[5] S. Sunter and A. Roy, "BIST for phase-locked loops in digital applications," in *Proc. IEEE Int. Test Conf.*, 1999, pp. 532–540.

[6] N. Abaskharoun and G. W. Roberts, "Circuits for on-chip sub-nanosecond signal capture and characterization," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2001, pp. 251–254.

[7] P. Dudek, S. Szczepanski, and J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a vernier delay line," *IEEE J. Solid-State Circuits*, vol. 35, pp. 240–247, Feb. 2000.

[8] B. D. Kulp, "Testing and characterizing jitter in 100BASE-TX and 155.52 Mbit/s ATM devices with a 1 Gsamples/s AWG in an ATE system," in *Proc. IEEE Int. Test Conf.*, 1996, pp. 104–111.

[9] A. H. Chan and G. W. Roberts, "A deep sub-micron timing measurement circuit using a single-stage vernier delay line," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2002, pp. 77–80.

[10] T. H. Lee and A. Hajimiri, "Oscillator phase noise: A tutorial," *IEEE J. Solid-State Circuits*, vol. 35, pp. 326–336, Mar. 2000.

[11] *User's Guide and Reference Manual for DTS-2079, DTS-2077, DTS-2075, 207 900-01 REV A*, Wavecrest Corporation, Road Edina, MN, 2000.

[12] T. A. Jackson and A. Albicki, "Analysis of metastability operations in *D*-latches," *IEEE Trans. Circuits Syst.*, vol. 36, pp. 1392–1404, Nov. 1989.

[13] H. Johnson and M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*. Englewood Cliffs, NJ: Prentice-Hall, 1993.

[14] C. Foley, "Characterizing metastability," in *Proc. IEEE Int. Symp. Advanced Research Asynchronous Circuits and Systems*, 1996, pp. 175–184.

[15] J. Proakis and D. Manolakis, *Digital Signal Processing: Principles, Algorithm, and Applications*, 3rd ed. Englewood Cliffs, NJ: Prentice-Hall, 1996.

[16] F. Herzel and B. Razavi, "A study of oscillator jitter due to supply and substrate noise," *IEEE Trans. Circuits Systems II*, vol. 46, pp. 56–62, Jan. 1999.

[17] J. A. McNeill, "Jitter in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 32, pp. 870–879, June 1997.

Antonio H. Chan (S'96–M'02) received the B.Eng. and M.Eng. degrees from McGill University, Montreal, QC, Canada, in 1999 and 2002, respectively.

In 2002, he was a Founding Technical Member of DFT Microsystems Inc., Montreal, QC, Canada, in the development of high-speed mixed-signal circuits. His main research interests include the design and testing methodology of mixed-mode circuits and systems relating to broadband communication systems.

Gordon W. Roberts (S'85–M'89) received the B.A.Sc. degree from the University of Waterloo, Canada, in 1983 and the M.A.Sc. and Ph.D. degrees from the University of Toronto, Canada, all in electrical engineering, in 1986 and 1989, respectively.

He is currently a Full Professor with McGill University. Montreal, QC, Canada, where he holds the James McGill Chair in the Department of Electrical and Computer Engineering. Over the years, he has conducted extensive research on analog integrated circuit design and mixed-signal test issues. He has cowritten two undergraduate textbooks, entitled: *SPICE For Microelectronic Circuits*, (New York: Oxford Univ. Press) and *An Introduction to Mixed-Signal IC Test Measurement* (New York: Oxford Univ. Press). He is also coauthor of three research monographs: *Analog Test Signal Generation Using Periodic SD-Encoded Data Streams*, (Norwell, MA: Kluwer); *Analog Signal Generation For Built-In Self-Test Of Mixed-Signal Integrated Circuits*; and *Design and Analysis of Log-Domain Filter Circuits*, (Norwell, MA: Kluwer). He has published over 110 papers in scientific journals and conferences, and has contributed 11 chapters to other books.

Dr. Roberts is a past Associate Editor of the IEEE TRANSACTION ON CIRCUITS AND SYSTEMS—PART II: ANALOG AND DIGITAL SIGNAL PROCESSING, and past associate editor for the *IEEE Design and Test of Computers Magazine*. He has also been a Distinguished Lecturer for the IEEE Computer Society and the Circuits and Systems Society. As a Professor, he has received numerous Department, Faculty, and University Awards, and has received several IEEE Awards for his work on mixed-signal testing. Currently, he is the Program Chair of the IEEE International Test Conference.