CES Chair for Embedded Systems

Prof. Dr. J. Henkel

Customized Embedded Processor Design

Lab SWS:4 ECTS:4 (SS2021)

The design of embedded processors, has experienced significant progress since past few years. This development has been characterized by the increasing demand for application-specific solutions in order to fulfil the diverse and contradictory requirements of low power consumption, high performance, low cost and most importantly an efficient time-to-market deployment of those processors.

Application Specific Instruction Set Processors (ASIP) are customized processors, having a specific instruction-set targeting a specific application to achieve an optimal solution for the above requirements. This customization can be addressed at different architectural levels by defining customized instructions, including/excluding predefined hardware blocks or setting processor parameters. We will select an application, profile it, design a power/area/speed efficient ASIP, and then use our infrastructure to benchmark it to compare cost & benefit in terms of performance, power, area, etc.

The **ASIP design flow** (Fig.1), includes analysing and profiling the targeted application, defining an ASIP accordingly, creating the special instruction, embedding required hardware blocks or configuring different architectural parameters. The synthesizable hardware description and complete compiler tool chain are generated automatically, and then the customized processor is implemented on an FPGA platform (Fig.5) using lab setup of Fig.4. This processor can be benchmarked for the given constraints using QuestaSim and Vivado tools.

Lab Structure:

Kick-off: at start of semester by mutual agreement
Weekly Sessions: Eight 2-3hours sessions per week
Lab Groups: Group of 2-3 Students to carry tasks
Mini Project: last session is a mini project, where each group has to customize the processor for a given application and present their work.

Lab Infrastructure: Available infrastructure for an ASIP design flow is based on:

- ASIPmeister: used to design ASIP with new instructions and create compiler tool chain, see Fig.2
- Dlxsim: used for instruction profiling
- QuestaSim: used to test the designed ASIP, see Fig.3
- Vivado: used to measure area, power, and timing
- These tools are auto-integrated via Makefile.

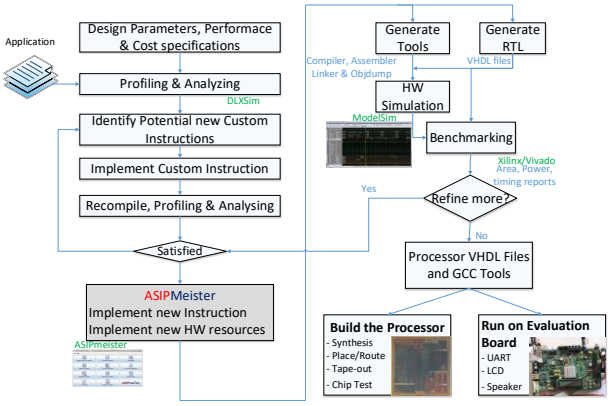

Fig 1: ASIP Design Flow

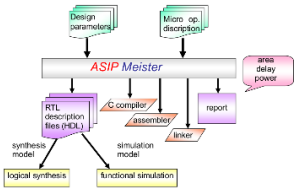

Fig 2: ASIPMeister Input/Output

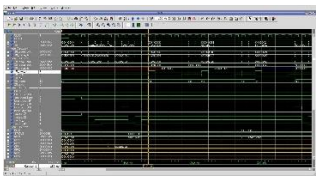

Fig 3: QuestaSim Simulation

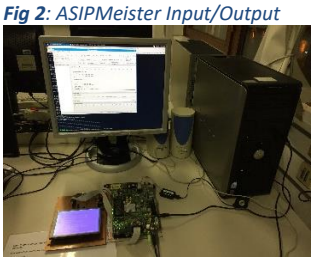

Fig 4: ASIP Lab Setup

Fig 5: FPGA Hardware

Beneficial Knowledge:

- Computer Organization & Architecture
- C & Assembly Language (basic)

Course of Studies:

- Electrical/Computer Engineering/Informatics

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CES Webpage *ILIAS Registration*

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