8 –
a -
jp: makes a relative jump from the actual PC. jpr: makes absolute jump and the difference in Execute phase jp: add the argument to PC. jpr: write the argument in PC
b -
Sub: takes 2 Registers and operate it
Subi: takes an immediate which is extended in ID phase. Because registers are 32b long but immediat is only 16b
c -
Both "Forward" Macros are used to avoid the Pipeline hazards(e.g. WAR and RAW), this macros are ment to move the result of the operation to the next step of the pipeline so the whole system doesnt need to fully stop to wait the result.

16 -
a – 417 clock Cycles
b – yes it has NOP with opcode 0x00000000
c – yes, and the first value word indicates Store Stack Pointer.

18 -
a - the request signal REQ_OUT was 1 then Ack was 0 before the first memory access. After the completion Ack went to 1.
the Data_IN: 0x017EFFC and Data_OUT: 00100000