Tutorial - ModelSim Simulation

Customized Embedded Processor Design

Application Specific Instruction-Set Processors- ASIP
Lab (Prakitikum)

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MODELSIM SIMULATION -TUTORIAL

VHDL Hardware SIMULATION

A. Setting up your first ASIP project directory structure:

1. Login to any *i83labpcXX.itec.kit.edu* directly or using SSH or using X2Go Client. For example, login as *asip-sajjad04* into *i83labpc02.itec.kit.edu*

2. Open shell terminal from the start menu. It should be in your default home directory. Go to the directory:

   ```
   ~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie:$
   ```

3. Set the proper path and parameters in "env_settings" like dlxsim path, project path and project name.

4. Go to the application directory, for example:

   ```
   ~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/Applications/Arith:$
   ```

   and type "***make clean***" clean this directory it there are previously generated files.

5. Generate the Compiler using ASIPmeister if you have a C application.

6. Compile the C application using "***make sim***". A directory "***BUILD_SIM***" is created which contains different temporary files and a .dlxsim file to be simulated in dlxsim (in this case it is "***Arith.dlxsim***"). In this directory, the files "***TestData.IM***" and "***TestData.DM***"are the file used during the ModelSim simulation.

7. Simulate your application in dlxsim simulator using "***make dlxsim***", just to verify the functionality.

8. Go to the directory:

   ```
   ~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie:$
   ```

   Open the ASIPmeister project, modify the CPU if required, and generate VHDL files for simulation/synthesis and files for compiler generation.

   ```
   asip04@i83labpc04:~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie:$ASIPmeister  brownie.pdb &
   ```

   This will create a meister folder in current directory having three subdirectories (brownie.sim, brownie.syn, brownie.sw) and some architectural and description files. This will also generate the compiler and assembler for the CPU.

9. Go to the directory:

```
          ˜/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/ModelSim:$
```

Start the ModelSim using "***vsim***"

```
asip04@i83labpc04:˜/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/ModelSim:$vsim &
```

10. If ModelSim asks for "modelsim.ini" choose the default one like "/Software/ModelSim/Model-Sim_6.6d/modeltech/modelsim.ini"

11. Open File Menu > New > Project and enter a project name and change the project location to the ModelSim directory in your project directory. Confirm the dialog with the OK button.

12. Choose "Add Existing File" button and browse to the "meister/brownie.syn" directory of your ASIP Meister project and select all the VHDL files for synthesis.

13. Again, choose "Add Existing File" button and add the testbench files: "tb_browstd32.vhd", "MemoryMapperTypes.vhd", "MemoryMapper.vhd", and "Helper.vhd" from the ModelSim directory of your current project.

14. [Optional] Configure the CPU Frequency for which you want to simulate your CPU, default is 50 MHz Open the ModelSim testbench ("tb_ browstd32.vhd"), search for CLK_PERIOD, and change the value accordingly in "ns".

B. Compile, Simulate and Run:

1. Compile the project using Compile Menu > Compile Order > Auto Generate. Every file should have a green mark behind its name, showing that the compilation was successful.

2. Run the simulation using Simulate Menu > Start Simulation. Open the work library, mark the entry "***cfg***" (that is the VHDL configuration for the testbench) in the list and press OK. That will start the simulation and you will get another two tabs attached to the Workspace window (sim / Files).

3. To load some predefined simulation settings, choose Tools Menu > Tcl > Execute Macro and select the "*wave_vhdl.do*" file in your ModelSim directory and press OK to load it. The wave-window is filled with certain signals that are useful to evaluate the simulation of the program execution on the processor.

4. [Optional] If you want to dump VCD file of your design for power estimation, you can enter following commands in ModelSim command prompt:

```
VSIM > vsim −t 1ns work.cfg
VSIM > vcd file test.vcd
VSIM > vcd add −r test/dut/*
```

5. Press the button "***Run all***" to run the simulation until it aborts. At the end of a simulation the message "Failure: Simulation End" is printed to show successful end of simulation. At the simulation end, the file "***TestData.OUT***" is created in your ModelSim directory. It contains the content of the simulated memory after the CPU finished working. Therefore, if your algorithm is storing the result in the memory you can find the values here.