KIT-Fakultät für Informatik
Institut für Technische Informatik

# Tutorial - Xilinx ISE Synthesis & Implementation

## Customized Embedded Processor Design

**Application Specific Instruction-Set Processors- ASIP**
Lab (Prakitikum)

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# XILINX ISE -TUTORIAL

## Synthesis and Implementation

**A. Xilinx ISE Framework for Hardware Implementation:**

1. Login to any ***i83labpcXX.itec.kit.edu*** directly or using SSH or using X2Go Client. For example, login as ***asip-sajjad04*** into ***i83labpc02.itec.kit.edu***

2. Open shell terminal from the start menu. It should be in your default home directory. Go to the project directory "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie:$***"

3. Set the proper path and parameters in "env_settings" like dlxsim path, project path and project name.

4. Go to an application directory for example "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/A*** and type "***make clean***" clean this directory it there are previously generated files.

5. Generate the VHDL files and Compiler if you have not done yet.

6. Compile the C application using "***make sim***".

7. Simulate your application in dlxsim simulator using "***make dlxsim***", just to verify the functionality.

8. Go to the directory "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie:$***" Open the ASIPmeister project, modify the CPU if required, and generate VHDL files for simulation/synthesis and files for compiler generation.

9. Go to the directory "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/ModelSim:$***" Simulate the design in ModelSim to verify hardware simulation.

10. Go to the directory "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie:$***" and type "ise &" to start Xilinx ISE.

11. Create new project using File Menu > New Project with following project settings:

```
Project Name: ISE_Framework
Project Path:
home/asip04/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/ISE_Framework
Device Family: Virtex5
Device: xc5vlx110t
Package: ff1136
```

12. Add the design and framework files by selecting "Project Menu > Add Copy of Sources" then brows to:

a. "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/ISE_Framework***" and select all the files

b. "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/ISE_Framework/IP-Cores***" and select all the files

c. "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/meister/brownie.syn***" and select all the files

13. Now you can synthesize, implement and generate programming file for the design using the following respectively:

    a. Processes Menu > Synthesize XST

    b. Processes Menu > Implement Design

    c. Processes Menu > Generate Programming File

14. Once the design is implemented you can see different reports using:

    a. Processes Menu > Place & Route > Generate Post Place & Route Static Timing > Detailed Reports > Place and Route Report

    b. Processes Menu > Place & Route > Generate Post Place & Route Static Timing > Detailed Reports > Post PAR Static Timing Report

    c. Processes Menu > Place & Route > Analyze Post Place & Route Static Timing > Timing Constraints

15. In the directory "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/Applications/Arith:$***" and type "hterm &" to start HyperTerminal to see the UART output if there is any.

16. In the directory "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/Applications/Arith:$***" and type "make fpga", it will combine the generate DM/IM file with your ISE generated bitstream. Finally, a new bitstream file contains your hardware CPU along with corresponding IM/DM files of your application will be generated in the folder "BUILD_FPGA". This bitstream will be used to configure the FPGA.

17. In the directory "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/Applications/Arith:$***" type "make upload": to upload the existing bitstream to the FPGA

**B. Xilinx ISE Framework for Benchmarking:**

18. To accurately measure the critical path and area of the ASIPmeister CPU, you can use ISE_Benchmark folder instead of ISE_Framework folder.

19. Go to the directory "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie:$***" and type "ise &" to start Xilinx ISE.

20. Create new project using File Menu > New Project with following project settings:

```
Project Name: ISE_BenchMark
Project Path:
home/asip04/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/ISE_BenchMark
Device Family: Virtex5
Device: xc5vlx110t
Package: ff1136
```

21. Add the design and framework files by selecting "Project Menu > Add Copy of Sources" then brows to:

    a. "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/ ISE_ BenchMark***" and select all the files

    b. "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/ meister/brownie.syn***" and select all the files

22. Now you can synthesize, implement and generate programming file for the design as before.

23. Once the design is implemented you can see different reports as before.

**C. Xilinx ISE Framework for XPower Power Estimation:**

24. To accurately measure the power consumption of the ASIPmeister CPU, you can create another folder ISE_XPower.

25. Go to the directory "***~/ASIP_SS17/Session1/ASIPMeisterProjects/brownie:$***" and type "ise &" to start Xilinx ISE.

26. Create new project using File Menu > New Project with following project settings:

```
Project Name: ISE_XPower
Project Path:
home/asip04/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/ISE_XPower
Device Family: Virtex5
Device: xc5vlx110t
Package: ff1136
```

27. Add only design files by selecting "Project Menu > Add Copy of Sources" then brows to "***~/ASIP_SS17/S***" and select all the files.

28. Now you can synthesize and implement the design as before.

29. Once the design is implemented you can open XPower tool using Processes Menu > Place & Route > Analyze Power Distribution (XPower Analyzer)

30. Then in XPower Tool, select "File Menu > OpenDesign" and set the properties as follows:

    a. Design File: /home/asip04/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/ ISE_ XPower/brownie32.ncd

    b. Physical Constraint File:/ home/asip04/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/ ISE_ XPower/ brownie32.pcf

    c. Simulation Activity File:/ home/asip04/ASIP_SS17/Session1/ASIPMeisterProjects/brownie/Model

31. After analysing the activity file, the CPU power is estimated. You can see total and dynamic power of the FPGA. Also, you can confirm that the VCD file is loaded properly by verify the clock value in XPower.