Hardware Implementation

Motivation and introduction

In this exercise, you will learn how to synthesize your project, implement it and download it on FPGA board and see the results on the URAT terminal.
The applications used in this session are Bubble sort algorithm (bs_basis) and (bs_bgeu) which will be implemented using the two CPUs dlx_basis and dlx_bgeu to form two versions:
Version1: basis CPU (dlx_basis) with basis bubble sort algorithm (bs_basis).
Version2: CPU which supports the instruction bgeu (dlx_bgeu).

Exercises

1) Creating the applications

1) Check if you directory already has the ISE_Framework folder which contains all the required IP and vhdl files to build you FPGA project.

2) Read the instructions 'Instructions for the FPGA board framework' to create the software and the hardware applications for bs_basis.
3) Create the software and the hardware applications for bs_bgeu.

Now, you have prepared the applications. So, you are ready for the next exercise.

2) Implementing project Version1 (send the solution for questions 4, 5 and 6 by email)
Read the hardware implementation tutorial (chapter 6) and do the following tasks:

1) Start ISE and create a new project which implements Version1 on the FPGA prototyping board
2) Initialize the created Bitstream with the application (chapter 6.3) and configure the FPGA by downloading the programming file on it and check the results

4) If your design works correctly, find out the design statistics (speed and area, see chapter 6.4)
5) Compute the accurate time (in ms) needed to sort the 20 numbers. Use the number of executed cycles (printed on the URAT interface) and the max. CPU frequency given by ISE (and the max. CPU frequency on the FPGA board, where the sorting is still correct) **HINT:** When you run bubble sort a second time by just pressing the reset button, then it will be significantly faster, as the array in the memory was already sorted from the first run! You have to upload the Bitstream again for a second test
6) Analyze the time and find the critical path (see chapter 6.5)

3) Implementing project Version2 (send the solution for questions 2 and 5 by email)

1) Create a new ISE project which implements Version2 on the FPGA prototyping board
2) Repeat the steps (2, 3, 4, 5, 6) from the second exercise
3) Compare the design statistics between the two versions

5) How does this affect the execution time (in cycles and ms)?

For the next session, read chapter 7