CES

Chair for Embedded Systems

Prof. Dr. J. Henkel



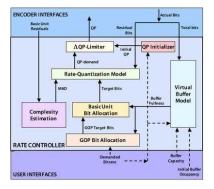
<u>Diplomarbeit</u>

16.April.2008

Development of a Power-Aware Rate Controller for H.264 Video Encoder

H.264/MPEG-4 AVC is one of the latest video coding standards and provides a bit rate reduction of 50% as compared to MPEG-2 with similar subjective visual quality. *Rate Controller* is one of the most important components where the designers have the flexibility to apply their ingenuity and come up with low cost and efficient solutions. The issue of encoder control became more significant with H.264 as this standard offers much more coding options compared with the previous coding standards. Considering the next-generation mobile devices, power is a critical design parameter and a power-aware *Rate Controller* is the key that can control the quality of the encoded video depending upon the available bit-rate, performance, and power budgets.







In our group, we are designing an optimized H.264 encoder application for a dynamically reconfigurable processor that needs to be equipped with a low-complexity power-aware *Rate Controller*. The scope of this Diplomarbeit covers the design of an efficient encoder control system considering power and performance. After designing and testing the control logic in our software framework for H.264, corresponding hardware accelerators need to be synthesized and simulated to get the power requirements.

Requirements:

Good Knowledge of C Knowledge of VHDL

Mentors:

M.Sc.-Inform. Muhammad Shafique, Dipl.-Inform. Lars Bauer,

Chances:

- 1) Learn the basics and current hot topics of Multimedia
- 2) Work with software simulator and synthesize your design for hardware to evaluate for performance and power consumption

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