Karlsruhe Institute of Technology

ASIP Lab Report

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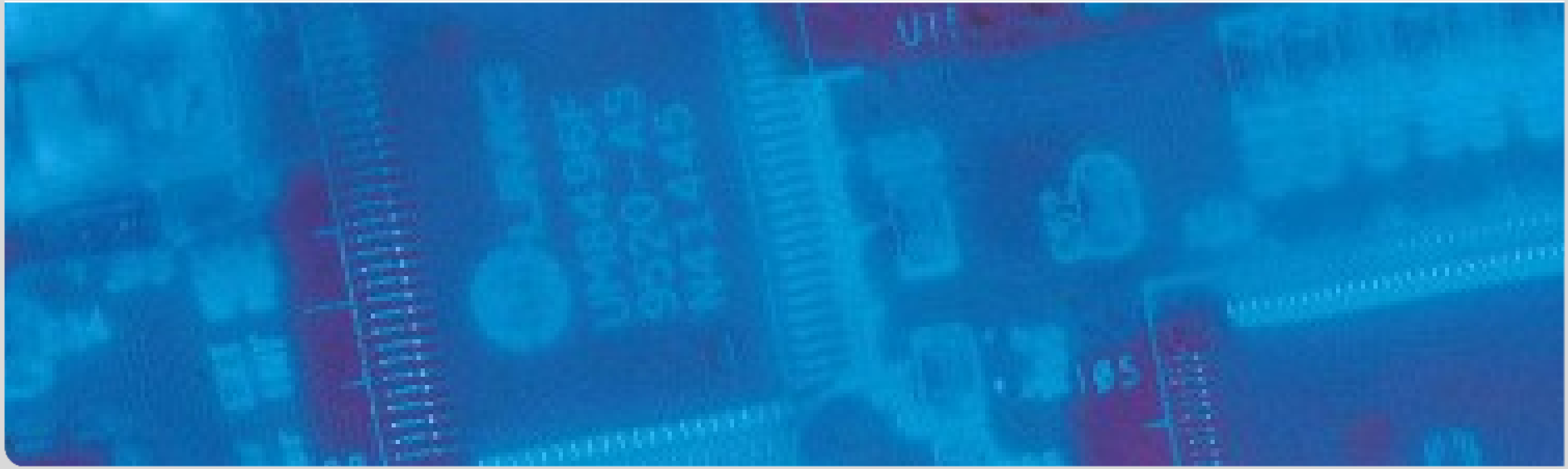

Starting Point

- Basic Processor
  - Benchmarks done with framework
  - Can already play the audio file on the FPGA

Cycles	Critial Path [ns]	Power [W]	Area [Sli. LUTs]	FPGA Freq [MHz]
444 239	*15.418*	*1.489*	*5577*	*100*

Optimizations

- Area
- Performance

Area: Reduce complexity

- Identifying components
  - Unused instructions
  - Unused hardware units
  - Reduce amount of available resource

Area: 32 → 16 registers

- Default 32 registers
  - Next step 16 registers
- Bad tool support
  - Requires a lot of manual work
  - Time constraint
    - 3 Weeks * 5h = 15h available for project
- Worth the risk?

Area: Multiplication

- Used exactly once (in assembly file)
  - SomeVariable = 2 * sizeof(…);
  - Replaced with an addition

- Removed hardware resource (MUL0) & instructions

Cycles	Critial Path [ns]	Power [W]	Area [Sli. LUTs]	FPGA Freq [MHz]
444 239 444 239	*15.418* 15.698	*1.489* 1.486	*5577* 5281	*100* 100

Area: Division

- Used a few times, but only for printing!
  - Removed printing from application

- Removed hardware resource (DIV0) & instructions

Cycles	Critial Path [ns]	Power [W]	Area [Sli. LUTs]	FPGA Freq [MHz]
444 239 436 917	*15.418* 16.171	*1.489* 1.477	*5577* 4858	*100* 100

Area: Remaining OPs

- Exhaustive search of all used instructions in assembly file

- Removed unused instructions

Cycles	Critial Path [ns]	Power [W]	Area [Sli. LUTs]	FPGA Freq [MHz]
444 239 436 917	*15.418* 15.580	*1.489* 1.465	*5577* 4815	*100* 100

Area: Summary

- Removed MUL0, DIV0 and unused instructions
  - Slightly reduced amount of cycles (1.7%)
  - Critical path and frequency constant
  - Slightly reduced power consumption (1.7%)
  - Noticeable area reduction (13.7%)

Cycles	Critial Path [ns]	Power [W]	Area [Sli. LUTs]	FPGA Freq [MHz]
444 239 436 917	*15.418* 15.580	*1.489* 1.465	*5577* 4815	*100* 100

Performance: customization of Instructions

- Identifying possible block of Instructions

  - **Branch statement**

    if (index < 0) index = 0;
    if (index > 88) index = 88;

  - **Shift and Add operations**

    vpdiff += step>>1;
    vpdiff += step>>2;

  - **Prediction operation**

    if (sign) valpred -= vpdiff;
    else   valpred += vpdiff;

Performance: Define new Instructions in CPU

- New instruction type
  - 4 registers

- New instructions Field
  - Calculate(for prediction)
  - Clamp(clamp output value)
  - Shift(for ADD and Shift operation)

Performance: Summary

- ADD clamp, calculate, and shift Instructions
  - reduced amount of cycles (22.7%)
  - Shorter critical path
  - Slightly reduced power consumption (1.02%)
  - increasing area

Cycles	Critial Path [ns]	Power [W]	Area [Sli. LUTs]	FPGA Freq [MHz]
559 177 455 395	*15.418* 8.328	*1.489* 1.507	*5577* 6215	*100* 100

Feedback (1)

- (1) Der notwendige Arbeitsaufwand für Lehrveranstaltung ist...angemessen oder unangemessen?

  What do you think? Why do you think so?

  - Required information scattered in lab manual
  - Tedious tasks (example adding bgeu op to dlxsim)
  - No Copy & Paste in ASIPMeister

Feedback (2)

- (2) Wie ist die Lehrveranstaltung strukturiert? sehr gut sehr schlecht?

  What do you think? Why do you think so?

  - No session specific tutorials
  - Outdated manual / information on session sheets

Feedback (3)

- (3) Which difficulties you faced in doing this lab, please share your feedback.
  - Instructions often unclear
  - ASIPMeister
  - Missing / outdated information