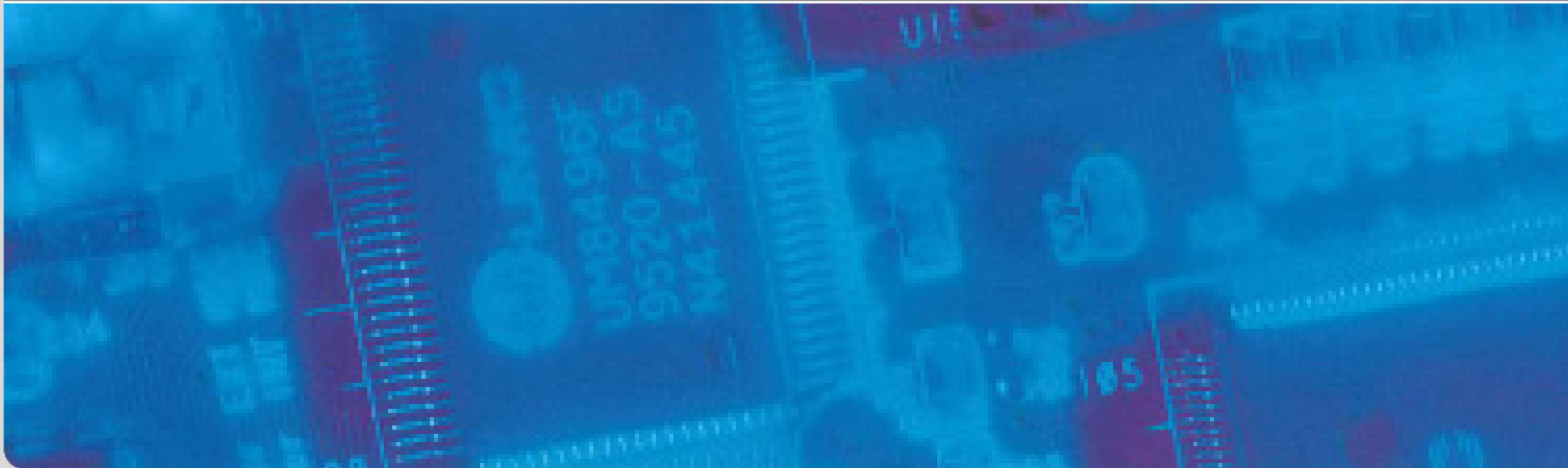


# Praktikum: Entwurf von eingebetteten applikationsspezifischen Prozessoren

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# Overview

- ASIP Design Strategies
- Measurements
- Further possibilities

# ASIP Design Strategies

## ■ 1st Strategy – optimized for **area** and potentially power:

- Reduce resources to required
  - Multiplier removed
- Reduce instructions to required

## ■ 2nd Strategy – optimized for **speed** (potentially energy):

- Add instructions specific to application C code

■ low\_saturate rd, rs0, const  
if ( rs0 < const ) rd = const;

■ high\_saturate rd, rs0, const  
if (rs0 > const) rd = const;

■ cond\_compl rd, rs0, rs1  
if (rs0[bit3]) rd = -rs1;  
else rd = rs1;

```
if ( sign )
    valpred -= vpdiff;
else
    valpred += vpdiff;
```

```
/* Step 5 - clamp output value */
if ( valpred > 32767 )
    valpred = 32767;
else if ( valpred < -32768 )
    valpred = -32768;
```

Normal

```
/*if ( sign )
    temp = -vpdiff;
else
    temp = vpdiff;*/
temp = cond_compl(sign, vpdiff);
valpred += temp;
```

```
/* Step 5 - clamp output value */
valpred = low_saturate1(valpred);
valpred = high_saturate1(valpred);
```

Speed

# Part of Micro Op Description

cond\_compl rd, rs0, rs1

high\_saturate / low\_saturate rd, rs0, const

```
cond = source0[3];
```

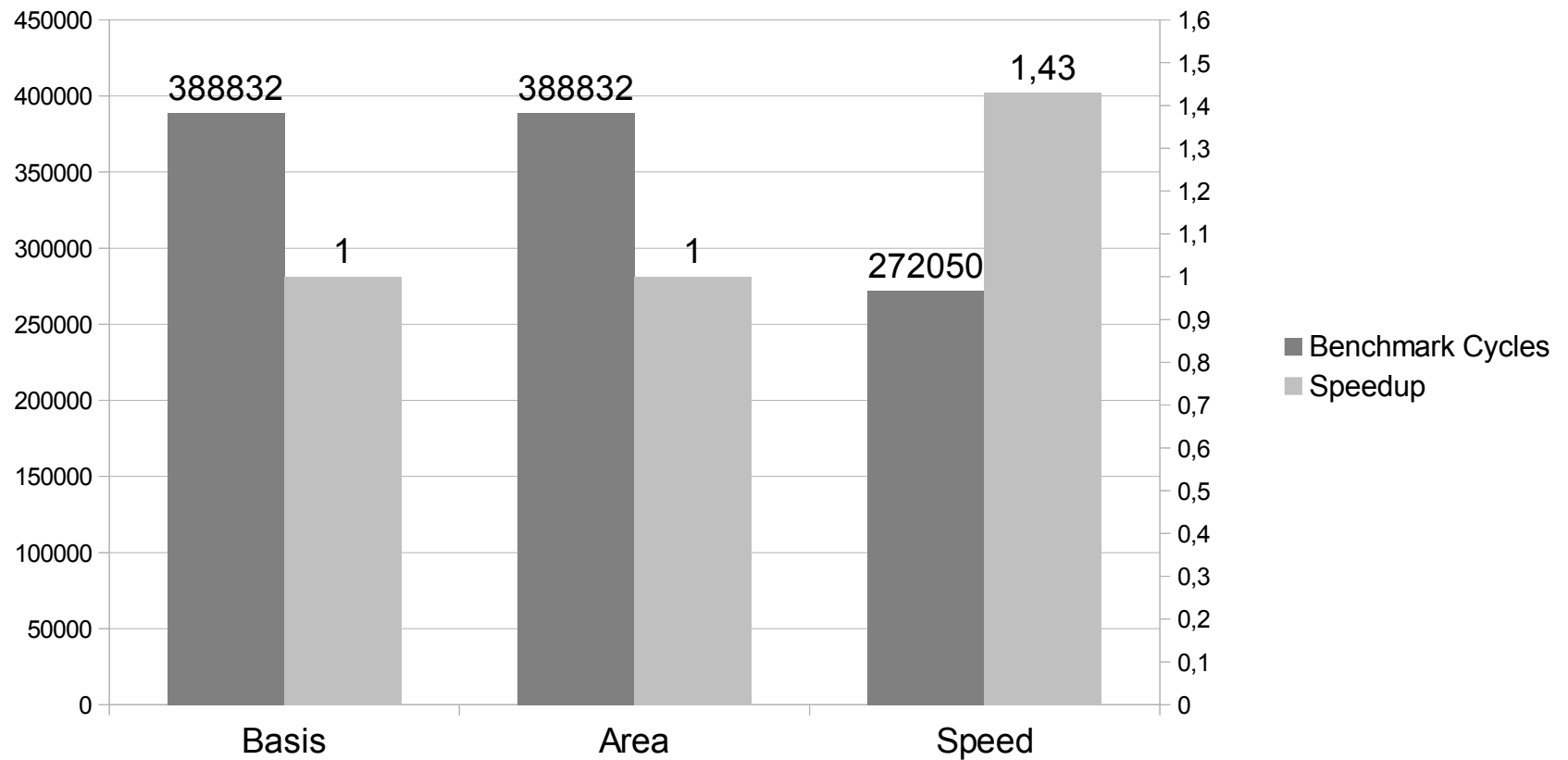
```
result = MUX0.sel(source0,source1,cond);
```

```
res0 = MUX0.sel(zero32,source1,cond);
```

```
res1 = MUX1.sel(source1,zero32,cond);    null = GPR.write0(rd, result);
```

```
<result, flag> = ALU0.sub(res1, res0);
```

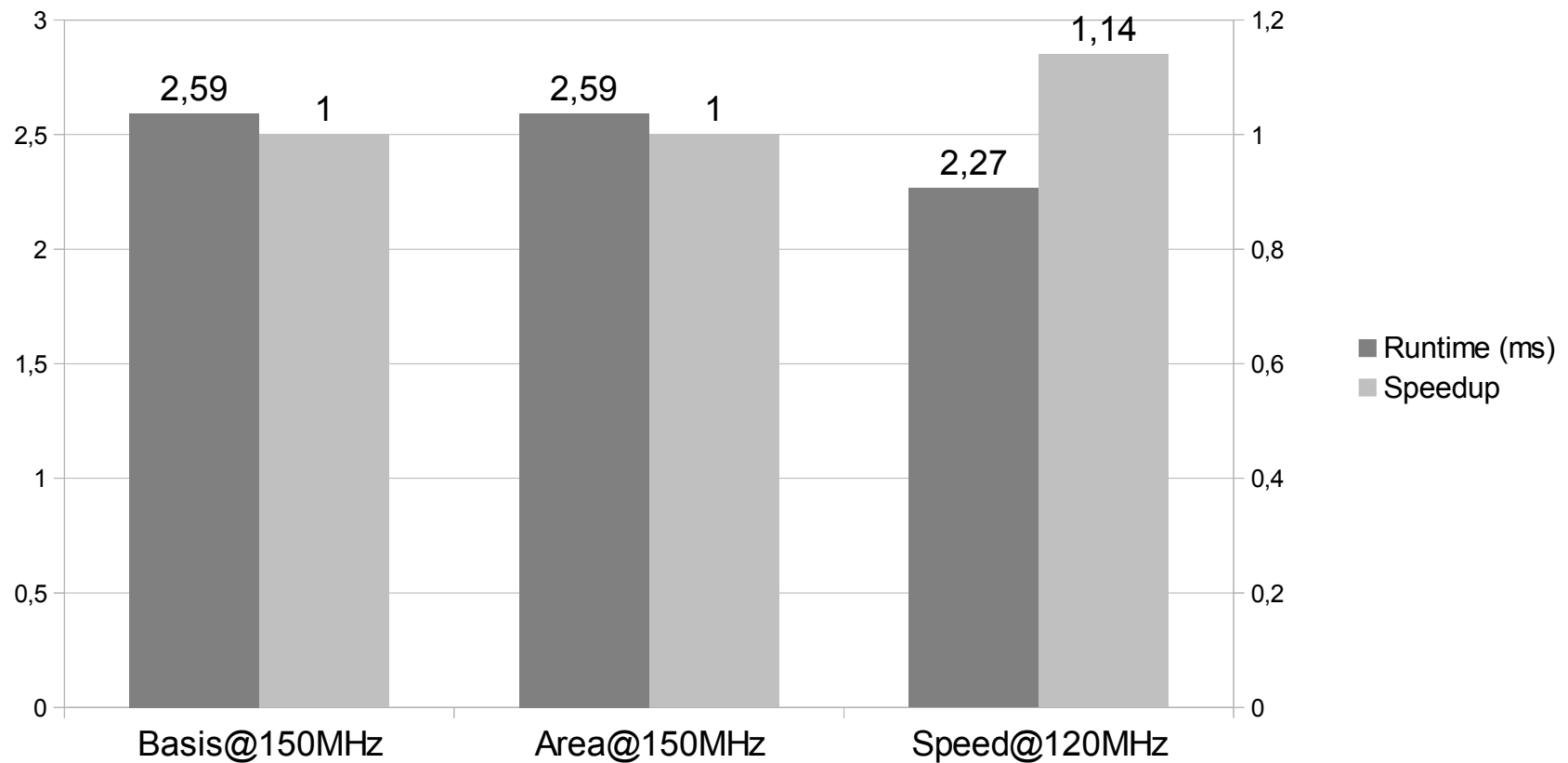
# Cycles



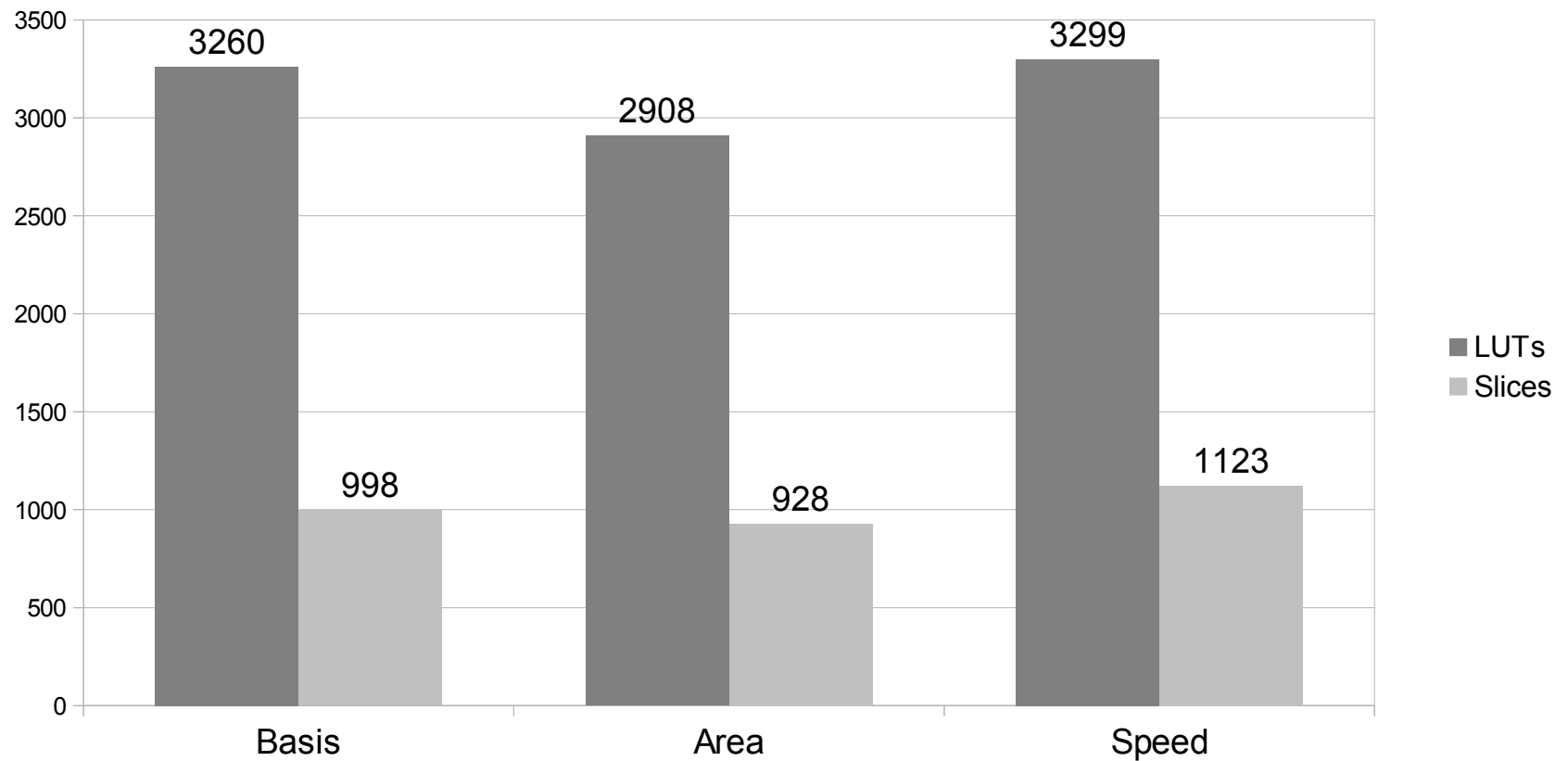
# Possible Frequencies

- Min: Benchmark fulfilled, tested from 30-150 Mhz
- Max: Reported maximum frequency from Xilinx ISE
- Basis
  - Max: 158.328MHz (benchmark used: 150Mhz)
  - Min: 60MHz
- Area
  - Max: 167.3MHz (benchmark used: 150MHz)
  - Min: 60MHz
- Speed
  - Max: 120.395MHz
  - Min: 50MHz

# Benchmark runtime at maximum frequency

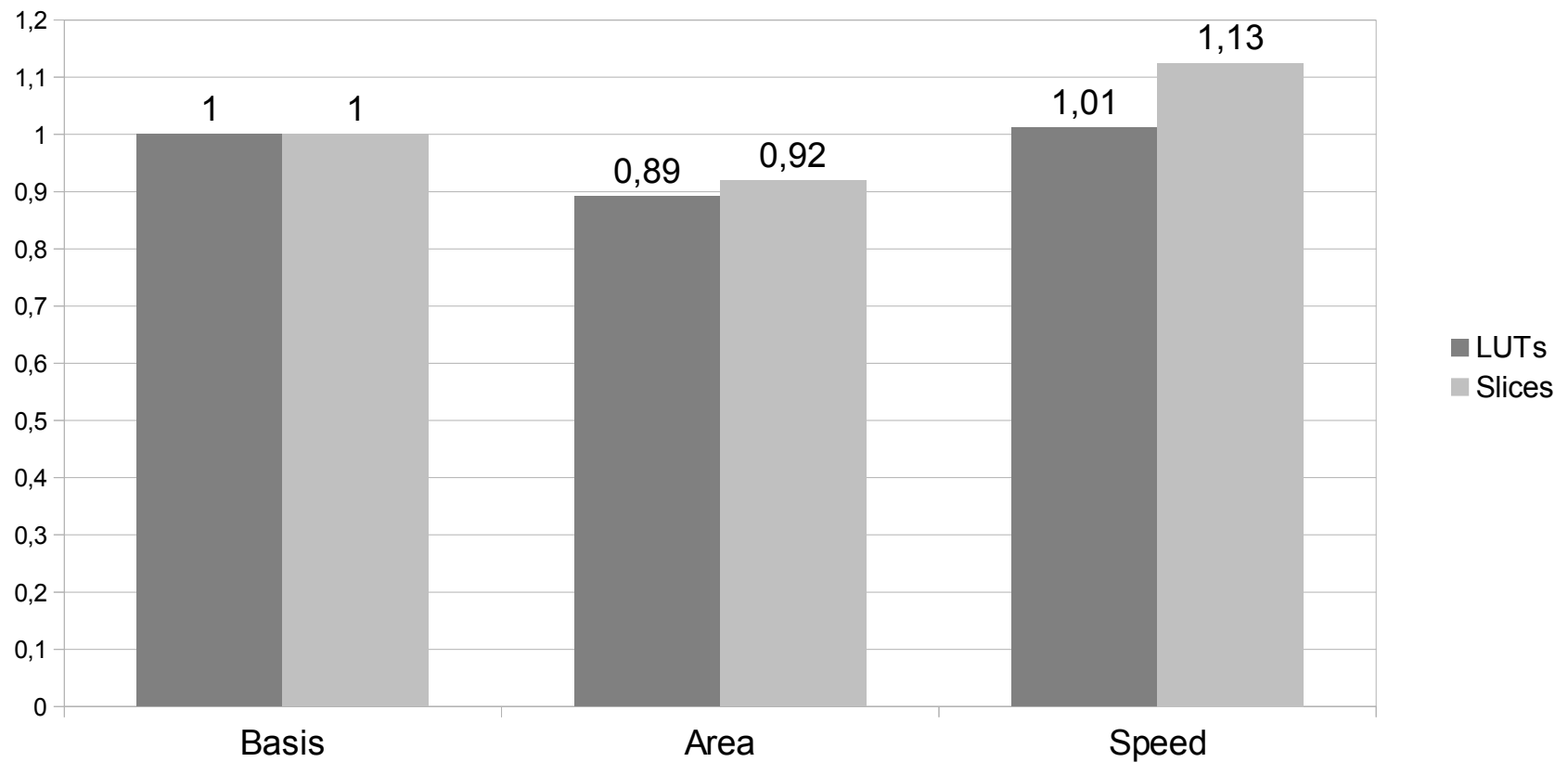


# Required Area

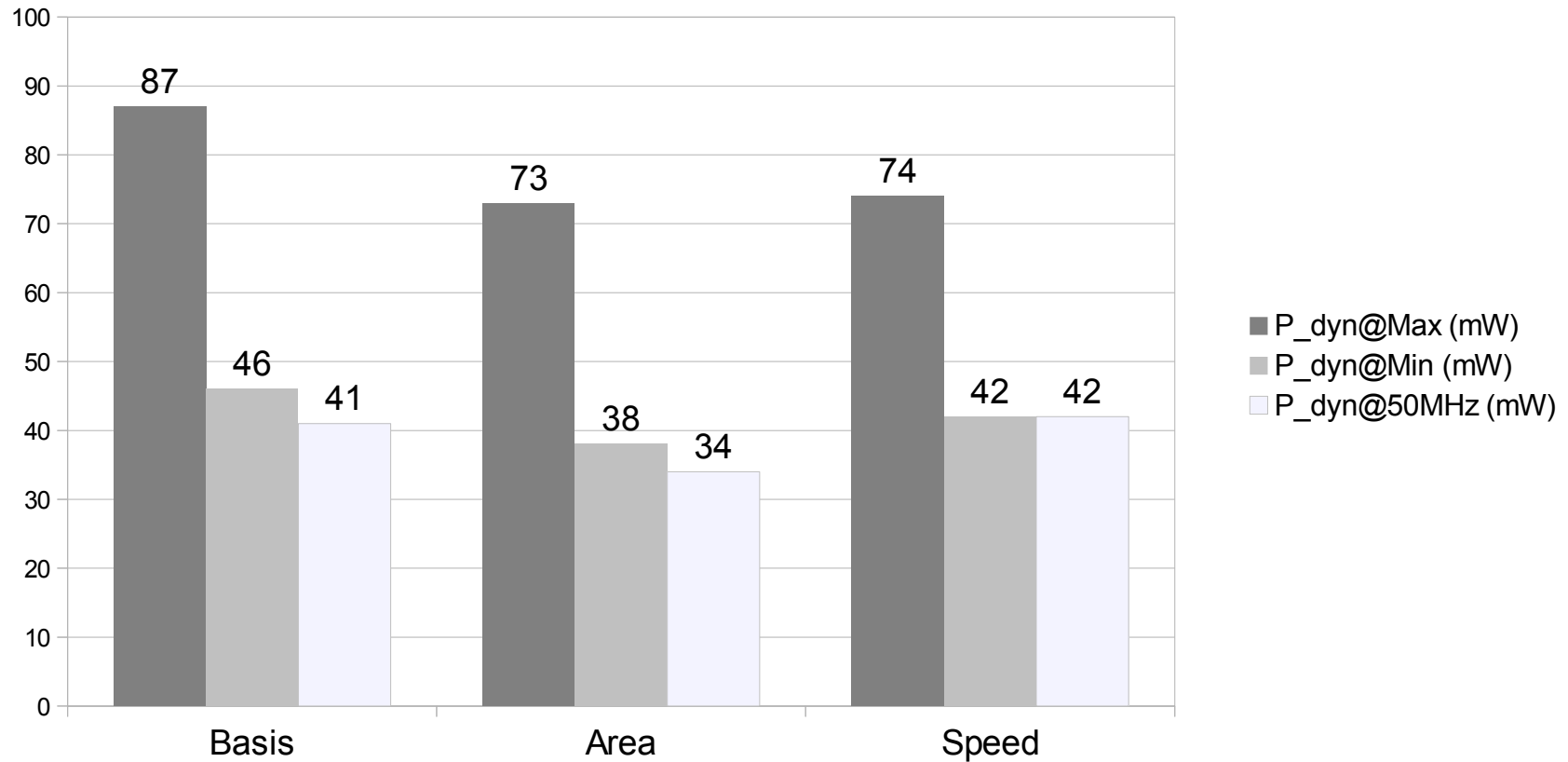




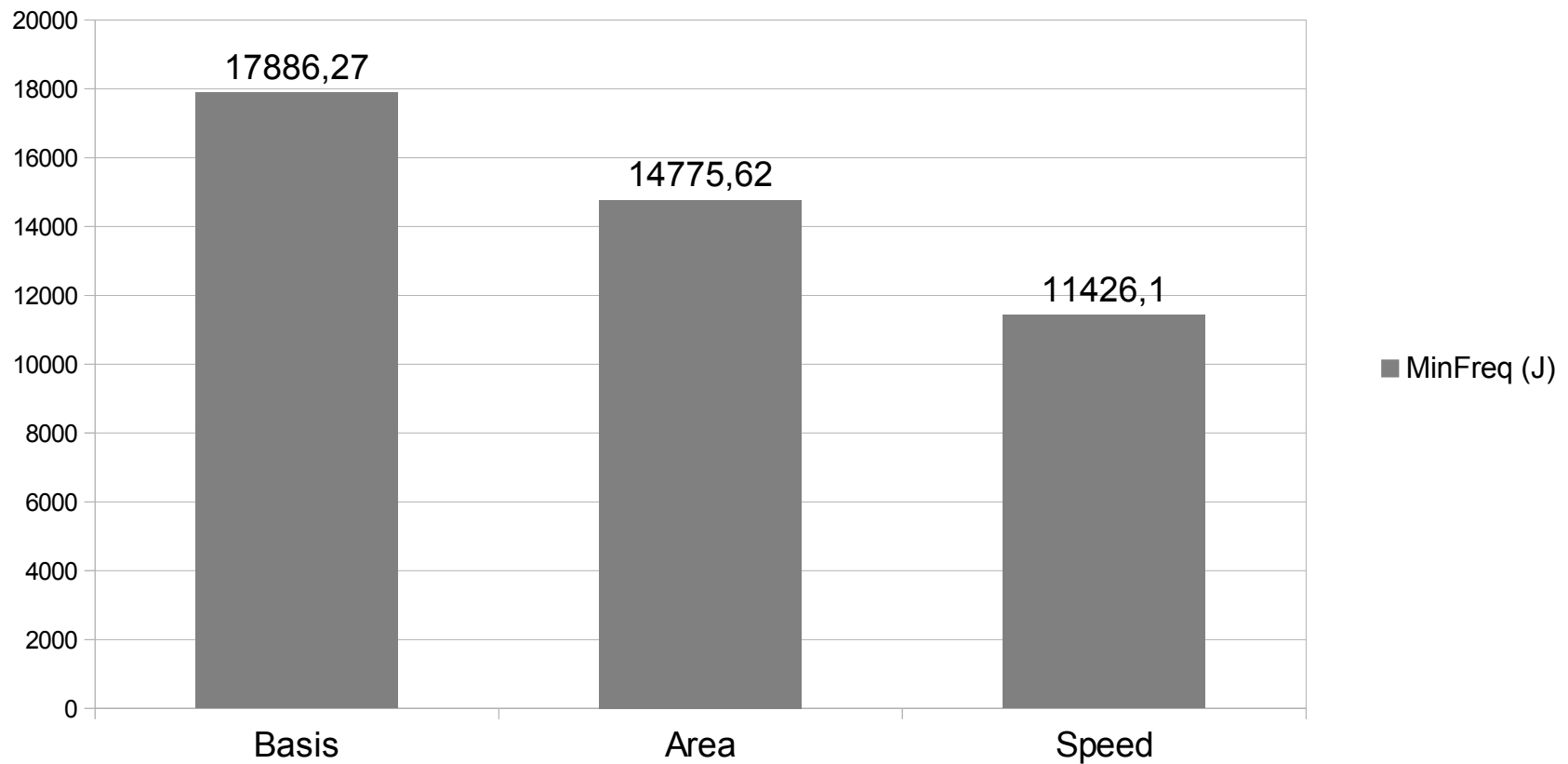
# Required Area (normalized)



# Power



# Energy for Application (minimum Frequency)



# Further possibilities

- Area:
  - Reduce general purpose registers (GPRs)
  
- Speed:
  - Special instructions for every step from 1 to 6
  
- Combine Area+Speed CPUs!

Thanks for your attention!  
Are there any questions?