Platform Flash In-System Programmable Configuration PROMs

DS123 (v1.0) April 29, 2003

Preliminary Product Specification

Features

- In-system programmable 3.3V PROMs for configuration of Xilinx FPGAs
- Low-power advanced CMOS FLASH process
- Endurance of 20,000 program/erase cycles
- Program/erase over full temperature range (–40°C to +85°C)
- IEEE Standard 1149.1 boundary-scan (JTAG) support
- Serial Slow/Fast configuration (up to 40 MHz)
- Cascadable for storing longer or multiple bitstreams
- 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals when VCCO is at 3.3V or 2.5V
- 3.3V tolerant I/O pins accept 3.3V, 2.5V, or 1.8V signals when VCCO is at 1.8V
- 3.3V, 2.5V, or 1.8V output capability
- Available in the V020 package
- Design support using the Xilinx Alliance and Foundation ISE series software packages.
- JTAG command initiation of standard FPGA configuration

Description

Xilinx introduces the Platform Flash series of in-system programmable configuration PROMs (Figure 1). This 3.3V family includes a 4-megabit, a 2-megabit, and a 1-megabit PROM that provide an easy-to-use, cost-effective method for reprogramming and storing large Xilinx FPGA configuration bitstreams. The Platform Flash PROM family supports both Master Serial and Slave Serial FPGA configuration modes.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after $\overline{CE}$ and OE are enabled, data is available on the PROM DATA (D0) pin that is connected to the FPGA D_{IN} pin. New data is available a short access time after each rising clock edge. The FPGA generates the appropriate number of clock pulses to complete the configuration. When the FPGA is in Slave Serial mode, the PROM and the FPGA are clocked by an external clock.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family or with the XC17V00 one-time programmable Serial PROM family.

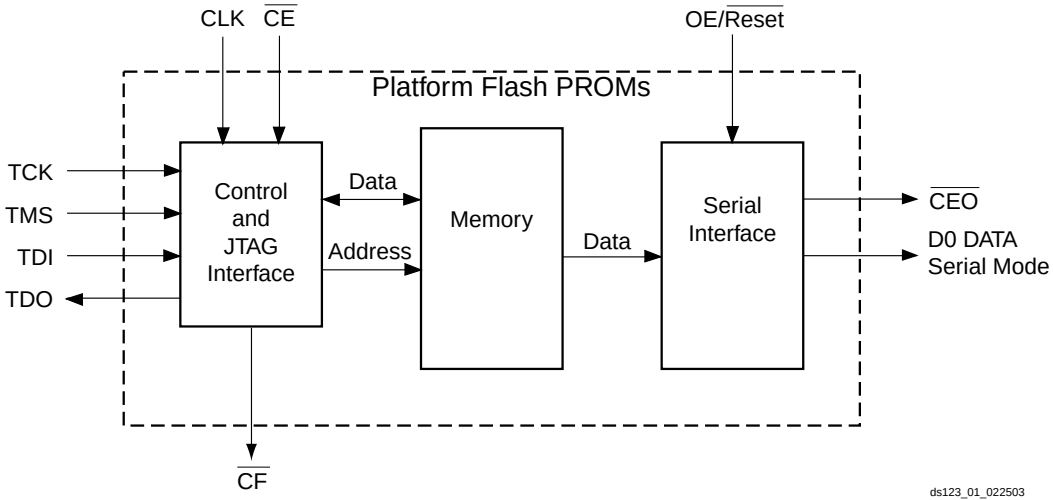


Figure 1: **Platform Flash PROMs Block Diagram**

Pinout and Pin Descriptions

Table 1 provides a list of the pin names and descriptions for the 20-pin V020 package.

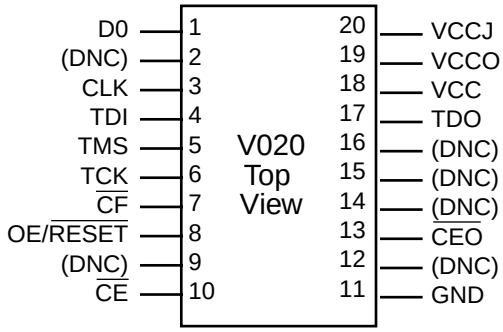
Table 1: **Pin Names and Descriptions**

Pin Name	Boundary Scan Order	Function	Pin Description	20-pin TSSOP (V020)
D0	4	Data Out	Serial Data Output. D0 is the DATA output pin to provide data for configuring an FPGA in serial mode.	1
	3	Output Enable		
CLK	0	Data In	Configuration Clock Input. Each rising edge on the CLK input increments the internal address counter if both $\overline{CE}$ is Low and OE/$\overline{RESET}$ is High.	3
OE/$\overline{RESET}$	20	Data In	Output Enable/Reset (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA output is in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM is reset. Polarity is NOT programmable.	8
	19	Data Out		
	18	Output Enable		
$\overline{CE}$	15	Data In	Chip Enable Input. When $\overline{CE}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA pins are put in a high-impedance state.	10
$\overline{CF}$	22	Data Out	Configuration Pulse (Open-Drain Output). Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command.	7
	21	Output Enable		
$\overline{CEO}$	12	Data Out	Chip Enable Output. Chip Enable Output ($\overline{CEO}$) is connected to the $\overline{CE}$ input of the next PROM in the chain. This output is Low when $\overline{CE}$ is Low and OE/$\overline{RESET}$ input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. $\overline{CEO}$ returns to High when OE/$\overline{RESET}$ goes Low or $\overline{CE}$ goes High.	13
	11	Output Enable		
GND			Ground.	11
TMS		Mode Select	JTAG Mode Select Input. The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50K ohm resistive pull-up on it to provide a logic “1” to the device if the pin is not driven.	5
TCK		Clock	JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.	6
TDI		Data In	JTAG Serial Data Input. This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50K ohm resistive pull-up on it to provide a logic “1” to the system if the pin is not driven.	4
TDO		Data Out	JTAG Serial Data Output. This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50K ohm resistive pull-up on it to provide a logic “1” to the system if the pin is not driven.	17
VCC			+3.3V Supply. Positive 3.3V supply voltage for internal logic.	18

Table 1: **Pin Names and Descriptions *(Continued)***

Pin Name	Boundary Scan Order	Function	Pin Description	20-pin TSSOP (V020)
VCCO			+3.3V, 2.5V, or 1.8V I/O Supply. Positive 3.3V or 2.5V supply voltage connected to the output voltage drivers and input buffers.	19
VCCJ			+3.3V or 2.5V JTAG Signals I/O Supply	20
DNC			Do not connect. (These pins must be left unconnected.)	2, 9, 12, 14, 15, 16

Pinout Diagram



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Xilinx FPGAs and Compatible PROMs

Table 2 provides a list of Xilinx FPGAs and compatible PROMs.

Table 2: **Xilinx FPGAs and Compatible PROMs**

Device	Configuration Bitstream	Platform Flash PROM
Virtex-II Pro™ FPGAs		
XC2VP2	1,305,440	XCF02S
XC2VP4	3,006,560	XCF04S
XC2VP7	4,485,472	XCF04S + XCF01S
XC2VP20	8,214,624	2 of XCF04S
XC2VP30	11,364,608	3 of XCF04S
XC2VP40	15,563,264	4 of XCF04S
XC2VP50	19,021,408	5 of XCF04S
XC2VP70	25,604,096	6 of XCF04S + XCF01S
XC2VP100	33,645,312	8 of XCF04S + XCF01S
XC2VP125	42,782,208	10 of XCF04S + XCF01S
Virtex™-II FPGAs		
XC2V40	360,160	XCF01S
XC2V80	635,360	XCF01S
XC2V250	1,697,248	XCF02S
XC2V500	2,761,952	XCF04S
XC2V1000	4,082,656	XCF04S
XC2V1500	5,659,360	XCF04S + XCF02S
XC2V2000	7,492,064	2 of XCF04S
XC2V3000	10,494,432	3 of XCF04S
XC2V4000	15,660,000	4 of XCF04S
XC2V6000	21,849,568	5 of XCF04S + XCF02S
XC2V8000	29,063,136	7 of XCF04S
Spartan-IIE FPGAs		
XC2S50E	630,048	XCF01S
XC2S100E	863,840	XCF01S
XC2S150E	1,134,496	XCF02S
XC2S200E	1,442,016	XCF02S
XC2S300E	1,875,648	XCF02S
XC2S400E	2,693,440	XCF04S
XC2S600E	3,961,632	XCF04S
Spartan-III FPGAs		
XC3S50	326,784	XCF01S
XC3S200	1,047,616	XCF01S
XC3S400	1,699,136	XCF02S
XC3S1000	3,223,488	XCF04S
XC3S1500	5,214,784	XCF04S + XCF01S
XC3S2000	7,673,024	2 of XCF04S
XC3S4000	11,316,864	3 of XCF04S
XC3S5000	13,271,936	3 of XCF04S + XCF01S

Capacity

Devices	Configuration Bits
XCF04S	4,194,304
XCF02S	2,097,152
XCF01S	1,048,576

In-System Programming

In-System Programmable PROMs can be programmed individually, or two or more can be daisy-chained together and programmed in-system via the standard 4-pin JTAG protocol as shown in Figure 2. In-system programming offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices. The Xilinx development system provides the programming data sequence using either Xilinx iMPACT software and a download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence. The iMPACT software also outputs serial vector format (SVF) files for use with any tools that accept SVF format and with automatic test equipment.

All outputs are held in a high-impedance state or held at clamp levels during in-system programming.

OE/RESET

The ISP programming algorithm requires issuance of a reset that causes OE to pulse Low.

External Programming

Xilinx reprogrammable PROMs can also be programmed by the Xilinx MultiPRO Desktop Tool or a third-party device programmer. This provides the added flexibility of using pre-programmed devices with an in-system programmable option for future enhancements and design changes.

Reliability and Endurance

Xilinx in-system programmable products provide a guaranteed endurance level of 20,000 in-system program/erase cycles and a minimum data retention of 20 years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

Design Security

The Xilinx in-system programmable PROM devices incorporate advanced data security features to fully protect the programming data against unauthorized reading via JTAG. Table 3 shows the security setting available.

The read security bit can be set by the user to prevent the internal programming pattern from being read or copied via JTAG. When set, it allows device erase. Erasing the entire device is the only way to reset the read security bit.

Table 3: **Data Security Options**

Default = Reset	Set
Read Allowed Program/Erase Allowed Verify Allowed	Read Inhibited via JTAG Program/Erase Allowed Verify Inhibited

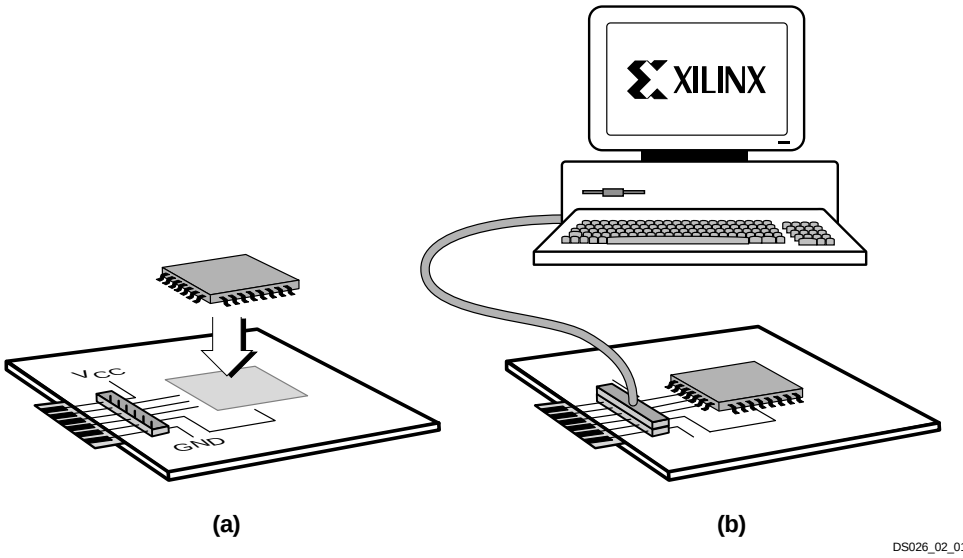


Figure 2: **In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable**

IEEE 1149.1 Boundary-Scan (JTAG)

The Platform Flash PROM family is fully compliant with the IEEE Std. 1149.1 Boundary-Scan, also known as JTAG. A Test Access Port (TAP) and registers are provided to support all required boundary scan instructions, as well as many of the optional instructions specified by IEEE Std. 1149.1. In addition, the JTAG interface is used to implement in-system programming (ISP) to facilitate configuration, erasure, and verification operations on the Platform Flash PROM device.

Table 4 lists the required and optional boundary-scan instructions supported in the Platform Flash PROMs. Refer to the IEEE Std. 1149.1 specification for a complete description of boundary-scan architecture and the required and optional instructions.

Instruction Register

The Instruction Register (IR) for the Platform Flash PROM is eight bits wide and is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI. The detailed composition of the instruction capture pattern is illustrated in Figure 3.

The ISP Status field, IR(4), contains logic “1” if the device is currently in ISP mode; otherwise, it contains logic “0”. The Security field, IR(3), contains logic “1” if the device has been programmed with the security option turned on; otherwise, it contains logic “0”.

Table 4: **Boundary Scan Instructions**

Boundary-Scan Command	Binary Code [7:0]	Description
Required Instructions		
BYPASS	11111111	Enables BYPASS
SAMPLE/ PRELOAD	00000001	Enables boundary-scan SAMPLE/PRELOAD operation
EXTEST	00000000	Enables boundary-scan EXTEST operation
Optional Instructions		
CLAMP	11111010	Enables boundary-scan CLAMP operation
HIGHZ	11111100	all outputs in high-impedance state simultaneously
IDCODE	11111110	Enables shifting out 32-bit IDCODE
USERCODE	11111101	Enables shifting out 32-bit USERCODE
Platform Flash PROM Specific Instructions		
CONFIG	11101110	Initiates FPGA configuration by pulsing $\overline{CF}$ pin Low once

	IR[7:5]	IR[4]	IR[3]	IR[2]	IR[1:0]	
TDI->	0 0 0	ISP Status	Security	0	0 1	->TDO

Notes:
1. IR(1:0) = 01 is specified by IEEE Std. 1149.1

Figure 3: **Instruction Register Values Loaded into IR as Part of an Instruction Scan Sequence**

Boundary Scan Register

The boundary-scan register is used to control and observe the state of the device pins during the EXTEST, SAMPLE/PRELOAD, and CLAMP instructions. Each output pin on the Platform Flash PROM has two register stages that contribute to the boundary-scan register, while each input pin only has one register stage.

For each output pin, the register stage nearest to TDI controls and observes the output state, and the second stage closest to TDO controls and observes the High-Z enable state of the pin.

For each input pin, the register stage controls and observes the input state of the pin.

Identification Registers

The IDCODE is a fixed, vendor-assigned value that is used to electrically identify the manufacturer and type of the device being addressed. The IDCODE register is 32 bits wide. The IDCODE register can be shifted out for examination by using the IDCODE instruction. The IDCODE is available to any other system component via JTAG.

The IDCODE register has the following binary format:

```
vvvv:ffff:ffff:aaaa:aaaa:cccc:cccc:ccc1
```

where

v = the die version number

f = the family code (50h for Platform Flash PROM family)

a = the ISP PROM product ID (46h for the XCF04S)

c = the company code (49h for Xilinx)

Note: The LSB of the IDCODE register is always read as logic “1” as defined by IEEE Std. 1149.1.

Table 5 lists the IDCODE register values for the Platform Flash PROMs.

Table 5: **IDCODES Assigned to Platform Flash PROMs**

ISP-PROM	IDCODE
XCF01S	05044093h
XCF02S	05045093h
XCF04S	05046093h

The USERCODE instruction gives access to a 32-bit user programmable scratch pad typically used to supply information about the device's programmed contents. By using the USERCODE instruction, a user-programmable identification code can be shifted out for examination. This code is loaded into the USERCODE register during programming of the Platform Flash PROM. If the device is blank or was not loaded during programming, the USERCODE register contains FFFFFFFFh.

Platform Flash PROM TAP Characteristics

The Platform Flash PROM family performs both in-system programming and IEEE 1149.1 boundary-scan (JTAG) testing via a single 4-wire Test Access Port (TAP). This simplifies system designs and allows standard Automatic Test Equipment to perform both functions. The AC characteristics of the Platform Flash PROM TAP are described as follows.

TAP Timing

Figure 4 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both boundary-scan and ISP operations.

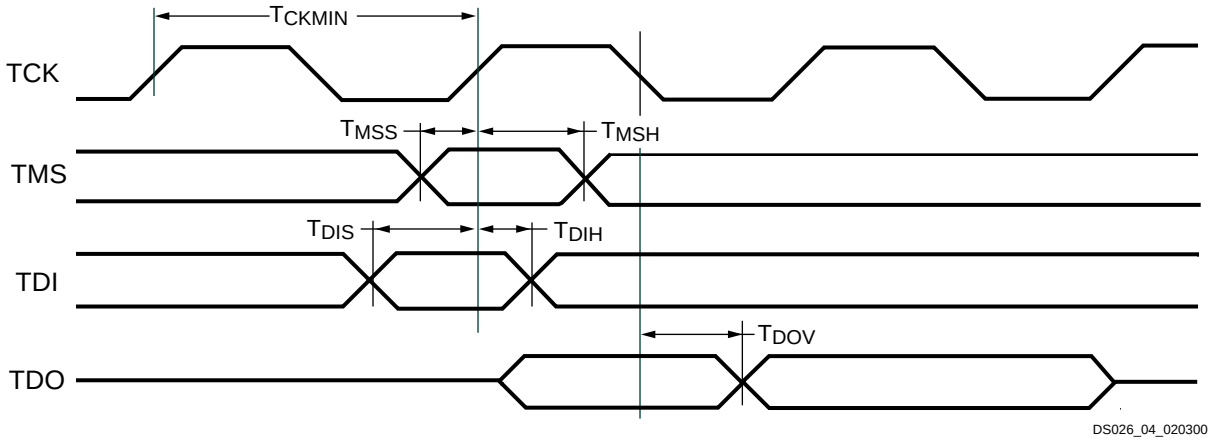


Figure 4: **Test Access Port Timing**

TAP AC Parameters

Table 6 shows the timing parameters for the TAP waveforms shown in Figure 4.

Table 6: **Test Access Port Timing Parameters**

Symbol	Parameter	Min	Max	Units
T_{CKMIN1}	TCK minimum clock period when V_{CCO} = 2.5V or 3.3V	100	-	ns
	TCK minimum clock period when V_{CCO} = 1.8V	TBD	-	ns
T_{CKMIN2}	TCK minimum clock period, Bypass Mode, when V_{CCO} = 2.5V or 3.3V	50	-	ns
	TCK minimum clock period, Bypass Mode, when V_{CCO} = 1.8V	TBD	-	ns
T_{MSS}	TMS setup time when V_{CCO} = 2.5V or 3.3V	10	-	ns
	TMS setup time when V_{CCO} = 1.8V	TBD	-	ns
T_{MSH}	TMS hold time when V_{CCO} = 2.5V or 3.3V	25	-	ns
	TMS hold time when V_{CCO} = 1.8V	TBD	-	ns
T_{DIS}	TDI setup time when V_{CCO} = 2.5V or 3.3V	10	-	ns
	TDI setup time when V_{CCO} = 1.8V	TBD	-	ns
T_{DIH}	TDI hold time when V_{CCO} = 2.5V or 3.3V	25	-	ns
	TDI hold time when V_{CCO} = 1.8V	TBD	-	ns
T_{DOV}	TDO valid delay when V_{CCO} = 2.5V or 3.3V	-	30	ns
	TDO valid delay when V_{CCO} = 1.8V	-	TBD	ns

Connecting Configuration PROMs

Connecting the FPGA device with the configuration PROM (see Figure 5 and Figure 6).

- The DATA output(s) of the PROM(s) drives the D_{IN} input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s) (in Master-Serial mode only).
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The OE/$\overline{RESET}$ pins of all PROMs are connected to the $\overline{INIT}$ pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch.
- The PROM $\overline{CE}$ input can be driven from the DONE pin. The $\overline{CE}$ input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

Initiating FPGA Configuration

The Platform Flash PROMs incorporate a pin named $\overline{CF}$ that is controllable through the JTAG CONFIG instruction. Executing the CONFIG instruction through JTAG pulses the $\overline{CF}$ low once for 300-500 ns, which resets the FPGA and initiates configuration.

The $\overline{CF}$ pin must be connected to the $\overline{PROGRAM}$ pin on the FPGA(s) to use this feature.

The iMPACT software can also issue a JTAG CONFIG command to initiate FPGA configuration through the “Load FPGA” setting.

Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. Xilinx PROMs are designed to accommodate the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated by the FPGA during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines are required to configure an FPGA. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK. If the user-programmable, dual-function D_{IN} pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. The Xilinx FPGA families take care of this automatically with an on-chip pull-up resistor.

Cascading Configuration PROMs

For multiple FPGAs configured as a serial daisy-chain, or a single FPGA requiring larger configuration memories in a serial configuration mode, cascaded PROMs provide additional memory (Figure 5). Multiple Platform Flash PROMs can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the downstream device. The clock inputs and the data outputs of all Platform Flash PROMs in the chain are interconnected. After the last data from the first PROM is read, the next clock signal to the PROM asserts its $\overline{CEO}$ output Low and drives its DATA line to a high-impedance state. The second PROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 7.

After configuration is complete, address counters of all cascaded PROMs are reset if the PROM OE/$\overline{RESET}$ pin goes Low or $\overline{CE}$ goes High.

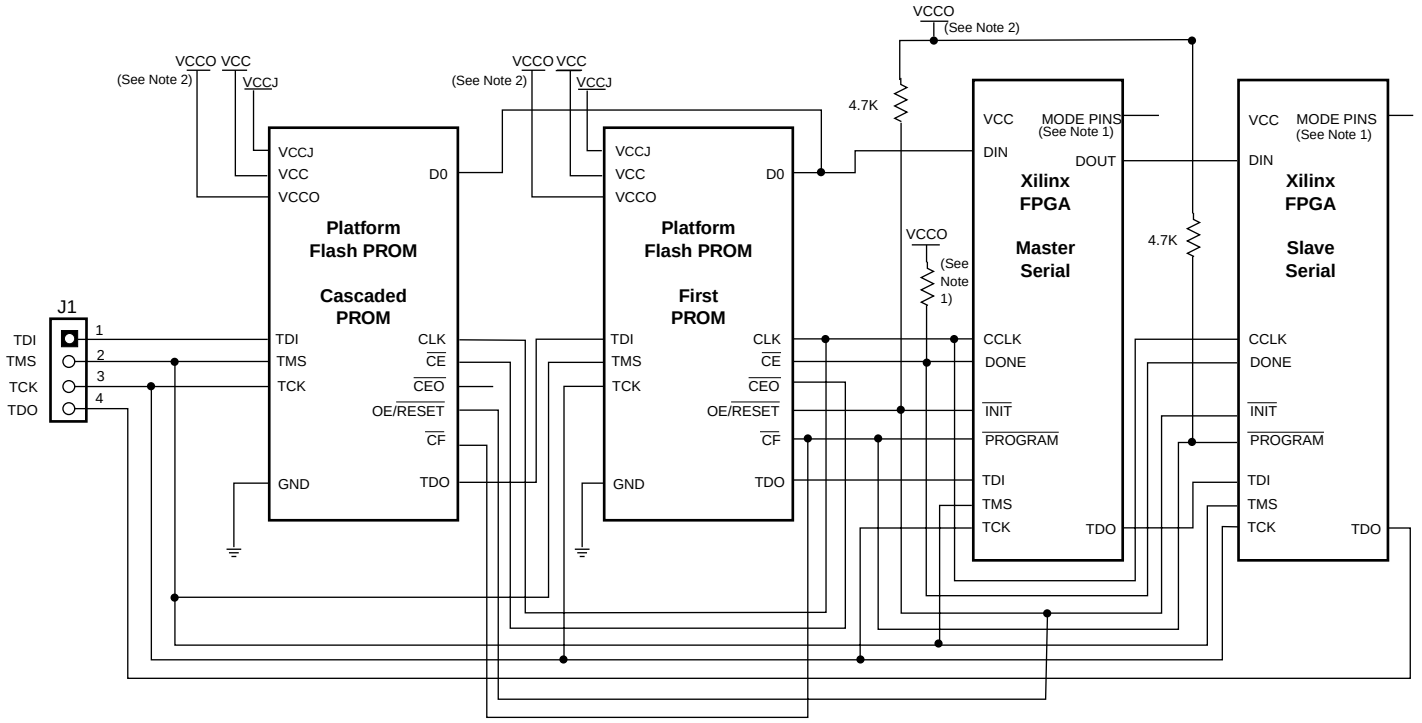
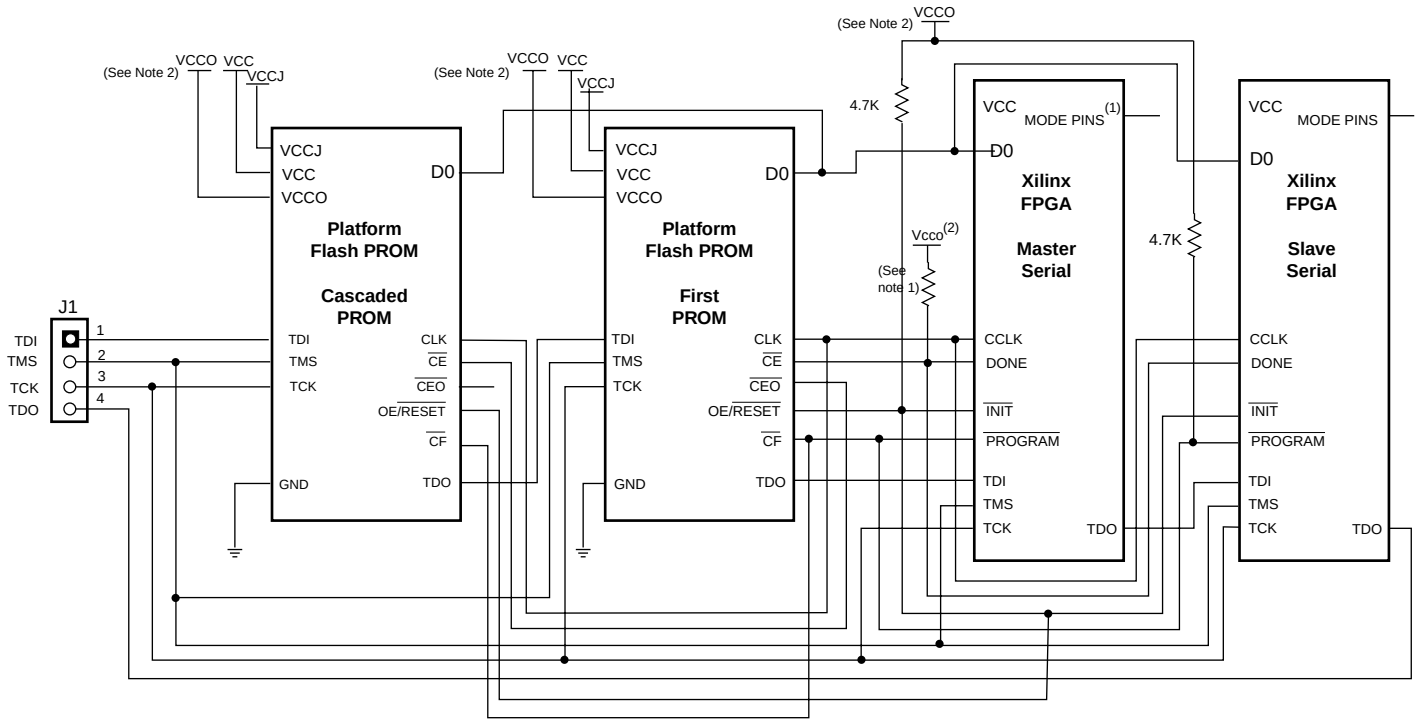


Figure 5: **Configuring Multiple Devices in Master/Slave Serial Mode**



Notes:

1 For Mode pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet.
2 For compatible voltages, refer to the appropriate FPGA data sheet.

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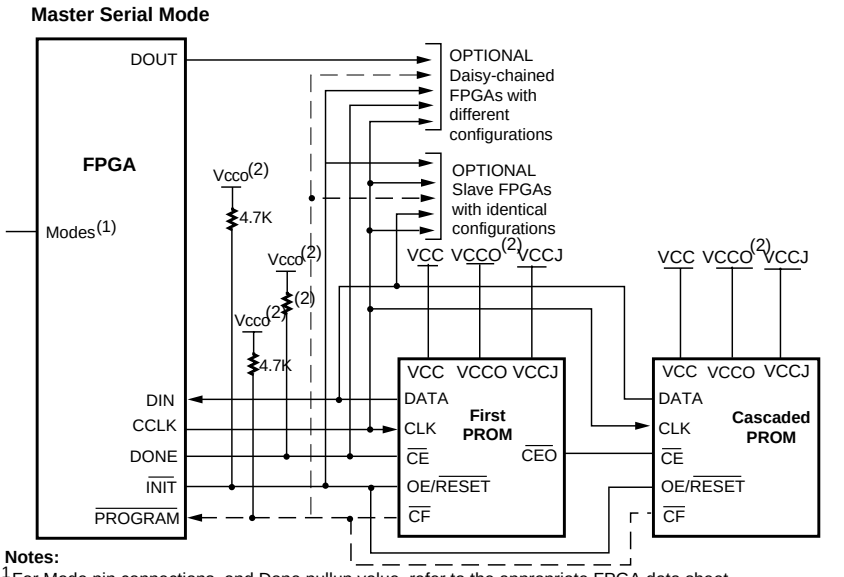
Figure 6: **Configuring Multiple Devices with Identical Patterns in Master/Slave Serial Mode**



Notes:

1 For Mode pin connections and Done pullup value, refer to the appropriate FPGA data sheet.
2 For compatible voltages, refer to the appropriate FPGA data sheet.

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Figure 7: **Master Serial Mode**

Reset Activation

On power up, OE/RESET is held low until the Platform Flash PROM is active (1 ms). OE/RESET is connected to an external resistor to pull OE/RESET HIGH releasing the FPGA INIT and allowing configuration to begin. If the power drops below 2.0V, the PROM resets. OE/RESET polarity is *not* programmable. See Figure 8 for power-up requirements.

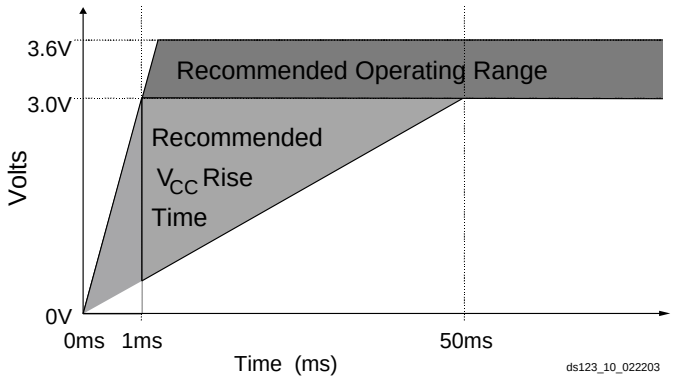


Figure 8: **V_{CC} Power-Up Requirements**

Standby Mode

The PROM enters a low-power standby mode whenever CE is asserted High. The address is reset. The output remains in a high-impedance state regardless of the state of the OE input. JTAG pins TMS, TDI and TDO can be in a high-impedance state or High. See Table 7.

5V Tolerant I/Os

The I/Os on each re-programmable PROM are fully 5V tolerant even when the core power supply is 3.3V if VCCO is at 3.3V or 2.5V. This allows 5V CMOS signals to connect directly to the PROM inputs without damage. In addition, the 3.3V V_{CC} power supply can be applied before or after 5V signals are applied to the I/Os. In mixed 5V/3.3V/2.5V systems, the user pins, the core power supply (V_{CC}), and the output power supply (V_{CCO}) can have power applied in any order. This makes the PROM devices immune to power supply sequencing issues.

Notes:
1. When VCCO is set to 1.8V, the I/Os are only 3.3V tolerant.

Customer Control Bits

The Platform Flash PROMs have various control bits accessible by the customer. These can be set after the array has been programmed using “Skip User Array” in Xilinx iMPACT software. The iMPACT software can set these bits to enable the optional JTAG read security.

Table 7: **Truth Table for PROM Control Inputs**

Control Inputs		Internal Address	Outputs		
OE/RESET	CE		DATA	CEO	I_{CC}
High	Low	If address ≤ TC(1): increment If address > TC(1): don’t change	Active High-Z	High Low	Active Reduced
Low	Low	Held reset	High-Z	High	Active
High	High	Held reset	High-Z	High	Standby
Low	High	Held reset	High-Z	High	Standby

Notes:
1. TC = Terminal Count = highest address value. TC + 1 = address 0.

Absolute Maximum Ratings(1,2)

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to +5.5	V
V_{TS}	Voltage applied to High-Z output	–0.5 to +5.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in.)	+220	°C
T_J	Junction temperature	+125	°C

Notes:
1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins can undershoot to –2.0V or overshoot to +7.0V, provided this over- or undershoot lasts less then 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Internal voltage supply	3.0	3.6	V
V_{CCO}	Supply voltage for output drivers for V_{CCO} at 3.3V operation	3.0	3.6	V
	Supply voltage for output drivers for V_{CCO} at 2.5V operation	2.3	2.7	V
	Supply voltage for output drivers for V_{CCO} at 1.8V operation	1.7	2.0	V
V_{CCJ}	Supply voltage for output drivers for V_{CCO} at 3.3V operation	3.0	3.6	V
	Supply voltage for output drivers for V_{CCO} at 2.5V operation	2.3	2.7	V
V_{IL}	Low-level input voltage for V_{CCO} at 3.3V or 2.5V	0	0.8	V
	Low-level input voltage for V_{CCO} at 1.8V	0	20% V_{CCO}	V
V_{IH}	High-level input voltage for V_{CCO}at 3.3V or 2.5V	2.0	5.5	V
	High-level input voltage for V_{CCO} at 1.8V	70% V_{CCO}	3.6	V
V_O	Output voltage	0	V_{CCO}	V
T_{VCC}	V_{CC} rise time from 0V to nominal voltage(1)	1	50	ms
T_A	Operating ambient temperature	–40°	85°	C

Notes:
1. At power up, the device requires the V_{CC} power supply to monotonically rise from 0V to nominal voltage within the specified V_{CC} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Figure 8.

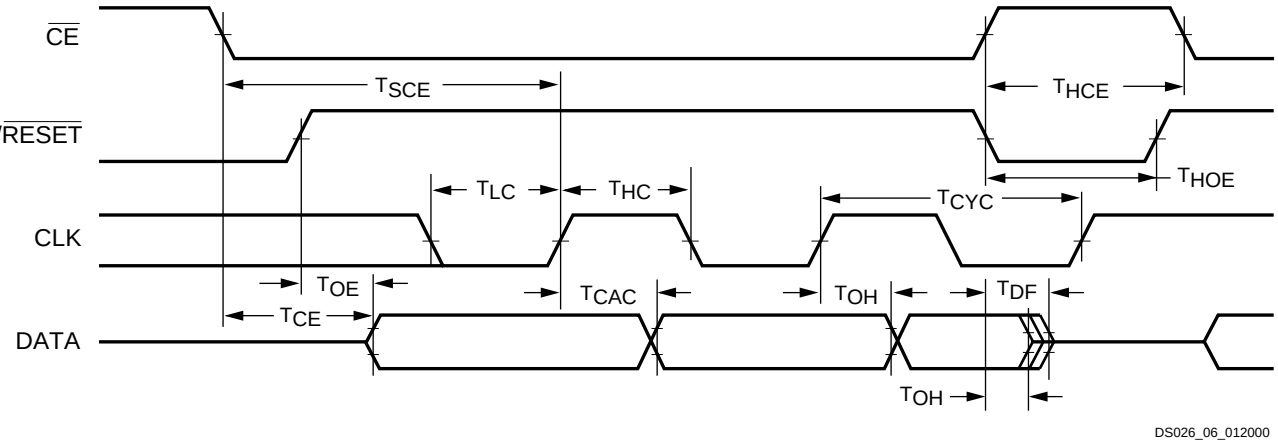
Quality and Reliability Characteristics

Symbol	Description	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/erase cycles (Endurance)	20,000	-	Cycles
V_{ESD}	Electrostatic discharge (ESD)	2,000	-	Volts

DC Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	High-level output voltage for 3.3V outputs	I_{OH} = –4 mA	2.4	-	V
	High-level output voltage for 2.5V outputs	I_{OH} = –500 µA	V_{CCO} – 0.4	-	V
	High-level output voltage for 1.8V outputs	I_{OH} = –50 µA	V_{CCO} – 0.4	-	V
V_{OL}	Low-level output voltage for 3.3V outputs	I_{OL} = 8 mA	-	0.4	V
	Low-level output voltage for 2.5V outputs	I_{OL} = 500 µA	-	0.4	V
	Low-level output voltage for 1.8V outputs	I_{OL} = 50 µA	-	0.4	V
I_{CC}	Supply current, active mode	25 MHz	-	10	mA
I_{CCS}	Supply current, standby mode	-	-	1	mA
I_{ILJ}	JTAG pins TMS, TDI, and TDO pull-up current	V_{CC} = MAX V_{IN} = GND	-	100	µA
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}	–10	10	µA
I_{IH}	Input and output High-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}	–10	10	µA
C_{IN} and C_{OUT}	Input and output capacitance	V_{IN} = GND f = 1.0 MHz	-	10	pF

AC Characteristics Over Operating Conditions for XCF04S, XCF02S, and XCF01S

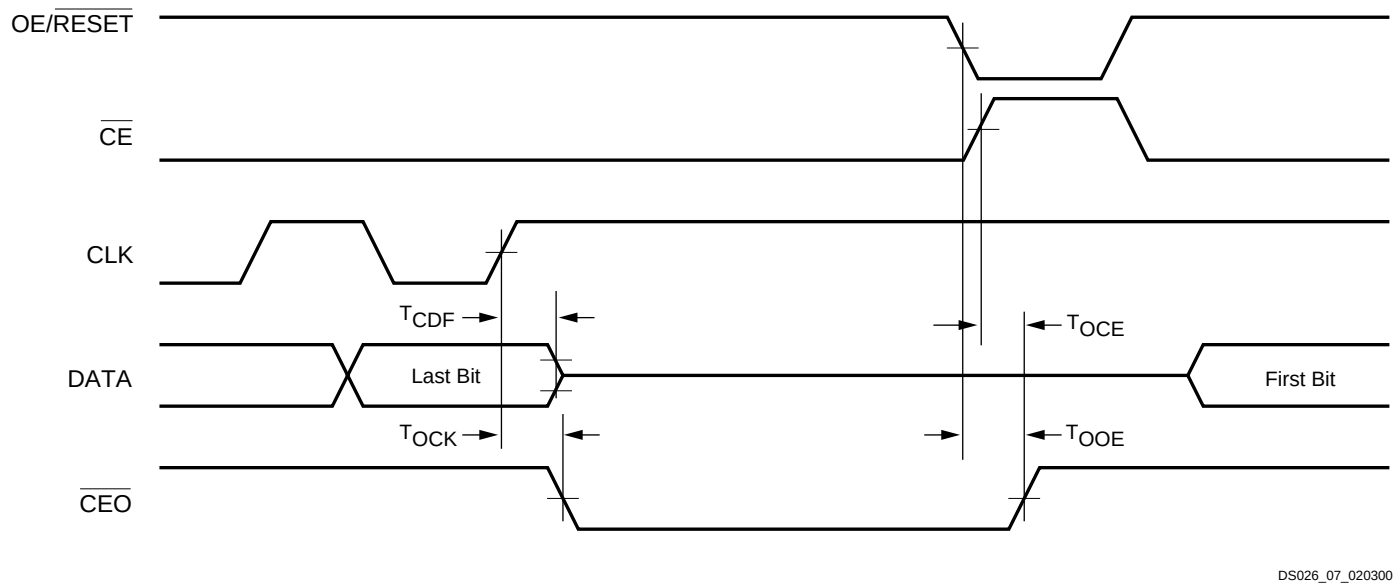


Symbol	Description	Min	Max	Units
T_{OE}	OE/$\overline{\text{RESET}}$ to data delay when V_{CCO} = 3.3V or 2.5V	-	10	ns
	OE/$\overline{\text{RESET}}$ to data delay when V_{CCO} = 1.8V	-	TBD	ns
T_{CE}	$\overline{\text{CE}}$ to data delay when V_{CCO} = 3.3V or 2.5V	-	20	ns
	$\overline{\text{CE}}$ to data delay when V_{CCO} = 1.8V	-	TBD	ns
T_{CAC}	CLK to data delay when V_{CCO} = 3.3V or 2.5V	-	20	ns
	CLK to data delay when V_{CCO} = 1.8V	-	TBD	ns
T_{OH}	Data hold from $\overline{\text{CE}}$, OE/$\overline{\text{RESET}}$, or CLK when V_{CCO} = 3.3V or 2.5V	0	-	ns
	Data hold from $\overline{\text{CE}}$, OE/$\overline{\text{RESET}}$, or CLK when V_{CCO} = 1.8V	TBD	-	ns
T_{DF}	$\overline{\text{CE}}$ or OE/$\overline{\text{RESET}}$ to data float delay(2) when V_{CCO} = 3.3V or 2.5V	-	25	ns
	$\overline{\text{CE}}$ or OE/$\overline{\text{RESET}}$ to data float delay(2) when V_{CCO} = 1.8V	-	TBD	ns
T_{CYC}	Clock periods(7) when V_{CCO} = 3.3V or 2.5V	50	-	ns
	Clock periods when V_{CCO} = 1.8V	TBD	-	ns
T_{LC}	CLK Low time(3) when V_{CCO} = 3.3V or 2.5V	10	-	ns
	CLK Low time(3) when V_{CCO} = 1.8V	TBD	-	ns
T_{HC}	CLK High time(3) when V_{CCO} = 3.3V or 2.5V	10	-	ns
	CLK High time(3) when V_{CCO} = 1.8V	TBD	-	ns
T_{SCE}	$\overline{\text{CE}}$ setup time to CLK (guarantees proper counting)(3) when V_{CCO} = 3.3V or 2.5V	25	-	ns
	$\overline{\text{CE}}$ setup time to CLK (guarantees proper counting)(3) when V_{CCO} = 1.8V	TBD	-	ns
T_{HCE}	$\overline{\text{CE}}$ High time (guarantees counters are reset) when V_{CCO} = 3.3V or 2.5V	250	-	ns
	$\overline{\text{CE}}$ High time (guarantees counters are reset) when V_{CCO} = 1.8V	TBD	-	ns

Symbol	Description	Min	Max	Units
T_{HOE}	OE/$\overline{\text{RESET}}$ hold time (guarantees counters are reset) when V_{CCO} = 3.3V or 2.5V	250	-	ns
	OE/$\overline{\text{RESET}}$ hold time (guarantees counters are reset) when V_{CCO} = 1.8V	TBD	-	ns

Notes:
1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. If T_{HCE} High < 2 µs, T_{CE} = 2 µs.
6. If T_{HCE} Low < 2 µs, T_{OE} = 2 µs.
7. This is the minimum possible T_{CYC}. Actual T_{CYC} = T_{CAC} + FPGA Data setup time. If FPGA Data setup time = 15 ns, the actual T_{CYC} = 15 ns +15 ns = 30 ns.

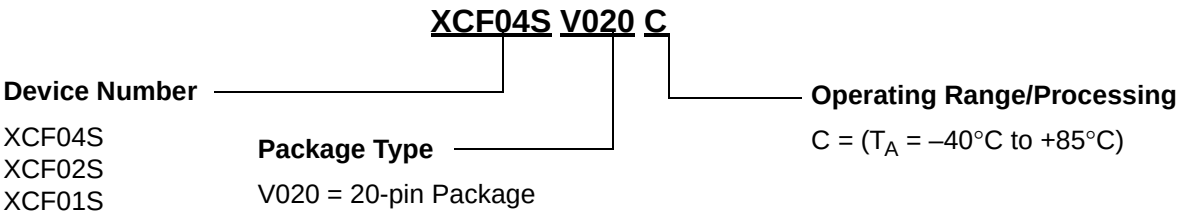
AC Characteristics Over Operating Conditions When Cascading for XCF04S, XCF02S, and XCF01S



Symbol	Description	Min	Max	Units
T_{CDF}	CLK to data float delay(2,3) when V_{CCO} = 2.5V or 3.3V	-	25	ns
	CLK to data float delay(2,3) when V_{CCO} = 1.8V	-	TBD	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3,5) when V_{CCO} = 2.5V or 3.3V	-	20	ns
	CLK to $\overline{CEO}$ delay(3,5) when V_{CCO} = 1.8V	-	TBD	ns
T_{OCE}	CE to $\overline{CEO}$ delay(3) when V_{CCO} = 2.5V or 3.3V	-	20	ns
	CE to $\overline{CEO}$ delay(3) when V_{CCO} = 1.8V	-	TBD	ns
T_{OOE}	OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 2.5V or 3.3V	-	20	ns
	OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 1.8V	-	TBD	ns

Notes:
1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. For cascaded PROMs minimum, $T_{CYC} = T_{OCK}$ + FPGA Data setup time.

Ordering Information

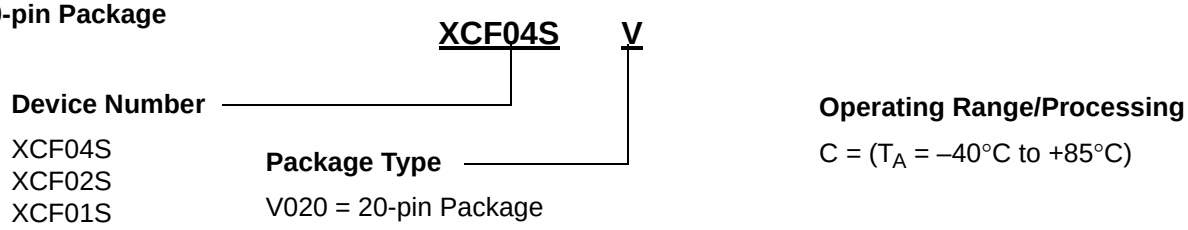


Valid Ordering Combinations

XCF04SV020 C
XCF02SV020 C
XCF01SV020 C

Marking Information

20-pin Package



Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/29/03	1.0	Xilinx Initial Release