Errata

The following are known problems with Rev. M of the AT89S8253 device:

1. SPI Communications

During SPI communications, when the SPI is disabled by clearing the SPE (SPCR.6) bit, the interface is only reset for one clock cycle afterwards. This will result in clock glitches or missing clocks if the user is trying to switch the clock modes (CPOL, CPHA) even if SPE is 0.

Workaround:

Make sure that in the software the SPE bit toggles 1 --> 0 after the mode bits have changed:

Assembly Code:

Change CPHA when SPI is still enabled (SPE = 1)

```
; SPCR was 50h
MOV SPCR, #014h ; clear SPE and set CPHA
ORL SPCR, #040h ; set SPE
```

Change CPHA when SPI is not enabled (SPE = 0)

```
; SPCR was 10h
MOV SPCR, #054h ; set SPE and set CPHA
ANL SPCR, #0BFh ; clear SPE
ORL SPCR, #040h ; set SPE
```

C Language:

Change CPHA when SPI is still enabled (SPE = 1)

```
/* SPCR was 0x50 */
SPCR = 0x14; /* clear SPE and set CPHA */
SPCR = SPCR | 0x40; /* set SPE */
```

Change CPHA when SPI is not enabled (SPE = 0)

```
/* SPCR was 0x10 */
SPCR = 0x54 /* set SPE and set CPHA */
SPCR = SPCR & 0xBF /* clear SPE */
SPCR = SPCR | 0x40 /* set SPE */
```

2. Timer 1 as Baud Rate Generator

Timer 1 does not work as a baud rate generator in Modes 0 or 1 for very low baud rates (< 50 bps).

Workaround:

For slow baud rates, use Timer 2 for baud rate generation instead. This problem will be completely fixed in revision N.

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