AN10878

Migrating to the LPC1700 series

Rev. 01 — 6 October 2009 **Application note**

Document information

Info	Content
Keywords	LPC1700, Migration, LPC2300/2400, ARM7, Cortex-M3
Abstract	This application note introduces the important features of the LPC1700 series (Cortex-M3 based), and details the differences when compared to the LPC2000 family (ARM7 based). This application note will help enable users have a smooth migration process from the LPC2000 family to the LPC1700 series.

Revision history

Rev	Date	Description
01	20091006	Initial revision.

Contact information

For additional information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Introduction

The LPC1700 microcontroller family is based on the ARM Cortex-M3 CPU architecture for embedded applications featuring a high level of support block integration and low power consumption. The LPC1700 microcontrollers incorporate key features like the AHB Matrix, Nested Vectored Interrupt Controller (NVIC) integrated with a SYSTICK timer, Wakeup Interrupt Controller (WIC), Memory Protection Unit (MPU), four reduced power modes, and a wide range of peripherals, making this simply the most powerful series of Cortex-M3 based microcontrollers in the marketplace.

The peripheral complement of the LPC1700 series includes up to 512 kB of flash memory, up to 64 kB of data memory, Ethernet MAC, USB Host/Device/OTG interface, 8-channel general purpose DMA controller, four UARTs, two CAN channels, two SSP controllers, SPI interface, three I^2C interfaces, 2-input plus 2-output I^2S interface, 8-channel 12-bit ADC, 10-bit DAC, motor control PWM, Quadrature Encoder interface, four general purpose timers, 6-output general purpose PWM, ultra-low power RTC with separate battery supply, and up to 70 general purpose I/O pins.

The LPC1700 series targets a wide range of applications, including eMetering, lighting, industrial networking, alarm systems, white goods and motor control.

The LPC1700 ARM Cortex-M3 microcontrollers differ not only in the core itself from the ARM7-based LPC2000, but also with the significant architectural differences, enhancements, and new peripherals that exist within the LPC1700 series. This application note attempts to introduce the important features of the LPC1700 series, and focuses on providing key differences which users must be aware of in order to have a smooth migration process from the LPC2000 ARM7 based microcontrollers to the LPC1700 ARM Cortex-M3 based microcontrollers.

The various topics covered in this application note are as follows:

1. Multilayer AHB Matrix and Split APB Bus
2. Memory Support
3. Key System Blocks
4. Power Structure and Management
5. Peripherals
6. Miscellaneous

2. Multilayer AHB matrix and split APB bus

2.1 Multilayer AHB (Advanced High-performance Bus) matrix

The ARM7-based microcontrollers (LPC2300/2400) utilize a dual AHB bus architecture which allows simultaneous operations from the following modules.

1. CPU operation from internal memory
2. USB operation with dedicated DMA
3. Ethernet operation with dedicated DMA
4. General purpose DMA operation from peripherals that can support DMA

The LPC1700 has been enhanced by adding a multi-layer AHB matrix to connect the Cortex-M3 buses and other bus masters to peripherals in a flexible manner that optimizes performance by allowing peripherals on different slave ports of the matrix to be accessed simultaneously by different bus masters.

Details of the multilayer AHB matrix connections are shown below:

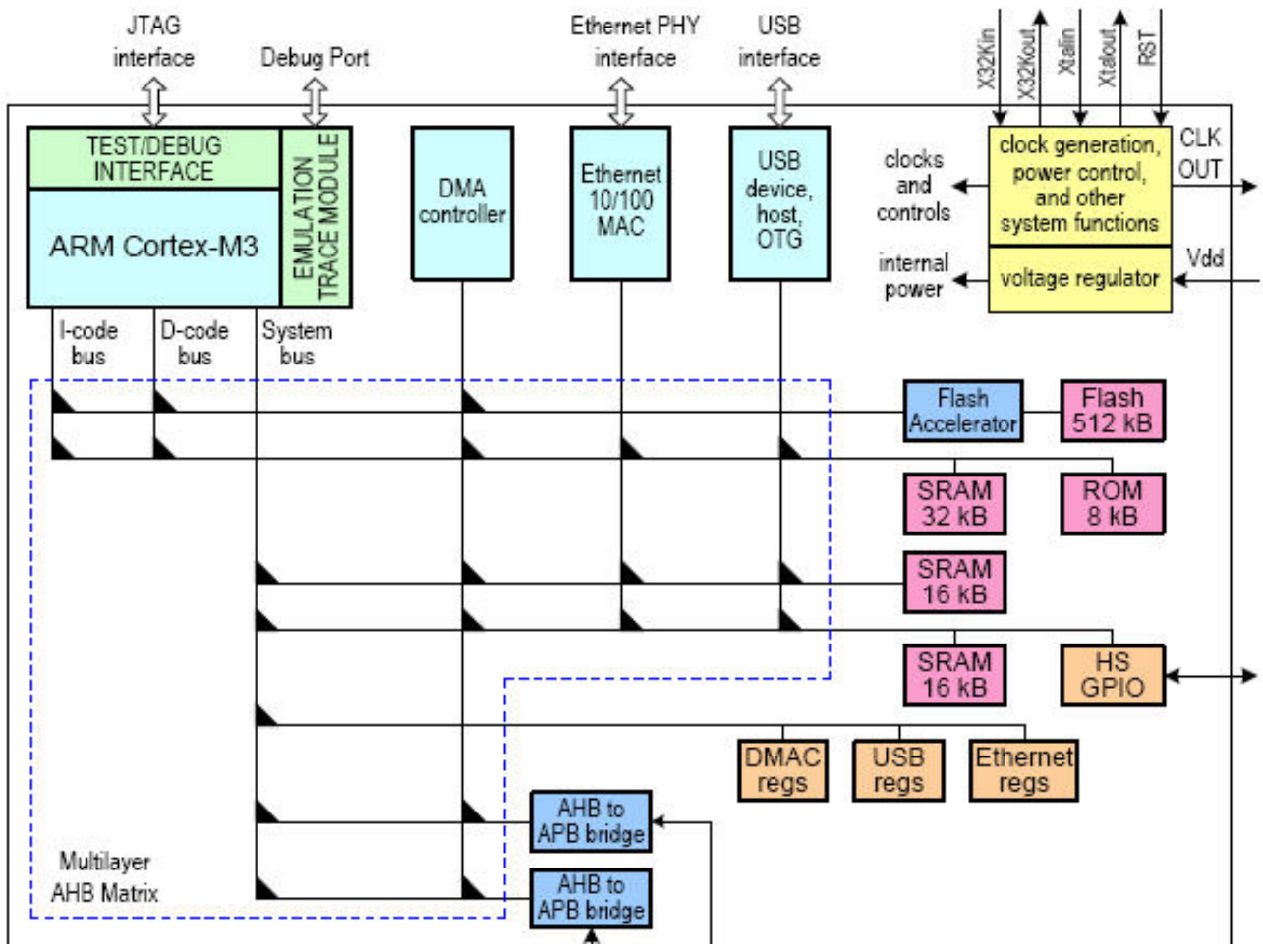

Fig 1. LPC1700 block diagram (top)

As shown in Fig 1, the ARM Cortex-M3 includes three AHB-Lite buses, one system bus, and the I-code and D-code buses: one bus dedicated for instruction fetch (I-code) and one bus for data access (D-code). The Multilayer AHB matrix provides a separate bus for each AHB master. The AHB masters include the ARM Cortex-M3, General Purpose DMA controller, Ethernet MAC, and the USB interface.

The AHB slaves include the Flash Accelerator, on-chip Flash memory, three on-chip SRAMs located separately, on-chip ROM where the boot-loader resides, High Speed GPIOs, DMA control registers, USB registers, and Ethernet registers. The peripherals supported in the LPC1700 series are connected to the two AHB to APB bridges (see Fig 2).

On the LPC1700, all the AHB masters have access to the on-chip Flash memory via Flash Accelerator, and the three on-chip SRAM memories allow simultaneous operation of the AHB masters with no arbitration delays as long as two masters don't attempt to access the same slave at the same time. The multilayer interconnect system allows simultaneous operation of the Ethernet DMA, USB DMA, General Purpose DMA, and CPU execution from on-chip flash and simultaneous access to be spread over three separate SRAMs with no contention between those functions.

2.2 Split APB bus

The various peripherals supported in the LPC1700 series of devices are located on two APB buses called APB slave group 0 bus (APB0) and APB slave group 1 (APB1). They are connected to the AHB masters (CPU and DMA) via the two AHB to APB bridges using two separate slave ports from the multilayer AHB matrix (see Fig 2).

As shown in Fig 2 below, the peripheral bus is split into two allowing the CPU and DMA to simultaneously access separate peripherals located on the APB buses at the same time. The shaded peripheral blocks in Fig 2 below support General Purpose DMA. For example, at the same time, the CPU can access SSP1 located on APB0 and the DMA can access SSP0 located on APB1. This flexibility allows more through-put with fewer stalls and reduces collisions between the CPU and DMA. The APB bridges are configured to buffer writes so that the CPU or DMA controller can access without waiting for APB write completion.

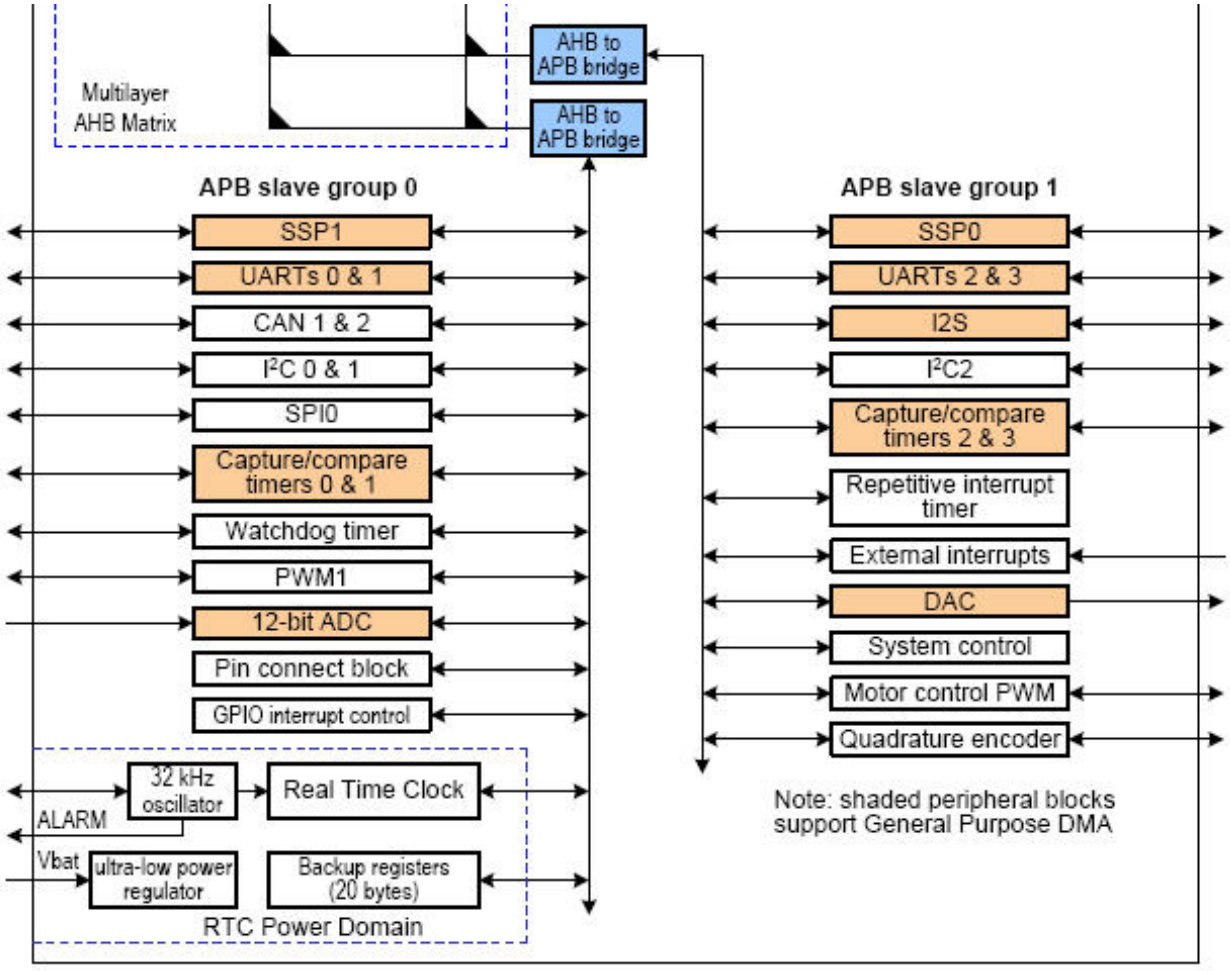

Fig 2. LPC1700 block diagram (bottom)

3. Memory support

Section 3 covers the following topics:

- Internal memories
- Flash accelerator
- Memory Protection Unit (MPU)

3.1 Internal memories

The ARM Cortex-M3 processor has a single 4 GB address space. Table 1 shows how this space is used on the LPC1700. The overall map of the entire address space implementation is different from the LPC2000 family (please see LPC1700 user manual for more details).

Table 1. LPC1700 memory usage and details

Address range	Use	Address range details and description
0x0000 0000 - 0x0003 FFFF	On-chip non-volatile memory	Flash memory (512 kB)
0x1000 0000 - 0x1000 7FFF	On-chip SRAM	Local SRAM – bank 0 (32 kB)
0x2007 C000 – 0x2007 FFFF	On-chip SRAM, typically for peripheral data	AHB SRAM – bank 0 (16 kB)
0x2008 0000 – 0x2008 3FFF	On-chip SRAM, typically for peripheral data	AHB SRAM – bank 1 (16 kB)
0x2009 C000 – 0x2009 FFFF	General Purpose I/O	
0x4000 0000 – 0x4007 FFFF	APB0 peripherals	Up to 32 peripheral blocks, 16 kB each
0x4008 0000 – 0x400F FFFF	APB1 peripherals	Up to 32 peripheral blocks, 16 kB each
0x5000 0000 – 0x501F FFFF	AHB peripherals	DMA controller, Ethernet interface, and USB interface
0xE000 0000 – 0xE00F FFFF	Cortex-M3 related functions	Includes the NVIC and System Tick Timer

Let's now revisit the multilayer AHB matrix which shows all the internal memories:

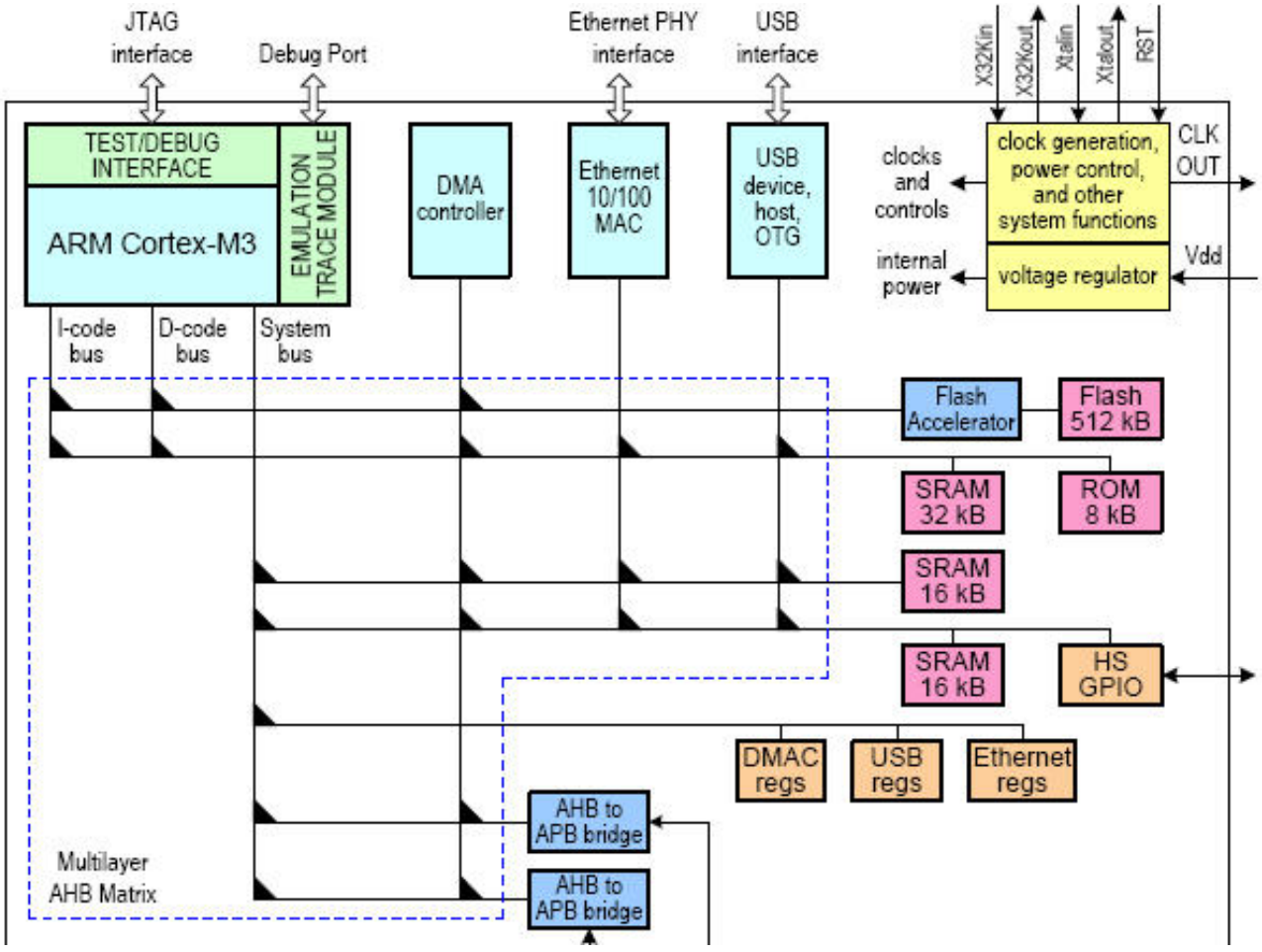

Fig 3. LPC1700 block diagram (top)

As you can see above, the LPC1700 series consists of the following internal memory support:

- On-chip Flash
  - Maximum 512 kB
  - Zero wait-state performance with Flash Accelerator
- On-chip SRAM
  - Total 64 kB
    - 32 kB SRAM is accessible by the CPU and DMA controller on a higher speed bus
    - Two additional 16 kB SRAM – separate slave port on the AHB multilayer matrix. The breakup is a key system feature since it allows the 3 AHB masters to spread over 3 separate RAMs that can be accessed simultaneously.
- On-chip ROM
  - 8 kB ROM consisting of the boot-loader and boot-block (Flash program/erase commands for ISP, IAP, and Real monitor routines)

On the LPC2000 family, the boot-block resided in part of the internal flash memory resulting in less user space. For example, the LPC2368 has on-chip flash of 512 kB where 504 kB is for user space and 8 kB is used by the boot-block. On the LPC1768, since the boot-block resides on the on-chip ROM, the full 512 kB on-chip flash is available for user space.

3.2 Flash accelerator

On the LPC2000 family, the Memory Accelerator Module (MAM) is used to maximize the performance of the ARM7 processor when it is running in the flash and attempts to have the next ARM instruction in its latches in time to prevent CPU fetch stalls.

On the LPC1700 series, the flash accelerator is an enhancement of the LPC2000 MAM block with additional configurable options and attempts to have the next Cortex-M3 instruction that will be needed in its latches in time to prevent CPU fetch stalls. As shown in the figure below, internally, the flash accelerator includes an array of eight 128-bit buffers to store both instructions and data in a configurable manner. *The operations within this module are completely transparent to the end user.* Programming this block is achieved by ONE register configuration alone and it is called the “FLASHCFG” Register.

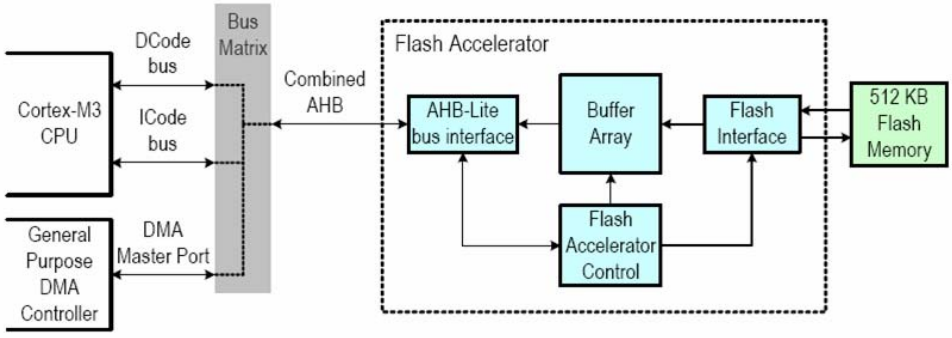

Fig 4. LPC1700 flash accelerator block diagram

After reset, the flash accelerator defaults to the enabled state. Software can turn memory access acceleration on or off, or change the acceleration configuration at any time.

Following reset, the flash access timing (i.e. FLASHTIM) is also set to a default value of 6 CPU clocks. This is considered as a “safe setting” and will work for any condition. As an illustration, if the application needs to execute at 20 MHz, the timing can be set to 1 CPU clock and if the application needs to execute at 100 MHz, the timing can be set to 5 CPU clocks.

Flash programming operations are not controlled by the flash accelerator, but are handled as a separate function.

3.3 Memory Protection Unit (MPU)

A Memory Protection Unit (MPU) is a component for memory protection and can support up to eight regions in the LPC1700. Each region can be broken up into 8 sub regions.

The MPU supports full support for protection regions, overlapping protection regions, access permissions and exporting memory attributes to the system.

The MPU can be used to enforce privilege rules, have separate processes running on the system via a real time OS and enforce access rules accordingly. Complete details on the MPU can be found in the Cortex-M3 Technical Reference Manual, on ARM.com.

Fig 5 contains a table from the technical reference manual for Cortex-M3 showing the instruction and data access permissions that are possible for a specific region.

Table 9-6 MPU Region Attribute and Size Register bit assignments

Bits	Field	Function		
[31:29]	-	Reserved.		
[28]	XN	Instruction access disable bit: 1 = disable instruction fetches 0 = enable instruction fetches.		
[27]	-	Reserved.		
[26:24]	AP	Data access permission field:		
	Value	Privileged permissions	User permissions	
	b000	No access	No access	
	b001	Read/write	No access	
	b010	Read/write	Read-only	
	b011	Read/write	Read/write	
	b100	Reserved	Reserved	
	b101	Read-only	No access	
	b110	Read-only	Read-only	
	b111	Read-only.	Read-only.	

Fig 5. LPC1700 MPU

4. Key system blocks

Section 4 covers the following topics:

- Clocking structure
- Clock out function
- Nested Vectored Interrupt Controller (NVIC)
- DMA engines

4.1 Clocking structure

In the LPC1700, the CPU frequency can be sourced from three independent oscillators (same as the LPC2300/2400 family) and run at a maximum frequency of 100 MHz. The independent oscillators are the Main Oscillator, the Internal RC Oscillator, and the RTC oscillator. Each oscillator can be used for more than one purpose as required in a particular application. Fig 6 shows the clock structure of the LPC1700.

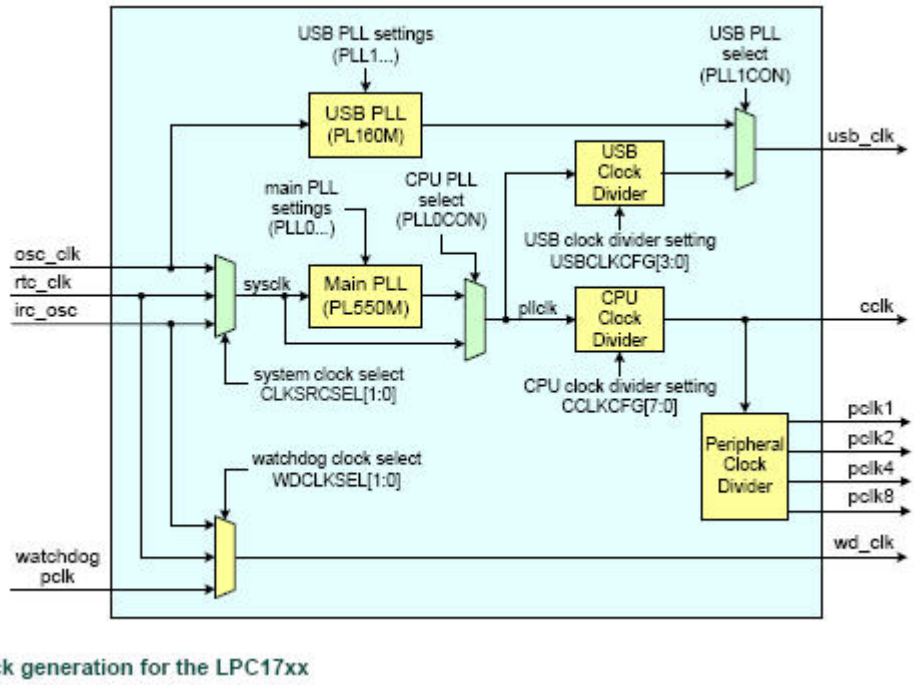

Fig 6. LPC1700 clock generation block diagram

Most of the clocking structure remains the same as LPC2000 family; however, there are additional features and flexibility to be aware of when using the LPC1700 devices:

1. The USB block on LPC1700 has its own dedicated PLL which is termed as PLL1. PLL1 accepts an input clock frequency in the range of 10 MHz to 25 MHz only. PLL1 receives its clock input from the main oscillator only and can be used to provide a fixed 48 MHz clock only to the USB subsystem. This is an option in addition to the possibility of generating the USB clock from PLL0. PLL1 is disabled and powered off on reset. If PLL1 is left disabled, the USB clock can be supplied by PLL0 if everything is set up to provide 48 MHz through that route. If PLL1 is enabled and connected via the PLL1CON register, it is automatically selected to drive the USB subsystem.
2. Similarly to the LPC2300/2400 family, clock for the watchdog can be derived from 3 sources - Internal RC oscillator (IRC), the APB peripheral clock (PCLK) and the RTC oscillator. A new implementation on the LPC1700 Watchdog peripheral is that the clock source selection can be locked by software, so that it cannot be modified. On reset, the clock source selection bits are always unlocked. When the IRC is chosen as the watchdog clock source, the watchdog timer can remain running in deep sleep mode (will be discussed later), and can reset or wakeup the device from that mode.
3. On the LPC1700, the RTC oscillator provides a 1 Hz clock to the RTC and a 32 kHz clock output that can be used as the clock source for PLL0 and CPU and/or the watchdog timer.

4.2 Clock out function

On the LPC1700 series, for system test and development purposes, any one of several internal clocks may be brought out on the CLKOUT function available on the P1.27 pin, as shown in Fig 7.

Clocks that may be observed via CLKOUT are the CPU clock, the main oscillator, the internal RC oscillator, the USB clock, and the RTC clock. Furthermore, the CLKOUT on the LPC1700 can be used to clock other units in the system as well.

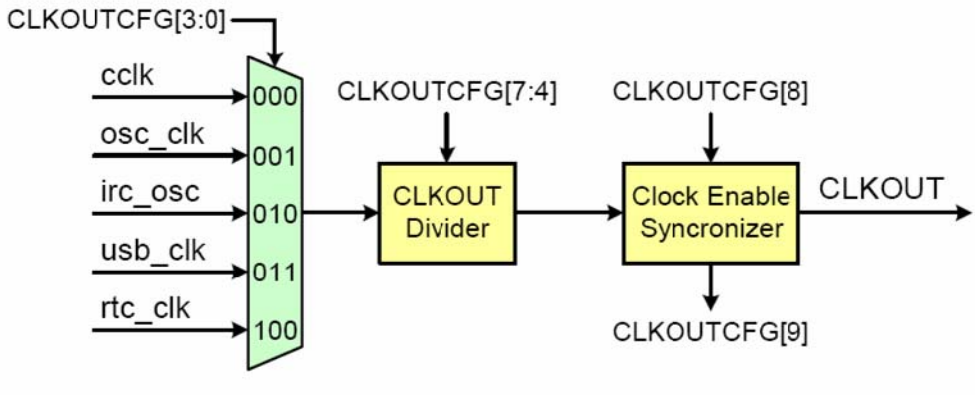

Fig 7. LPC1700 clock out selection

4.3 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M3 core. One of the key features of the LPC1700 series is its interrupt structure and exception handling managed by the NVIC.

Because the ARM7 core was not designed with an interrupt controller, ARM7 microcontroller vendors have added a Vectored Interrupt Controller which supports two interrupt lines: fast interrupt and the general purpose interrupt line which handled all of the interrupt sources within the device. Also, the interrupt structure in the ARM core is not deterministic; the time taken to terminate or abort an instruction under execution when the interrupt occurs is available. Second, the ARM7 core's interrupt structure does not naturally support nested interrupts; further software is required.

The NVIC on the LPC1700 overcomes these limitations and is designed to have very low interrupt latency, extremely fast and deterministic. Interrupt entry always take 12 cycles and then 12 cycles to return from servicing.

In the LPC1700, the NVIC supports:

- 35 vectored interrupts
  - A programmable priority level of 0-31 for each interrupt with hardware priority level masking. A higher level corresponds to a lower priority, so level 0 is the highest interrupt priority
  - Grouping of priority values into group priority and sub-priority fields which enables different levels of nested interrupt handling.
  - An external Non-Maskable Interrupt (NMI) feature used for when an interrupt should never be disabled in the normal operation of the system and response time is critical for non-recoverable hardware errors.
  - Re-mapping the interrupt vector table to alternate locations in the memory map is controlled via the Vector Table Offset Register (VTOR) contained in the NVIC. MEMMAP register is used in the LPC2000 family to select whether the ARM interrupt vectors are read from the Boot ROM, User Flash, or RAM.

- Stack operations
  - The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no software instruction overhead. In the ARM7 core, serial pop and push actions were required in software for every exception entry and exit.
- Sleep on exit mode
  - The NVIC is also involved in the power-management of the integrated sleep modes, such as the Sleep On Exit mode, in which the device moves into low-power mode as soon as it exits the lowest priority interrupt-service routine and stays in sleep state until another exception is encountered.
- SysTick Timer
  - The NVIC integrates a System Tick (SysTick) timer, a 24-bit down timer that is ideal for a Real Time Operating System or other scheduled tasks since it can generate interrupts at regular time intervals.

4.4 DMA engines

Like the LPC2300/2400 family, there are also three main DMA engines in the LPC1700 series:

1. Dedicated DMA for Ethernet
2. Dedicated DMA for USB
3. General Purpose DMA which allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions.

On the LPC2300/2400 family, the DMA controller has two channels and supports SD/MMC, two SSP and I2S interfaces.

On the LPC1700 series, key features of the DMA are:

- Eight DMA channels with a four-word FIFO per channel.
- Support for two SSP interfaces, I2S interface, four UART interfaces, 12-bit ADC and 10-bit DAC interfaces.
- DMA can also be triggered by a Timer match condition.
- GPIO registers are accessible by the GPDMA controller to allow DMA data to or from GPIOs, synchronized to any DMA request

The table in Fig 8 shows which peripherals support single requests and which peripherals support burst requests.

Peripheral Function	DMA Single Request Input (DMACSREQ)	DMA Burst Request Input (DMACBREQ)
SSP0 Tx	0	0
SSP0 Rx	1	1
SSP1 Tx	2	2
SSP1 Rx	3	3
ADC	4	4
I²S channel 0	-	5
I²S channel 1	-	6
DAC	-	7
UART0 Tx / MAT0.0	-	8
UART0 Rx / MAT0.1	-	9
UART1 Tx / MAT1.0	-	10
UART1 Rx / MAT1.1	-	11
UART2 Tx / MAT2.0	-	12
UART2 Rx / MAT2.1	-	13
UART3 Tx / MAT3.0	-	14
UART3 Rx / MAT3.1	-	15

Fig 8. LPC1700 DMA support

5. Power structure and management

Section 5 covers the following topics:

- Power domains
- Power down modes and
- Wakeup Interrupt Controller (WIC)

5.1 Power domains

There are 3 main power domains in the LPC1700

1. $V_{DD(reg)(3V3)}$ – on-chip voltage regulator (2.4 V to 3.6 V)
2. $V_{DD(3V3)}$ – I/O pads (2.4 V to 3.6 V)
3. VBAT (2.1 V to 3.6 V) - Power only to the RTC and Backup Registers
4. VDDA (2.7 V to 3.6 V) – Analog Supply Power to 12 Bit ADC
5. VREFP (2.7 V to 3.6 V) - Analog Reference Voltage to 12 Bit ADC (2.7 V to 3.6 V)

5.2 Power modes

On the LPC2000 family, there are four reduced power modes: Idle, Sleep, Deep-Sleep, Power-down, and Deep Power-down modes.

On the LPC1700 series, there are also four reduced power modes: Sleep, Deep-Sleep, Power-down, and Deep Power-down modes.

The following sections cover the power reduction modes for the LPC1700.

5.2.1 Sleep mode

Sleep mode on the LPC1700 corresponds to Idle mode on LPC2000 series devices. In this mode, CPU execution is suspended and peripherals continue to run. In Sleep mode, execution of instructions is suspended until either a Reset or an interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Wake up from Sleep mode will occur whenever any enabled interrupt occurs.

5.2.2 Deep-sleep mode

Deep-Sleep mode on the LPC1700 corresponds to the Sleep mode on LPC2000 devices. When the chip enters the Deep Sleep mode, the main oscillator is powered down, and nearly all clocks are stopped. The IRC remains running and can be configured to drive the Watchdog Timer, allowing the Watchdog to wake up the CPU. The 32 kHz RTC oscillator is not stopped and RTC interrupts may be used as a wakeup source. The flash is left in the standby mode allowing a quick wakeup. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep Sleep mode and the logic levels of chip pins remain static. Wake up from Deep Sleep mode will occur by either a Reset or certain specific interrupts that are able to function without clocks.

5.2.3 Power-down mode

Power-down mode behaves the same between the LPC2000 family and LPC1700 series. Power-down mode does everything that Deep Sleep mode does, but it also turns off the flash memory. Wake up from Power-down mode can be brought about by Non-Maskable Interrupt (NMI), External Interrupts EINT0 through EINT3, GPIO interrupts, the Ethernet Wake-on-LAN interrupt, Brownout Detect, an RTC Alarm interrupt, a USB input pin transition, or a CAN input pin transition, when the related interrupt is enable

5.2.4 Deep power-down mode

Deep power-down mode behaves the same in both the LPC2000 family and LPC1700 series. In this mode, power is shut off to the entire chip with the exception of the Real-Time Clock (RTC), the RESET pin, the Wake-Up Interrupt Controller (discussed later), and the RTC backup registers (discussed later). To optimize power conservation, the user has the additional option of turning off or retaining power to the 32 kHz oscillator. Wake up from Deep power-down mode will occur when an external reset signal is applied, or the RTC interrupt is enabled and an RTC interrupt is generated.

6. Wake-Up Interrupt Controller (WIC)

The Wake-up Interrupt Controller (WIC) is an integral feature of the LPC1700 which wasn't available in the LPC2000 family. The Nested Vectored Interrupt Controller (NVIC) is unable to prioritize or detect interrupts while powered off in deep-sleep or power-down modes, so knowing when to come out of these modes is impossible without enabling the CPU and wasting power. The WIC can emulate the full NVIC behavior, uses minimal power, and enables the chip to wake up from Deep-Sleep and Power-down mode (without the use of NVIC) when it receives the interrupts below.

- Interrupts used:
  - NMI, external interrupts EINT0 through EINT3, GPIO interrupts, Ethernet wake-on-LAN interrupt, brownout detect, RTC alarm, CAN activity interrupt and USB activity interrupt

The WIC is not programmable, and does not have any registers or user interface. It operates entirely from hardware signals and no software programming is required.

7. Peripherals

With a rich set of peripherals, the LPC1700 series is a great fit for wide variety of applications. Peripherals available in the LPC1700 series are shown in Fig 10 below.

New peripherals in the LPC1700 series are Motor Control PWM, Quadrature Encoder Interface (QEI), Repetitive Interrupt Timer (RIT), System Tick Timer, and the 12-bit ADC.

LPC1700 Peripherals	Timers / PWM									Serial Interfaces											Analog Features						
	WatchDog	Timers (32-bit)	Timers (16/32-bit)	PWM (6-channel PWM)	Motor Control PWM	Quadrature Encoder Interface	Repetitive Interrupt Timer	System Tick Timer	RTC	UARTs	I^2C	I^2S	SPI	SSP	CAN	USB Device	USB Host	USB OTG	Ethernet	12-bit ADC	10-bit DAC	Brown-Out Detect (BOD)	Power-On Reset (POR)	Main PLL	USB PLL	Internal RC Oscillator (4MHz)
LPC1768	1	2	2	1	1	1	1	1	1	4	3	1	1	2	2	1	1	1	1	1	1	1	1	1	1	1
LPC1766	1	2	2	1	1	1	1	1	1	4	3	1	1	2	2	1	1	1	1	1	1	1	1	1	1	1
LPC1765	1	2	2	1	1	1	1	1	1	4	3	1	1	2	2	1	1	1	-	1	1	1	1	1	1	1
LPC1764	1	2	2	1	1	1	1	1	1	4	3	-	1	2	2	1	-	-	1	1	-	1	1	1	1	1
LPC1758	1	2	2	1	1	1	1	1	1	4	2	1	1	2	2	1	1	1	1	1	1	1	1	1	1	1
LPC1756	1	2	2	1	1	1	1	1	1	4	2	1	1	2	2	1	1	1	-	1	1	1	1	1	1	1
LPC1754	1	2	2	1	1	1	1	1	1	4	2	-	1	2	1	1	1	1	-	1	1	1	1	1	1	1
LPC1752	1	2	2	1	1	1	1	1	1	4	2	-	1	2	1	1	-	-	-	1	-	1	1	1	1	1
LPC1751	1	2	2	1	1	1	1	1	1	4	2	-	1	2	1	1	-	-	-	1	-	1	1	1	1	1

Fig 9. LPC1700 peripherals

Register sets and definitions for peripherals which are common between the LPC1700 and LPC2000 families remain the same allowing users to easily re-use software.

7.1 Peripheral enhancements

Peripherals which existed in the LPC2000 family have been introduced with new features which users can take advantage of when migrating to the LPC1700 series. The following peripherals have been enhanced:

7.1.1 I^2C-bus

In the LPC1700, there are three I^2C interfaces (I2C0/I2C1/I2C2).

I2C0 has been enhanced to support Fast Mode Plus (1 Mbit/s) and can be configured through the I2CPADCFG register.

I2CPADCFG	Symbol	Value	Description	Reset value
0	SDADRV0		Drive mode control for the SDA0 pin, P0.27.	0
		0	The SDA0 pin is in the standard drive mode.	
		1	The SDA0 pin is in Fast Mode Plus drive mode.	
1	SDAI2C0		I^2C mode control for the SDA0 pin, P0.27.	0
		0	The SDA0 pin has I^2C glitch filtering and slew rate control enabled.	
		1	The SDA0 pin has I^2C glitch filtering and slew rate control disabled.	
2	SCLDRV0		Drive mode control for the SCL0 pin, P0.28.	0
		0	The SCL0 pin is in the standard drive mode.	
		1	The SCL0 pin is in Fast Mode Plus drive mode.	
3	SCLI2C0		I^2C mode control for the SCL0 pin, P0.28.	0
		0	The SCL0 pin has I^2C glitch filtering and slew rate control enabled.	
		1	The SCL0 pin has I^2C glitch filtering and slew rate control disabled.	
31:4	-		Reserved.	NA

Fig 10. LPC1700 I2C0 – Fast mode configuration register

All three I^2C interfaces can provide support for optional address recognition of four addressable slaves on the I^2C-bus. In the slave mode, the I^2C hardware can look for any one of its four slave addresses (7 bits) and the general call address. If one of these addresses is detected, an interrupt is requested.

Finally, all three I^2C interfaces have been enhanced with monitor mode to monitor traffic on the I^2C-bus. Without actually participating in traffic or interfering with the I^2C-bus, device can monitor traffic. An interrupt will be generated on ANY address received. This will enable the part to monitor all traffic on the bus.

Registers added with regards to multiple address recognition in slave mode and new monitor mode are I^2C Slave Address Registers (I2ADR1 to 3), I^2C Slave Address Mask Registers (I2MASK0 to 3), Monitor Mode Control Register (MMCTRL), and Data Buffer Register (I2DATA_BUFFER). Please see the LPC1700 User manual for further details.

7.1.2 I^2S-bus

The LPC1700 I^2S interface has clocking enhancements to provide support for wide range of I^2S codecs. A separate Master Clock output, for both transmit and receive channels, has been added in the LPC1700 I^2S interface to support a clock up to 512 times the I^2S sampling frequency. The master clock (MCLK) can be generated using a fractional rate generator, dividing down the frequency of PCLK_I2S, to meet a wide range of audio sample rates.

Lastly, in addition to master and slave modes, which are independently configurable for the transmitter and the receiver, several different clock sources are possible, including variations that share the clock and/or WS between the transmitter and receiver. This last option allows using I^2S with fewer pins, typically four. Please see the I^2S operating mode section in the LPC1700 User manual for further details.

7.1.3 UART

Similar to the LPC2000 family, the LPC1700 series has four UART interfaces (UART0/1/2/3) where UART0/2/3 can support IrDA and UART1 can support modem interface.

The new features on the UART1 interface are the RS-485/EIA-485 mode and 9-bit support.

This is a key feature and it is not available on all the LPC2000 ARM7 devices.

7.1.4 9-bit support

With 9-bit support, UART1 can be configured as an addressable slave. The addressable slave is one of multiple slaves controlled by a single master. The UART master transmitter will identify an address character by setting the parity (9th) bit to '1'. For data characters, the parity bit is set to '0'. UART1 can be assigned a unique address and can be programmed to either manually or automatically reject data following an address which it is not assigned to.

7.1.5 RS-485/EIA-485 support

With RS-485/EIA-485 support, UART1 can be set to the following modes:

7.1.5.1 RS-485 Normal Multidrop Mode (NMM)

In this mode, an address is detected when a received byte causes the UART to set the parity error and generate an interrupt.

If the receiver is disabled, any received data bytes will be ignored and will not be stored in the RXFIFO. When an address byte is detected (parity bit = '1') it will be placed into the RXFIFO and an Rx Data Ready Interrupt will be generated. The processor can then read the address byte and decide whether or not to enable the receiver to accept the following data.

While the receiver is enabled, all received bytes will be accepted and stored in the RXFIFO regardless of whether they are data or address. When an address character is received a parity error interrupt will be generated and the processor can decide whether or not to disable the receiver.

7.1.5.2 RS-485 Auto Address Detection (AAD) mode

In this mode, the UART1 receiver will compare any address byte received (parity = '1') to the 8-bit address programmed into the RS485ADRMATCH register.

If the receiver is disabled, any received byte will be discarded if it is either a data byte OR an address byte which fails to match the RS485ADRMATCH value. When a matching address character is detected it will be pushed onto the RXFIFO along with the parity bit, and the receiver will be automatically enabled and can generate an Rx Data Ready Interrupt.

While the receiver is enabled, all bytes received will be accepted and stored in the RXFIFO until an address byte which does not match the RS485ADRMATCH value is received. When this occurs, the receiver will be automatically disabled in hardware and the received non-matching address character will not be stored in the RXFIFO.

7.1.5.3 RS-485/EIA-485 auto direction control

Since RS-485 supports multiple nodes per line and because all of the nodes share a data path, only one driver can be enabled at a time. Before transmitting, a driver must be sure that the previous driver has been disabled. With auto direction control feature, the program code doesn't have to toggle a signal to enable and disable the driver, and a transmitting driver doesn't need to allow extra time to be sure that the previous driver has been disabled. The auto direction control allows the option of allowing the transmitter to automatically control the state of either the RTS pin or the DTR pin as a direction control

output signal to control the enable line so the driver is disabled as quickly as possible, soon after the stop bit.

7.1.6 Real-Time Clock (RTC)

Similar to the LPC2000 family, the Real Time Clock (RTC) on LPC1700 is a set of counters for measuring time when system power is on, and optionally when it is off. It uses very little power when its registers are not being accessed by the CPU, especially reduced power modes. On the LPC1700, the RTC is clocked by a separate 32 kHz oscillator that produces a 1 Hz internal time reference and alarm interrupt can be generated for a specific date/time.

Key differences in the RTC domain between the LPC1700 and LPC2000 are:

1. The battery SRAM which is available in the LPC2300/2400 series has been replaced with 20 bytes of Battery-backed storage registers in the LPC1700 series.
2. Calibration counter has been implemented in the LPC1700 which allows adjustment to better than 1 sec/day with 1 sec resolution. This is not available in the LPC2000 family.
3. The ALARM output signal which is available in the LPC2300/2400 series is not available in the LPC1700 devices.

8. Miscellaneous

The following sections cover additional topics which users need to keep in mind when migrating from the LPC2000 family to the LPC1700 series:

8.1.1 Pin compatibility

To provide users a smooth migration from ARM7 to Cortex-M3, the LPC1768 was designed to be pin-to-pin compatible with LPC2368. This compatibility allows users to evaluate both the Cortex-M3 and ARM7-based products in the same socket and to choose the right microcontrollers for the application.

8.1.2 Open-drain mode

This is a new LPC1700 feature which is not available in the LPC2000 family. The open drain mode causes the pin to be pulled low normally if it is configured as an output and the data value is 0. If the data value is 1, the output drive of the pin is turned off, equivalent to changing the pin direction. This combination simulates an open drain output. See user manual for further details.

Table 77. Open Drain Pin Mode Select register Bits

PINMODE_OD0 to PINMODE_OD4 Values	Function	Value after Reset
0	Pin is in the normal (not open drain) mode.	00
1	Pin is in the open drain mode.	

Fig 11. LPC1700 – Open drain mode

8.1.3 Repeater mode

Repeater mode enables the pull-up resistor if the pin is to logic HIGH and enables the pull-down resistor if the pin is set to logic LOW. This causes the pin to retain its last

known state if it is configured as an input and is not driven externally. The state retention is not applicable to the Deep Power-down mode. Repeater mode may typically be used to prevent a pin from floating (and potentially using significant power if it floats to an indeterminate state) if it is temporarily not driven.

Table 76. Pin Mode Select register Bits

PINMODE0 to PINMODE9 Values	Function	Value after Reset
00	Pin has an on-chip pull-up resistor enabled.	00
01	Repeater mode (see text below).	
10	Pin has neither pull-up nor pull-down resistor enabled.	
11	Pin has an on-chip pull-down resistor enabled.	

Fig 12. LPC1700 – Repeater mode

8.1.4 Debug support

On the LPC2000, available debug interfaces are the standard JTAG interface and the ETM (Embedded Trace Macrocell) interface.

On the LPC1700, along with the standard JTAG and ETM interfaces, Serial Wire Debug (SWD) interface and Serial Wire Output (SWO) are new features available for debug options.

Serial Wire Debug (SWD) has the same functionality as the JTAG interface (5 pins) and is a two-pin debugging mode that uses only a clock and data interface.

Serial Wire Output (SWO) is used for trace functions and uses 1 pin for trace output.

Note that the ETM function in LPC1700 is functionally very different than the trace that is available for previous ARM7 based devices, using only 5 pins instead of 10 for trace data. Finally, the ARM Cortex-M3 in the LPC1700 is configured to support up to eight hardware breakpoints and four data watchpoints. The tables below indicate the various pin functions related to debug and trace.

.

Table 601. JTAG pin description

Pin Name	Type	Description
TCK	Input	**JTAG Test Clock.** This pin is the clock for debug logic when in the JTAG debug mode.
TMS	Input	**JTAG Test Mode Select.** The TMS pin selects the next state in the TAP state machine.
TDI	Input	**JTAG Test Data In.** This is the serial data input for the shift register.
TDO	Output	**JTAG Test Data Output.** This is the serial data output from the shift register. Data is shifted out of the device on the negative edge of the TCK signal.
$\overline{\text{TRST}}$	Input	**JTAG Test Reset.** The $\overline{\text{TRST}}$ pin can be used to reset the test logic within the debug logic.
RTCK	Output	**JTAG Returned Test Clock.** This is an extra signal added to the JTAG port, and is included for backward pin compatibility with LPC23xx series devices that share the same pinout as this device. RTCK is not normally used with the Cortex-M3. For designs based on ARM7TDMI-S processor core, this signal could be used by external JTAG host interface logic to maintain synchronization with targets having a slow or varying clock frequency. For details refer to "Multi-ICE System Design considerations Application Note 72 (ARM DAI 0072A)".

Table 602. Serial Wire Debug pin description

Pin Name	Type	Description
SWDCLK	Input	**Serial Wire Clock.** This pin is the clock for debug logic when in the Serial Wire Debug mode.
SWDIO	Input / Output	**Serial wire debug data input/output.** The SWDIO pin is used by an external debug tool to communicate with and control the Cortex-M3 CPU.
SWO	Output	**Serial Wire Output.** The SWO pin optionally provides data from the ITM and/or the ETM for an external debug tool to evaluate.

Table 603. Parallel Trace pin description

Pin Name	Type	Description
TRACECLK	Input	**Trace Clock.** This pin provides the sample clock for trace data on the TRACEDATA pins when tracing is enabled by an external debug tool.
TRACEDATA[3:0]	Output	**Trace Data bits 3 to 0.** These pins provide ETM trace data when tracing is enabled by an external debug tool. The debug tool can then interpret the compressed information and make it available to the user.

Fig 13. LPC1700 – Debug and trace pins

8.1.5 IAP location

Similar to LPC2000, LPC1700 supports In-Application Programming (IAP) commands allowing erase and write operations on the on-chip flash memory, as directed by the end-user application code.

In the LPC1700, the IAP location entry point is different than the LPC2000 and it is 0x1FFF1FF1.

8.1.6 Boot ROM re-mapping

In the LPC1700, following a hardware reset, a portion of the Boot ROM is temporarily mapped to address 0 and automatically switches the map to point to Flash memory prior to user code being executed. However, if execution is halted immediately after reset by a debugger, the debugger should correct the mapping for the user by using the MEMMAP register which allows portion of the Boot ROM to be mapped to address 0 or flash memory is mapped to address 0. This is normally transparent to the user and important for tool vendors to be aware of.

9. Conclusion

In conclusion, the migration from the LPC2000 family to the LPC1700 series is a smooth process since a majority of the peripheral functions remains the same while also allowing users to take advantage of the new peripherals, and enhancements mentioned above. In addition, the LPC1700 is pin-to-pin compatible with the popular ARM7-based NXP LPC2300 series. This compatibility allows customers to evaluate both the Cortex-M3 and ARM7-based products in the same socket and to *choose the right microcontrollers for their applications*.

The LPC1700 devices are the fastest Cortex-M3 microcontrollers available in the market, and as mentioned before, users can take advantage of the LPC1700's bus architecture especially for applications requiring simultaneous high bandwidth data streams from Ethernet, USB and CAN without bottlenecks.

10. Legal information

10.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

10.2 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is for the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

10.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

11. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, email to: salesaddresses@nxp.com

Date of release: 6 October 2009
Document identifier: AN10878_1