

MOSFET Fabrication Lab

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Abstract—The MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) is a critical component of modern technology. At lab-scale, its fabrication demonstrates the principles of semiconductor processing and offers perspective on the impressive automation and technological achievements found in a modern semiconductor fab.

In this lab, we fabricated an n-type MOSFET, starting with a silicon wafer and applying a rigorous process including photolithography, oxide removal, growth, diffusion, electron beam evaporation and metal deposition, and lift-off. The reasoning and details of the fabrication procedure are presented, along with an introduction to the technology and discussions of the physics underlying device operation, the reasoning behind fabrication steps, and models available to understand processes. Where possible, images of lab equipment and the device are provided, and although no quantitative data were collected during this experiment, synthetic data and plots are presented to illustrate the principles of fabrication processes.

Overall, n-MOSFET devices are suggested by imagery to have been successfully produced, and valuable exposure to and knowledge of device fabrication were gained.

I. INTRODUCTION

THE MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) is the underlying technology enabling all modern electronics. They are the smallest feature of interest, often used as a metric for the technological achievements in the miniaturization of transistors and performance of electronics. Although devices are now approaching the theoretical limitations of miniaturization due to the size of the electron wave function/quantum tunneling, for the past half-century Moore's law has held, and transistors per chip have roughly doubled every 2 years [1]. MOSFETs remain the dominant technology in integrated circuits and are of great importance to any aspiring electrical engineer.

The MOSFET was invented at Bell Labs in 1959-1960 by Mohamed Atalla and Dawon Kahng, building on previous work by Bardeen, Brattain and Shockley, also at Bell Labs, in 1947 that developed the transistor [2], and Frosch and Derick who developed the first field effect transistor, also at Bell Labs in 1957 [3].

The heart of a MOSFET is the toggleable electron (or hole) channel. This channel is toggled by application of voltage to a gate oxide. The channel's input and output are the source and drain [4]. The dimensions of a MOSFET can vary wildly, from the micron scale used in this fabrication down to a few

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nanometers in the most recent devices. The limiting factor in what dimensions may be achieved is the accuracy and precision of the photolithography step, which will be discussed in more detail later.

MOSFET operation, diagrams and device physics are described in more detail in Appendix 1. PPE, materials, and instruments used in the fabrication process will be described in the next section, with more detailed information provided in Appendix 2.

II. FABRICATION

The fabrication process can be understood as repeated steps of cleaning, oxidation (in ambient conditions or thermally driven), patterning with photolithography, and deposition of metals. At each step, a feature is typically created by cleaning and removing oxide from a surface, applying photoresist and developing a pattern for the desired feature, and laying down the material(s) desired for that feature. This process is described in detail, in chronological order below.

A. Module 1: Cleaning and Field Oxide Formation

Silicon wafers were acquired commercially to be used as the substrate for this fabrication process. The native oxide, SiO₂, that forms on silicon in ambient conditions is of insufficient quality for device operation, therefore a field oxide is grown. However, impurities may already exist on the surface of the sample whether by contamination during manufacturing or exposure to the ambient environment. Therefore, before this field oxide can be grown, the wafers must be prepared and cleaned to remove the native oxide and any impurities.

Wafer surfaces are cleaned using acetone, methanol, isopropanol alcohol (IPA), and deionized water. Wafers are soaked in each solvent for at least two minutes. Multiple solvents are used both to ensure dissolution of contaminants, and to remove residue of one solvent with another (e.g. acetone leaves residues, this is avoided by subsequent rinsing with water). This procedure is conducted repeatedly throughout this process and is termed 'solvent cleaning' and is done within the solvent station pictured below within the CHTM cleanroom.

After the surfaces are cleaned, the native oxide may be removed. This is achieved using piranha solution (a mixture of sulfuric acid and hydrogen peroxide) and buffered oxide etchant (BOE, a mixture of hydrofluoric acid and ammonium fluoride). This process is extremely hazardous and conducted in a dedicated bench while wearing specialized PPE, as described in Appendix 2.

In this particular step, all native oxide was removed from the surface of the wafers; in future steps, a layer of photoresist will serve to protect an oxide where desirable.

After cleaning and native oxide removal, wafers were placed in a furnace for 30 hours for dry thermal oxidation to form the desired field oxide.

III. MODULE 2: PHOTOLITHOGRAPHY AND WET ETCH OF FIELD OXIDE

The objective of this module is to remove the field oxide that has been formed on the samples, but only on the source and drain regions of the device. The photolithography step applied below is used to protect the remainder of the sample from etching, and thereby only remove the field oxide from intended regions.

Samples, now with a field oxide, are first cleaned according to the solvent cleaning procedure. This is done to remove surface contamination prior to the subsequent step.

Photolithography is then performed; photolithography is the procedure by which complex patterns are ‘printed’ on the substrate. This step involves first coating the clean wafers with a layer of photoresist, a polymer-matrix mixture that will soften and become soluble upon irradiation with light. This irradiation is controlled both by the parameters of the light source, and with a photomask: a pattern that permits light to pass only through desired regions and thus obscures certain areas of the wafer and exposes others. After coating with photoresist, samples are soft-baked to partially harden the photoresist polymer by removal of solvents, after which the samples are irradiated.

After irradiation, the source and drain regions within the photoresist are rendered soluble by developer solution. Samples are developed at the developer bench, which involves soaking in photoresist-specific developer solution and then rinsing with DI water, after which the irradiated regions of the sample are exposed and free of photoresist.

The samples are then subjected to an oxygen plasma descum, which cleans the exposed areas, the intended source and drain. The field oxide is then removed. Thus, areas around the source and drain regions are prepared for subsequent doping.

The photoresist, developer solution, lab benches used for preparation and instruments used for irradiation and plasma descum and their parameters are all detailed in Appendix 2.

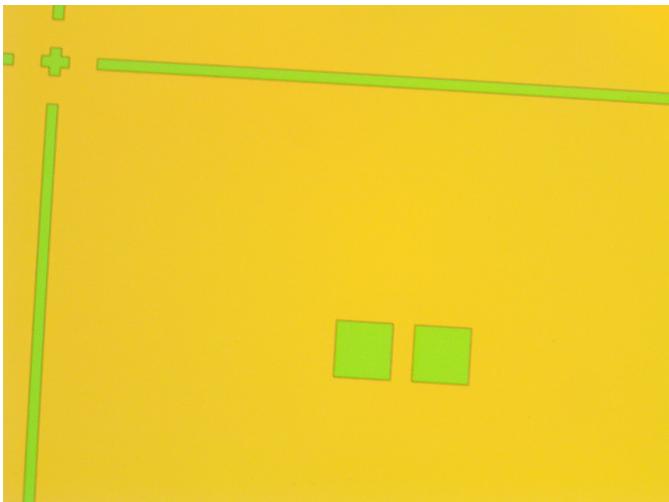


Fig. 1: Post-field oxide etch, showing the source and drain regions exposed.

IV. MODULE 3: PRE-DEPOSITION DIFFUSION

In this step the source and drain, now exposed, are doped such as to have a different band gap than the underlying silicon substrate. This enables the MOSFET channel to form upon applied voltage. Further details on operation are supplied in Appendix 1.

Native oxide is first removed from the samples, after which the source and drain regions have the silicon substrate completely exposed. The dopant is then applied: in this experiment we use phosphosilicate glass (PSG), effectively a coating that supplies phosphorus to the source and drain regions; the phosphorus enters into the substrate via two diffusion steps, detailed below. The PSG is spin-coated onto the wafer. The source and drain regions are the only areas to undergo diffusion, however, as the remainder of the wafer remains protected by photoresist that was left intact by the photolithography step.

After spin-coating, the PSG-coated samples are hard-baked at 200C for 30 minutes in an oven, then the samples are input to a furnace to supply thermal energy to drive diffusion into the wafer at the source and drain regions. This is the first of two diffusion steps and serves to supply a bolus of phosphorus into the silicon substrate that will be further driven into the substrate in a second step.

After diffusion, BOE is used to remove the PSG.

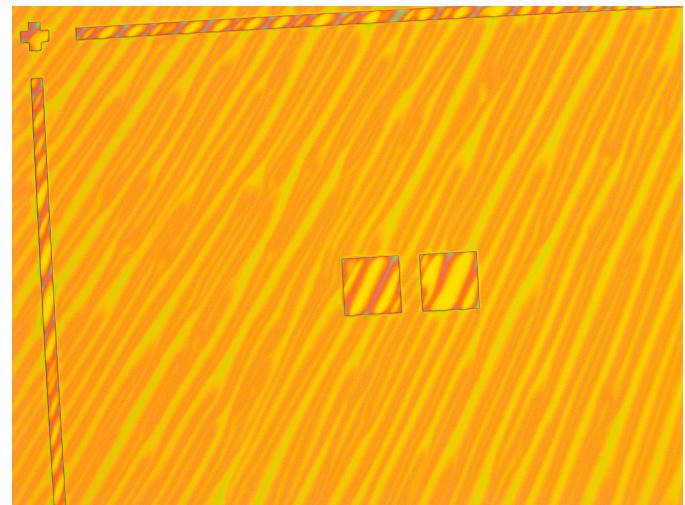


Fig. 2: Samples with PSG coating.

V. MODULE 4: FIELD OXIDE ETCH FOR GATE DEFINITION

We now pattern the sample to prepare the gate region, where voltage is applied to toggle the MOSFET channel. The gate requires a quality oxide to be grown and therefore the field oxide must be removed after patterning. The photoresist pattern for the source and drain remains on the wafer; the second pattern for the gate is aligned to the first, and the sample is then irradiated and developed. This means that two different patterns of photoresist will coat the wafer simultaneously.

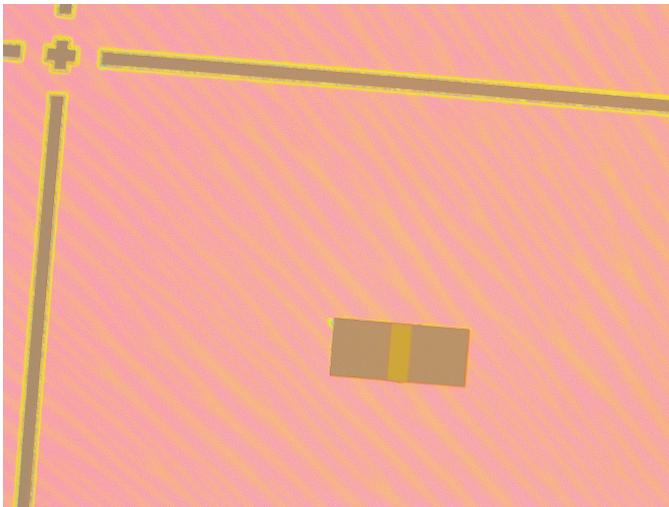


Fig. 3: Samples with gate pattern.

The pattern is formed via photolithography and the field oxide is removed.

VI. MODULE 5: GATE OXIDATION, DOPANT DRIVE-IN AND CONTACT ETCH

The source, drain and gate regions are now patterned and free of photoresist. A bolus of phosphorus has now been injected into the source and drain regions, and the gate region is prepared for oxide growth. Growth of the gate oxide and drive-in of the phosphorus occurs simultaneously.

Samples are cleaned and native oxides removed. They are then loaded into a furnace to complete thermal oxidation and dopant drive-in. Drive-in occurs at 1100°C for 35 minutes with nitrogen flowing.

Oxidation occurs non-selectively: at the gate as intended, and undesirably at the source and drain regions. The oxide formed at the source and drain regions must therefore be removed. This is achieved by another photolithography step, patterning the samples, exposing the source and drain regions, and removing their thermal oxides by soaking in BOE for 8-13 minutes.

At this point, we now have n+ doped source and drain regions, a quality gate oxide, and photoresist coating the remainder of the samples.

VII. MODULE 6: ALUMINUM EVAPORATION AND CONTACT ANNEAL

Metal contacts are next formed at the source and drain regions. This is achieved by depositing metal (aluminum) via electron-beam evaporation deposition.

First, the pattern for the metal contacts at the gate, source, and drain regions is formed by photolithography; outside the intended areas, the photoresist will protect the rest of the device from undesirable aluminum deposition. Once developed, the native oxide is removed from the source and drain regions with BOE.

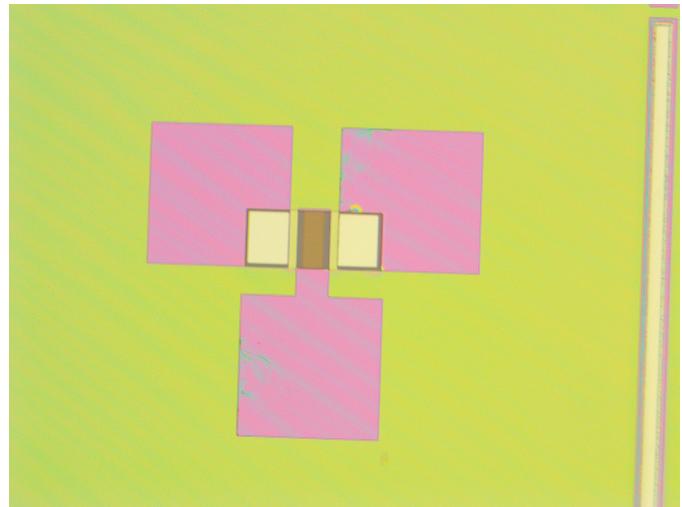


Fig. 4: Samples with contact pattern, prior to aluminum deposition.

The samples are then loaded into an electron-beam evaporator that deposits the aluminum onto the sample. This tool and its operation are further detailed in Appendix 2.

After deposition of aluminum, a lift-off process (detailed in Appendix 2) is used to remove the photoresist, which also removes the aluminum not deposited on the source, drain and gate areas. This is the final addition of material to the sample.

In the final step, samples are loaded into a diffusion furnace to anneal the aluminum contacts. This produces the final device: an n-type MOSFET built on a silicon substrate, with phosphorus-doped source and drain regions topped with aluminum contacts, and a gate region with a quality oxide and aluminum contact.

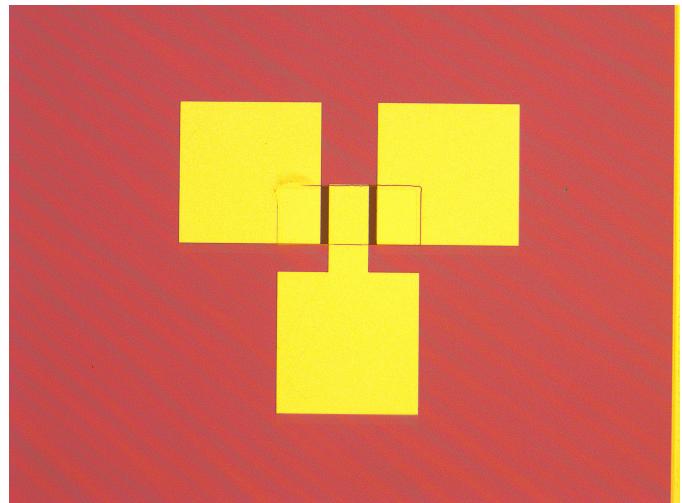


Fig. 5: Final device, showing the source, drain and gate regions.

VIII. DISCUSSION

This lab demonstrated successful fabrication of an n-type MOSFET device, beginning with a silicon wafer substrate and applying multiple rounds of photolithography and development, oxidation, metal deposition, and frequent cleaning and removal of native oxides. The process is laborious and lengthy, and requires multiple weeks of lab sessions to complete. The

accuracy, precision, and meticulousness required to conduct each step safely and effectively was well illustrated.

Beginning from a silicon wafer substrate, we cleaned its surface and removed its native oxide to allow for photolithography and initial patterning to define the source and drain regions. These regions were subsequently doped with phosphorus using PSG and a two-step drive in process. A second photolithography step defined the gate region. The gate, source, and drain regions were cleaned and exposed and then heated in a furnace for thermal oxidation and formation of gate oxide. A third photolithography step coated and protected the gate region and exposed the source and drain regions, allowing for removal of undesired gate oxide. The fourth photolithography step coated the samples, exposing only the source, drain and gate regions. The metal contacts were then created by electron beam deposition of aluminum, which coated the entire sample. A lift-off step removes remaining photoresist, leaving aluminum only at the source, drain, and gate regions. The samples were then loaded into a furnace for annealing the aluminum contacts, yielding the finished n-MOSFET devices.

Characterization of samples was outside the scope of this work. The images of the device-in-progress at each step, and the image of the final device all suggest successful fabrication. However exact material dimensions, properties, and device performance are all unknown. Quantitative data were not collected in this experiment. Therefore, synthetic data are used below to discuss the underlying reasoning of different steps such as diffusion and oxidation.

A. Diffusion

Doping of the source and gate regions is desired to create localized n+ silicon. A two-step drive-in process is used: the first injects dopants near the surface of the silicon, represented as surface concentration C_s and the second step (simultaneous with gate oxide formation) drives these dopants further into the silicon substrate, creating the desired doped regions. This process can be modeled using Fick's laws [5]. The solutions to Fick's first and second law are expressed with the following equations. For pre-deposition diffusion, where a bolus of dopants is initially injected:

$$C(x, t) = C_s \operatorname{erfc} \left(\frac{x}{(2\sqrt{Dt})} \right)$$

Where \sqrt{Dt} is the diffusion length. The second step, drive-in diffusion, is modeled with a concentration profile given by:

$$C(x, t) = \frac{Q_T}{\sqrt{\pi Dt}} \exp \left(-\frac{x^2}{4Dt} \right)$$

Where Q_T is directly related to the initial bolus dose of dopants injected in pre-deposition diffusion.

The expected profiles of pre-deposition and drive-in diffusion can be shown using synthetic data as shown in Figure 6. This plot demonstrates that the dopants are first injected at or near the surface of the substrate. This bolus amount is then driven deeper into the substrate in the second step, as one can observe from the more gradual slope penetrating deeper into the sample. The reasoning for this two-step process is that one can control

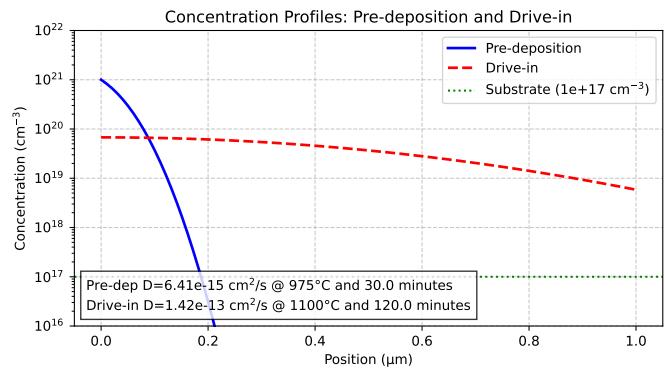


Fig. 6: Diffusion concentration profiles for pre-deposition and drive-in processes.

the amount of dopants injected into the sample in one step, remove the PSG source of dopants, then complete drive-in and achieve the desired doping profile in the second diffusion step, in tandem with gate oxide formation.

This process allows for controlled amounts of dopants to be injected and a specific doping profile to be achieved. The doped regions are critical to device function, as detailed in Appendix 1.

B. Oxidation

Native oxides readily form in ambient conditions on silicon. These native oxides are undesirable and are removed by piranha solution and BOE throughout the fabrication process.

The gate oxide is higher quality than the native oxides and is formed via dry thermal oxidation in furnace. The gate oxide's role in device performance is detailed in Appendix 1. The formation of the oxide can be modeled using the Deal-Grove model [6], again discussed here using synthetic data. The model accounts for diffusion constants, etc. and is represented as:

$$x^2 + \left(\frac{2D}{k} \right) x = \frac{2DC_o}{C_1}(t + \tau)$$

Where

$$\tau = \frac{(t_{ox}^2 + 2Dt_{ox}/k)C_1}{2DC_o}$$

Which is often simplified to:

$$x^2 + Ax = B(t + \tau)$$

Where $A = \frac{2D}{k}$ and $B = \frac{2DC_o}{C_1}$. A, B, and τ can be readily had from tables. Applying this model with the process parameters in this protocol yields the plot below.

This plot shows the growth of silicon dioxide over time according to the Deal-Grove model using parameters for dry oxidation at 1100°C. The curve demonstrates how oxide thickness increases at first linearly, then non-linearly with time, at first limited by the reaction-rate to form silicon dioxide then by diffusion. The model allows for predicting oxide growth rates under the defined conditions.

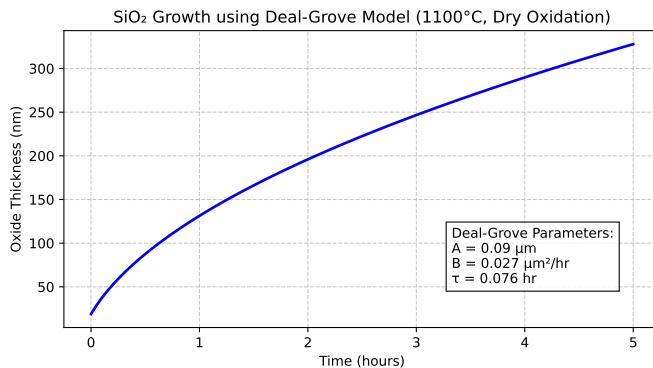


Fig. 7: Silicon dioxide growth based on the Deal-Grove model. The oxide thickness is plotted against time for dry oxidation of silicon at 1100°C.

IX. CONCLUSION

n-MOSFET devices were fabricated according to a rigorous sequence of steps including photolithography, oxidation, diffusion, electron beam evaporation and annealing. The principles of different processes and equations to model them were well-illustrated and discussed using synthetic data. The knowledge and exposure acquired throughout this lab are highly useful and transferable to continued research activities and future pursuits.

ACKNOWLEDGMENTS

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APPENDIX 1: DEVICE PHYSICS AND OPERATION

The MOSFET is constructed of a source, gate, and drain. A conductive channel is toggled (formed or is disrupted, depending on the type of MOSFET) upon application of voltage to the gate. This experiment fabricated an enhancement-type n-MOSFET, so the channel is formed upon applied bias; the rest of this discussion will also focus on n-MOSFET. The source and drain are rectifying p-n junctions composed of doped substrate, topped with metal contacts. The gate is composed of undoped substrate, a gate oxide, and the metal contact. Technically a fourth contact may exist attached to the bottom of the substrate, but this is outside the scope of this experiment.

This device operates in enhancement mode, where the conductive channel (n-type inversion layer) is formed upon application of sufficient voltage to the gate. A channel does not exist without enough applied voltage, only a small leakage current. The gate voltage is denoted as V_G and upon exceeding a threshold voltage V_{th} the channel is formed and current may pass between the source and drain. This results in the desired behavior of a transistor: toggable current, allowing for device I/O and representation of bits 1/0.

The figure immediately below (reproduced from Neamen) shows a cross-section of an n-MOSFET and energy band diagrams demonstrating the underlying physics. Before V_{th} is reached, $V_G < V_{th}$, the potential barrier from the source to drain is too high for electrons to traverse. However, when $V_G > V_{th}$ the potential is lowered enough (inversion) so that electrons can traverse from source to drain; interim processes as V_G approaches V_{th} are termed accumulation and weak inversion [4].

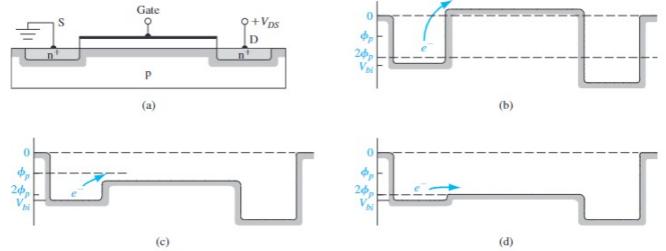


Figure 11.3 | (a) Cross section along channel length of n-channel MOSFET. Energy-band diagrams along channel length at (b) accumulation, (c) weak inversion, and (d) inversion.

Fig. 8: Cross-section of an n-MOSFET and energy band diagrams demonstrating device operation, reproduced from Neamen.

The figures below also show the formation of the inversion layer and behavior of electrons/carriers within [4].

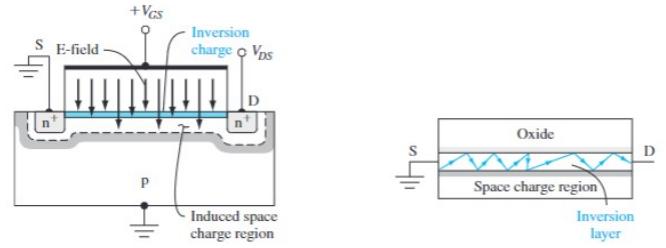


Figure 11.8 | Vertical electric field in an n-channel MOSFET.

Figure 11.9 | Schematic of carrier surface scattering effects.

Fig. 9: Cross-section of an n-MOSFET demonstrating formation of inversion layer and electron channel, reproduced from Neamen.

The effect of increasing voltage on the channel is shown in the figure below, where the inversion layer only forms once $V_G > V_{th}$:

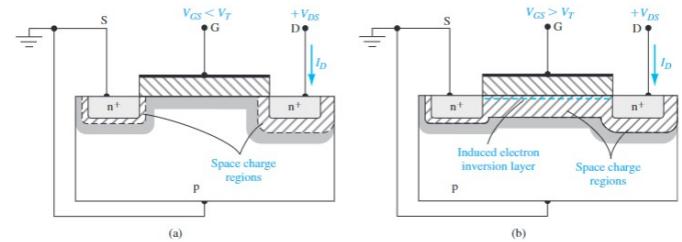


Figure 10.10 | The n-channel enhancement mode MOSFET (a) with an applied gate voltage $V_{GS} < V_T$ and (b) with an applied gate voltage $V_{GS} > V_T$.

Fig. 10: n-MOSFET cross section showing the effect of increasing gate voltage on the channel, reproduced from Neamen.

The current across the MOSFET is related to the applied voltage, along with device geometry and material characteristics. This is shown in the figure below, where the current is plotted against gate voltage; the relationship is quadratic in

the subthreshold region before reaching asymptotic behavior in the saturation region.

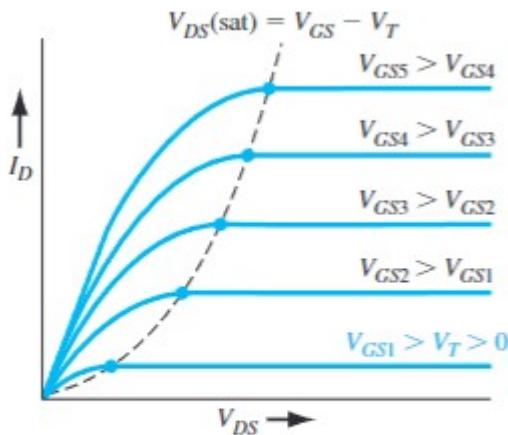


Figure 10.40 | Family of I_D versus V_{DS} curves for an n-channel enhancement mode MOSFET.

Fig. 11: I/V characteristics of an n-MOSFET, reproduced from Neamen.

This relationship is defined by the following equation, which relates applied voltage, threshold voltage, channel length, electron mobility in the channel and channel width using the following equations. The first equation is valid in the non-saturation region:

$$I_D = \frac{W\mu_n C_{ox}}{2L} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

And the second equation defines the relationship in the saturation region:

$$I_D = \frac{W\mu_n C_{ox}}{2L} (V_{GS} - V_T)^2$$

Where I_D is the drain current, μ_n is the electron mobility, C_{ox} is the oxide capacitance per unit area, W is the channel width, L is the channel length, and V_{DS} is the source-drain voltage.

We therefore see that the device design, applied voltage and the quality of oxide all impact current and device performance. There is a ceiling on the current achievable with a given device, but a discussion of breakdown voltages and other limitations is outside the scope of this experiment.

The nature of the MOSFET architecture allows for relatively simple fabrication steps, where the resolution of the photolithography patterning technique is the principal limitation on device scale down. These advantages in fabrication and the reliability of the MOSFET in operation are why it has become the dominant technology for integrated circuits.

APPENDIX 2: MATERIALS, EQUIPMENT AND PROCEDURES

A. PPE

The PPE used throughout the experiments typically included a cleanroom bunny suit, nitrile gloves overlaid with latex gloves, hair bonnet, mask, optionally beard cover, and safety glasses.

Additional PPE is used during the oxide removal process, which uses piranha solution and buffered oxide etchant, including an acid apron and specialized gloves and face shield.

B. Materials

Material Safety Data Sheets (MSDS) for these chemicals are available at <https://www3.cthm.unm.edu/MSDS/> while connected to the UNM network or VPN.

Oxide removal uses piranha solution (a mixture of sulfuric acid and hydrogen peroxide) and buffered oxide etch (BOE, a mixture of hydrofluoric acid and ammonium fluoride).

Solvent cleaning uses acetone, isopropanol alcohol (IPA), methanol, deionized water and compressed nitrogen gas.

Chemicals used during photolithography include hexamethyldisilazane (HMDS), AZ-5214E photoresist, AZ400K 1:4 developer, and deionized water.

Doping uses phosphosilicate glass.

Electron beam lithography uses aluminum, which is evaporated and deposited on the samples.

Lift-off uses acetone, IPA and compressed nitrogen gas.

C. Equipment and Procedures

1) *Solvent Cleaning:* Solvent cleaning in this experiment involves soaking the samples in each solvent for a minimum of two minutes. This occurs within the solvent station, pictured below. Solvents are poured into beakers and samples are transferred between each using tweezers, then dried with compressed nitrogen gas.



Fig. 12: Solvent bench.

The typical regimen is acetone, methanol/IPA, deionized water followed by drying with compressed nitrogen gas. Soft-bakes are used to remove solvents.

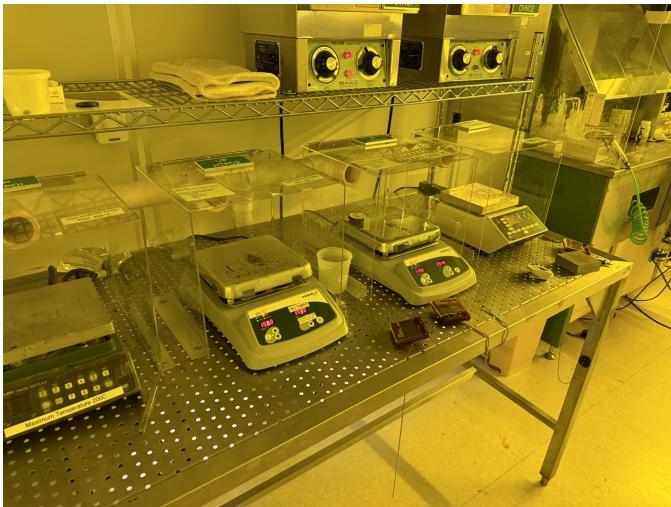


Fig. 13: Hot plates used for soft- and hard-bakes



Fig. 15: Mask Aligner

2) *Photolithography*: HMDS is first applied as an adhesive for the photoresist using a disposable plastic dropper. Photoresist (AZ-5214E throughout this experiment) is then spin-coated onto samples: samples are first loaded onto the sample holder, vacuum is applied to hold the sample during spinning, and photoresist is applied with a disposable plastic dropper until the sample is coated. Spin-coating throughout this experiment occurs at 3000rpm.

After spin-coating, samples are soft-baked at 90°C for 90 seconds to remove solvents and partially harden the photoresist coating to make it suitable for subsequent alignment, exposure and development.

Exposure occurs on the Karl-Suss instrument, using i-line (365 nm) and an exposure time of 25 seconds.

Development refers to soaking the exposed samples (with weakened, soluble photoresist) in developer solution, throughout this experiment AZ400K 1:4, for 45 seconds. Then samples are rinsed in deionized water baths.

After development, samples are subjected to a dehydration-bake, at 150C for 5 minutes to remove solvents and harden remaining photoresist.

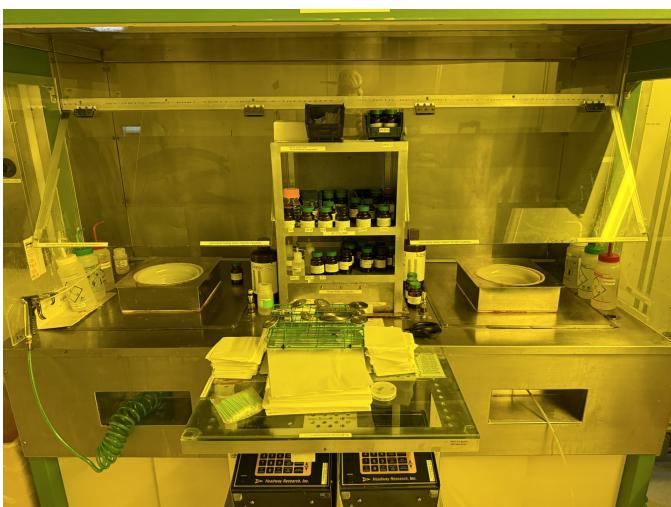


Fig. 14: Photoresist bench



Fig. 16: Developer bench

3) *Descumming*: Oxygen plasma is used to descum the exposed areas. Different settings are used per step.

For cleaning the source and drain regions after initial development, descumming occurs for 2 minutes, 0.1 Torr, 100V.

Prior to metal deposition, samples are descummed (cleaning the exposed source, drain and gate regions) for 20 minutes at 100 mTorr at 100V setting.



Fig. 17: Plasma descrubber

4) Oxide Removal (Piranha and BOE): Oxide removal is achieved with soaking in piranha solution for 5 minutes and in BOE for 30 seconds.

Prior to PSG application, samples are soaked in BOE for 14 minutes to ensure the surface of the silicon substrate is exposed.

Gate oxide removal required soaking in BOE for 8-13 minutes.

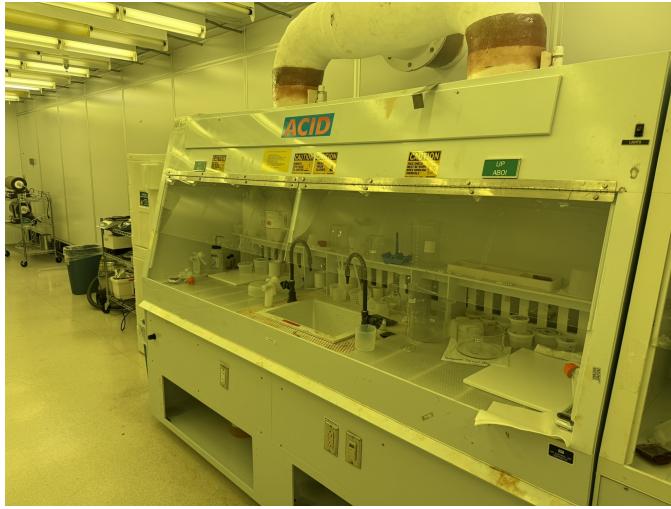


Fig. 18: Acid bench, where piranha and BOE are used to remove oxides

5) Alignment procedure: In the case of the first pattern being transferred to the sample, alignment is concerned with fitting to the dimensions of the wafer. This is done visually. Alignment of two or more patterns is achieved by using alignment markers included within the photomask patterns. This is done by first partially aligning one pair of markers, identifying another pair on the opposite side of the sample, and then iteratively aligning the two pairs, swapping back and forth to gradually eliminate runout. This is better explained with the two figures below that demonstrate misalignment and runout:

6) Electron Beam Deposition of Contact Metal: An electron beam evaporator is used to evaporate and deposit aluminum onto the samples. The parameters used in this experiment are:

a pressure of 1e-6 Torr, 9.8kV, and 33.3 minutes of operation. The deposition rate was 1 Angstrom per second, and 200nm of aluminum was deposited.



Fig. 19: Electron beam evaporator

7) Lift-off: In this procedure, we ‘lift-off’ the photoresist and any materials that may be on top of the photoresist. In this experiment, this preserves the metal contacts atop the source, gate and drain regions but removes photoresist and excess aluminum from the rest of the device.

The lift-off procedure is conducted immediately after deposition of aluminum. Samples are soaked in acetone for 24 hours at ambient temperature. The acetone is then rinsed off with IPA, and compressed nitrogen gas is used to dry the samples.

Acetone is chosen as the solvent for our lift-off step for its specificity to dissolve the photoresist, while leaving the metal contacts intact. It is also readily available.

8) Annealing Metal Contacts: Samples are annealed in the diffusion furnace with flowing nitrogen, at 450°C for 30 minutes.



Fig. 20: Diffusion furnace

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