Intel® Curie™ Module

Design Guide

August 2016

Revision 1.0

Revision History

Revision	Description	Date
1.0	Initial release	August 2016

§

Tables

Figures

1 Introduction

This document provides design recommendations for the Intel® Curie™ platform, which is based on the Intel® Quark™ SE system on a chip. Technical implementation examples provided are derived from the functional reference circuits.

Note: The guidelines provided in this document are based on preliminary simulation work done at Intel while developing systems based on the Intel® Curie™ module and the Intel® Quark™ SE micro-controller. This work is ongoing, and the recommendations are subject to change.

Note: All 3rd party components shown in this document are for reference example purpose only and customers have to evaluate and choose the right components based on their use case.

CAUTION: If the guidelines listed in this document are not followed, it is very important that the designers perform thorough signal integrity and timing simulations. Even when following these guidelines, Intel recommends the critical signals to be simulated to ensure proper signal integrity and flight time.

1.1 Audience and purpose

The Intel® Curie™ Platform Design Guide is provided as an aid for hardware designers and system integrators.

The functional reference circuits were created to provide information and guidance on the following subjects:

- Block diagrams of system level communications and functional reference circuits interface configurations
- System mechanicals and board topology, routing requirements; and layout recommendations
- Power distribution, reset logic, boot sequencing; and energy management
- Factory test, debug, recovery; and troubleshooting
- Alternate implementation options

Note: This design guide has been developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues. Design recommendations are based on Intel's simulations and lab experience and are strongly recommended, if not necessary, to meet the timing and signal quality specifications. They should be used as an example but may not be applicable to particular designs. The guidelines recommended in this document are based on experience, simulation, and preliminary validation work done at Intel while developing the Intel® Curie™ processor-based platform. This work is ongoing, and recommendations are subject to change.

Metric units are used in some sections in addition to the standard use of U.S. customary system of units (USCS). If there is a discrepancy between the metric and USCS units, assume the USCS unit is most accurate. The conversion factor used is 1 inch (1000 mils) = 25.4 mm.

1.2 References

Table 1 **References**

Document name
Intel® Curie™ Datasheet

1.3 Terminology

Table 2 **Terminology**

Term	Definition
ADC	Analog-to-digital converter
ANT	Antenna
AON	Awake-ON
SoC	Intel® Quark™ SE
BALUN	Balanced-unbalanced
BLE	Bluetooth* low energy
BOM	Bill of materials
CPU	Central processing unit
CTS	Clear to send
Intel® Curie™ Module	Intel's highly integrated module based on the Intel® Quark™ SE SoC
DCCM	Closely coupled data memory
DSP	Digital signal processor
ERM	Eccentric Rotating Mass
FAR	False acceptance rate
Finish	The material used to protect the exposed copper on the PCB
FRR	False rejection rate
FW	Firmware
GUI	Graphical user interface
Impedance	The effective resistance of a trace, circuit or component
NFC	Near field communication
OEM	Original equipment manufacture
OS	Operating system
OTP	One-time programmable
PMA	Power matters alliance
PCB	Printed circuit board
POR	Power-on reset
PRU	Port replacement unit
PTU	Power transmit unit
PWM	Pulse width modulation
Qi	An interface standard developed by the Wireless Power Consortium for inductive electrical power transfer
RAM	Random access memory.
RF	Radio Frequency
Soldermask	An electrically insulating material covering traces on the external layers of a PCB
SW	Software
Space	The distance between copper features (such as traces) on the PCB
Trace	A copper line on the PCB used to connect components
UART	Universal asynchronous receiver transmitter.
VIA	Plated hole in the PCB used to connect layers
WPC	Wireless Power Consortium.
X-Y	The area of a board (the length of each side)
Z	The thickness of a board (the Z dimension)

2 System Fundamentals

2.1 Block diagrams

The next two block diagrams shows the Intel® Curie™ module and then the module within a typical platform.

Figure 1 **Intel® Curie™ module block diagram**

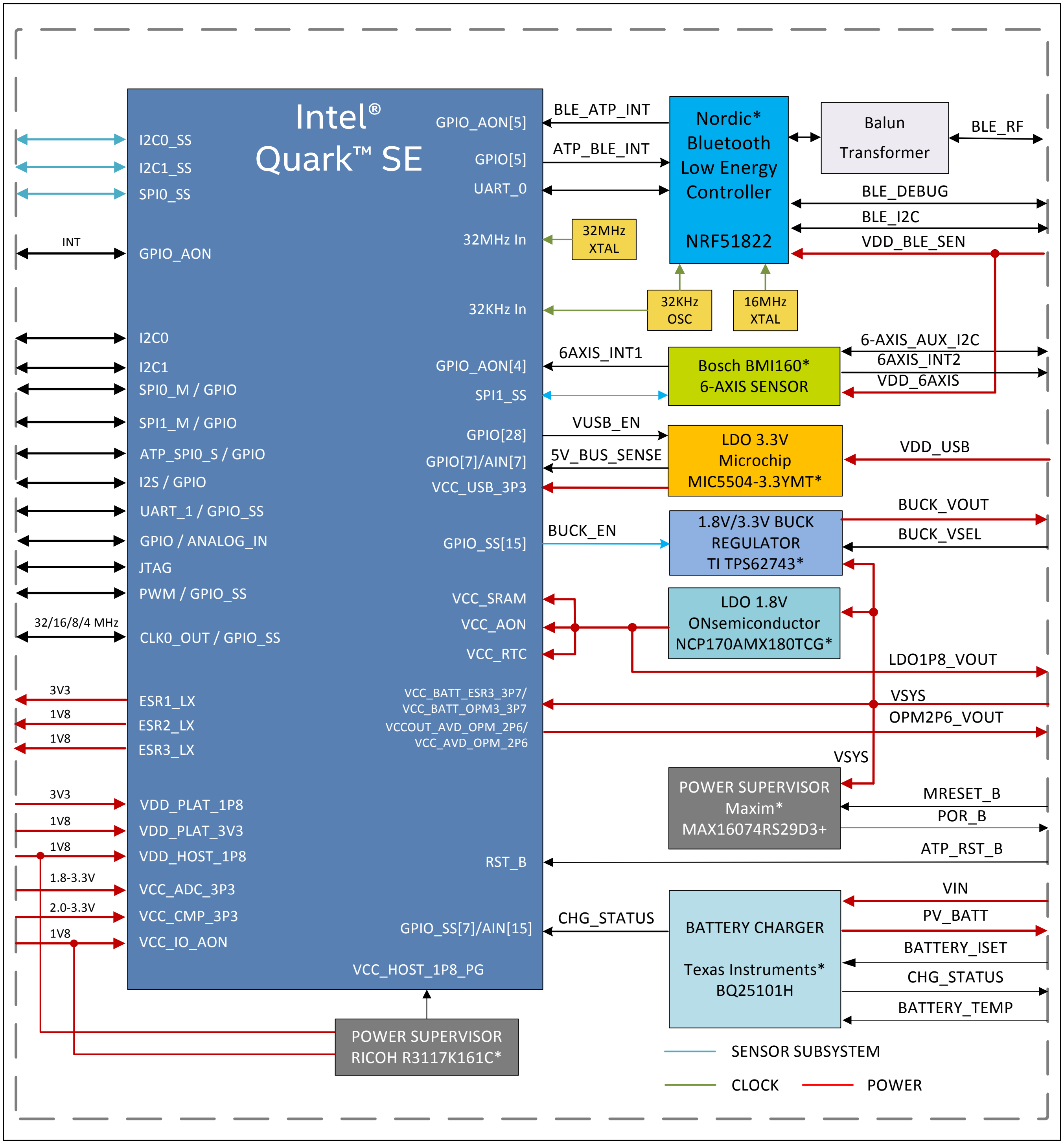
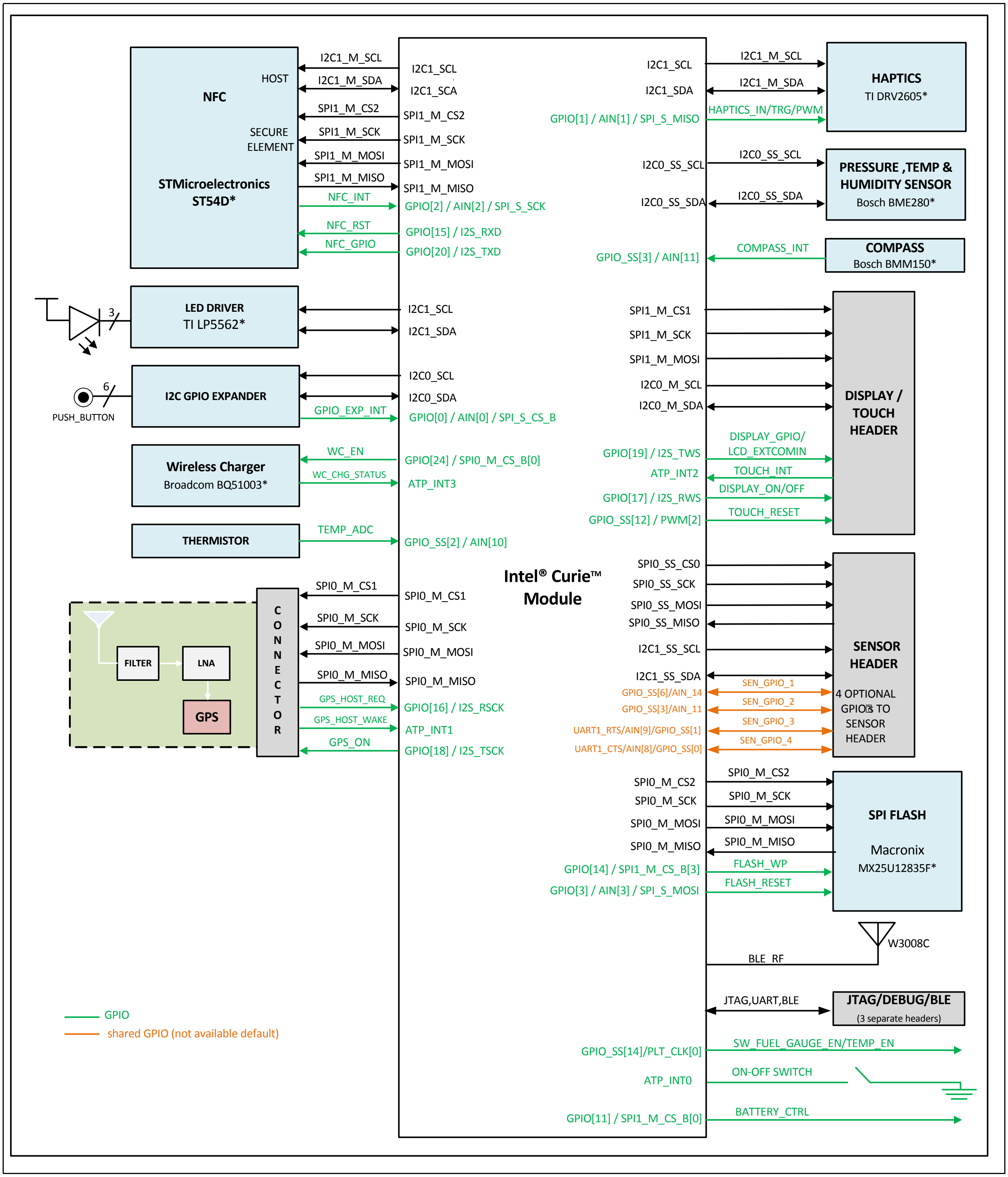


Figure 2 **Conceptual device block diagram**



2.2 Platform electrical specifications

Refer to the Intel® Curie™ Module datasheet for complete specification.

2.3 Intel® Curie™ module footprint

Refer to the Intel® Curie™ module manufacturing guide for more information.

2.3.1 Breakout pitch of module

Due to the lateral pitch (0.0224” or 0.57 mm) on the Intel® Curie™ module package, there is a space of 0.0124” between the pads that requires a Trace and Space of 0.004” / 0.1” for breakout of the package on the external layer.

3 Power and Energy

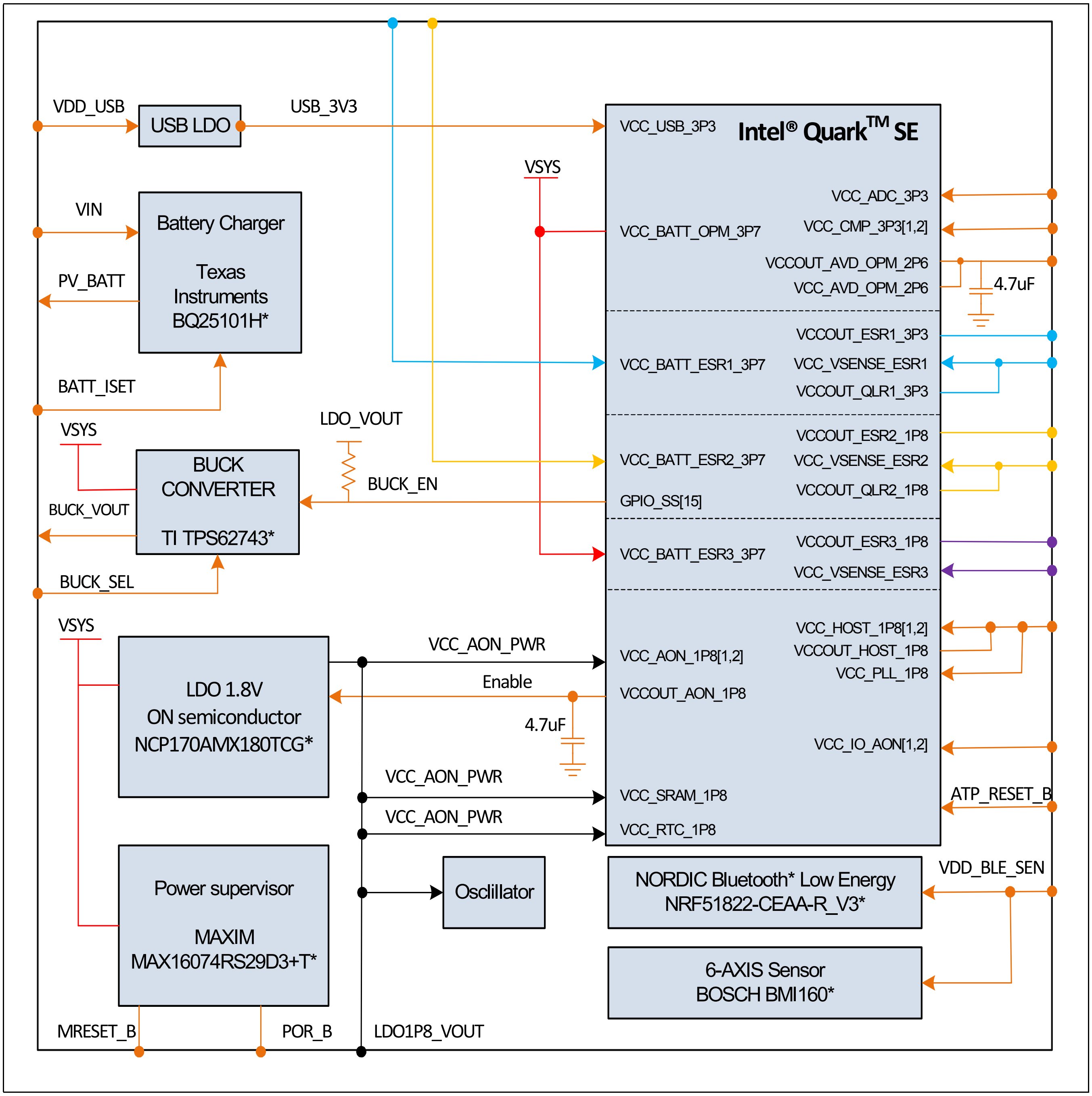
The power input of the Intel® Curie™ module is intended to be supplied by direct USB power, a charging device; or a battery as selected from a priority basis of those available.

3.1 Power requirements and distribution

The Intel® Curie™ module requires a clean and stable power supply. Poorly designed regulators or filters that drift at low loads or that do not handle transit changes with precision can impact module performance and reliability.

Refer to the Intel® Curie™ module datasheet for power numbers.

Figure 3 **Power distribution inside Intel® Curie™ module**



Note: The above diagram is for reference only; power connections within the module cannot be modified.

3.2 Power supervisor, reset and voltage regulators

3.2.1 Power supervisor

The Intel® Curie™ input power is monitored for a threshold level by power supervisor circuit present inside the module.

If the system voltage falls below 2.9 VDC, the power supervisor will pull the POR_B pin LOW to keep SoC in reset state.

3.2.2 Manual reset logic

While the Intel® Curie™ does not include a physical reset, it does provide support manual reset switches and it is recommended to design them into your device by pulling the ATP_RST_B line to ground, holding the CPU in reset.

3.2.3 AON IO Power

This pin powers the AON block of the Intel® Curie™ and must comply with the timing sequence shown in Figure 12

If the IO voltage is 1.8V, it is recommended to use LDO1P8_VOUT to power this pin.

It can be fed by other power supplies also provided it meets the power sequence requirements. If the IO voltage is set to 3.3 VDC, then supplying from the ESR1 regulator is permitted.

3.2.4 VSYS

Main power input for the Intel® Curie™. This supplies the OPM regulator, AON block, ESR3 and BUCK regulator.

Use a 0.1uF decoupling capacitor.

3.2.5 Comparator power

CMP_3P3_VCC is the comparator block power input pin. Use 0.1uF decoupling capacitor. Use a clean power supply for good performance. Keep the power supply traces away from high frequency signals, DC-DC converters, and RF.

3.3 Battery charging and management

3.3.1 Integrated charging device

The Intel® Curie™ module has a built-in, low-leakage single-path Li-ion / Li-Po battery charger. This battery charger supports 3.8V batteries with charging voltage of 4.35V.

Charge current is hardware configurable from 60mA to 250mA by reference voltage at the BATT_ISET pin.

The minimum battery capacity supported is 120mAH (assuming the standard battery charge current is 0.5C) If the battery charge current is less than 60mA, an external charger should be used and not the internal charger.

The charger has three phases of charging: pre-charge to recover a fully discharged battery, fast-charge constant current to supply the charge safely; and voltage regulation to safely reach full capacity. The fast-charge current is programmable and the pre-charge current is 20% of fast-charge and termination current is 10% of the fast-charge current.

If the battery voltage is below the 2.5V, the battery is considered discharged and a preconditioning cycle begins. The charging happens at the pre-charge current level. Once the battery voltage has charged to the 2.5V threshold, fast-charge is initiated and the fast-charge current is applied.

The typical battery charger circuit is shown below. For low power or smaller size battery application, it is good to use a load switch on the VBATT to VSYS path to implement a ship mode circuit. The ship mode circuit will help increase the shelf life of the product.

VIN should be connected to the charging source (for example USB VBUS). Battery should be connected to the PV_BATT. CHG_STATUS indicates the charging status and LOW indicates charging and HIGH indicates charging completed.

Connect the BATT_TEMP to the NTC of the battery if available. If not, connect it to a 10K resistor and it will disable the temperature monitor. BATT_ISET is used to configure the battery charger current (also called as fast charge current) by connecting an external resistor to GND.

Table 3 **Formula to calculate resistor for battery charge current**

RISET = KISET / IOUT

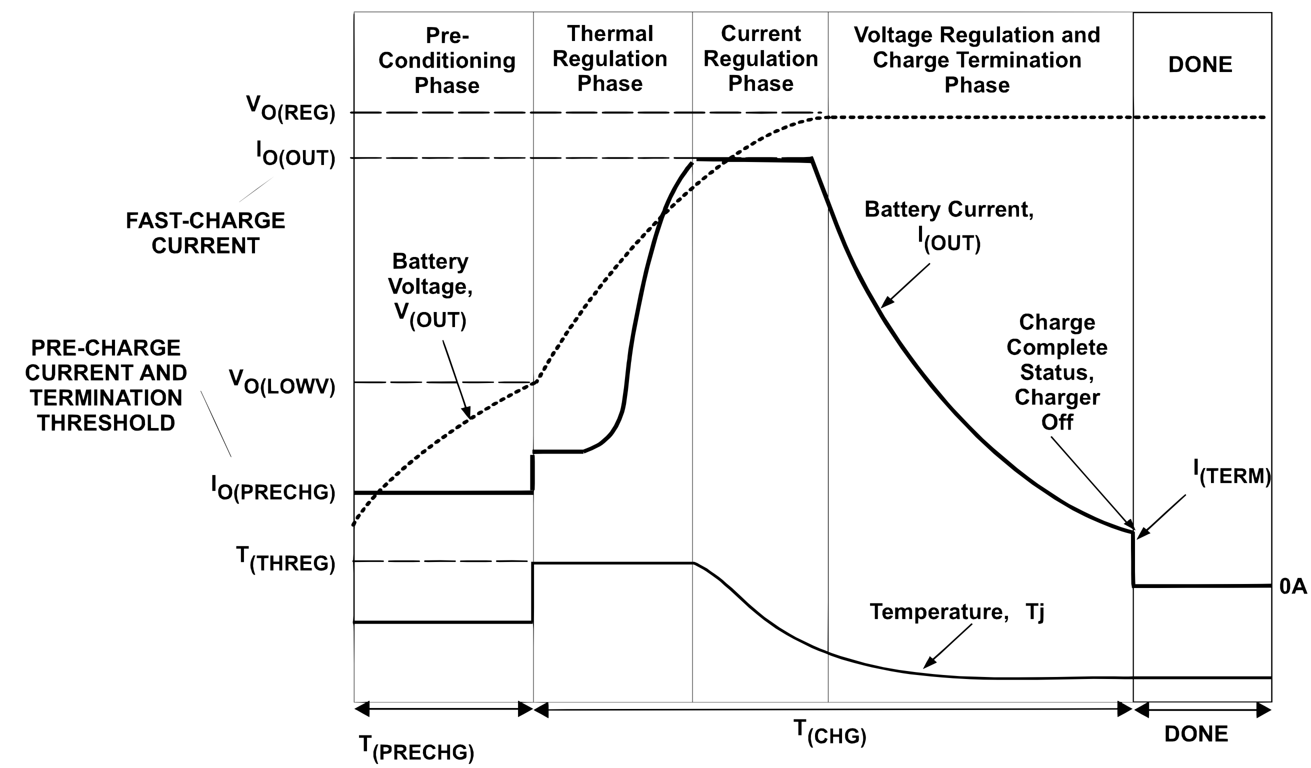
Where:

IOUT is the desired fast charge current

KISET is the gain factor whose value is 135 A ohms Typical. (Min 129 and Max 145)

3.3.1.1 Integrated charger profile

Figure 4 **Battery charging profile example**



3.3.2 Charging circuit example

In the example circuit shown below:

VIN is connected to the charging source (for example USB VBUS).

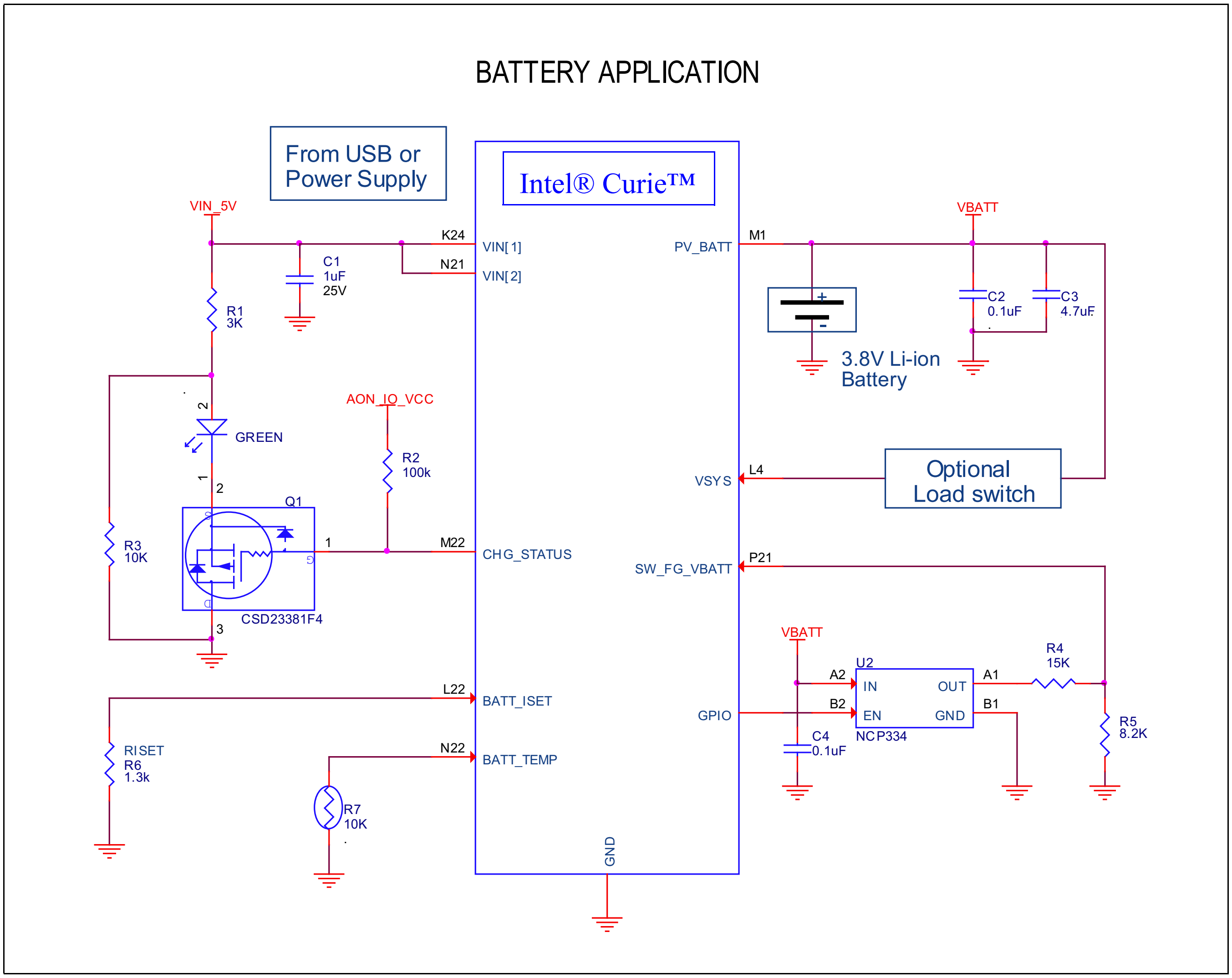
PV_BATT is connected to the battery.

CHG_STATUS indicates the charging status and LOW indicates charging and HIGH indicates charging completed.

BATT_TEMP connects to the NTC of the battery if available. If not connect it to a 10K resistor and it will disable the temperature monitor.

BATT_ISET is used to configure the battery charger current (also called as fast charge current) by connecting an external resistor to GND.

Figure 5 **Battery application - example circuit**



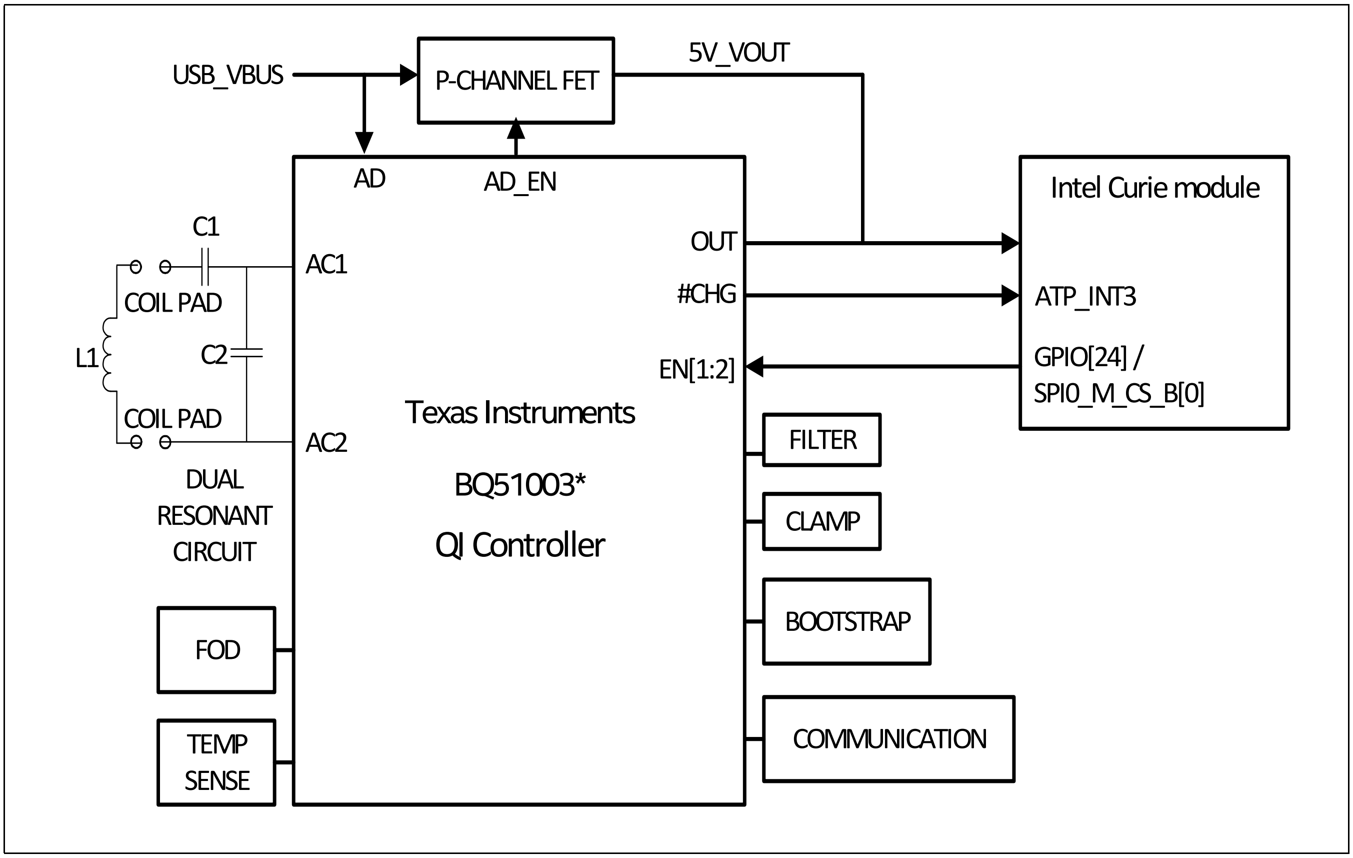
3.3.3 Wireless charger

This example is based on the Texas Instruments BQ51003* device, a WPC/Qi based wireless with these key features:

- Provides 5 VDC output to charge a battery
- WPC v1.1 compliant communication control
- 93% overall peak AC-DC efficiency
- Full synchronous rectifier
- Temperature monitoring inputs

Note: Contact the original device datasheet for latest product information.

Figure 6 **Wireless charger - example circuit**



3.3.4 Charing status indicator

The CHG_STATUS pin on Intel® Curie™ is an open drain that indicates charging in progress with a LOW (0) signal and that charge is complete with a HIGH (1) signal. This can drive a simple LED or other indicator circuit.

If BATTERY_TEMP signal is connected to ground, this disables the internal battery charger and makes the CHG_STATUS pin available for other use as GPIO_SS_[7] or AIN[15].

3.3.5 Charging mode (wired / wireless) selection and indicator

When an external source, like wired USB power, raises the AD pin above 3.6 VDC then the wireless charger is disabled and the AD_EN output is driven HIGH to switch ON the external P_Channel FET.

Adapter mode can be enabled by providing low to the EN[1:2] control pin. In this mode, wired and wireless power modes are enabled but priority is provided to wired power.

Wired and wireless charging power can be disabled through setting EN[1:2] high.

Charging indication pin is provided to AON_GPIO of SoC, through which battery charging can be detected.

The conceptual design can include a green LED to indicate when 5 VDC is available either through wireless charger or USB.

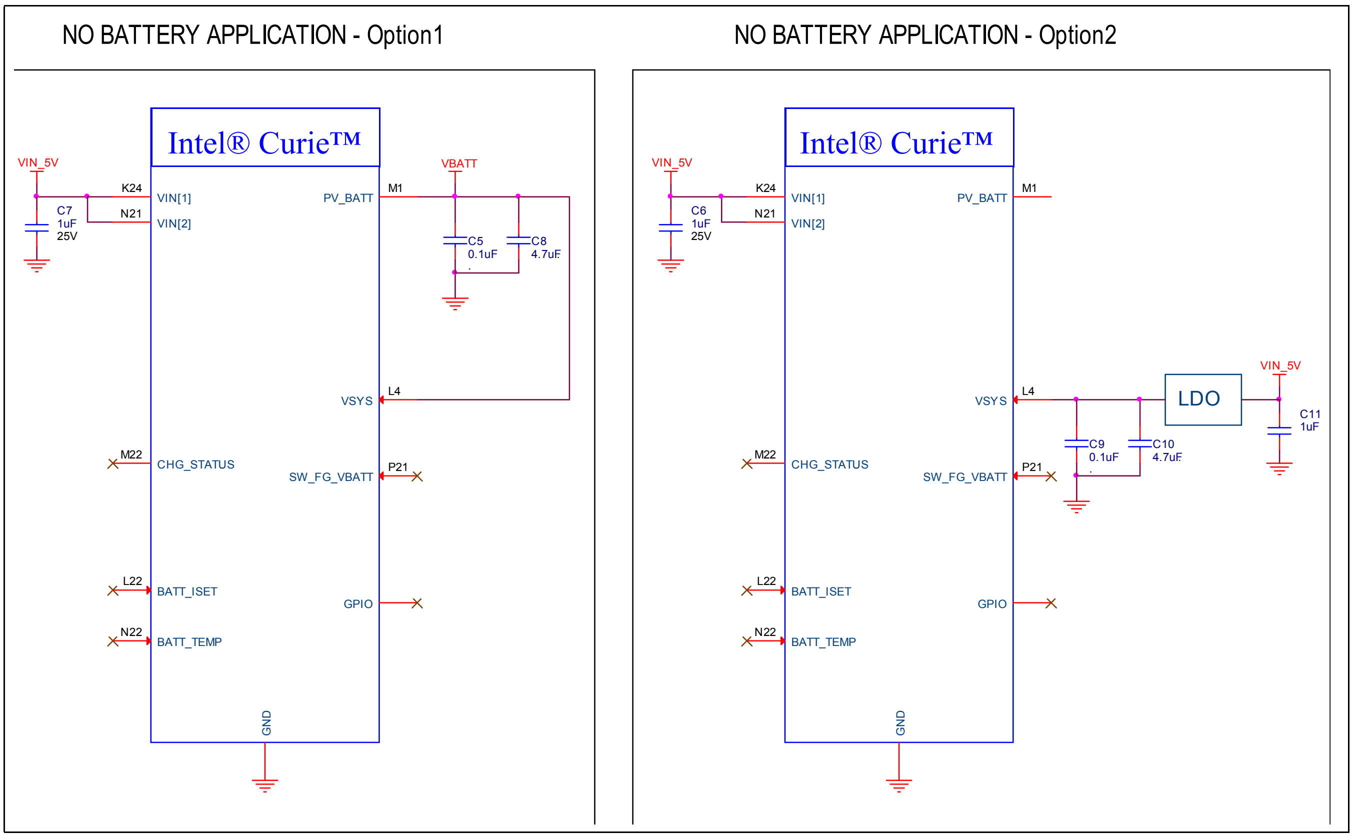
3.4 No battery configuration

For designs that function on direct power sources and without a battery connected, implementing one of the following two circuit schemes is recommended for best results.

Leaving BATT_TEMP open puts the charger in NO BATTERY mode, where the charger does not attempt to charge the battery.

The VIN1, VIN2, BATT_ISET, CHG_STATUS and PVT_BATT can be left open if no battery is present in the system.

Figure 7 **Example circuits for no battery application**

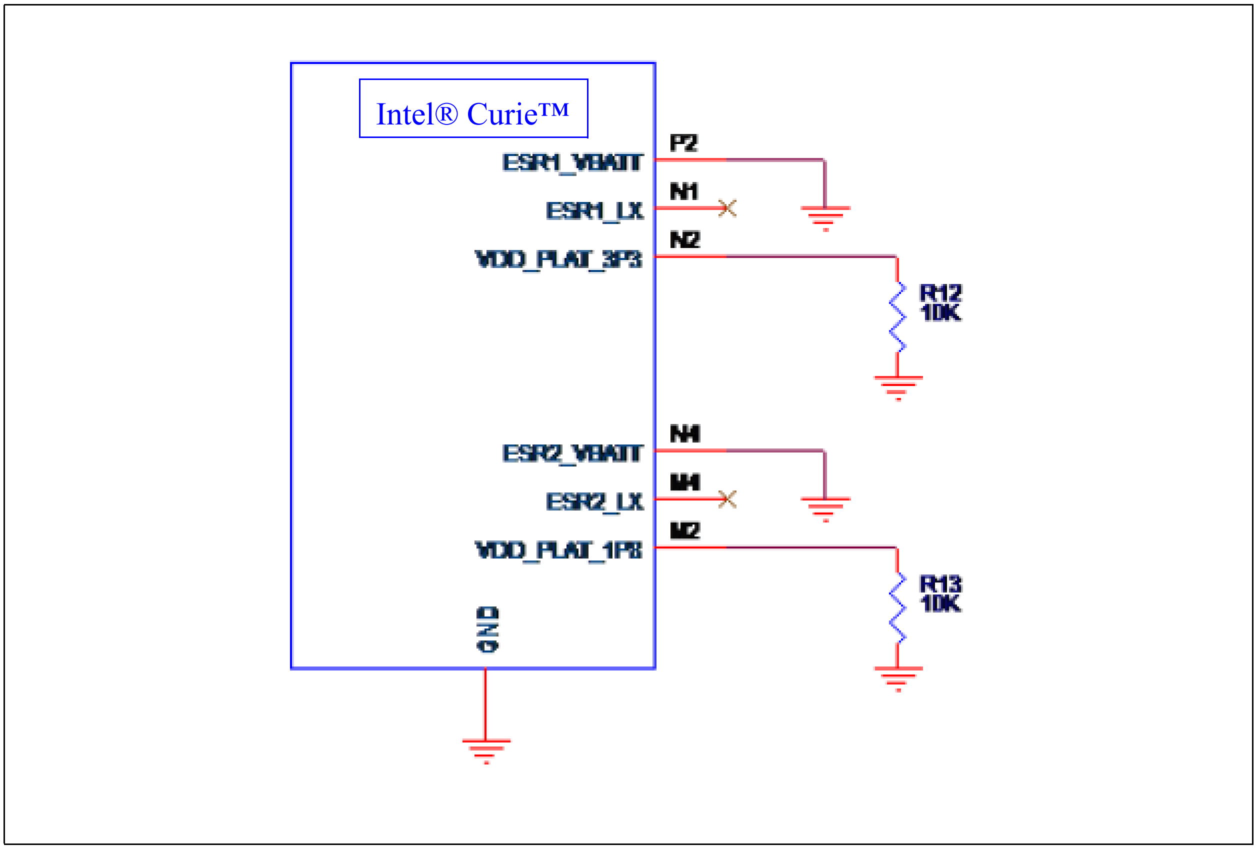


3.4.1 ESR1 and ESR2 regulators

Do NOT use these regulators. It is highly recommended to connect the pins below to reduce leakage current.

- ESR1_VBAT and ESR2_VBATT - connect to ground
- ESR1_LX and ESR2_LX - leave open
- VDD_PLAT_3P3 and VDD_PLAT_1P8 - connect using 10k resistor to ground

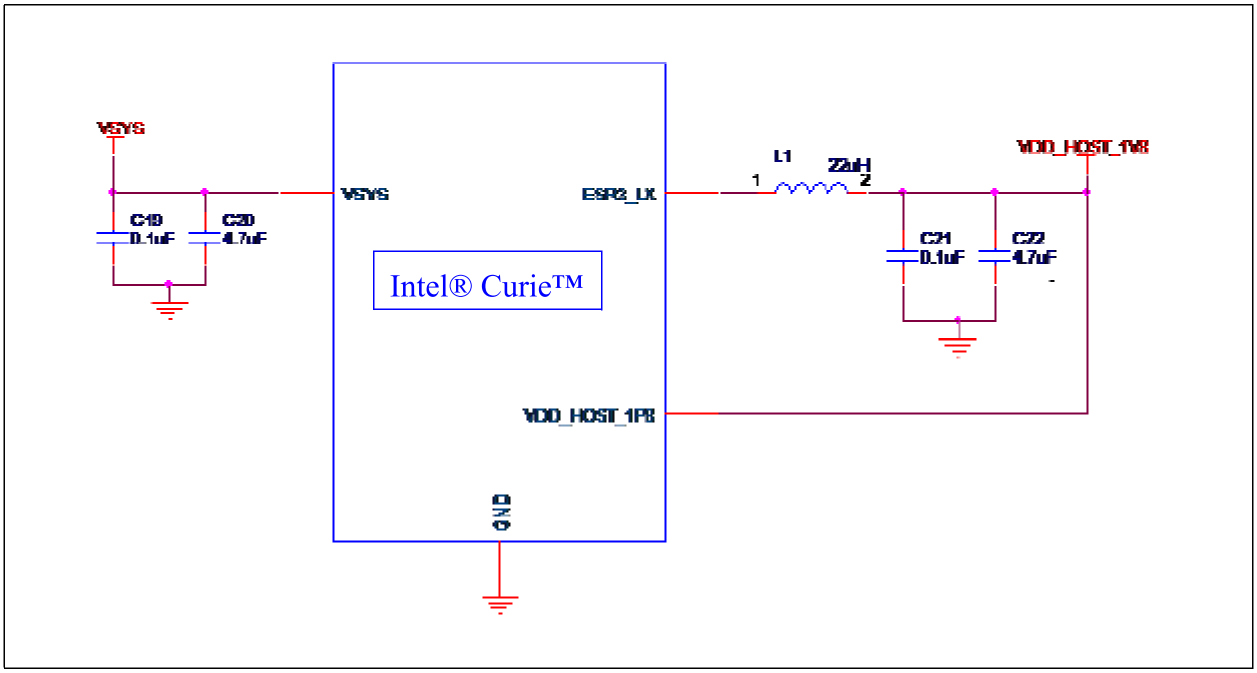
Figure 8 **ESR1 and ESR2 regulator**



3.4.2 ESR3 regulators

.The purpose of the ESR3 regulator is to power the core of Intel® Curie™ module. Maximum capacity of the ESR3 regulator is 100mA and typical output is 1.8V +/-10%. Use this to power Intel® Curie™ module only and DO NOT use it for any other purpose.

Figure 9 **ESR3 regulator**



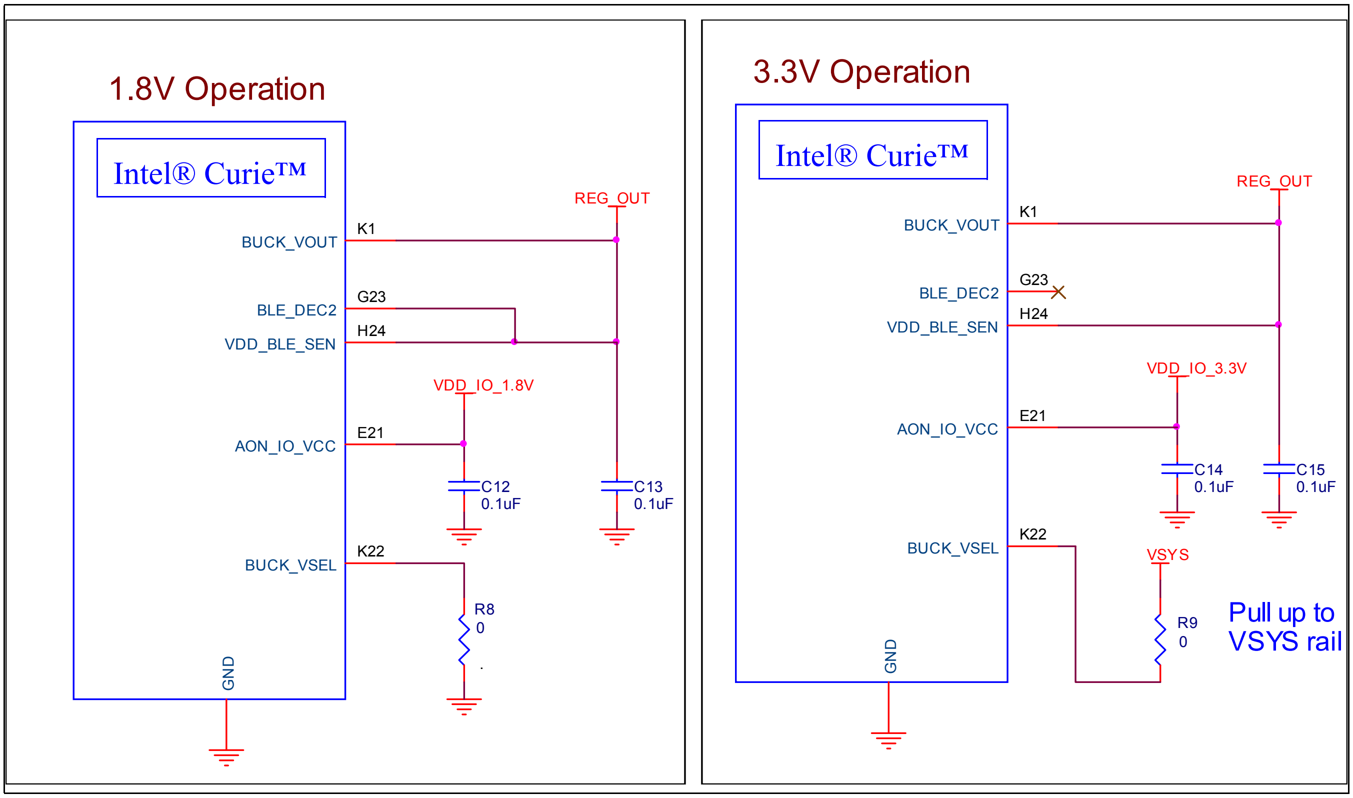
3.4.2.1 Bluetooth* and sensor power

The Bluetooth and sensor block within Intel® Curie™ are powered by a common source, this can be 1.8V or 3.3V.

The voltage levels of VDD_BLE_SEN should match with AON_IO_VCC which is the IO power supply of module.

It is recommended to use the BUCK_OUT of the Intel® Curie™ to power the VDD_BLE_SEN. The Intel® Quark™ SE SoC can disable this converter when not needed; typical 70nA quiescent current consumption.

Figure 10 **Example Circuit for Bluetooth operating at 1.8 VDC**

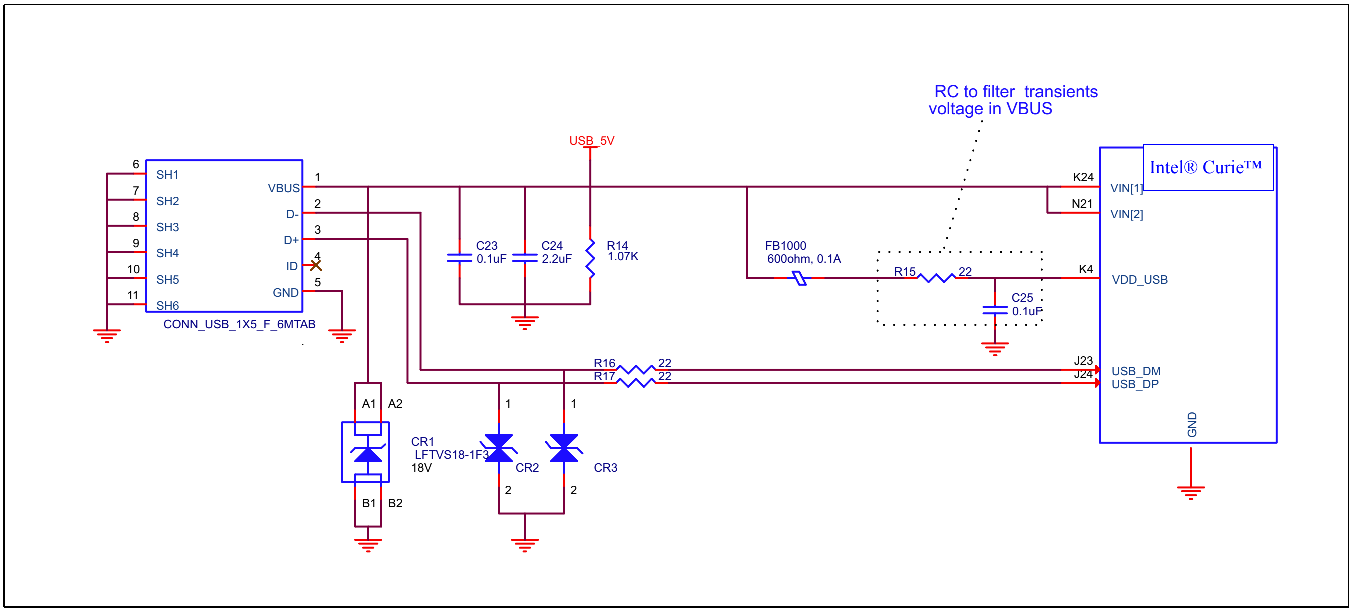


3.4.3 USB power and protection circuit

VDD_USB powers the USB logic in Intel® Curie™ module. This should be connected to USB VBUS using a RC network. The purpose of the RC network is to suppress any surges in the VBUS. 22 ohm and 0.1uF should be good value for the RC. It is highly recommended to have a protection device on the USB VBUS and the DP/DM lines of USB.

Figure 11 provides a circuit-example of USB filtering and protection.

Figure 11 USB power and protection example circuit



3.5 Power ON sequencing

Figure 12 shows the power sequence diagram of Intel® Curie™ module; timings shown are typical results.

All rails except VSYS and AON_IO_VCC are outputs.

VIN is the system power supply.

AON_IO_VCC has to be supplied externally.

It is recommended to use VCC_AON_PWR to power the AON_IO_VCC. If it is fed by any other source, the design must ensure the timing specifications are met.

The internal TPS62743 buck regulator is fed by VSYS; VSYS enable is controlled by the a module GPIO.

During power on the TPS62743 is enabled and can be turned off if needed by the software.

Figure 12 **Intel® Curie™ power sequence**

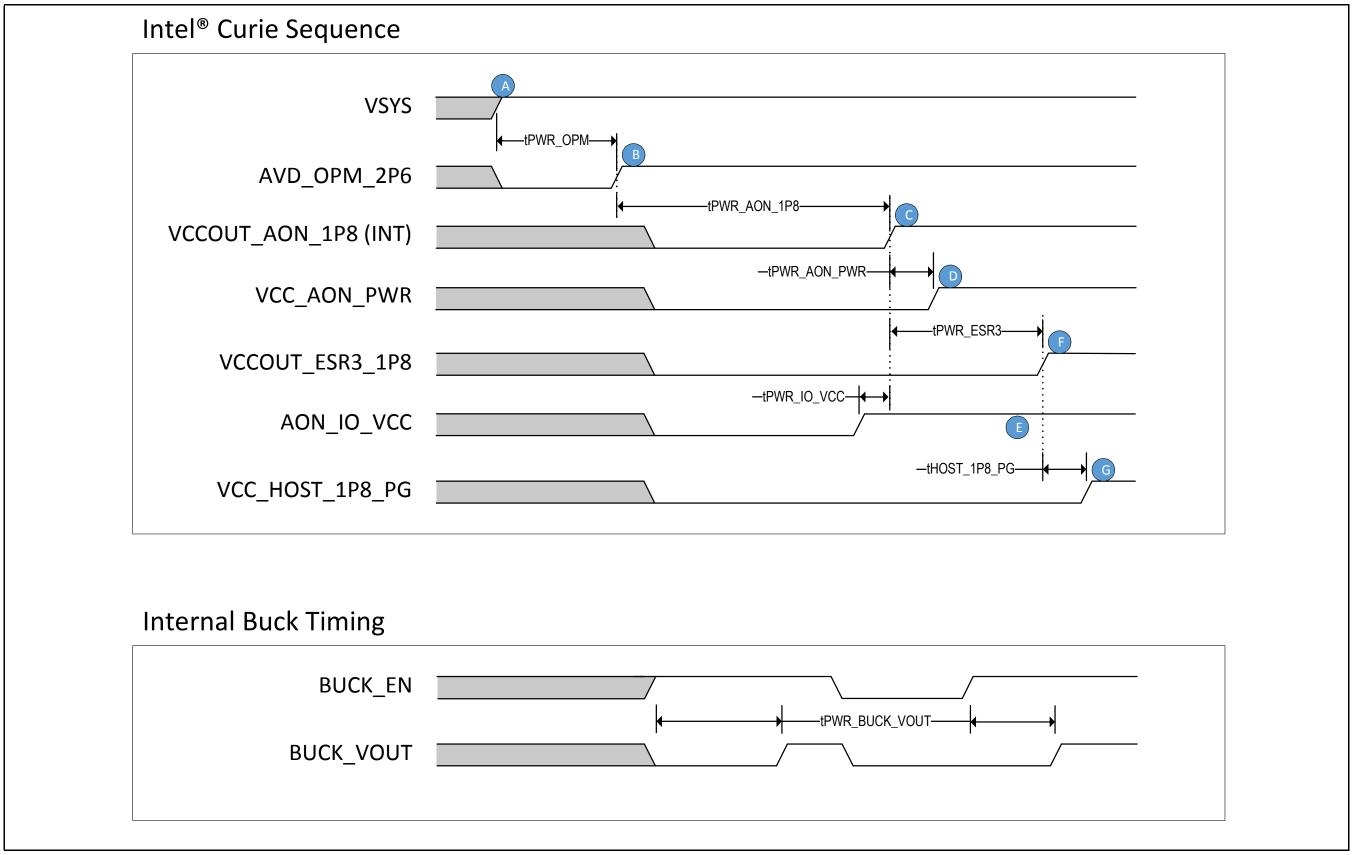


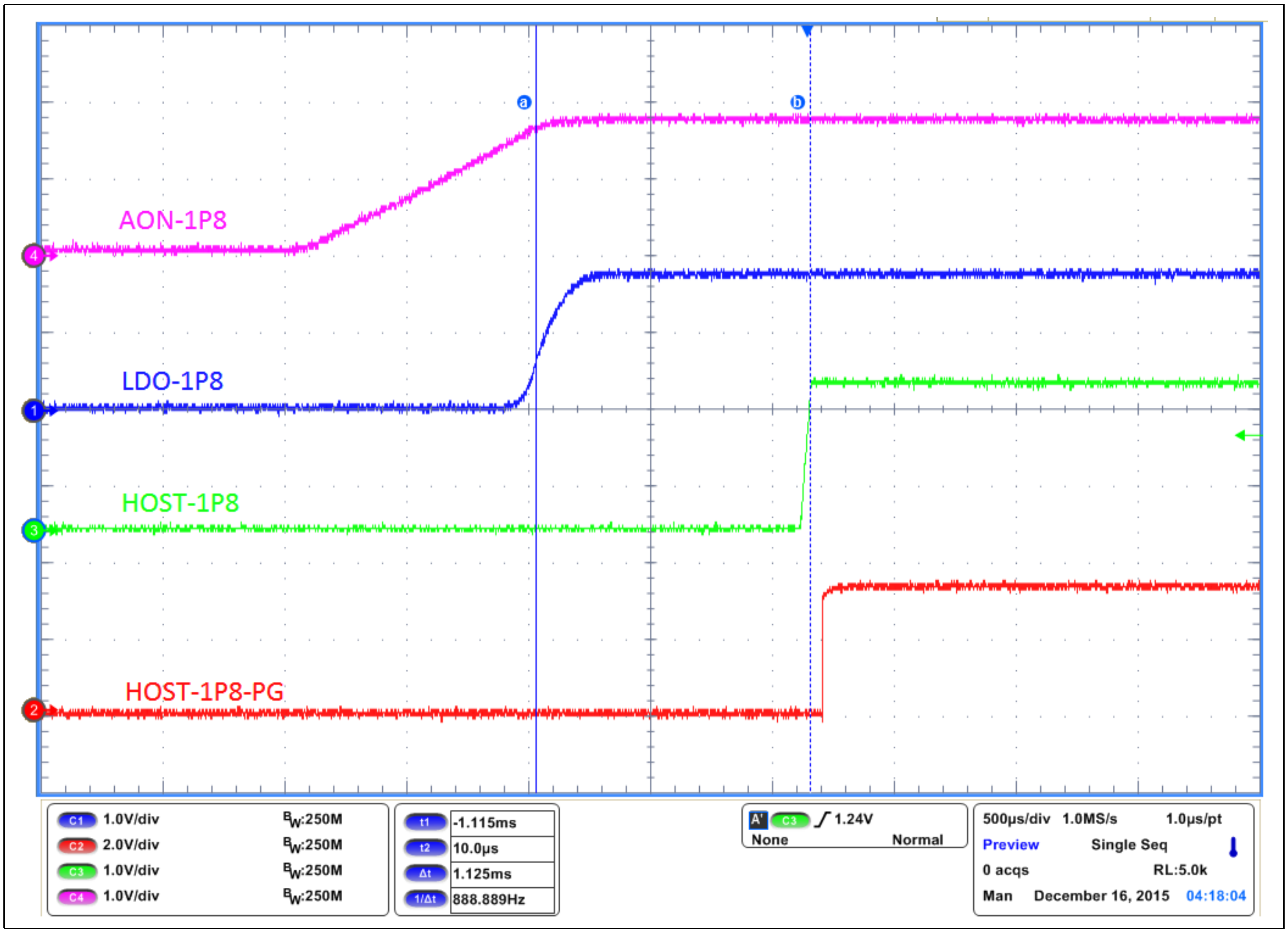
Table 4 **Buck parameters**

Parameter	Min	Typ	Max	Units
tPWR_OPM		20		µs
tPWR_AON_1P8		6		ms
tPWR_AON_PWR		200		µs
tPWR_ESR3		1.125		ms
tPWR_IO_VCC	0			ms
tHOST_1P8_PG		100		µs
tPWR_BUCK_VOUT		10	25	ms

3.5.1 AON_1P8, LDO_1P8, HOST_1P8 and HOST_1P8-PG

Following diagram shows the timing measured between VCCOUT_AON_1P8, VCC_AON_PWR, VCC_HOST_1P8 and VCC_HOST_1P8_PG.

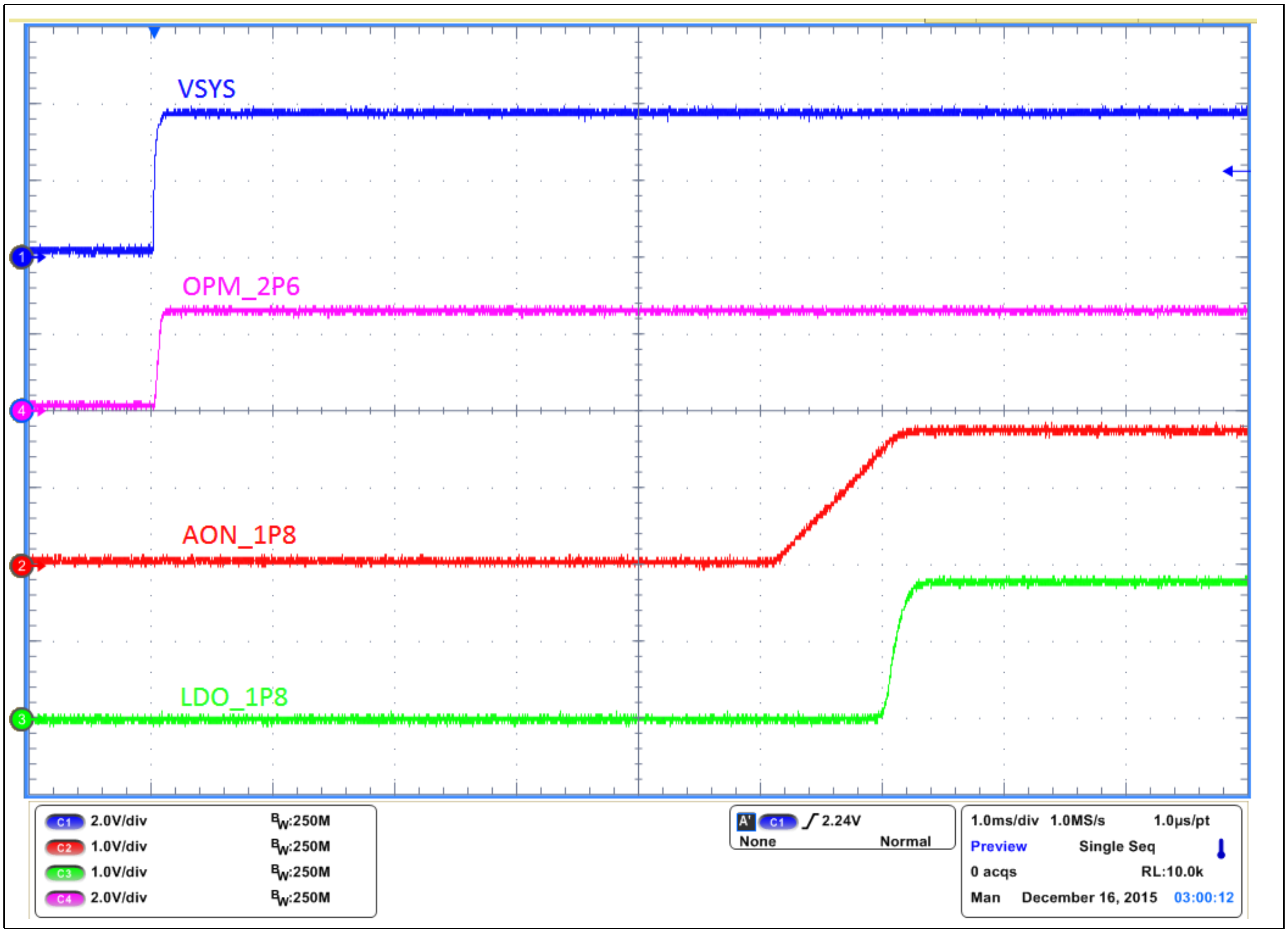
Figure 13 **AON_1P8, LDO_1P8, HOST_1P8 and HOST_1P8-PG - Oscilloscope capture**



3.5.2 VSYS, OPM_2P6, AON_1P8 and LDO_1P8

Following diagram shows the timing measured between VIN, AVD_OPM_2P6, VCCOUT_AON_1P8 and VCC_AON_PWR.AON_1P8, ESR1 and ESR2

Figure 14 **AON_1P8, ESR1 and ESR2 - Oscilloscope capture**



4 Platform Subsystems

4.1 Analog power and input routing

4.1.1 ADC ground

Inputs to the Intel® Curie™ module Analog to Digital Converter (ADC) are multiplexed with the IO pins of the Intel® Curie™ module and a separate analog GND plane is highly recommended for return path of analog signals. Follow best practices, which include these analog guidelines:

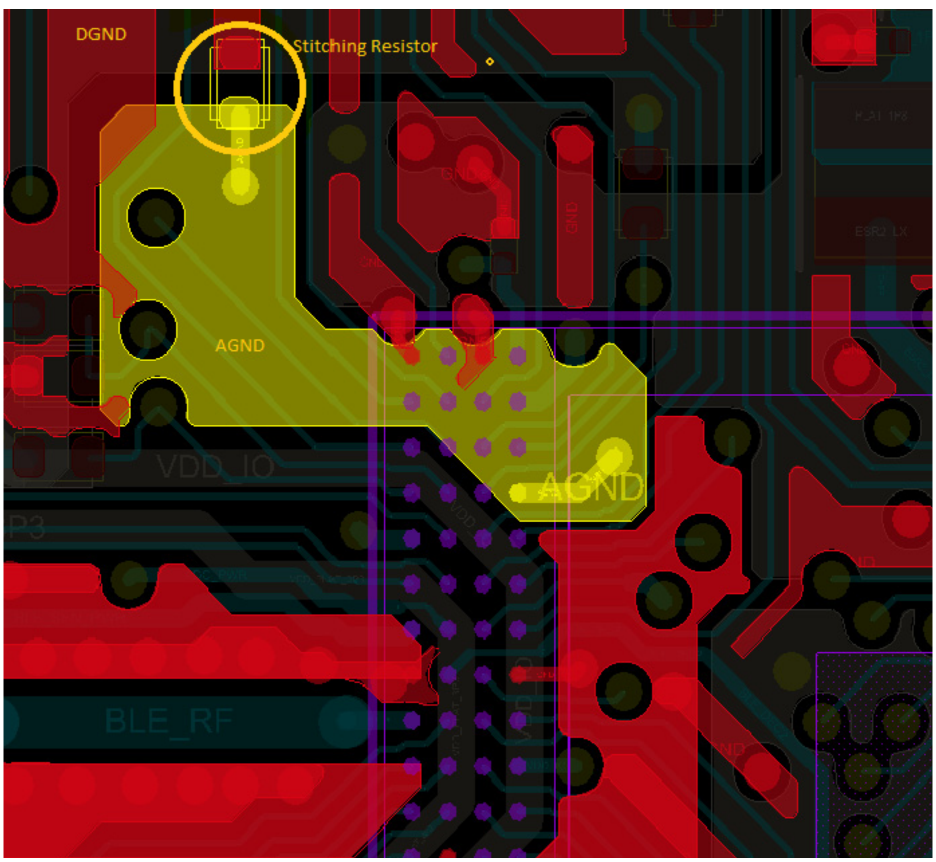
- Provide dedicated GND planes for analog ground, connected to digital ground at a single point.
- Analog signals and analog GND should be kept away from:
  - high speed digital signals
  - switching mode power supplies
  - crystals and oscillators
  - other design specific components which can generate noise across traces or through planes

4.1.1.1 ADC Power

ADC_3P3_VCC is the ADC block power input pin. Use 0.1uF decoupling capacitor. Use a clean power supply for good performance. Keep the power supply traces away from high frequency signals, DC-DC converters and, RF.

This image shows a large analog ground around the Intel® Curie™ module ADC input pins and bridge to digital ground.

Figure 15 **Example ADC ground**



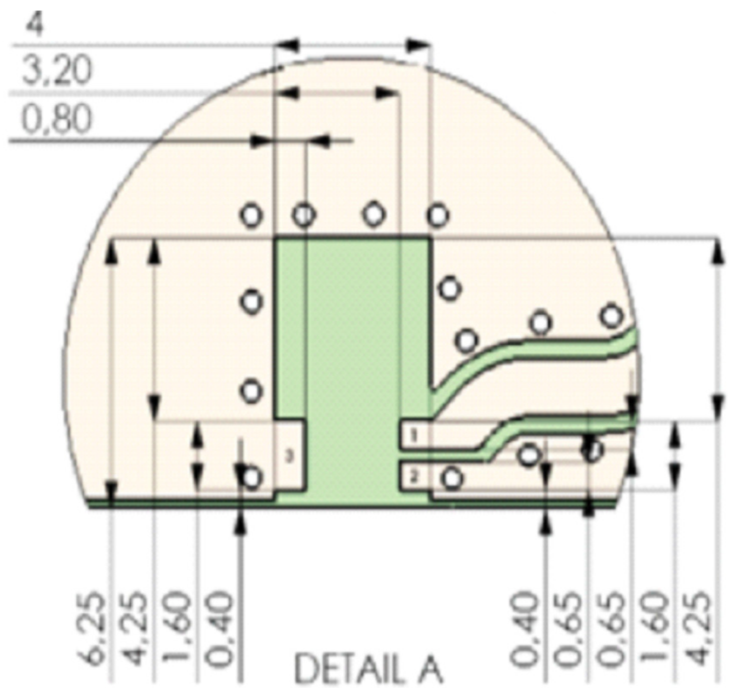
4.2 Bluetooth® low energy device and antenna

4.2.1 Antenna placement

The functional reference circuits utilizes a Pulse W3008C ceramic chip antenna that can excite a host circuit board to radiate at 2.4-2.48 GHz frequencies in an omni-directional pattern. Reference to the manufacturer datasheet for more details.

This solution requires a ground clearance of 4.00 mm x 6.25 mm under the SMT antenna with all metalization removed from all circuit board layers under the antenna. EMI shields and rings can limit antenna performance, place battery away from antenna. Example of matching network is shown on Figure 16

Figure 16 **Pad dimensions for chip antenna**



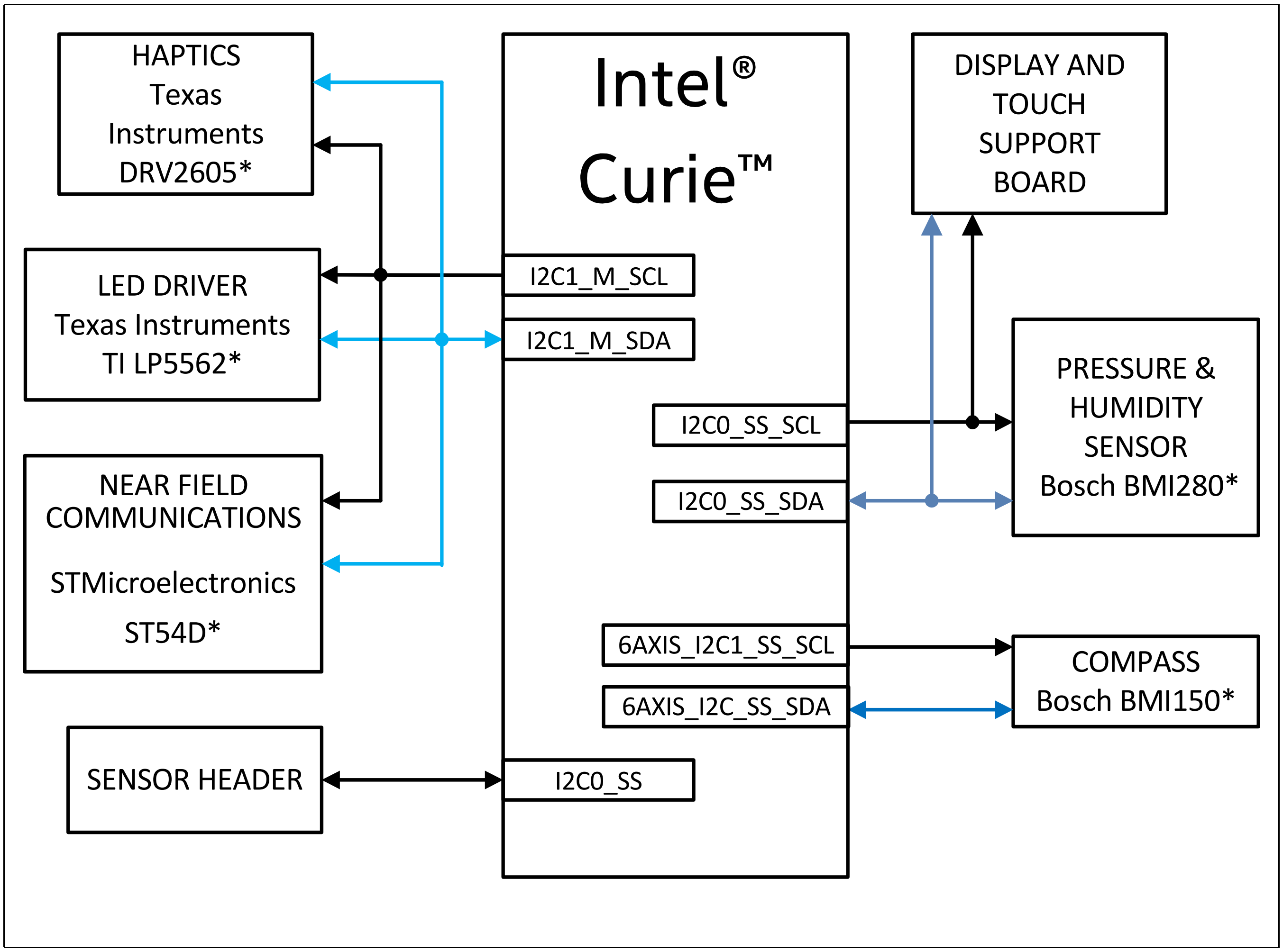
4.3 I^2C interface design guidelines

There are four I^2C ports for Intel® Curie™. Two ports are for generic use and two are dedicated ports for sensor subsystem. These operate in both master and slave mode. Both 7-bit and 10-bit addressing modes are supported and support standard (100 kbps), fast mode(400 kbps) and fast mode plus (1 Mbps).

4.3.1 I^2C connections on the functional reference circuits

The following diagram shows an example I^2C interface for a Intel® Curie™ module-based platform; maximum speeds are listed in Table 5

Figure 17 **Example of I^2C connection for a typical device**



4.3.2 I^2C interface signals

Table 5 **I2C interface signals**

Name	Type	Max Frequency / Data Rate	Description
I2C[0:1]_SCL I2C[0:1]_SDA	I/O	1 MHz	Main I2C[0:1] clock and data
I2C_SS[0:1]_CLK I2C_SS[0:1]_DATA	I/O	400 KHz	Sensor Subsystem I2C clock and data

4.4 LED driver example

The diagram below shows the I²C interface connections communicating with an external LED driver module.

The functional reference circuits includes a Texas Instruments LP5562 LED Driver connected through I2C1_M (address 0) to provide the features to Intel® Curie™ module-based devices:

- Four independently programmable LED outputs with 8-bit current setting (from 0mA to 25.5mA with 100uA steps)
- Flexible PWM control for LED outputs
- SRAM program memory for lighting pattern
- Three program execution engines with flexible instruction set
- Maximum current draw from Intel® Curie™ module to be less than 25mA

Figure 18 **LED driver block diagram for a tricolor module**

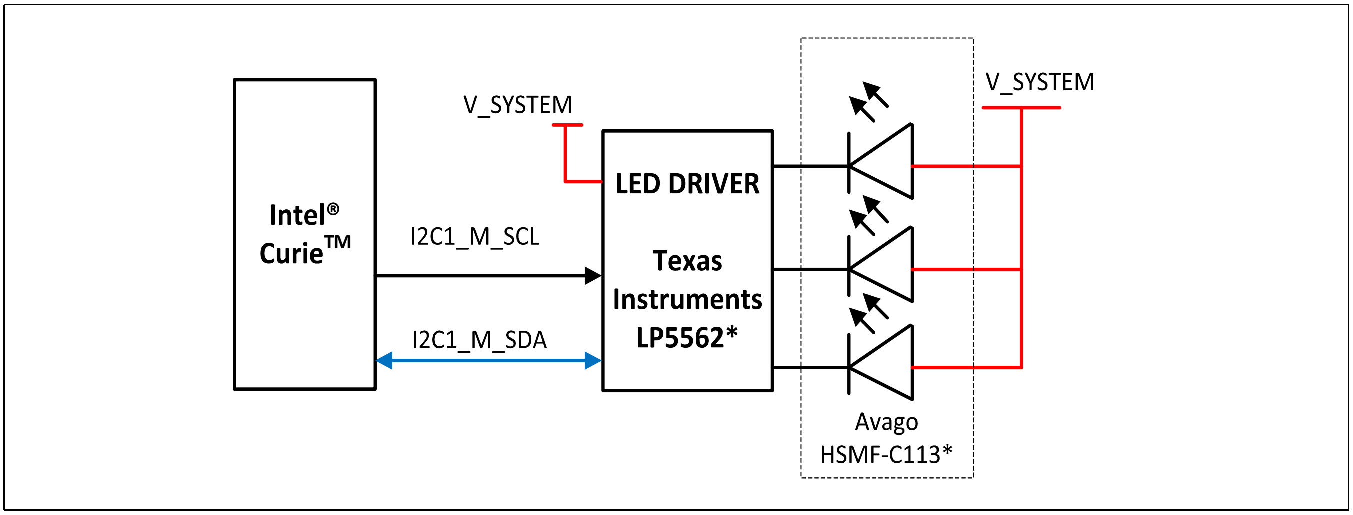
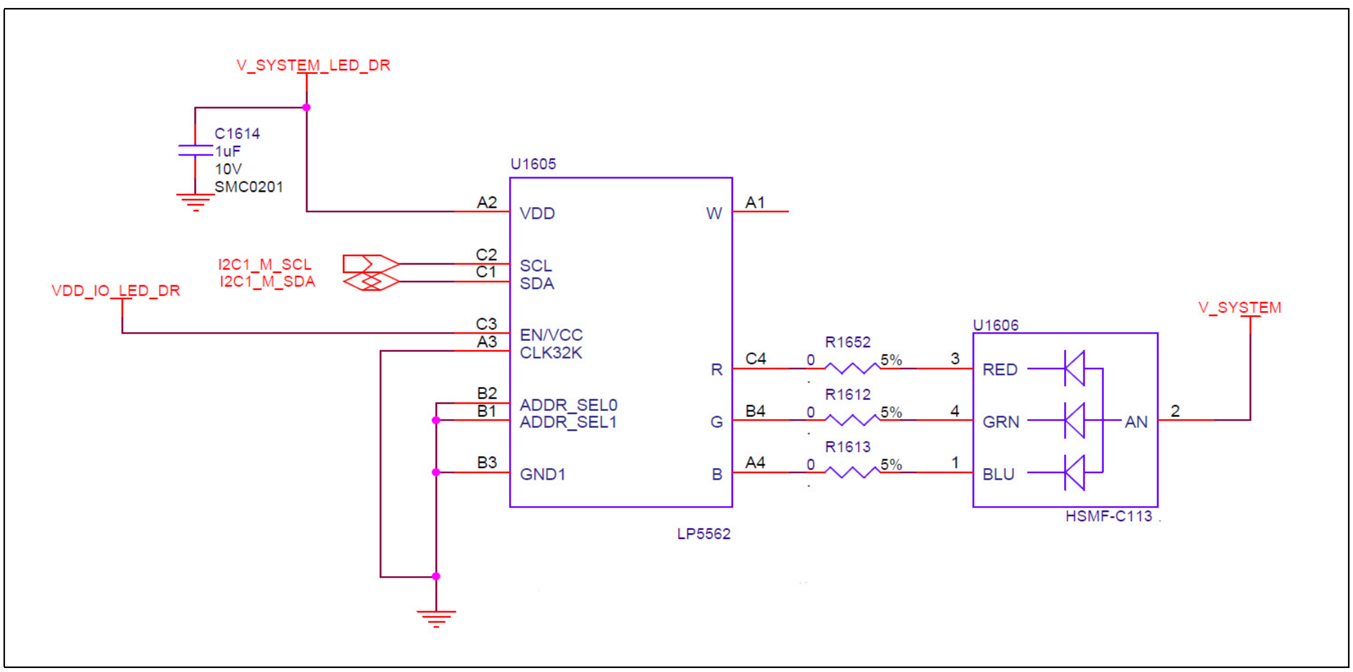


Figure 19 **LED driver example circuit for a tricolor module**



4.5 I2S interface design guidelines

The following I2S interface signals are not implemented on the functional reference circuits; these ports are connected to J1200 connector and can be used externally if needed, and are to be left unconnected if not used.

4.5.1 Signals for the I2S interface

Table 6 **I2S interface signals**

Name	Type	Maximum Audio Sample Rate	Description
I2S_RSCK I2S_TSCK	I/O	48 KHz	Clock signal for I2S
I2S_RXD I2S_RWS	I	48 KHz	RX Data for I2S
I2S_TXD I2S_TWS	O	48 KHz	TX Data for I2S

4.5.2 I2S interface routing guidelines

Table 7 **I2S platform routing guidelines**

I2S Interface	Max Drive Strength
I2S_RSCK	4mA (1.8V IO), 7.6mA (3.3V IO)
I2S_TSCK	8mA (1.8V IO), 7.6mA (3.3V IO)
I2S_RXD	4mA (1.8V IO), 7.6mA (3.3V IO)
I2S_RWS	4mA (1.8V IO), 7.6mA (3.3V IO)
I2S_TXD	8mA (1.8V IO), 7.6mA (3.3V IO)
I2S_TWS	8mA (1.8V IO), 7.6mA (3.3V IO)

4.6 Sensors

Intel® Curie™ has an integrated 6-axis sensor module interfaced with the Intel® Quark™ SE processor by exclusive use of SPI1_SS. This device makes available the 6-AXIS_AUX_I2C port for connection to an external environmental sensor.

Powering sensors with an Awake-ON rail will allow them to generate interrupt based wake events to the processor.

4.6.1 Integrated 6-axis sensor interfaces

The I2C master interface from the six axis sensor can be connected to an external digital compass.

Table 8 **Interface signals**

Name	Type	Maximum Frequency / Data Rate	Description
6Axis_SCL 6Axis_SDA	I/O	1 MHz	Clock and Data
6Axis_int2	I/O	400Hz	GPIO

Note: The 6-axis sensor is powered in common with the Bluetooth® low energy device.

4.6.2 Environmental inputs

4.6.2.1 Pressure and Humidity sensor

The concept shows the usage of Bosch* BME280 pressure/humidity/temperature sensor connected with Intel® Curie™ module over I2C0_SS, which support up to 400 kHz. Consult the manufacturer's datasheet for the latest details on specific features, including:

- I2C digital interface
- Operating pressure range of 300-1100hPa and relative humidity of 0 to 100%.
- Up to 16 over-sampling rate

4.6.2.2 Magnetometer (Geo Compass)

The concept shows the usage of Bosch* BME150 3-axis magnetometer connection through the Bosch BMI160 6-axis I2C for synchronized operation with the accelerometer and gyroscope. Consult the manufacturer's datasheet for the latest details on specific features, including:

- I2C digital interface
- On-chip interrupt controller
- Magnet field resolution of ~ 0.3uT

.

Figure 20 **Extended environmental sensor block diagram**

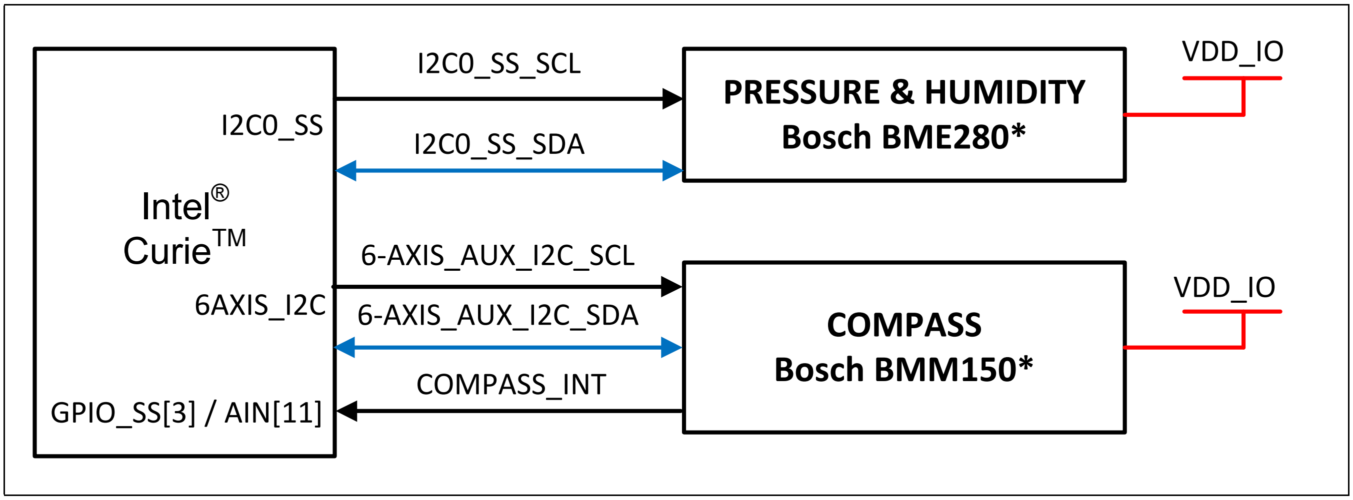
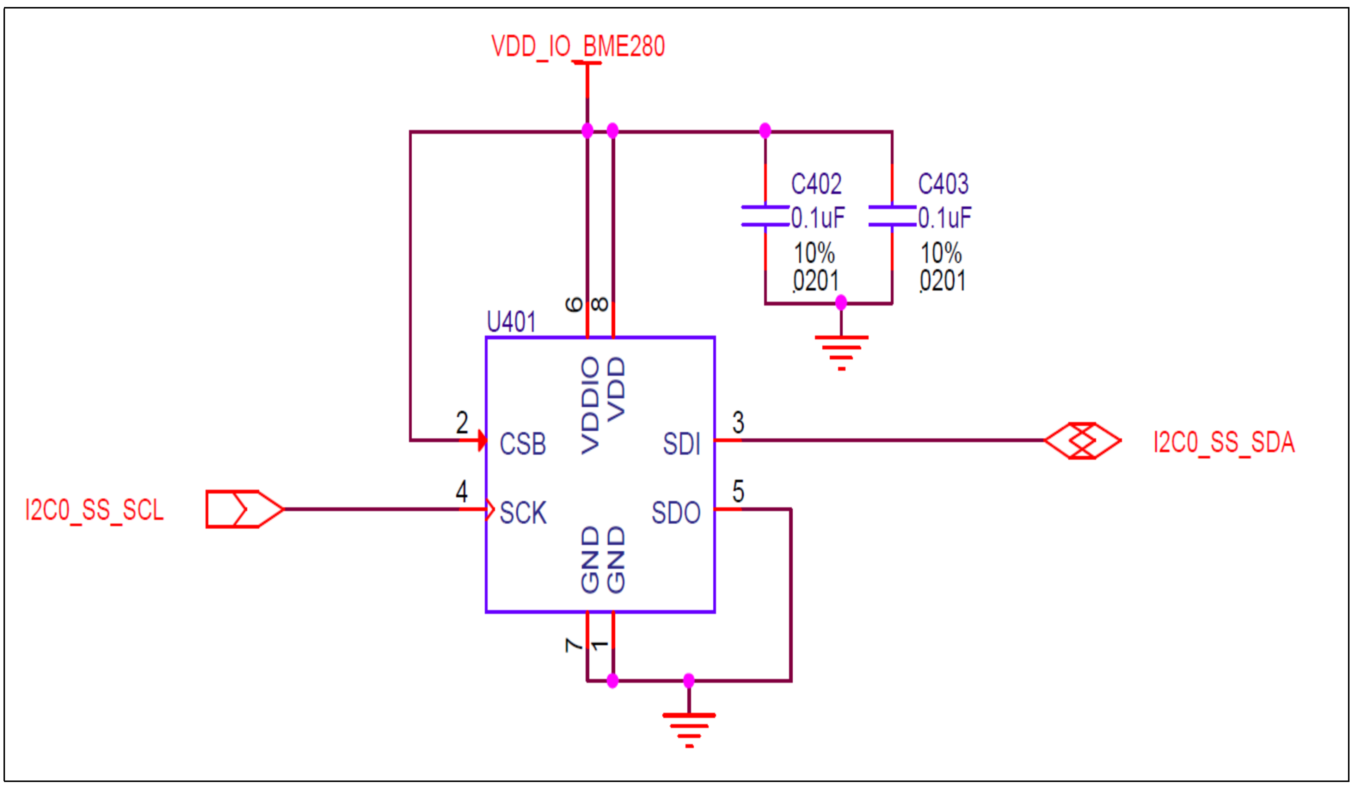


Figure 21 **External environmental sensor example circuit**



4.7 Haptics

4.7.1 Device driver

The concept shows the connection to a Texas Instrument* DRV2605 haptic driver using I2C1_M.

Consult the manufacturer's datasheet for the latest details on specific features, including:

- I2C digital interface
- On-chip interrupt controller
- Magnet field resolution of ~ 0.3uT

4.7.2 Reference Eccentric Rotating Mass (ERM) device

The functional reference circuits is configured with an ERM unit from Precision Microdrives (304-103)*.

Consult the manufacturer's datasheet for the latest details on specific features, including:

- Rated operating voltage of 2.7V
- Rated vibration speed of 14000rpm [+/-3000]
- Maximum rated operating current of 75mA

Figure 22 **Haptic driver block diagram**

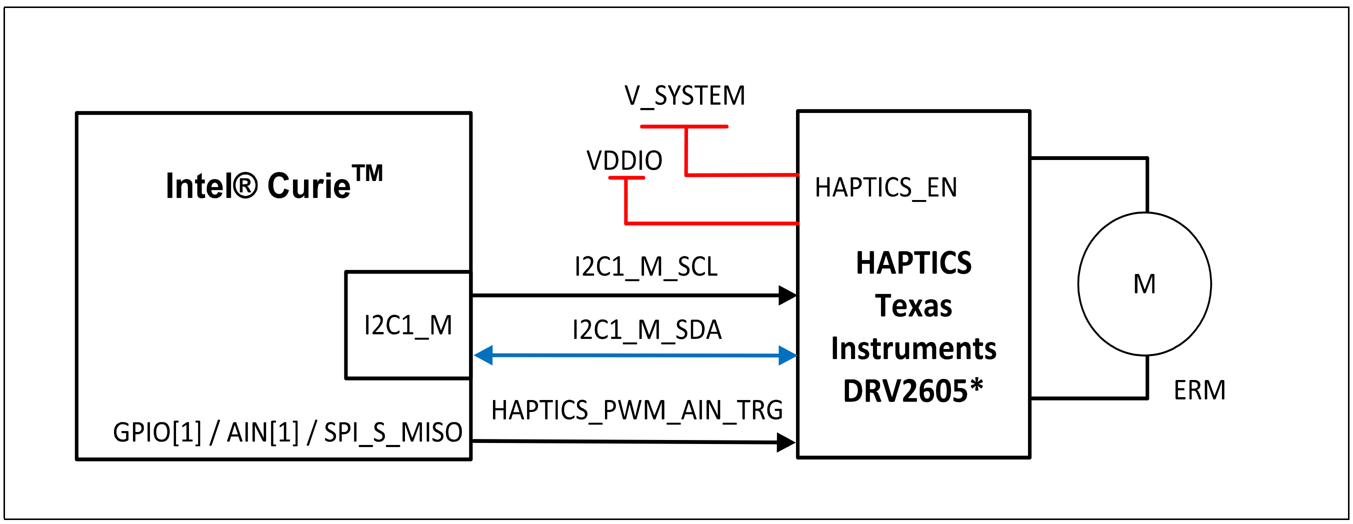
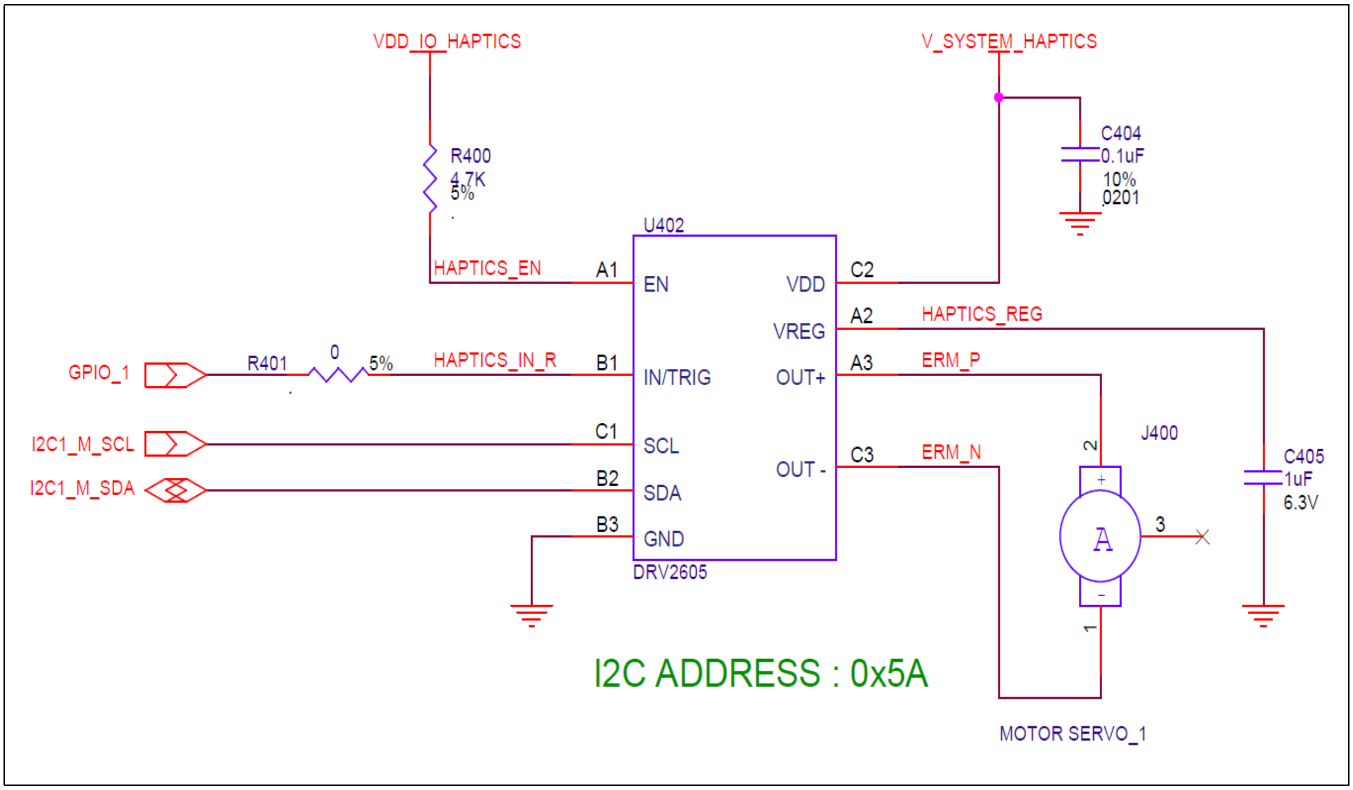


Figure 23 **Haptic driver - example circuit**

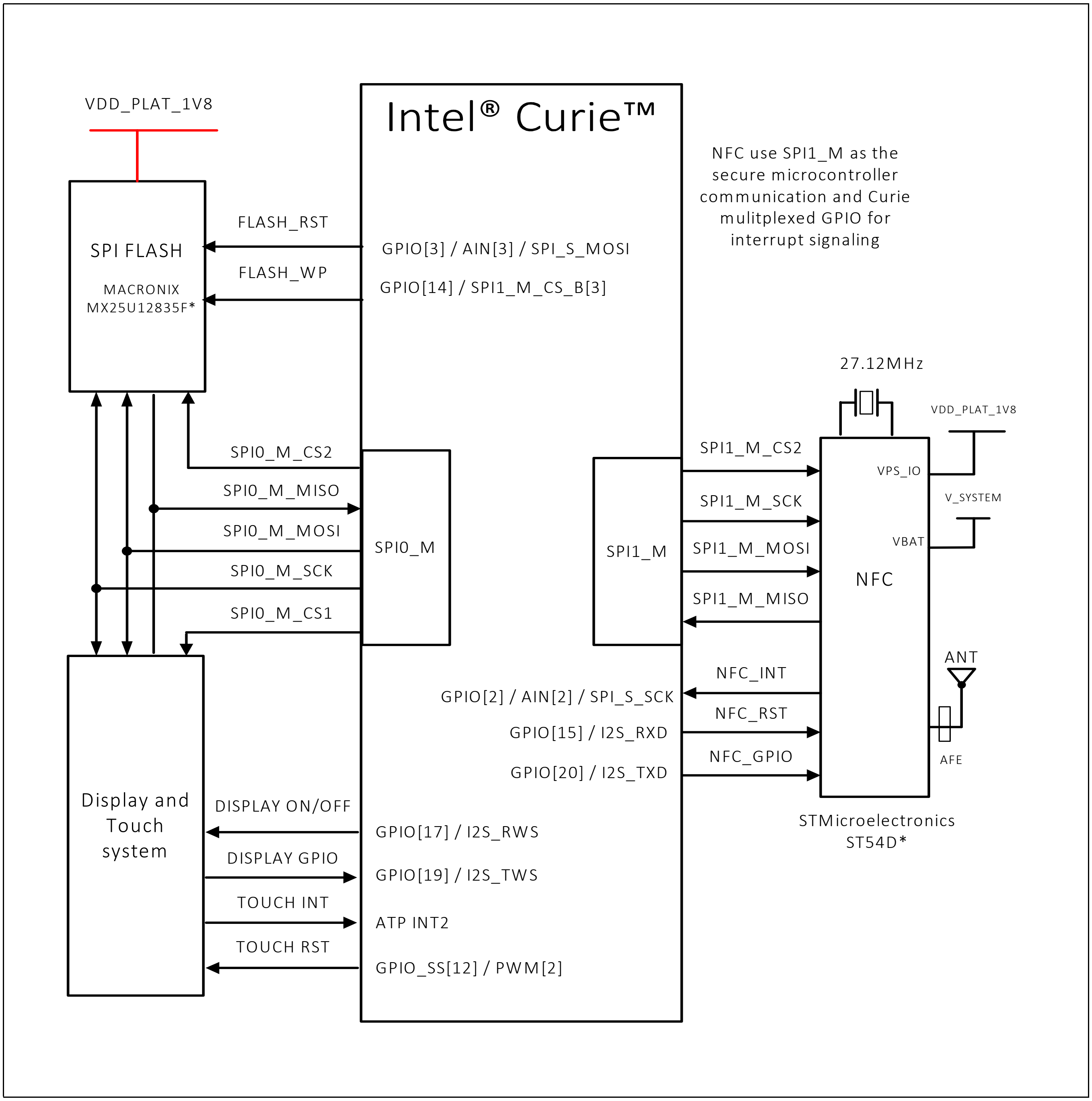


4.8 SPI interface

Intel® Curie™ module has four SPI interfaces, three are available externally and only two are used on the functional reference circuits.

Figure 24 shows a simplified block diagram of typical SPI connections for flash memory, display/touch and NFC solutions

Figure 24 **SPI simplified topology example**



4.8.1 SPI interface signals on the Intel® Curie™ module

Examples of SPI signals used in this concept design are outlined below.

Table 9 **Intel® Curie™ SPI interface signals**

Name	Input / Output	Maximum Frequency / Data Rate	Description
SPI0_M_SCK	Output	16 MHz	SPI Serial Clock
SPI0_M_CS[2:0]_N	Output	8 MHz	SPI Chip Select.
SPI0_M_MISO	Input	8 Mbps	SPI Slave Output Master Input
SPI0_M_MOSI	Output	8 Mbps	SPI Master Output Slave Input
SPI1_M_SCK	Output	16 MHz	SPI Serial Clock
SPI1_M_CS[3:0]_N	Output	8 MHz	SPI Chip Select.
SPI1_M_MISO	Input	8 Mbps	SPI Slave Output Master Input
SPI1_M_MOSI	Output	8 Mbps	SPI Master Output Slave Input

4.9 Flash memory

The functional reference circuits use a Macronix MX25U12835F* serial flash memory for additional storage.

A maximum of 128Mb can be connected with the Intel® Curie™ module SPI0_M interfaces.

Figure 25 **SPI simplified topology example**

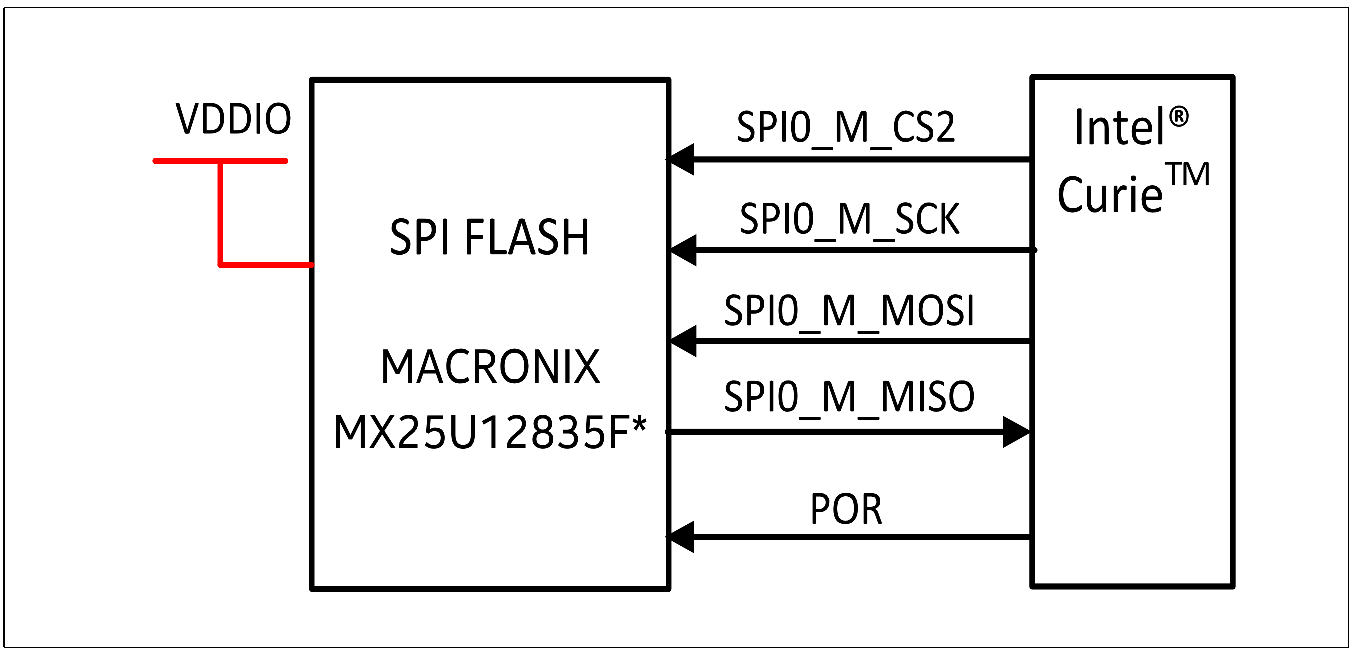
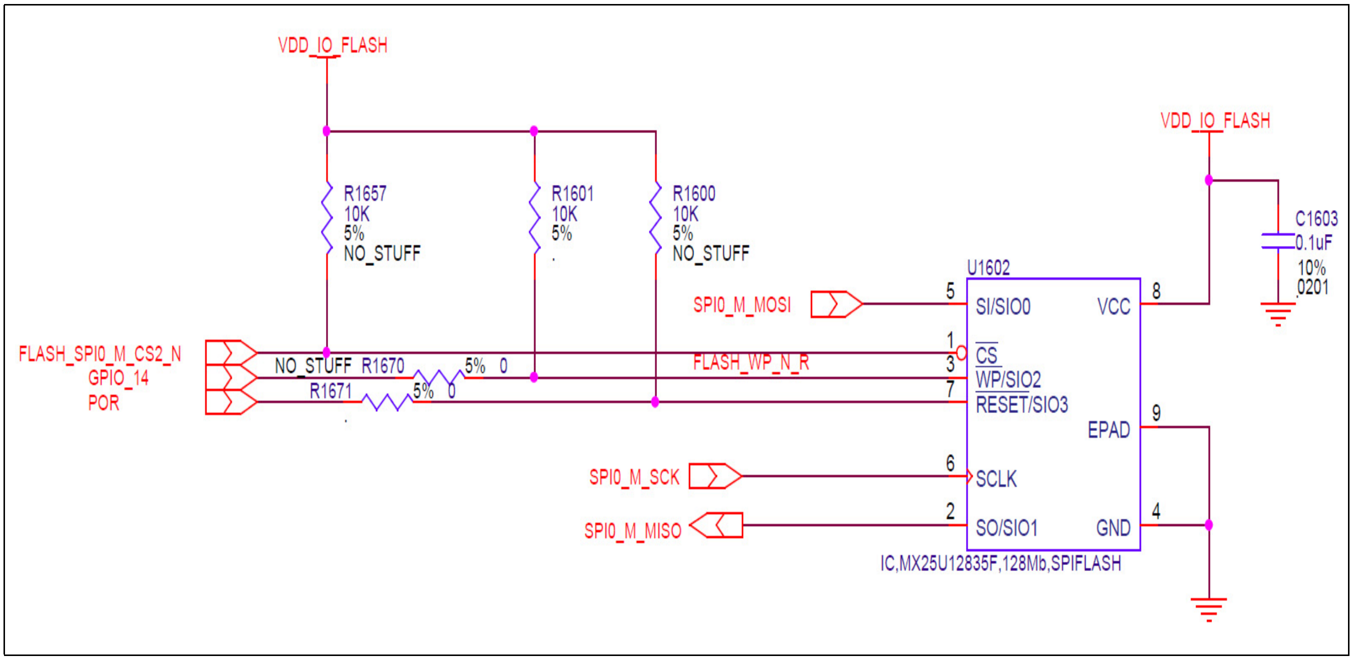


Figure 26 **Flash memory circuit for SPI interface**



4.10 Display panel and touch controller

An example showing Sharp S010B7DH02* display panel and a Cypres (I2C) CY8CTST241* capacitive touch screen controller are shown for reference.

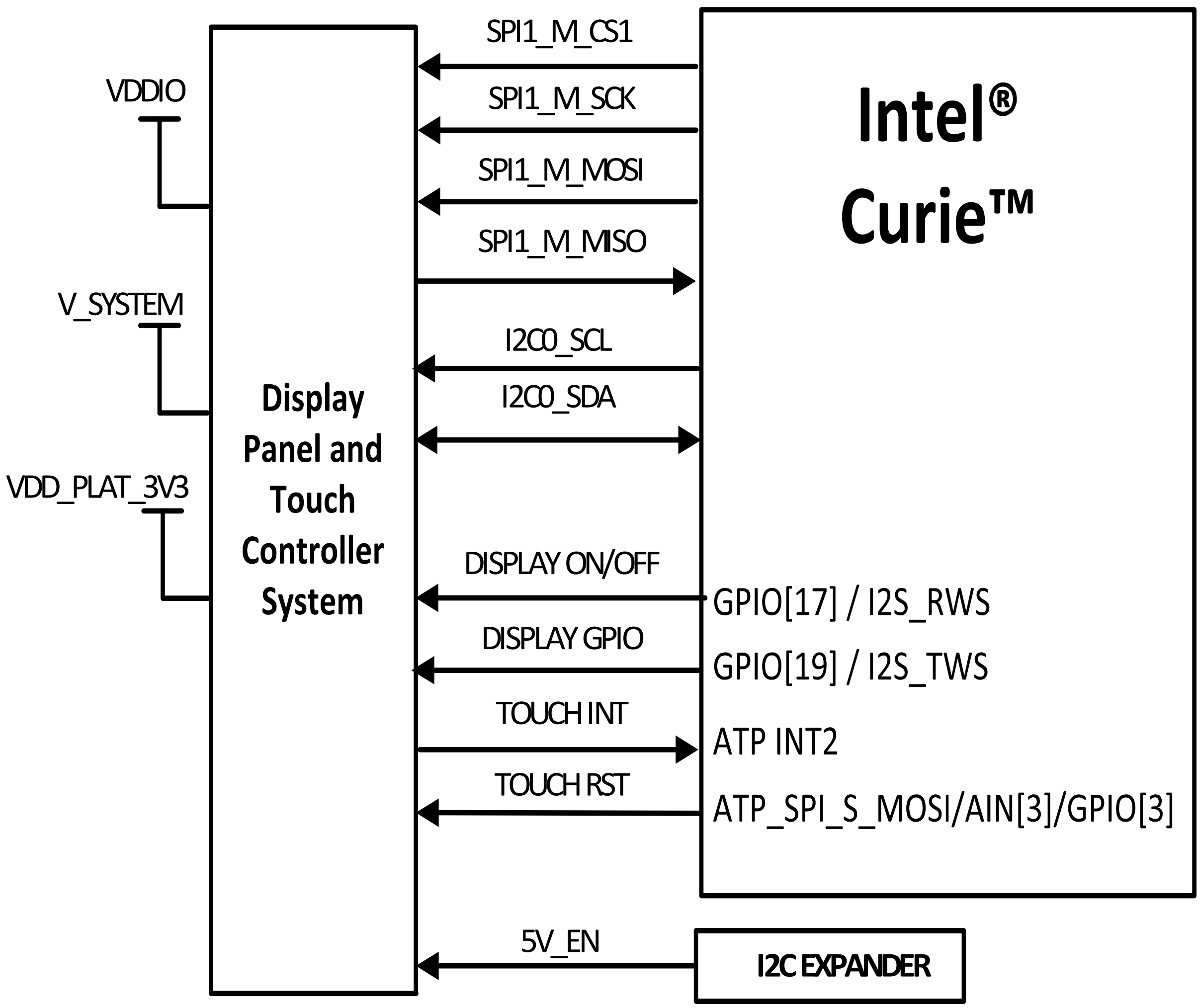
Consult the Sharp LS010B7DH02 datasheet for additional information on these features:

- Transflective panel of white and black
- Digital SPI interface
- 1.02 inch screen with 96 x 150 resolution
- 1 bit internal memory for data storage within the panel

Consult the Cypress* CY8CTST241 datasheet for additional information on these features:

- Up to 32 sense pin
- Large object detection
- Resistant to LCD noise
- Wide supply voltage range from 1.71V to 5.5V
- Integrated voltage regulator

Figure 27 **External display topology example**



4.11 Near Field Communication (NFC)

This example is designed around a ST Microelectronics ST54D* NFC controller with in-built secure element.

The NFC controller is connected to Intel® Curie™ module on I2C1-M (NFC Router communication) and SPI1_M (for secure micro-controller communication) interface. The NFC support card emulation mode is supported and a dedicated interrupt pin is connected to Intel® Curie™ module GPIO.

4.11.1 NFC controller features

- Integrated AFE
- Optimized power consumption modes
- I2C slave interface up to 1Mbps
- Integrated 36Kb EEPROM
- Support up to three external secure element

4.11.2 Secur microcontroller features

- ARM SecurCore SC300* 32-bit RISC core
- 1280 Kbytes of flash memory available
- Single wire protocol (SWP) interface for communications with NFC router in SIM/NFC application
- SPI slave interface for non-SIM application

Figure 28 **NFC connections**

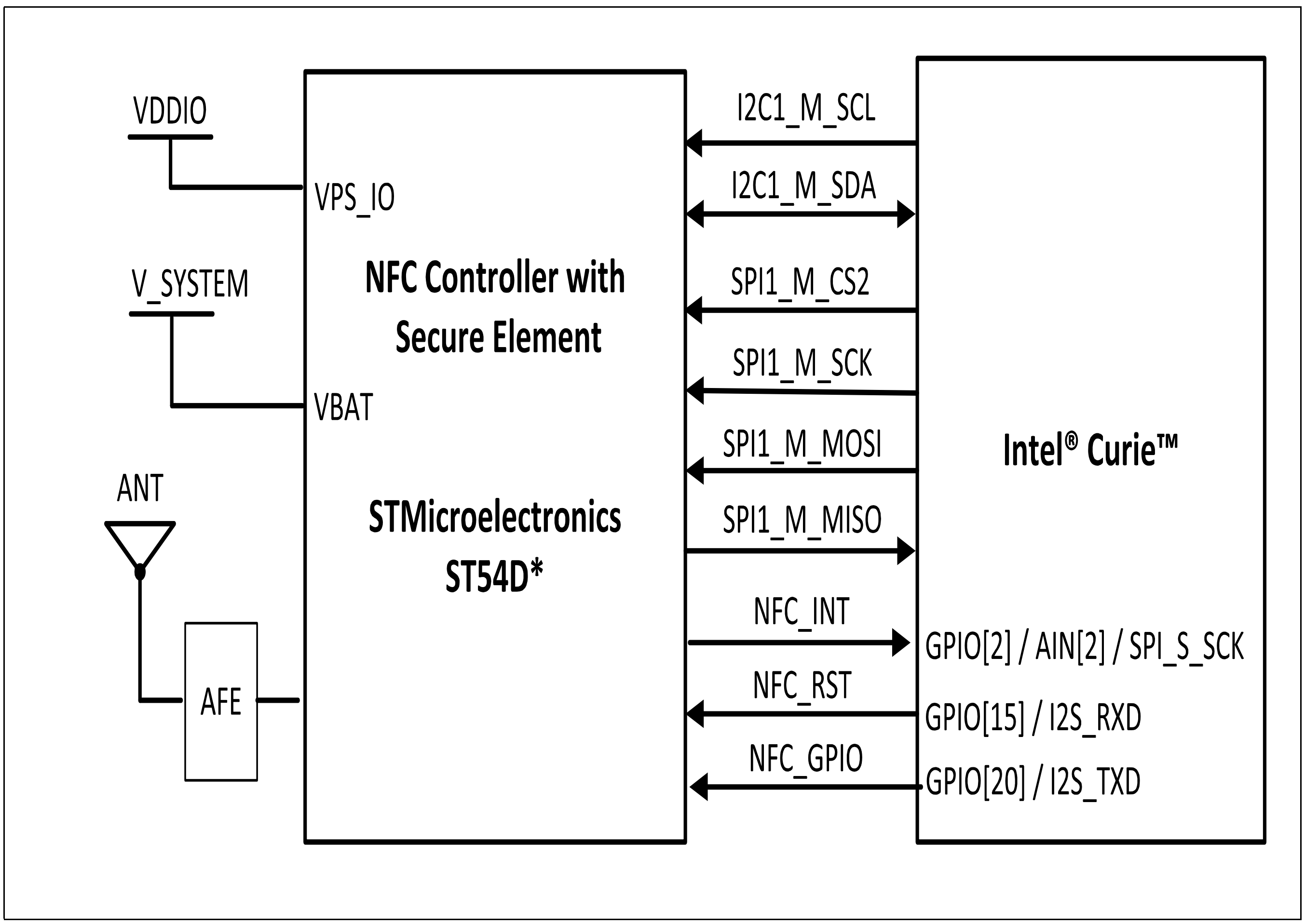
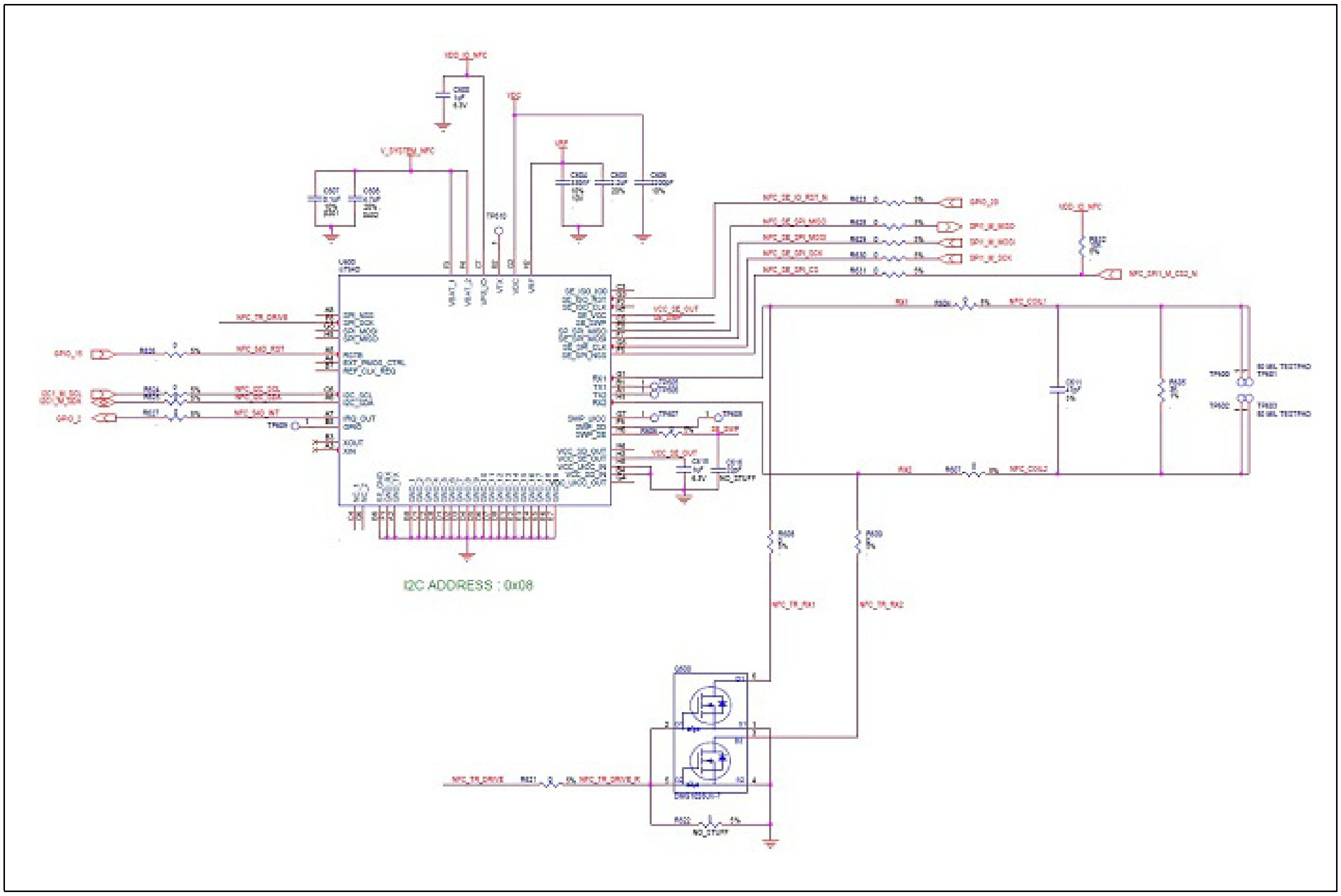


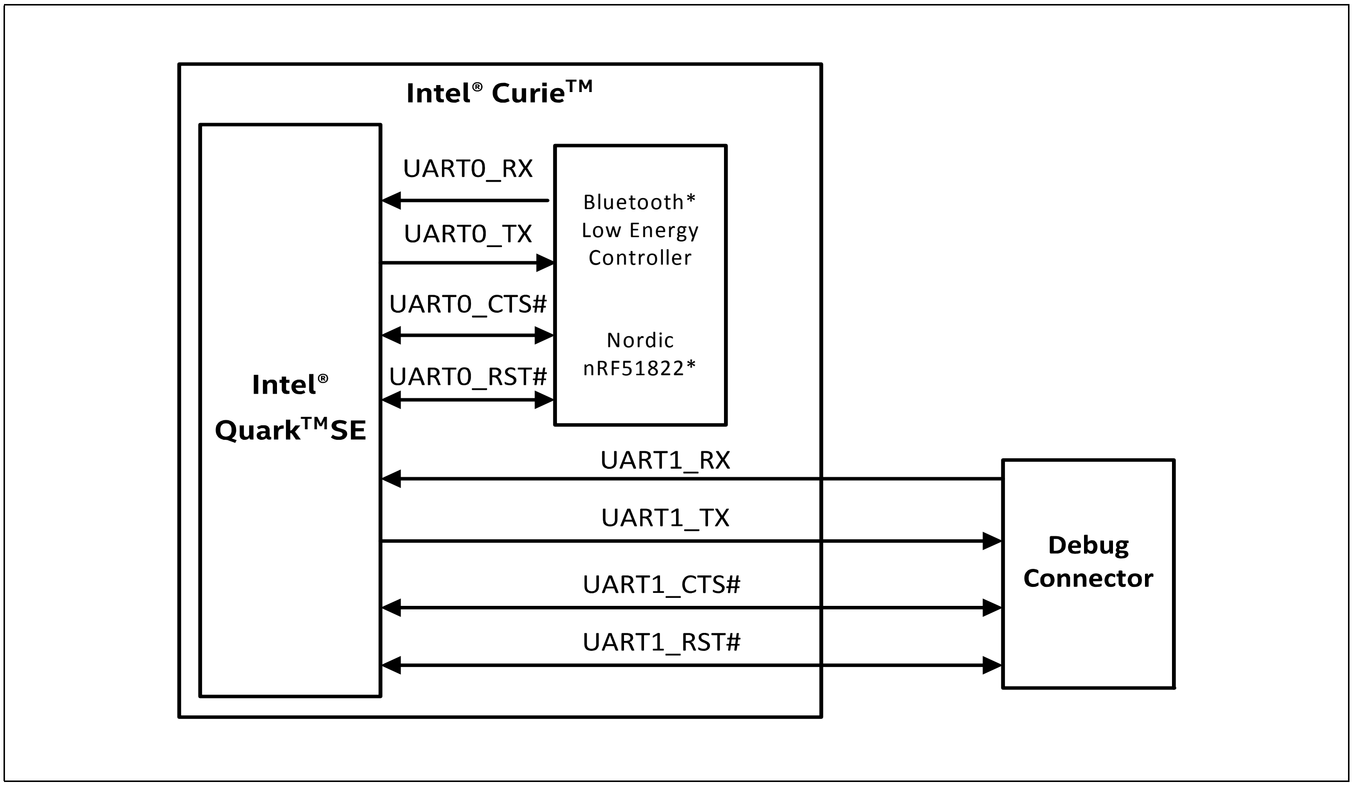
Figure 29 **NFC - example circuit**



4.12 UART0 for Bluetooth® low energy

Intel® Curie™ contains two instances of a UART controllers within the module, UART0 is dedicated to the integrated Nordic nRF51822* Bluetooth Low Energy controller while UART1 is available for use with mobile data systems and debug tools.

Figure 30 **UART interface topology**



4.13 UART1 interface signals

Table 10 shows the UART1 interface signals available to the platform design.

Table 10 **UART interface signals**

Name	Type	Max Data Rate	Description
UART1_RX	I	2 MHz	High-speed receive data input
UART1_TX	O	2 MHz	High-speed transmit data
UART1_RTS	I	2 MHz	High-speed request to send
UART1_CTS	O	2 MHz	High-speed clear to send

Note: UART signals not implemented on a platform can be left unconnected.

4.14 USB interface design considerations

Consult these general routing and placement guidelines when laying out a new design to minimize signal quality and EMI:

- Maximum trace length is 4 inches.
- Do not route traces under crystals, oscillators, clock synthesizers, magnetic devices, or ICs with strong clocks.
- Follow the 20 × h rule by keeping traces at least [20 × (height above the plane)] mils away from the edge of the plane (VCC or GND, depending on the plane the trace is over).

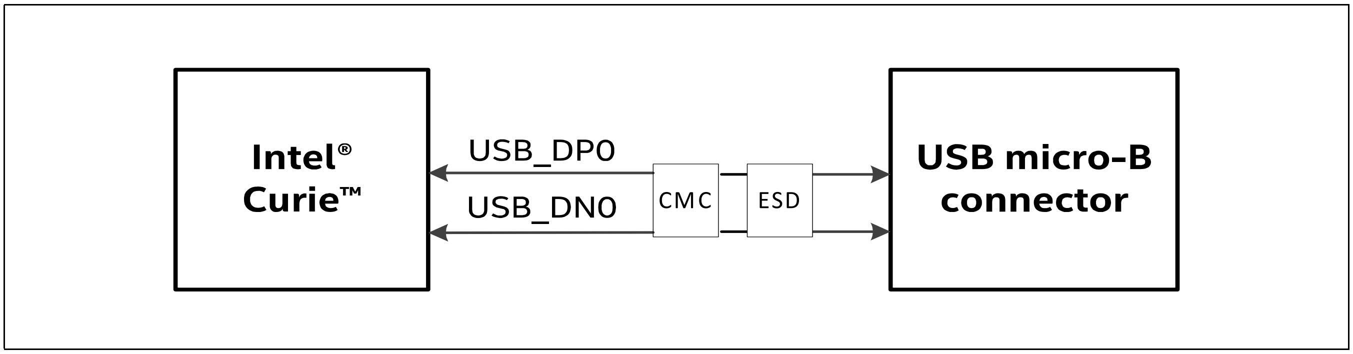
For an example stackup, the height above the plane is 4.5 mils (0.114 mm). This calculates to a 90-mil (2.286 mm) spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

- Avoid stubs on high-speed USB signals because stubs cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils (5.08 mm).
- We recommend placing a low ESR 1 µF ceramic cap close to the VDD_USB pin.
- If a USB port is not implemented on the platform, USB_DP/N[x] signals can be left unconnected.
- Protect USB lines are with ESD diodes for safe performance.
- A 1.07K bleeding resistor added in USB power line can provide an immediate discharge path for USB power.

Table 11 **USB 1.1 differential pair length matching table**

Signal Name	Type	Max Frequency / Data Rate	Description
USB_DP	Input / Output	12 Mbps	Universal serial bus port differential (USB Data+)
USB_DM	Input / Output	12 Mbps	Universal serial bus port differential (USB Data-)

Figure 31 **USB 1.1 port topology**



4.14.1 USB 1.1 length matching

Table 12 **USB 1.1 differential pair length matching table**

Signal	Total initra pair screw
USB_DP	150 mils
USB_DM	150 mils

5 Circuit Board Recommendations

5.1 Fundamental design rules

All of the routing guidelines (W/S, isolation, length requirement) are modeled around a 4-layer, Type II printed circuit board.

If different PCB stackup is implemented, the electrical guidelines (impedance, insertion loss) provided in this design guide must be followed to ensure that the layout meets the platform recommendations.

These rules pertain to all the subsystems discussed in this chapter.

- The length values are tested and measured as package-pin-to-package-pin.
- The break-out and break-in minimum spacing ratio is 1:1 for all interfaces.
- The trace width/intra-spacing for differential pairs and trace width for single-ended signals depend on the impedance.
- For analog signals, it is important to keep the analog ground return path clean from digital noise to maintain high signal-to-noise ratio.
- All inputs, tristate buses and signals that are not connected must be pulled up or down by the firmware or hardware to prevent oscillation. This is especially important for enable or control signals like JTAG TMS signal.
- Unused and reserved signals are terminated as no connection, unless specified otherwise.
- Power sources and input regulation components must remain stable across the entire operating range of voltage and device systems.

5.2 PCB thickness and stackup

Stackup refers to the thickness as comprised of the number of layers, the PCB technology (and via details), the thickness of each layer and the Cu weights on each layer. Fab drawings have a stackup or cross section figure.

The concept referenced in this document uses high density interconnect, Type 3, 4-layer board technology.

Trace width for Radio Frequency and high speed signal driver impedance must be determined per the stackup selected.

5.2.1 Two-layer boards

Intel® Curie™ module can be placed on a two-layer board for simple designs that have limited buses susceptible to interference noise, or when the footprint is not a primary constraint and signals can be physically separated to improve noise tolerance.

Table 13 **Two-layer stackup design**

Layer	Type	Material	Thickness (mm)	Dielectric Constant	Trace Width (mm)
	Surface	Air		1	
	Solder Mask	FR-4	0.02	4.2	
Top	Conductor	Copper	0.036	4.2	0.102
	Dielectric	FR-4	1.48	4.2	
Bottom	Conductor	Copper	0.036	4.2	0.102
	Solder Mask	FR-4	0.02	4.2	
	Surface	Air		1	

5.2.2 Four-layer stackup

Table 14 **Four-layer stackup design**

Layer	Type	Material	Thickness (mm)	Dielectric Constant	Trace Width (mm)
	Surface	Air		1	
	Solder Mask	FR-4	0.05	4.5	
Top	Conductor	Copper	0.015	1	0.13
	Dielectric	FR-4	0.068	4.5	

Table 14 **Four-layer stackup design**

Layer	Type	Material	Thickness (mm)	Dielectric Constant	Trace Width (mm)
	Surface	Air		1	
L2_GND1	Conductor	Copper	0.015	4.5	0.1
	Dielectric	FR-4	0.55	4.5	
L3_GND2	Conductor	Copper	0.015	4.5	0.1
	Dielectric	FR-4	0.068	4.5	
Bottom	Conductor	Copper	0.015	1	0.13
	Solder Mask	FR-4	0.053	4.5	
	Surface	Air		1	
Total Thickness: 1.6 mm					

5.2.3 Six-layer stackup

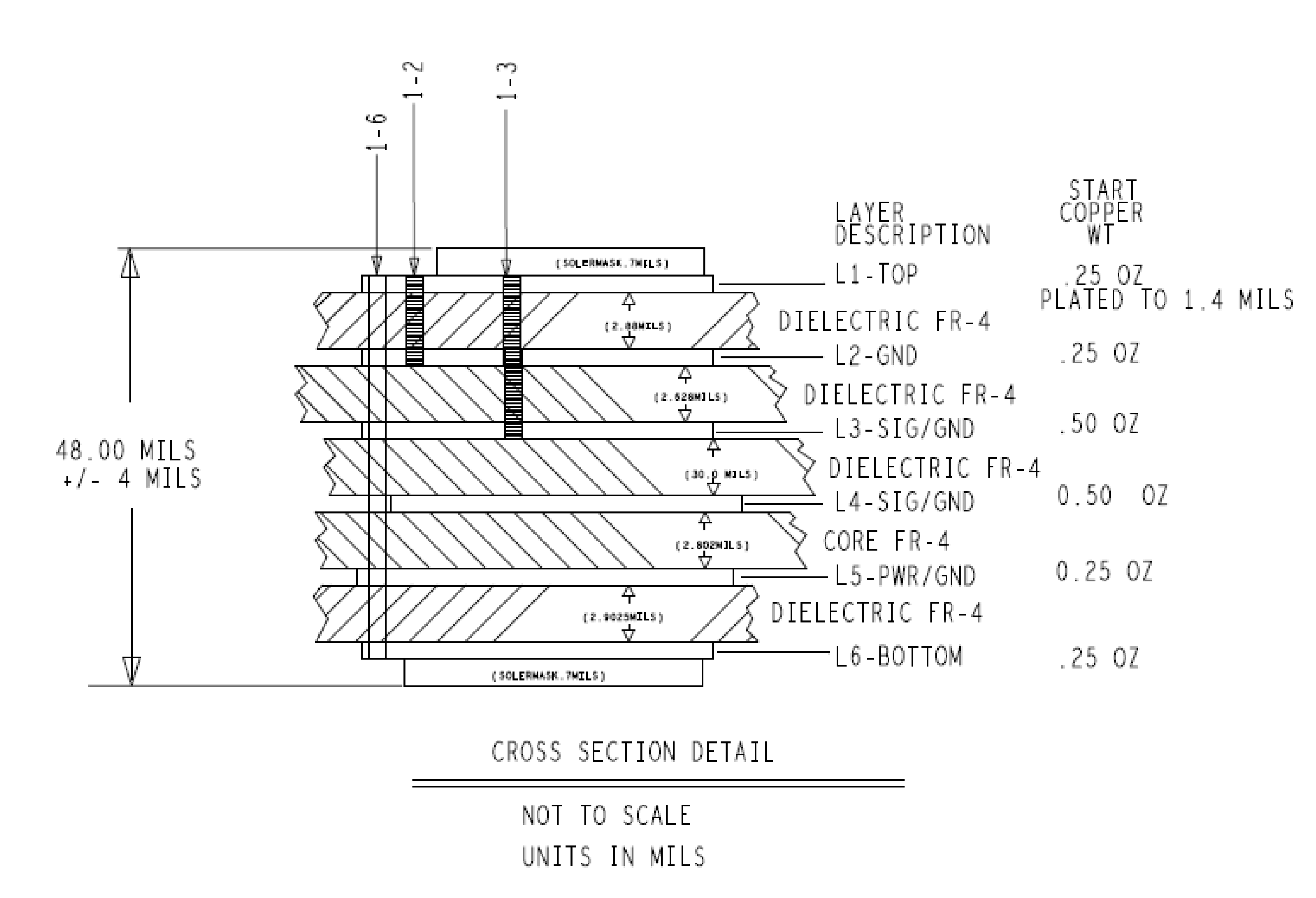
This next example is a 48mil thick, 6-layer, HDI type II board with blind vias from 1-2 and 1-3, with additional thruhole vias. This board contains 1.4 oz copper (Cu) on the outer layers and 0.25 – 0.50 oz copper on the inners layers, as detailed below.

Table 15 **Six-layer stackup design**

Layer	Type	Material	Thickness (mm)	Dielectric Constant	Trace Width (mm)
	Surface	Air		1	
	Solder Mask	FR-4	0.05	4.5	
Top	Conductor	Copper	0.015	1	0.13
	Dielectric	FR-4	0.068	4.5	
L2_GND1	Conductor	Copper	0.015	4.5	0.1
	Dielectric	FR-4	0.55	4.5	
L3_PWR1	Conductor	Copper	0.015	4.5	0.1
	Dielectric	FR-4	0.2	4.5	
L4_CLK1	Conductor	Copper	0.015	4.5	0.1
	Dielectric	FR-4	0.55	4.5	
L5_GND2	Conductor	Copper	0.015	4.5	0.1
	Dielectric	FR-4	0.068	4.5	
Bottom	Conductor	Copper	0.015	1	0.13
	Solder Mask	FR-4	0.053	4.5	
	Surface	Air		1	
Total Thickness: 1.6 mm					

5.2.3.1 Six-layer stack up cross section

Figure 32 **Thickness of a six layer stackup**



§

6 Debug and Production Options

6.1 JTAG connector or test pads

Traditional JTAG connections can be routed to test points or header pins as best suited for the need and design intent.

- JTAG_TDO
- JTAG_TDI
- JTAG_TCK
- JTAG_TMS
- JTAG_RST_B

Figure 33 **Block diagram of the debug ports on the Intel® Curie™ module**

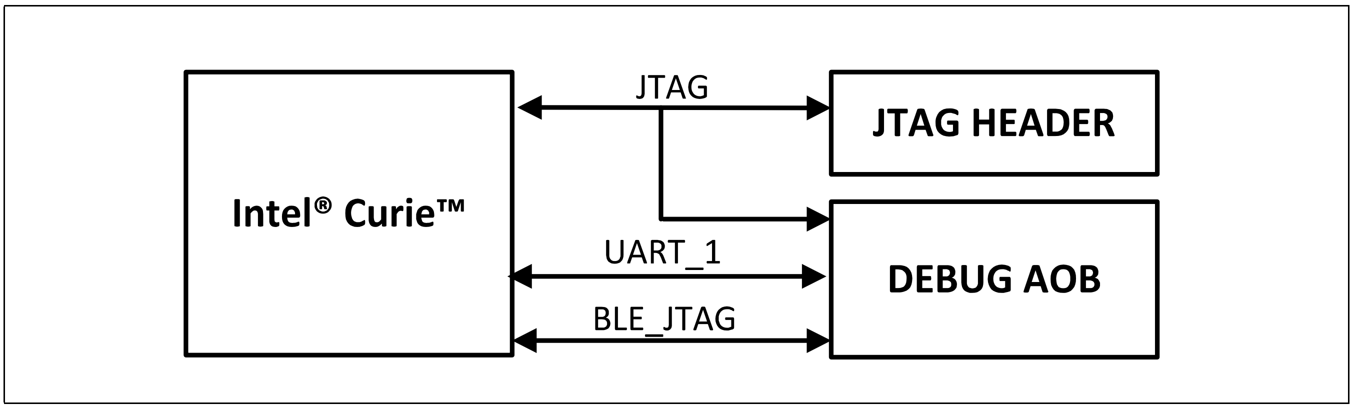
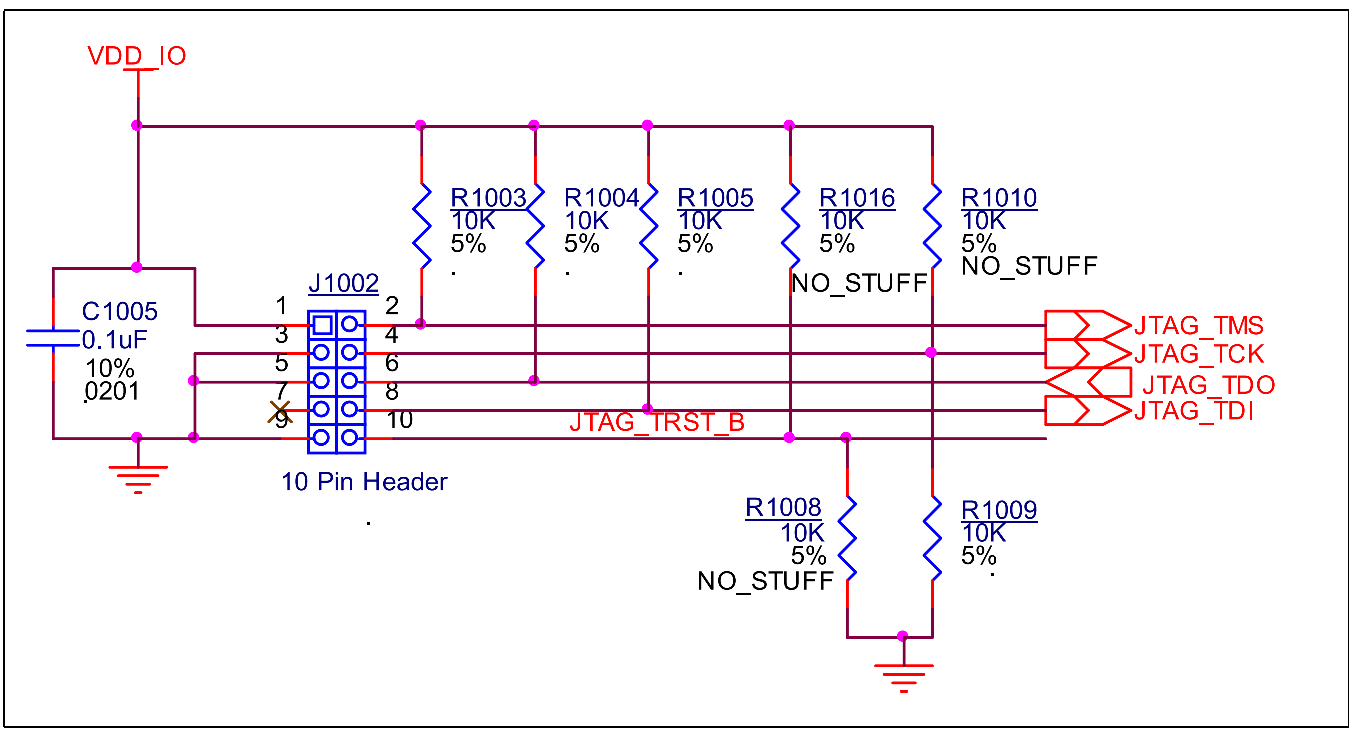


Figure 34 **Debug ports on the Intel® Curie™ module**



6.2 Power rail test pads

Test points for primary voltage rails, LDO outputs; and a clean ground are very helpful to debug and for device measurements.

6.3 UART test pads

Intel® Curie™ module, when in manufacturing mode, sends out messages on the UART right from power up. Thus access to the UART will provide additional access to system functions and information logs.

- AIO_05_UART_RX
- AIO_05_UART_TX

6.4 Bluetooth® low energy test pads

A Jlink emulator can be sued to program, or reprogram, the Bluetooth® low energy firmware. The board digital ground needs to be connected between the board and Jlink emulator. Also vref from Jlink emulator needs to connect to the same voltage level as the VDD_BLE_SEN, This allows the emulator to communicate to the Bluetooth® low energy with correct logic level.

- BLE_SWDIO
- BLE_SW_CLK

Note: Jlink software utility allow the users to program a BLE image in .bin or .hex format. Refer to Jlink users manual and Nordic* website for more information.