BJT

Bipolar Junction Transistor

Transistor → Transfers Resistance from i/p to o/p

Junction → (E.B + C.B)

J_E J_C

Bipolar → Bi + Polar

Bi → (2)

Polar → Polarities (or) Charges

Positive Charge & Negative Charge

Positive Charge → Holes

Negative Charge → electrons

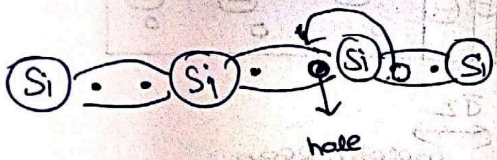
BJT : An electronic device which transfers current from i/p Resistance to O/P Resistance ~~from~~ i/p to o/p & produces current with the help of Both Positive & negative charged particle

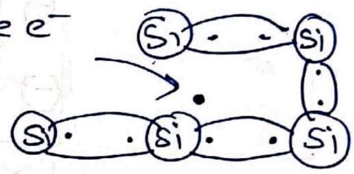
Construction of BJT :

- PnP
  - maj: holes
  - min: e⁻s
- nPn
  - e⁻s
  - holes

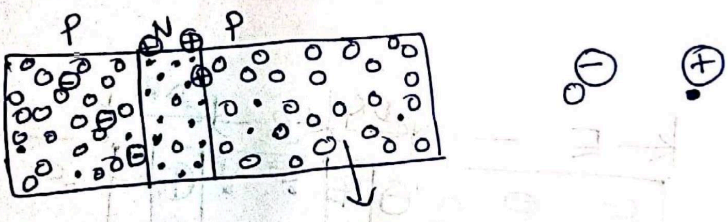
hole current → Boundede⁻

e⁻s current → free e⁻





PNP Transister :



Intrinsic "si" layer.
"Ge"

① Diffusion

② CVD

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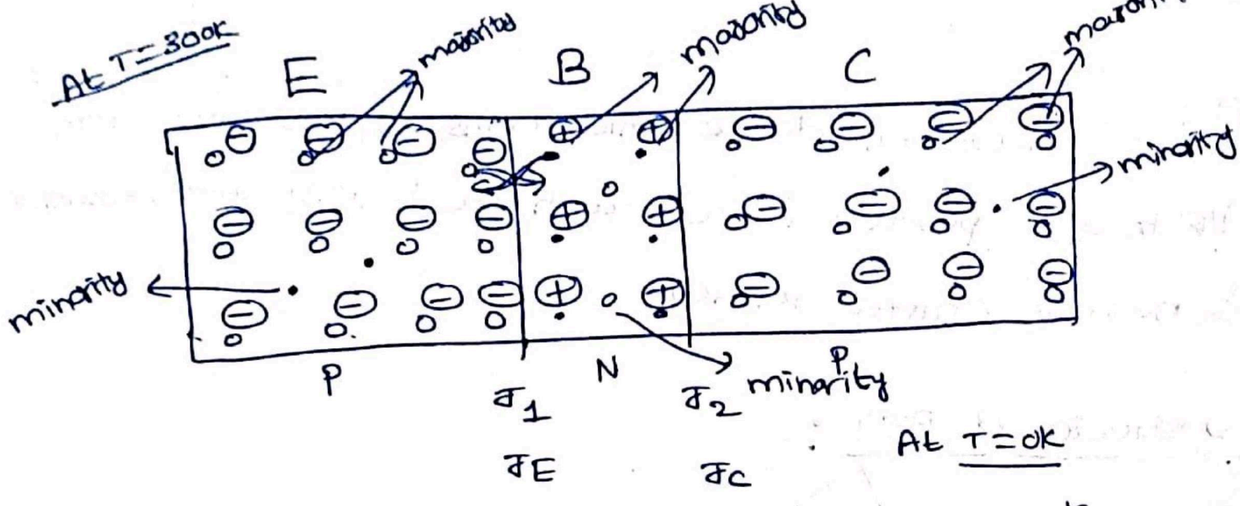
At T=300K



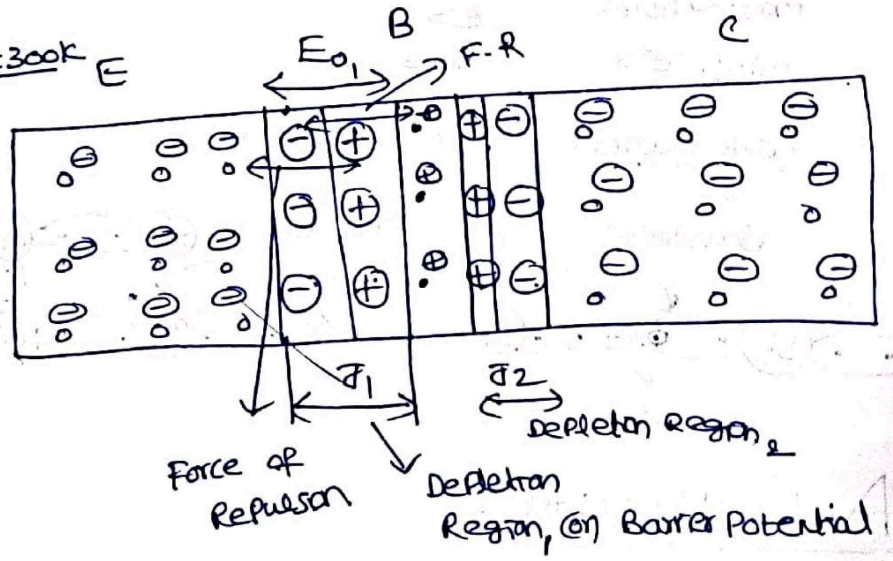
At T=0K

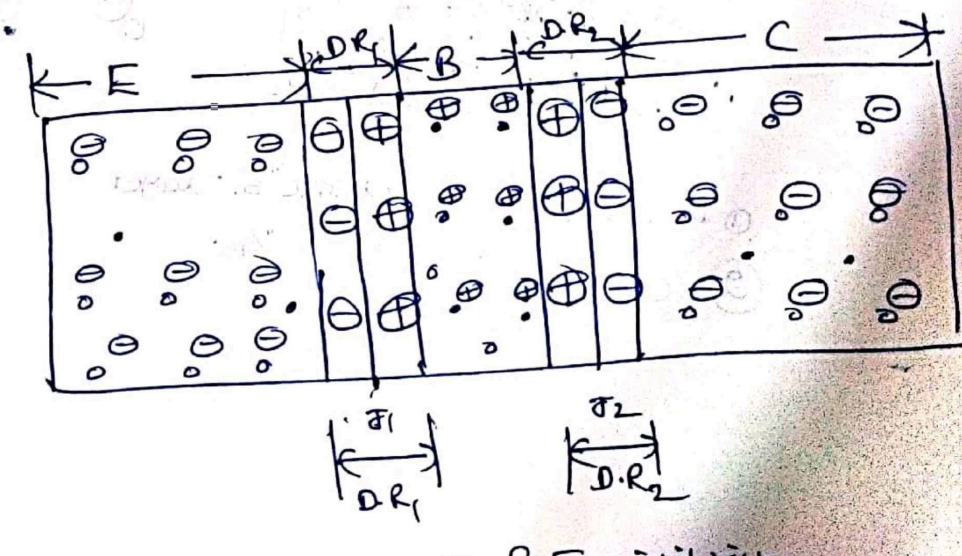
At T=300K

KT

Triode ⟶ E, B, C

At T=300K





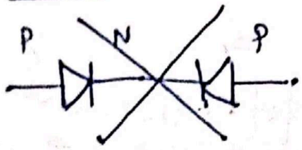
At T=300K & Equilibrium

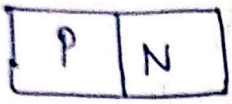
Schematic Diagram (or) symbol of BJT :

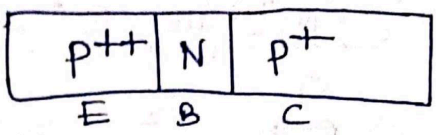
P-N Diode

Barrier

BJT

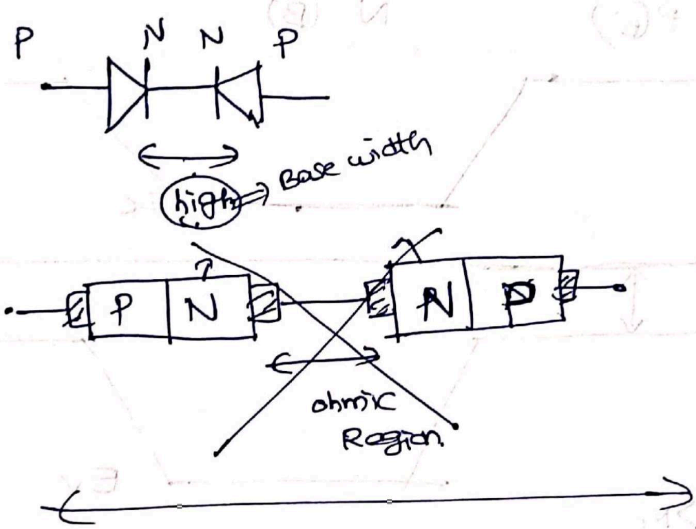


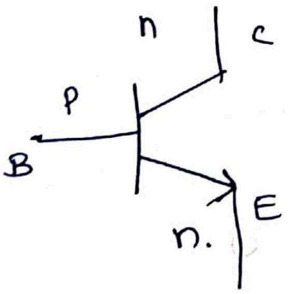




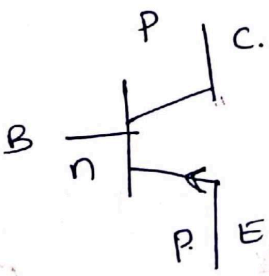
Will back to back connection of two PN diodes can form a BJT ??

NO





npn



pnp

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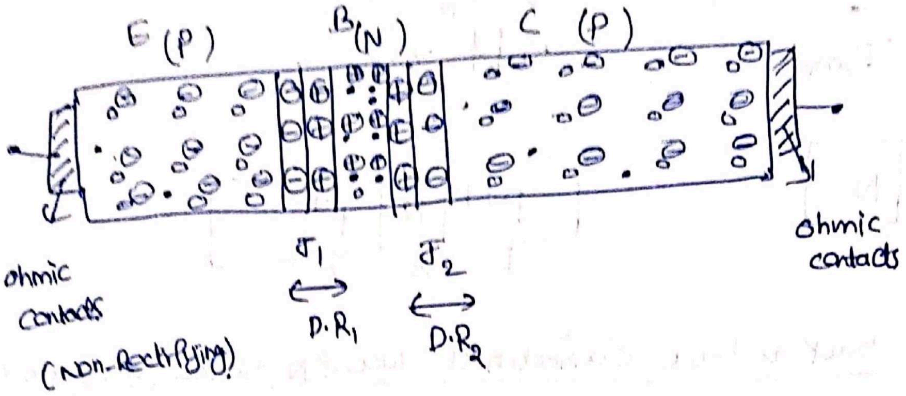
(7)

Fermi- Energy diagram of BJT in open ckt condition

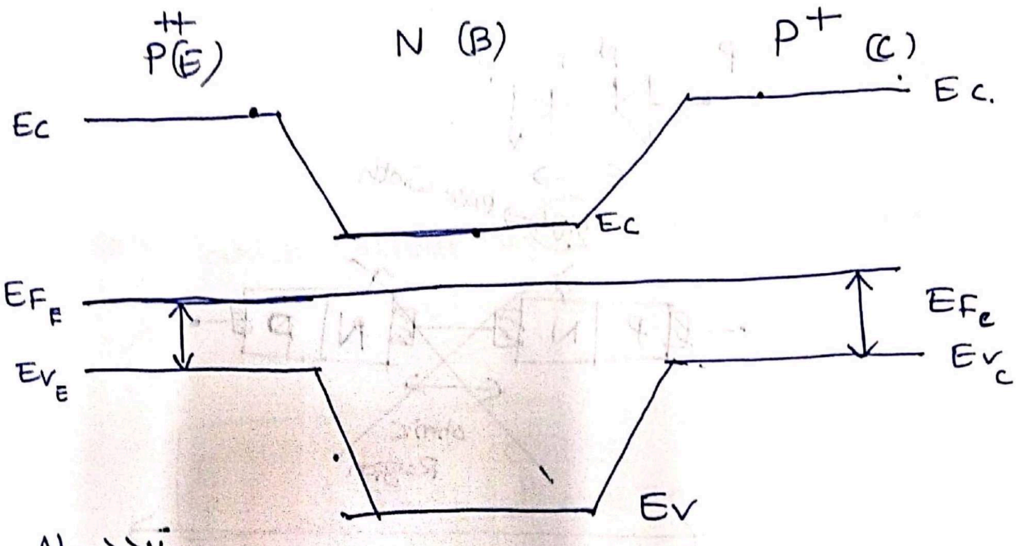
(or) Equilibrium

①

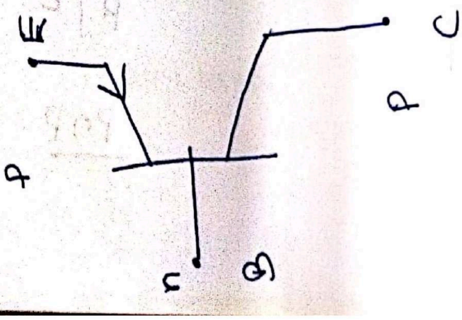
②



$\phi_m < \phi_s$



$N_E >> N_C$



Design specifications of E, B, C in BJT

① Size

② Doping

Terminal	Size	Doping
Emitter	moderate.	Heavily.
Base	Thin.	lightly
collector	High	moderately

ambiguity

Neamen & Karmalkar Sir

↓

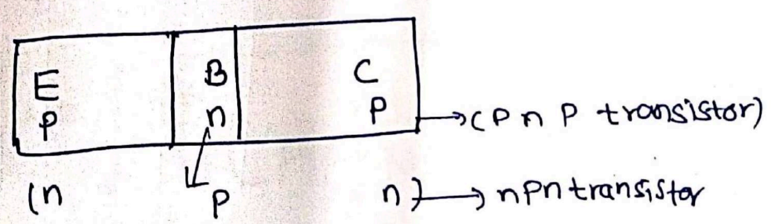
moderately

lightly.

Emitter: Emits e^-s, ie it supplies e^-s to O/P (or) holes to the Base.

Base : control action (it controls the supply of e^-s (or) holes from i/p to O/P)

collector: which collects the e^-s (or) holes & produces current as O/P.



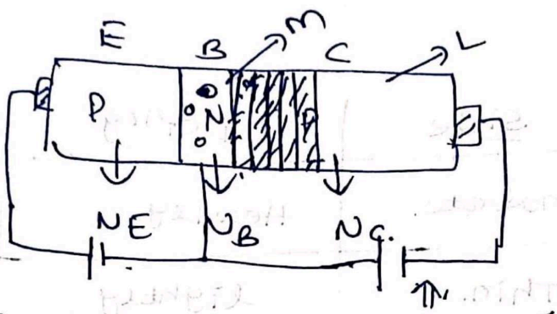
N_D

Power dissipation $= P = \sigma E$ watts/cm3

$\Downarrow P \propto \frac{1}{A \text{ (or) volume} \Uparrow}$

Collector- High

If Base is moderately doped ??



(i) $N_E >> N_C > N_B$ (milliman)

(ii) $N_E >\geq N_B > N_C$ (Karmalkar sir)

TOPICS like

⇒ Base width modulation

⇒ Punch through (or) Reach-through

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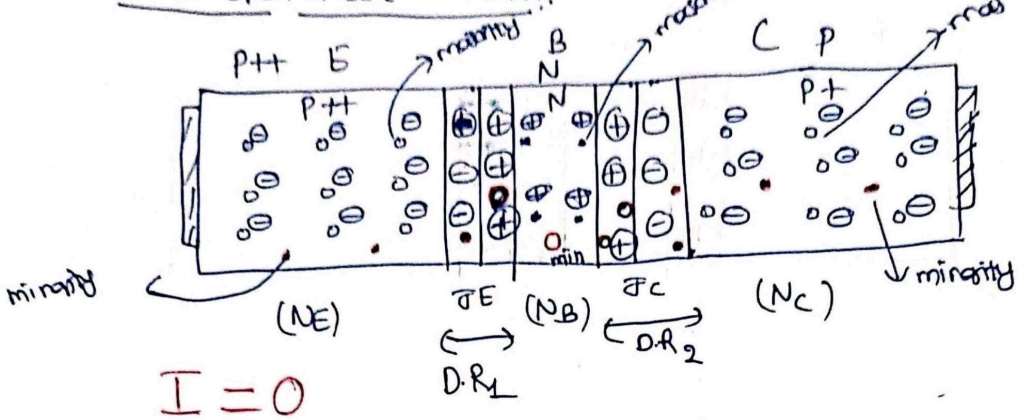
working of BJT :

(i) under open circuit condition :



I = 0

$$V_{bi_1} = \frac{KT}{q} \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) = \frac{KT}{q} \ln\left(\frac{N_E N_B}{n_i^2}\right)$$

$$V_{bi_2} = \frac{KT}{q} \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) = \frac{KT}{q} \ln\left(\frac{N_C \cdot N_B}{n_i^2}\right)$$

$N_E >> N_C > N_B$ $\qquad V_{bi_1} > V_{bi_2}$

$p^{++} \quad p^{+} \quad n$

$$\Downarrow w_1 = \sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_E} + \frac{1}{N_B}\right)(V_{bi_1})} \simeq 0.7 \text{ v.}$$

$10^{17}, 10^{13}, 10^{19}$

$$\Uparrow w_2 = \sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_C} + \frac{1}{N_B}\right)(V_{bi_2})} \simeq 0.6$$

~~$w_1 > w_2$~~
~~$(V_{bi_1} > V_{bi_2})$~~

$\boxed{w_2 > w_1}$

$\boxed{w_{D.R_2} > w_{D.R_1}}$

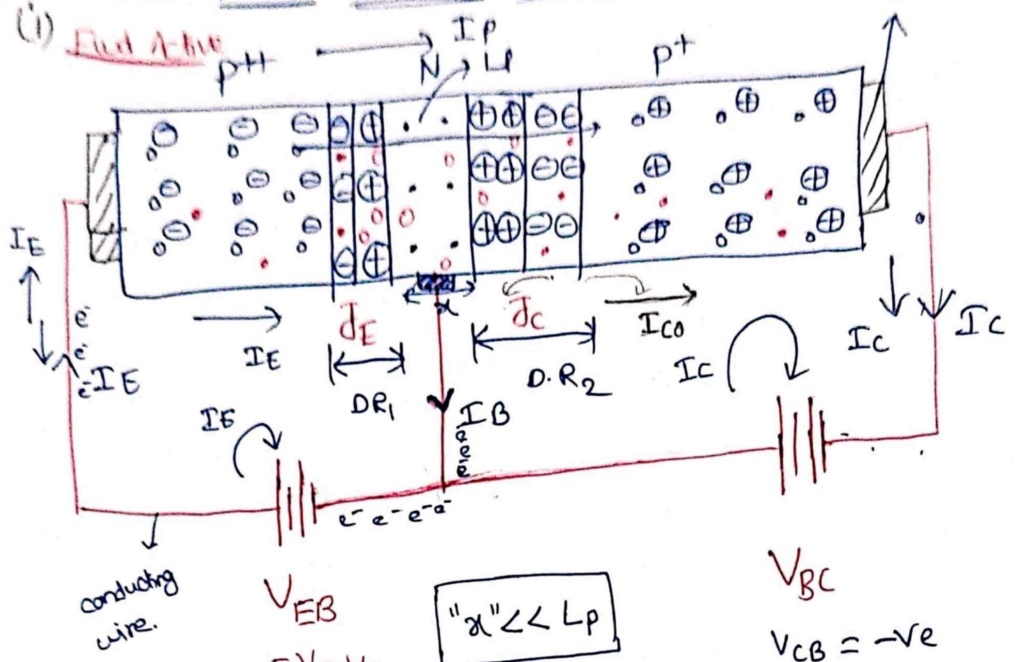
$w_1 = \sqrt{10^{-19} \times 0.7}$

$w_2 = \sqrt{10^{-15} \times 0.6}$

$\boxed{w_2 > w_1}$

Working of BJT in closed ckt condition: modes of operation of BJT

(i) Fwd Active



$V_{EB} = V_E - V_B$

$\boxed{\text{"}x\text{"} << L_p}$

$L_p = \sqrt{D_p \cdot \tau_p}$

V_{BC}

$V_{CB} = -ve$
$= V_C - V_B$
$= (-ve)$

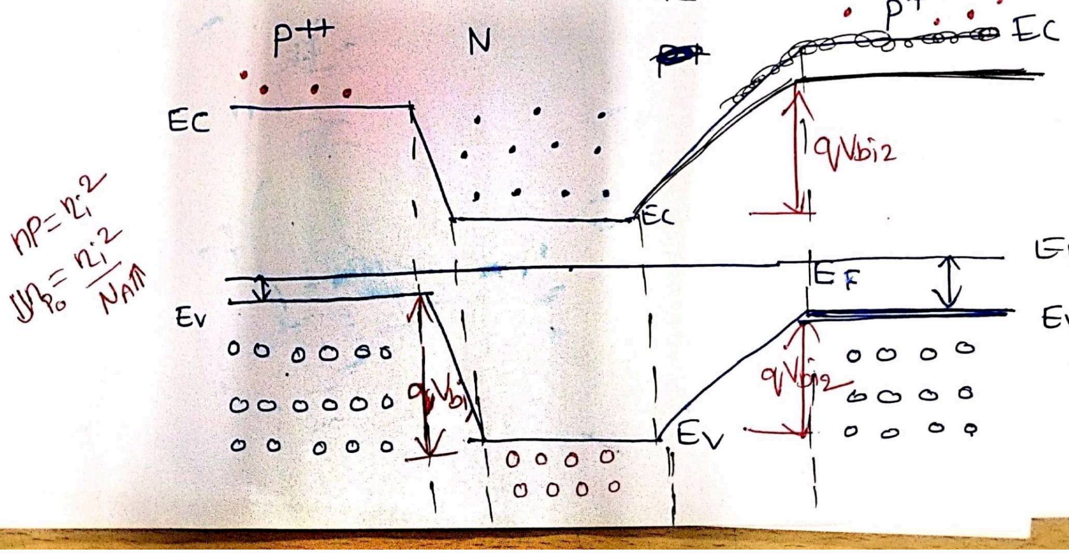
$V_{EB} = +ve$

$V_{CB} = -ve$

According to conservation of charge (KCL)

$$\boxed{I_E = I_B + I_C}$$

current entering into the device — current leaving from the device



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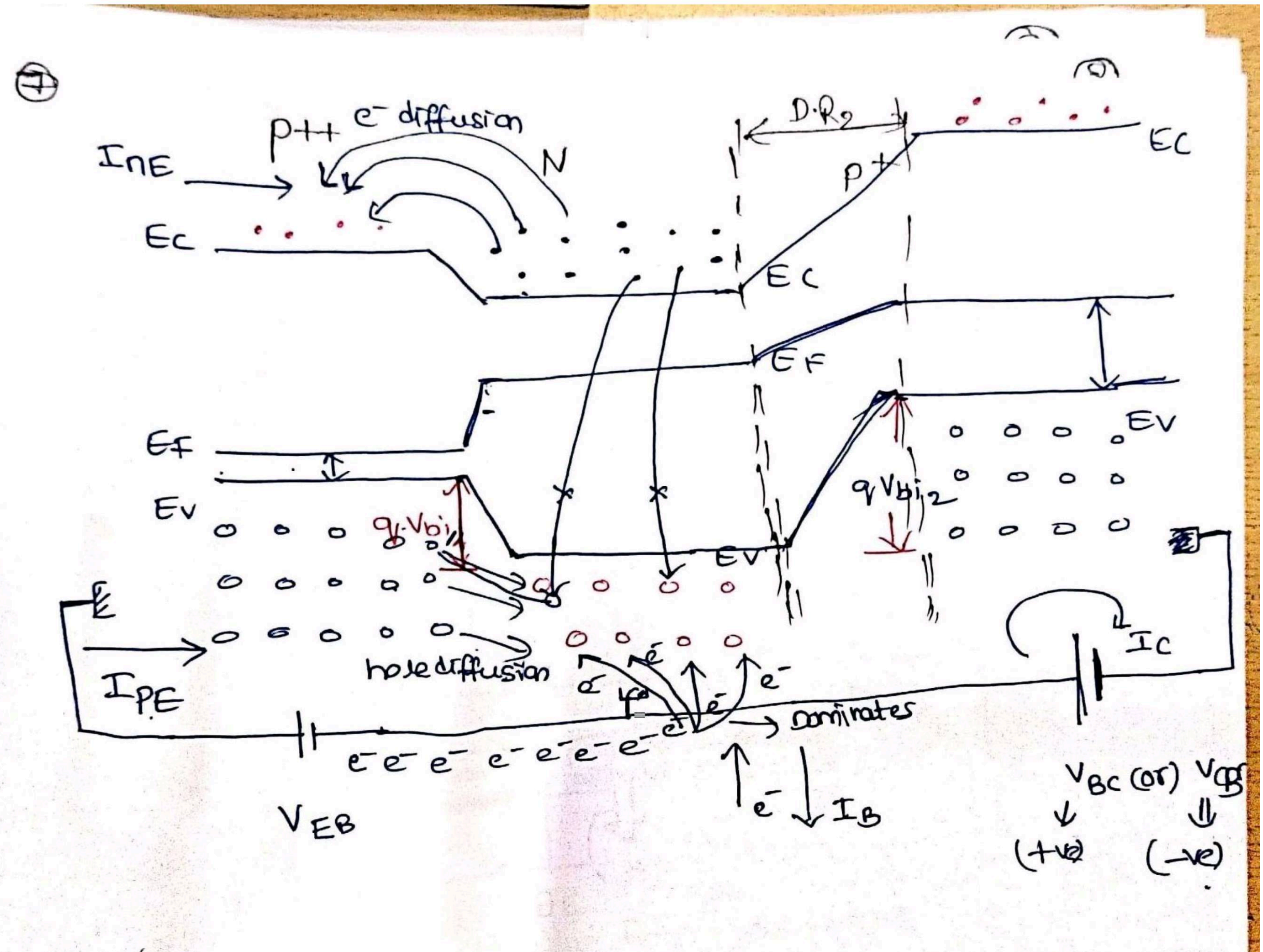

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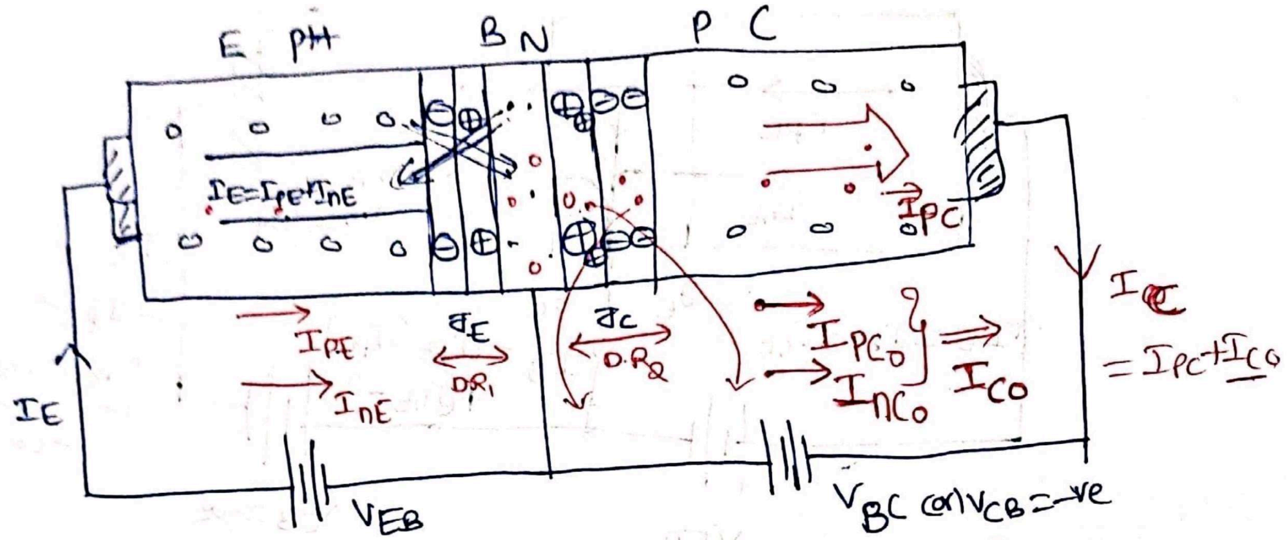
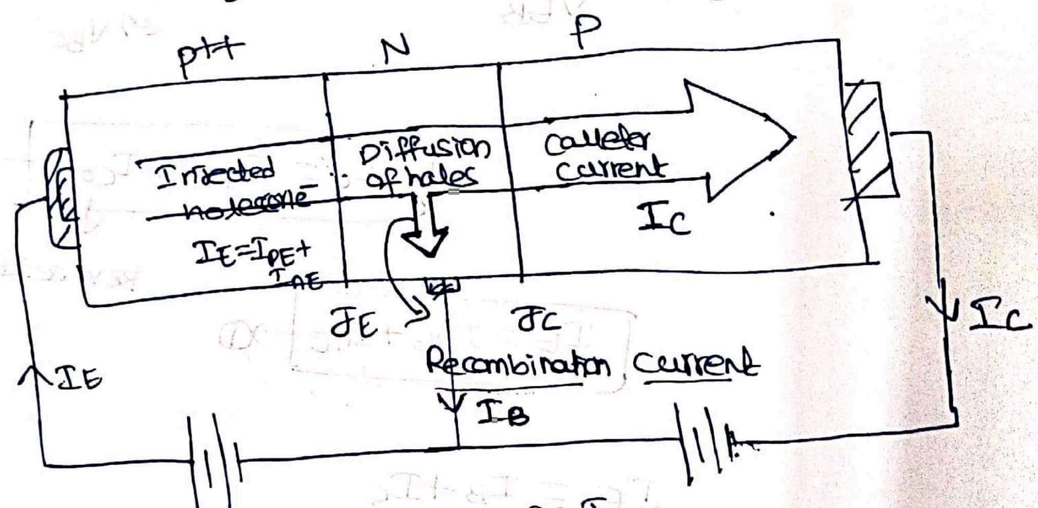
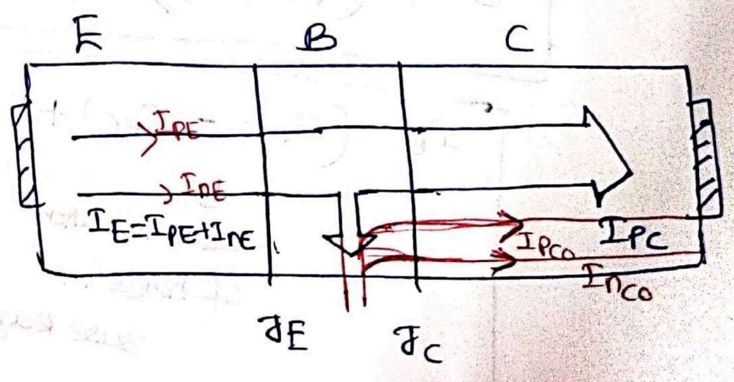
Current components of BJT in Forward Active mode:

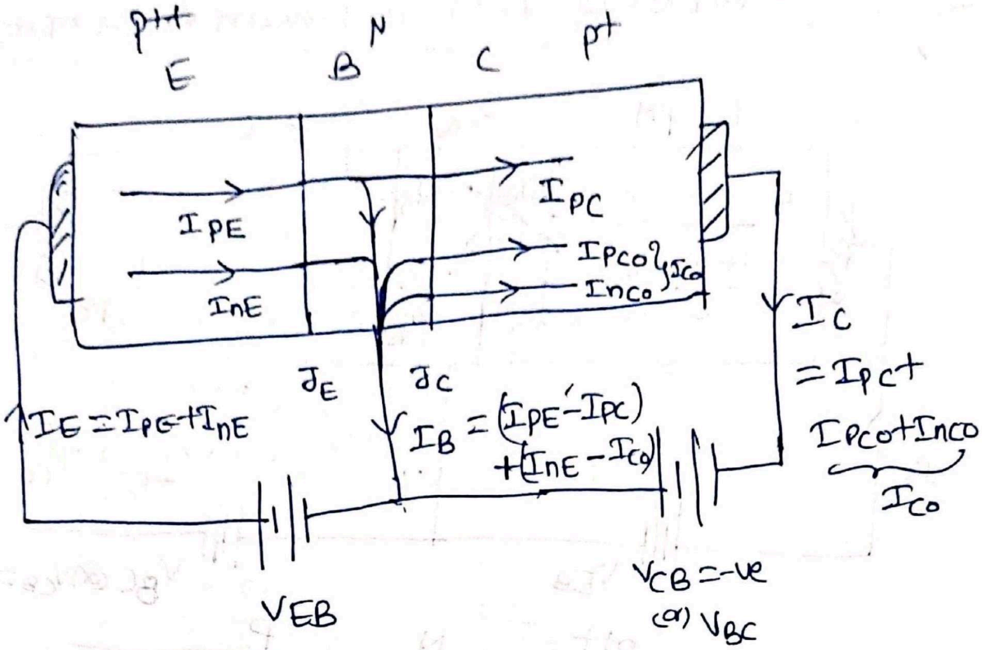




$$\text{i/p} \leftarrow I_E = \overset{\text{Re.I}}{I_B} + I_C \rightarrow \text{o/p}$$

$$\boxed{I_C = \underset{\text{i/p}}{I_E} - \underset{\text{Loss}}{I_B}}$$





$$\boxed{I_C = I_{pC} + I_{co}} \rightarrow (2)$$

I_{co}: Reverse saturation current

$$\boxed{I_E = I_{pE} + I_{nE}} \rightarrow (1)$$

$$I_E = I_B + I_C$$

$$I_B = I_E - I_C$$

$$= (I_{pE} + I_{nE}) - (I_{pC} + I_{co})$$

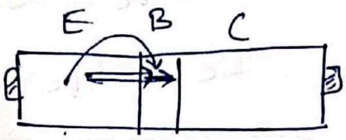
$$\boxed{I_B = (I_{pE} + I_{nE}) - (I_{pC} + I_{pco} + I_{nco})} \rightarrow (3)$$

$$I_B = \underbrace{(I_{pE} - I_{pC})}_{\text{Recombination of holes in Base Region}} + \underbrace{(I_{nE} - I_{co})}_{\text{Recombination of e's in Base Region.}}$$

Performance parameters:

1. Emitter Injection efficiency (γ^*)
2. Base Transportation factor (β^*)
3. DC current gain (α, β, γ).

1. Emitter Injection efficiency (γ^*)



$$\gamma^* = \frac{I_{pE}}{I_E}$$

$$I_E = I_{pE} + I_{nE}$$

$$\boxed{\gamma^* = \frac{I_{pE}}{I_{pE} + I_{nE}}}$$

2. Base Transportation factor: (β^*)

$$\beta^* = \frac{I_{pC}}{I_{pE}}$$

3. DC gain (or) DC current gain (α, β, γ).

$$CB - \alpha = \frac{o/p}{i/p} = \frac{I_C}{I_E}$$

$$CE - \beta = \frac{I_C}{I_B}$$

$$CC - \gamma = \frac{I_E}{I_C}$$

$$\alpha = \frac{o/p}{i/p} = \frac{I_C}{I_E} = \frac{I_{pc}}{I_E}$$

$$I_C = I_{pc} + I_{Co}$$

$$I_C \simeq I_{pc}$$

$$\alpha = \frac{I_{pc}}{I_E}$$

$$I_{pc} = \alpha I_E$$

$$I_C = I_{pc} + I_{Co}$$

$$\boxed{I_C = \alpha I_E + I_{Co}} \Rightarrow C \cdot B$$

CB

$$\boxed{I_C = \alpha I_E + I_{CBO}}$$

Reverse sat current in CB when emitter is open.

CE :

$$\boxed{I_C = \beta I_B + I_{CEO}}$$

CC :

$$\boxed{I_E = \gamma I_B + I_{CCO}}$$

Relation b/w α, β^*, γ^*

$$\gamma^* = \frac{I_{pE}}{I_E}$$

$$\beta^* = \frac{I_{pc}}{I_{pE}}$$

$$\alpha = \frac{I_{pc}}{I_E} = \left(\frac{I_{pc}}{I_{pE}}\right) \times \frac{I_{pE}}{I_E}$$

$$\boxed{\alpha = \beta^* \times \gamma^*}$$

Relation b/w α, β, γ.

$$\alpha = \frac{I_{pc}}{I_E}$$

neglecting Reverse sat Currents

$$I_c = I_{pc} + \cancel{I_{co}}$$

$$I_c \simeq I_{pc}$$

$$\boxed{\alpha = \frac{I_c}{I_E}} \quad \boxed{\beta = \frac{I_c}{I_B}} \quad \boxed{\gamma = \frac{I_E}{I_B}}$$

Relation b/w α, β, γ:

(18)

$$\boxed{I_E = I_B + I_C} \rightarrow (1)$$

$$\frac{(1)}{I_B} \qquad \frac{I_E}{I_B} = \frac{\cancel{I_B}}{\cancel{I_B}} + \frac{I_C}{I_B}$$

$$\boxed{\gamma = 1 + \beta} \qquad \boxed{\beta = \gamma - 1}$$

$I_C = \alpha I_E \rightarrow (2)$

sub eq (1) in (2)

$$I_C = \alpha(I_B + I_C)$$

$$I_C = \alpha I_B + \alpha I_C$$

$$I_C - \alpha I_C = \alpha I_B$$

$$I_C(1-\alpha) = \alpha I_B$$

$$\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

$I_C = \beta I_B \rightarrow (3)$

$$I_C = \beta(I_E - I_C)$$

$I_E = I_B + I_C$

$I_B = I_E - I_C$

$$I_C = \beta I_E - \beta I_C$$

$$I_C + \beta I_C = \beta I_E$$

$$(1+\beta) I_C = \beta I_E$$

$$\alpha = \frac{I_C}{I_E} = \frac{\beta}{1+\beta}$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

$$\boxed{\alpha = \frac{\gamma - 1}{\cancel{1} + \gamma - \cancel{1}} = \frac{\gamma-1}{\gamma}}$$

$$\gamma = 1 + \beta$$

$$\gamma = 1 + \frac{\alpha}{1-\alpha}$$

$$\boxed{\gamma = \frac{1 - \cancel{\alpha} + \cancel{\alpha}}{1-\alpha} = \frac{1}{1-\alpha}}$$

Relation between α, β & γ

We Know that $\boxed{I_E = I_B + I_C} \rightarrow (1)$

Divide eq (1) with I_E, we will get

$$\frac{I_E}{I_E} = \frac{I_B}{I_E} + \frac{I_C}{I_E}$$

$$1 = \frac{I_B}{I_E} + \frac{I_C}{I_E}$$

$$1 = \frac{I_B}{I_E} + \alpha \quad \left(\because \alpha = \frac{I_C}{I_E}\right)$$

$$1 - \frac{I_B}{I_E} = \alpha$$

$$\alpha = 1 - \frac{I_B}{I_C} \times \frac{I_C}{I_E} = 1 - \frac{1}{\beta} \times \alpha$$

$\Big(\because$ CB $\Rightarrow \alpha = \frac{I_C}{I_E}$

CE $\Rightarrow \beta = \frac{I_C}{I_B}$

CC $\Rightarrow \gamma = \frac{I_E}{I_B}\Big)$

$$\alpha = 1 - \frac{\alpha}{\beta}$$

$$1-\alpha = \frac{\alpha}{\beta}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}} \rightarrow (2)$$

"β" interms of "α"

To get the Relation "α" in terms of "β" add 1 to eq (2) on both sides

$$\beta+1 = \frac{\alpha}{1-\alpha} + 1$$

$$\beta+1 = \frac{\cancel{\alpha}+1-\cancel{\alpha}}{1-\alpha} = \frac{1}{1-\alpha}$$

$$1+\beta = \frac{1}{1-\alpha}$$

$$1-\alpha = \frac{1}{1+\beta}$$

$$1-\frac{1}{1+\beta} = \alpha \Rightarrow \boxed{\alpha = \frac{\cancel{1}+\beta-\cancel{1}}{1+\beta} = \frac{\beta}{1+\beta}}$$

$$\therefore \boxed{\alpha = \frac{\beta}{1+\beta}} \rightarrow (3)$$

we know that $I_E = I_B + I_C \longrightarrow ①$ Divide it with "I_B" we get

$$\frac{I_E}{I_B} = \frac{\cancel{I_B}}{\cancel{I_B}} + \frac{I_C}{I_B}$$

$$\frac{I_E}{I_B} = 1 + \frac{I_C}{I_B}$$

$\left(\because \text{ we know that } \gamma = \frac{I_E}{I_B}\right.$

$\beta = \frac{I_C}{I_B}$

$$\boxed{\gamma = 1+\beta} \longrightarrow ④$$

But we know that $\beta = \frac{\alpha}{1-\alpha}$

so from ④ $\gamma = 1 + \frac{\alpha}{1-\alpha} = \frac{1-\cancel{\alpha}+\cancel{\alpha}}{1-\alpha} = \frac{1}{1-\alpha}$.

$$\boxed{\gamma = \frac{1}{1-\alpha}}$$

& we can write "α" interms of γ i.e.

$1-\alpha = \frac{1}{\gamma}$ $\quad 1 - \frac{1}{\gamma} = \alpha \Rightarrow \boxed{\alpha = \frac{\gamma - 1}{\gamma}}$

Relation b/w α, β, γ :

⇒ "α" interms of β & γ is

$$\boxed{\alpha = \frac{\beta}{1+\beta}, \quad \alpha = \frac{\gamma - 1}{\gamma}}$$

⇒ "β" interms of α & γ is

$$\boxed{\beta = \frac{\alpha}{1-\alpha}, \quad \beta = \gamma - 1}$$

⇒ γ interms of α & β is

$$\boxed{\gamma = \frac{1}{1-\alpha}, \quad \gamma = 1+\beta}$$

Circuit configurations of BJT :

(i) There are three circuit configurations of BJT

(i) common Emitter
(ii) common Base
(iii) common collector.

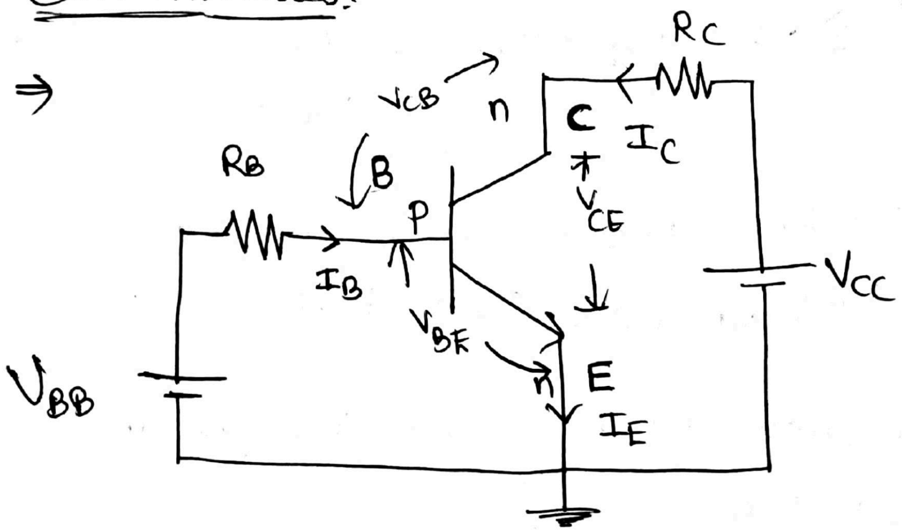
Common Emitter : Emitter is grounded & Emitter is common to both input (Base) and output (collector)

Common Base : Base is grounded & Base is common to both input (Emitter) and output (collector)

Common collector : collector is grounded & collector is common to both input (Base) and output (Emitter)

Common Emitter :

⇒



⇒ The emitter is grounded, Emitter is common to Base and collector.

⇒ R_B ⇒ Input Resistance , R_C ⇒ output Resistance

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⇒ R_B, R_C ⇒ will provide drop in input voltage, Inorder to reduce the sudden changes in voltage.

⇒

From KCL of the above circuit, $\boxed{I_E = I_B + I_C}$

The gain of the common emitter ckt configuration is "β"

$$\beta = \frac{\text{output of the collector (hole current in pnp)}}{\text{Input current}}$$

$$\boxed{\beta = \frac{I_{pC}}{I_B}}$$

where $I_C = I_{pC} + I_{CO}$, so $I_{pC} \simeq I_{pC}$; since I_{CO} is negligible

$I_C \simeq I_{pC}$

$$\boxed{\beta = \frac{I_{pC}}{I_B} \quad (\text{or}) \quad \beta \simeq \frac{I_C}{I_B}}$$

As we know that $I_C = I_{pC} + I_{CO} \longrightarrow$ (A)

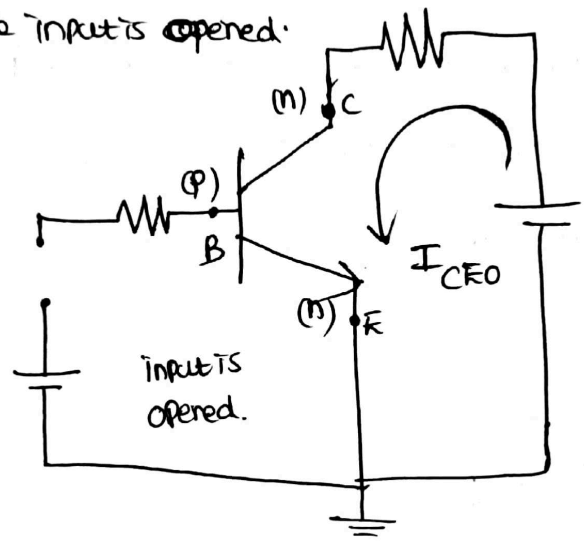
$\therefore I_{pC} = \beta I_B \longrightarrow$ (B)

substitute eq (B) in eq (A)

$$\boxed{I_C = \beta I_B + I_{CO}} \longrightarrow (C)$$

$$\boxed{I_C = \beta I_B + I_{CO}}$$

where I_{CO} is the Reverse saturation current, which is measured in between Collector & Emitter when Base is opened (or) the input is opened.



$$I_C = I_{CEO}\Big|_{\text{when } I_B=0 \text{ (or) Base is opened}}$$

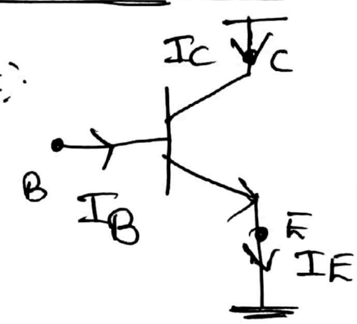
whence apply input

$$\boxed{I_C = \beta I_B + I_{CEO}}$$

I_{CEO} = Reverse saturation current b/w Collector & emitter (or) collector to emitter reverse saturation current

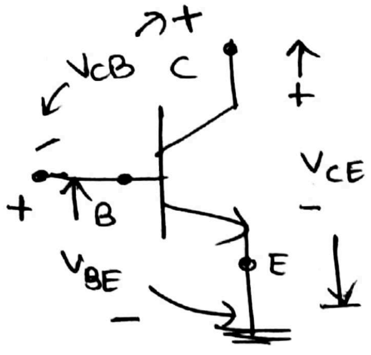
KVL & KCL in CE: (In Fwd active mode)

KCL:



$$\boxed{I_E = I_B + I_C}$$

KVL:



For npn

By applying KVL

$$-V_{BE} - V_{CB} + V_{CE} = 0$$

$$\boxed{V_{CE} = V_{CB} + V_{BE}}$$

V-I Characteristics of CE Amplifier:

⇒ To draw the VI characteristics, we know which two port n/w parameters that we are using for the Analysis of Transistor. Because we have grounded one of the three terminals of BJT, so we have to use two port N/W parameters

⇒ Among the six ($^4C_2$) two port N/W Parameters, we are using "h-Parameter model" to analyze BJT

Why we are using h-Parameter model for the Analysis of BJT?

In BJT, the output current (I_C) and input voltage (V_{BE}) are dependent parameters like h-Parameter model.

In h-parameter model

$$V_1 = h_{11} I_1 + h_{12} V_2$$

$$I_2 = h_{21} I_1 + h_{22} V_2$$

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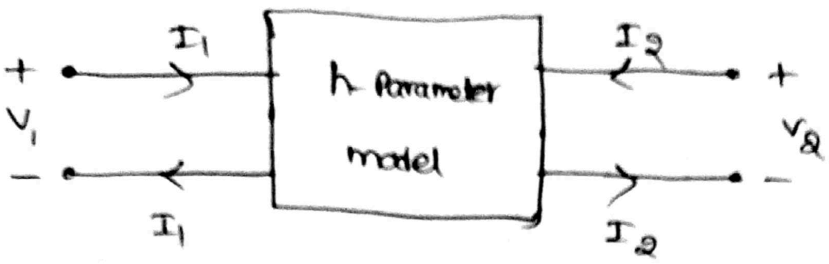


$V_1, I_1 \Rightarrow$ Input voltage & current

$V_2, I_2 \Rightarrow$ output voltage & current

where V_1, I_2 are dependent parameters

Similarly In BJT input voltage V_{BE} and output current I_C are dependent parameters So

$$V_1 = V_{BE} \qquad V_2 = V_{CE}$$
$$I_1 = I_B \qquad I_2 = I_C$$

So h-parameter model for BJT is

$$V_{BE} = h_{11} I_B + h_{12} V_{CE}$$
$$I_C = h_{21} I_B + h_{22} V_{CE}$$

$\Rightarrow$ Since I_C (Output current) depends on Input current (I_E) and output voltage (V_{CE}), i.e In Forward active mode $I_C = f(I_E)$ and if we $\Uparrow$ V_{CE}, $I_C \Uparrow$. So I_C depends on I_E & V_{CE}

$$\therefore \boxed{I_C = h_{21} I_B + h_{22} V_{CE}}$$

⇒ Input voltage V_{BE} depends on V_{CE} and I_E. i.e If we ⇑ (increase) V_{CE}, Reverse bias across J_C ⇑, then width of the depletion Region ⇑ and penetrates into Base Region, due to this Effective Base width ⇓, so now we have to give less V_{BE} to make the holes to penetrate into Base Region.

ie input voltage V_{BE} to be given ⇓, because of the reduction in I_B (due to ⇓ in I_B, I_C ⇑ which makes the I/P to be given less than previous input for the required I_C which requires less "V_{BE}" to be given to get "I_C".

(∵ ⇑ = Increase ; ⇓ = Decrease)

So
$$\boxed{\begin{aligned} V_{BE} &= h_{11} I_B + h_{12} V_{CE} \\ I_C &= h_{21} I_B + h_{22} V_{CE} \end{aligned}} \begin{aligned} &\longrightarrow Ⓐ \\ &\longrightarrow Ⓑ \end{aligned}$$

⇒ To draw the input V-I characteristics of the BJT, we need i/p voltage (V_{BE}) on x-axis and input current (I_B) on y-axis

So From eq Ⓐ

$$\underline{V_{BE}} = h_{11} \underline{I_B} + h_{12} V_{CE} \Rightarrow V_{CE} \text{ constant}$$

$$I_C = h_{21} I_B + h_{22} V_{CE}$$

To draw the V-I c/s for $\underline{V_{BE}}$ and $\underline{I_B}$, $\underline{V_{CE} \text{ is constant}}$

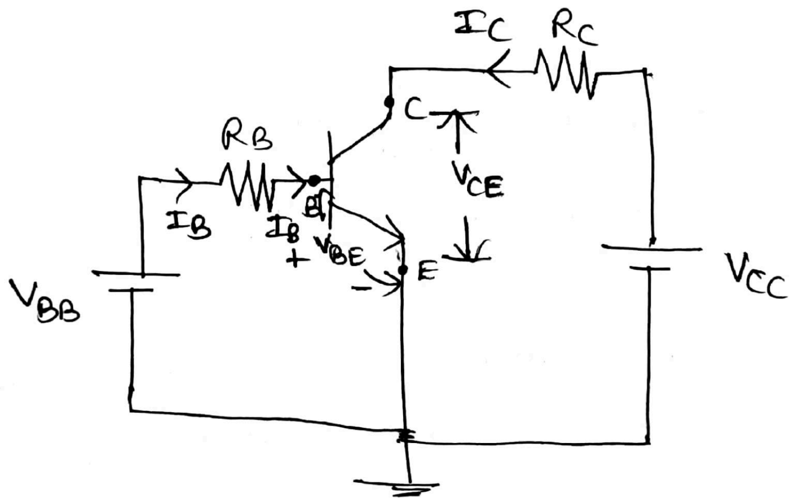
⇒ To draw the Input V-I c/s for V_{BE} and I_B, the output Voltage (V_{CE}) is constant.

⇒ Similarly to draw the output V-I c/s for V_{CE} and I_C, the input current I_B is constant.

$$I_C = h_{21} I_B + h_{22} V_{CE}$$

Input V-I Characteristics of CE Amplifier:

⇒ To draw the V-I characteristics of CE Amplifier, output Voltage is kept constant.



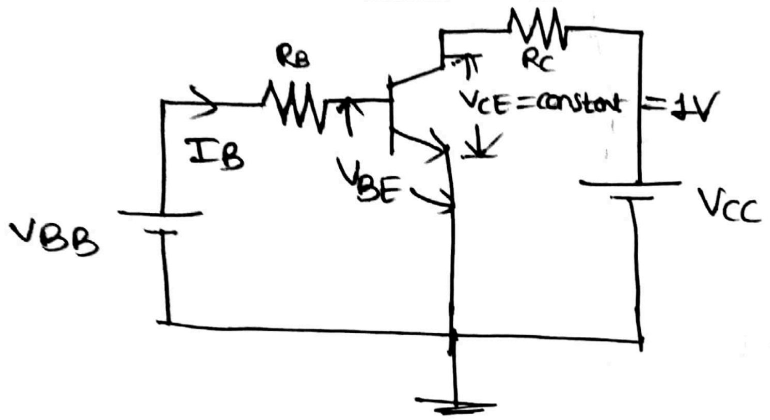
Input Voltage of BJT is "V_{BE}" and Input current "I_B" will be drawn when V_{CE} is constant

⇒ The practical circuit connection to measure voltage V_{BE} and current I_B includes Voltmeter and Ammeter

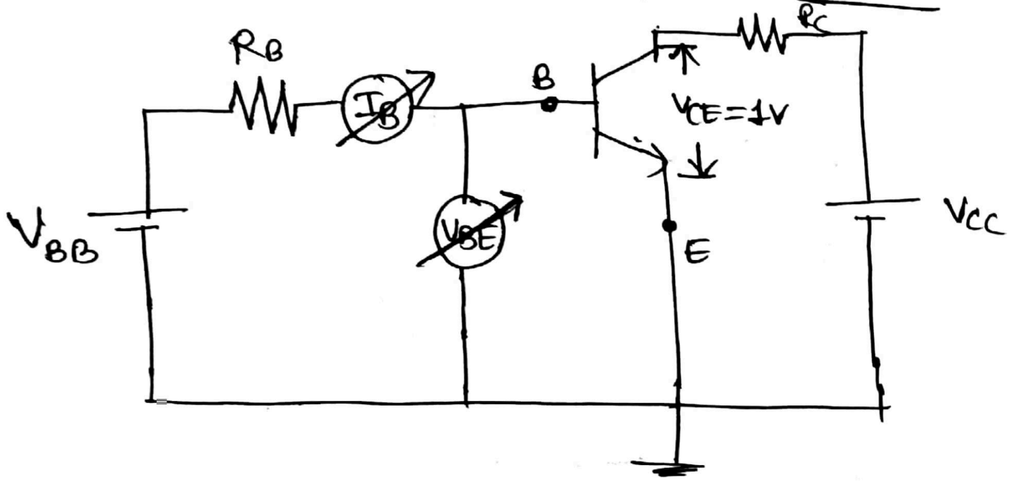
$$\underset{\text{Variable}}{V_{BE}} = h_{11} \underset{\text{Variable}}{I_B} + h_{12} \underset{\text{Keep it as a Constant to draw i/p V-I c/s}}{V_{CE}}$$

Case(i)

when $V_{CE} = 1V$ (Fixed (or) constant)

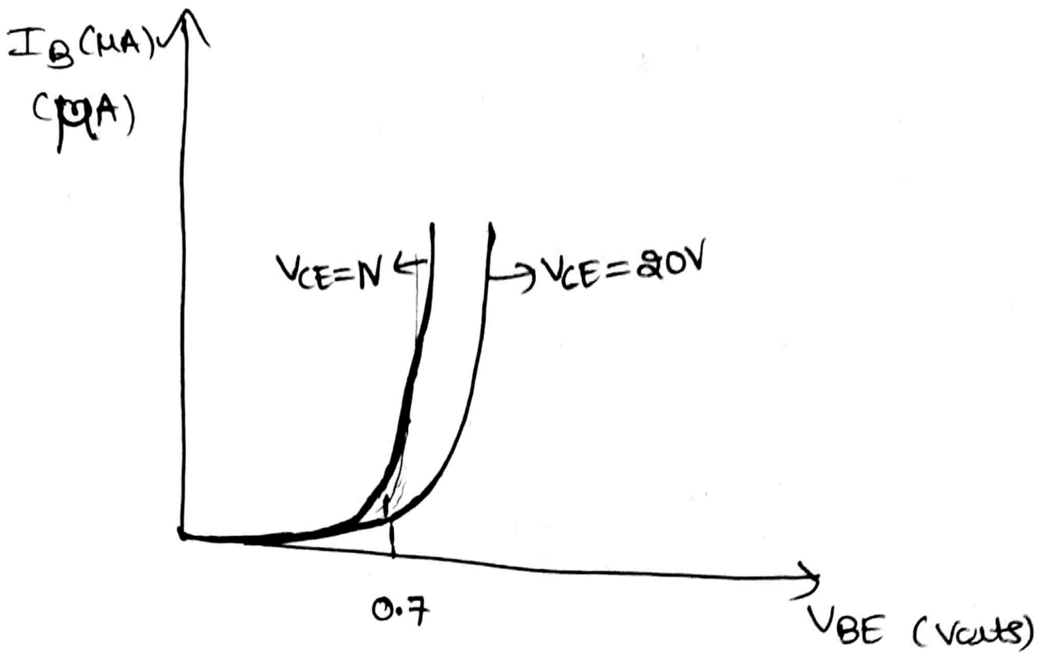


Practical circuit to measure voltages & currents

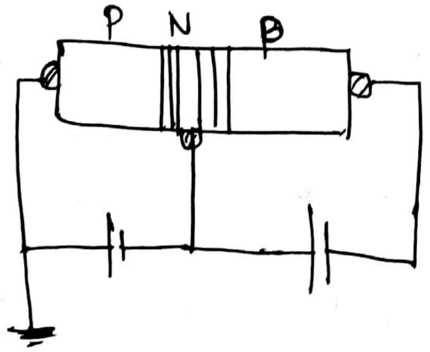


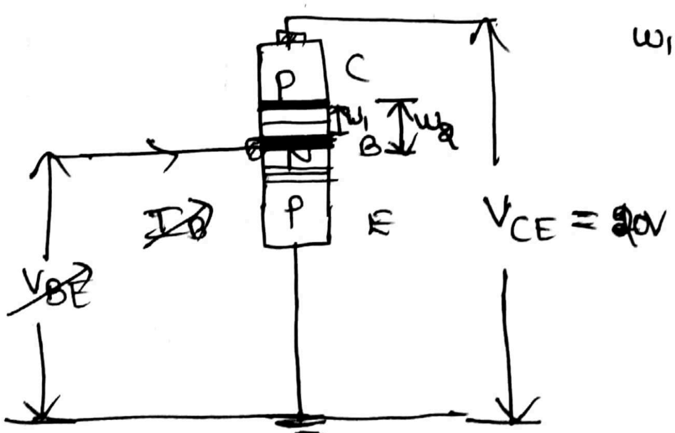
⇒ when we keep output voltage constant $V_{CE}=1V$ (or) (Sometimes $V_{CE}=0V$)

The input characteristics V_{BE} vs I_B are same as PN diode VI characteristics ie when we ⇑ V_{BE}, I_B⇑ exponentially after Cut in Voltage (0.7) for V_{CE} = small values (V_{CE}=0.1 to 1)



<u>Case (ii)</u> For <u>$V_{CE}=20V$</u>

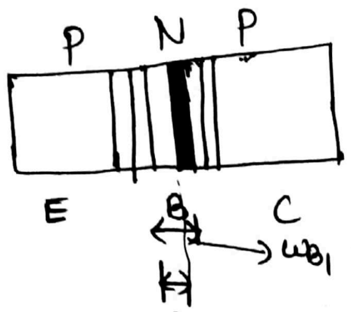




W_1 = width of D.R when $V_{CE}=1V$

W_2 = width of D.R when $V_{CE}=20V$

⇒ The depletion Region width ⇑ becoz of the Reverse bias Voltage $V_{CE}=20V$ ie "W_1" ⇑ to "W_2" and Penetrates more into Base Region, so that width of the Base Region ⇓

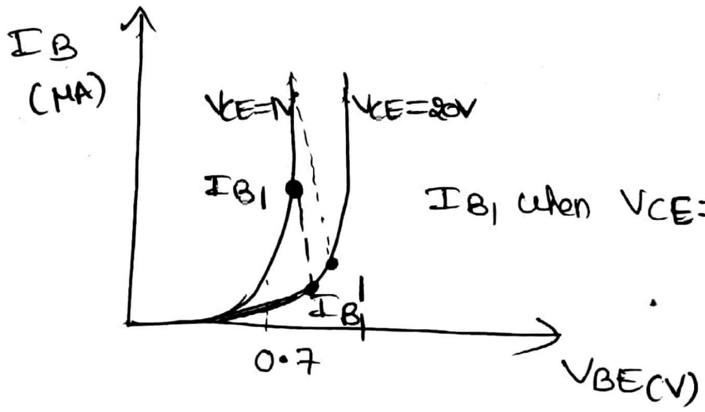


$\rightarrow W_{B_1}$ = Effective Base width when $V_{CE} = 1V$

$\rightarrow W_{B_2}$ = Effective Base width when $V_{CE} = 20V$

⇒ Becoz of the Reverse Voltage $V_{CE} = 20V$, the width of the Depletion Region ⇑ and Effective Base width ⇓, This process is called "Base width modulation" (or) "Early Effect"

⇒ Because of the Early Effect, Base width ⇓, so Recombination Region ⇓. then Recombination Current (I_B) ⇓



I_{B_1} when $V_{CE}=1V$ and I'_{B_1} when $V_{CE} = 20V$ are different

I_{B_1} ⇓ to I'_{B_1} for the same input V_{BE} becoz of the ⇑ in Reverse Voltage V_{CE} from 1 to 20V

Parameters to be obtained from the input VICs of CE:

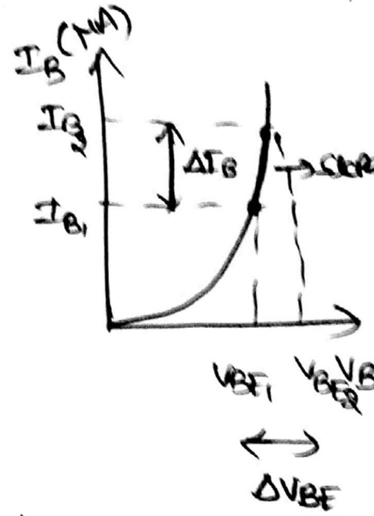
$$V_{BE} = h_{11} I_B + h_{12} \underline{V_{CE}}$$ constant

Input Resistance (R_i) $= h_{11} = \left.\dfrac{V_{BE}}{I_B}\right|_{V_{CE}=0}$

$h_{12} = \left.\dfrac{V_{BE}}{V_{CE}}\right|_{I_B=0}$ – Reverse Voltage gain

$h_{11} = \frac{V_{BE}}{I_B} = \frac{\text{Input voltage}}{\text{Input current}} = \text{Input Resistance } R_i$

$$\boxed{R_i = h_{11} = \frac{V_{BE}}{I_B}}$$



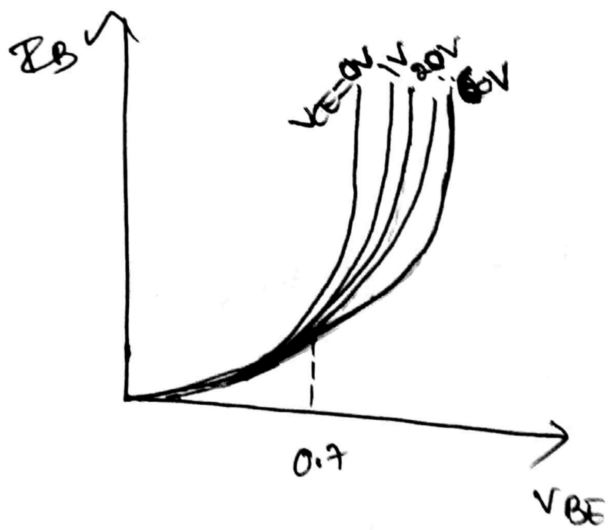
$\text{slope} = \frac{\Delta I_B}{\Delta V_{BE}} = \frac{1}{h_{11}} = \frac{1}{R_i}$

Slope of I/P VI c/s is

$$\text{Slope} = \frac{\Delta I_B}{\Delta V_{BE}} = \frac{1}{h_{11}} = \frac{1}{R_i} = \frac{1}{\text{Input Resistance}}$$

∴ So $\boxed{\text{Input Resistance } (R_i) = \frac{1}{\text{slope of I/P VI c/s}}}$

<u>Input VI c/s of CE is:-</u>



$$\boxed{R_i = \frac{\Delta V_{BE}}{\Delta I_B} = h_{11}}$$

Output V-I charateristics of CE Amplifier:

⇒ output characteristics are drawn between output voltage (V_{CE}) and output current (I_C)

From h-parameter model

$$\boxed{\underbrace{I_C}_{\text{o/p current}} = h_{21} \underbrace{I_B}_{\text{I/p current constant}} + h_{22} \underbrace{V_{CE}}_{\text{output Voltage}}}$$

While ~~calculating~~ drawing output V-I characteristics Input current (I_B) is constant

we know that in Common Emitter configuration o/p current

$$\boxed{I_C = \beta I_B + I_{CEO}} \longrightarrow (a)$$

we can also write this eq (a) as below from the output current equation of common base circuit configuration

ie In CB o/p current

$$I_C = \alpha I_E + I_{CBO} \qquad (\because I_E = I_B + I_C)$$

$$I_C = \alpha(I_B + I_C) + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$I_C = \underbrace{\left(\frac{\alpha}{1-\alpha}\right)}_{\to \beta} I_B + \frac{1}{1-\alpha} I_{CBO}$$

we know that $\beta = \frac{\alpha}{1-\alpha}$ then I_C becomes

$$\boxed{I_C = \beta I_B + \frac{1}{1-\alpha} I_{CBO}} \rightarrow (b)$$

Compare equations (a) and (b) we can write

$$\boxed{I_{CEO} = \frac{1}{1-\alpha} I_{CBO}}$$

So the o/p current equation of common emitter configuration can also be represented in terms of 'α' as

$$I_C = \beta I_B + \frac{1}{1-\alpha} I_{CBO} \rightarrow (c)$$

(or)

$$I_C = \beta I_B + I_{CEO} \rightarrow (d)$$

⟹ To draw the output characteristics, the input current I_B is constant

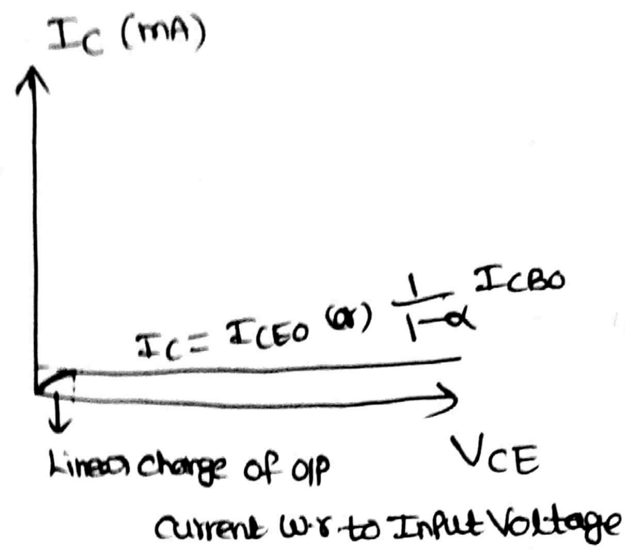
From equation (d)

$$I_C = I_{CEO} \Big|_{I_B = 0}$$

(or)

From eq (c) $I_C = \frac{I_{CBO}}{1-\alpha} \Big|_{I_B = 0}$

Case(i) when $I_B = 0$



Case(ii) when $I_B \neq 0$ ($I_B = 10\,\mu A, 20\,\mu A$ - - -)

⇒ If Input current $I_B = 10\,\mu A$ (or) a non-zero Value, the output varies in accordance with the input ie it is a function of input current and output voltage

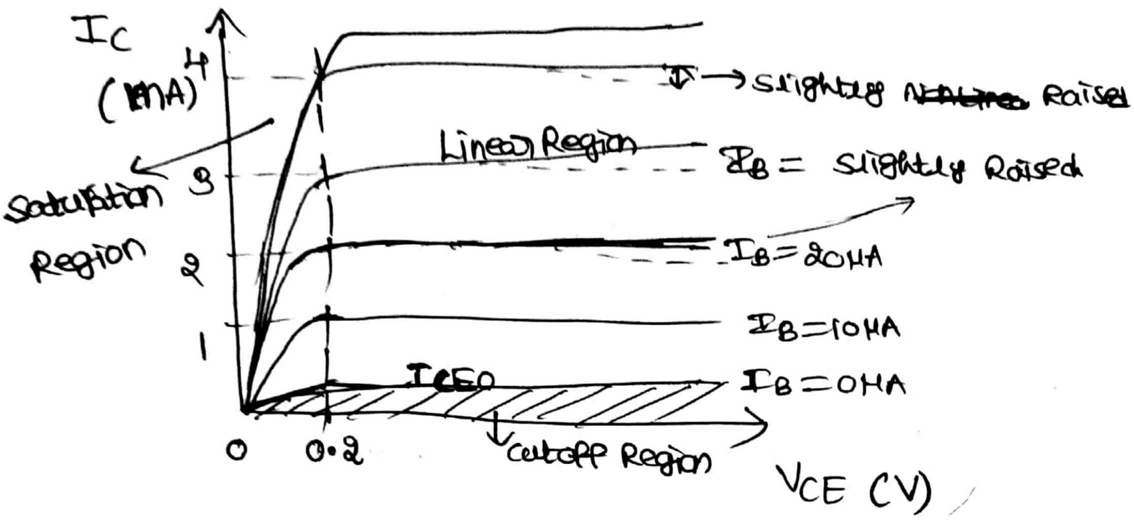
⇒ I_C varies Linearly with output Voltage V_{CE} and it reaches to a maximum value, ie called saturation current I_{CEO} when $I_B = 0$ (Base is open).

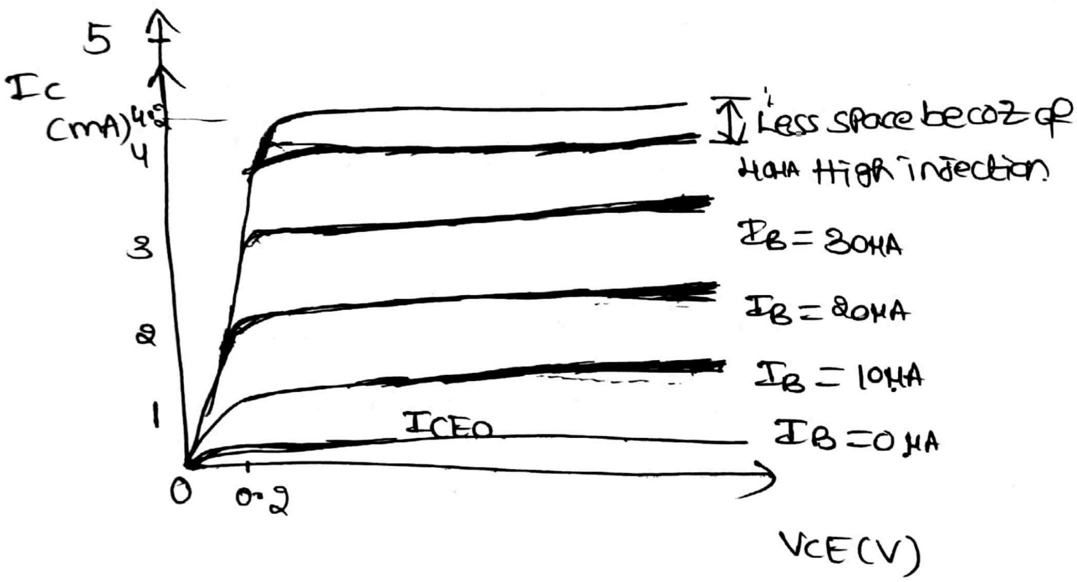
⇒ when $I_B \neq 0$ ie when $I_B = 10\,\mu A, 20\,\mu A$ - - - -, then the output $\boxed{I_C = \beta I_B + I_{CEO}}$ & Before Reaching the saturation current It varies Linearly with Voltage V_{CE}.

For Further values of "I_B" $= 20\,\mu A$ - - - , the value of I_C ⇑ with input I_B and I_C increases Linearly with V_{CE} Before reaching saturation

$I_C \Uparrow = \beta I_B \Uparrow + I_{CEO}$

$I_C \Uparrow$ Linearly with V_{CE} before Reaching saturation





$\Rightarrow$ As the $I_B \Uparrow$, the injection into Base Region $\Uparrow$, ie ~~I~~ due to that gain (β) $\Downarrow$

ie $\boxed{\left(\beta = \frac{I_C}{I_B \Uparrow}\right)} \Downarrow$

$$\text{gain} = \beta = \frac{I_C}{I_B}$$

$\Downarrow \beta$ If we $\Uparrow I_B$

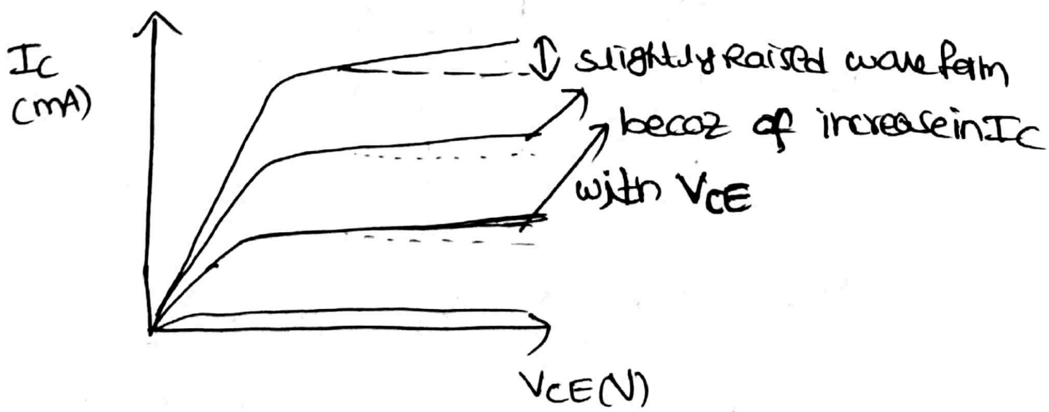
$\beta \Rightarrow$ can also be written as

$$\boxed{\beta = \frac{\Delta I_C}{\Delta I_B}}$$

$\Rightarrow$ Becoz of the increase in I_B, the Recombination also increases, Becoz of that Recombination current output current $I_C \Downarrow$ so gain $\Downarrow$ ie ($\beta \Downarrow$)

$\Rightarrow$ The lines which are shown as slightly raised are not Straight Lines becoz As we are $\Uparrow V_{CE}$, the Depletion Region $\Uparrow$ and Penetrates into Base Region which reduces the Effective Base Width called as Base width modulation (or) Early Effect

$\Rightarrow$ ✱ Due to the Early Effect $I_C \Uparrow$ becoz of the Reduction of Recombination current with respect to "V_{CE}". So As $V_{CE} \Uparrow$ the collector current $I_C \Uparrow$, becoz of the Early effect. So the graphs are not straight lines, they are just slightly raised with respect to V_{CE}

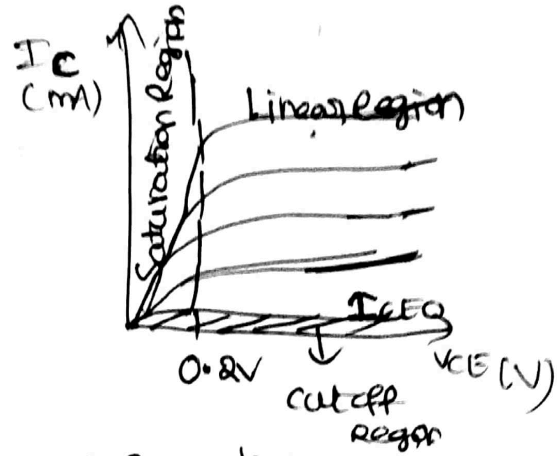


⇒ There are three Regions of operation in output Characteristics of CE

ⓐ cutoff Region

ⓑ Saturation Region

ⓒ Linear Region



Cutoff Region:

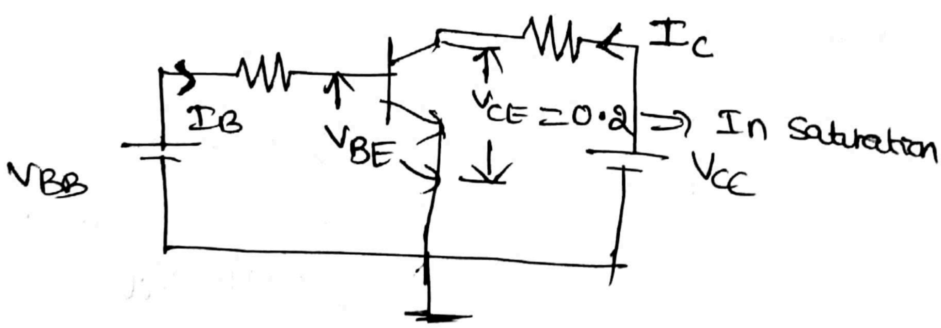
⇒ The Region below I_{CEO} (or) $I_B = 0$) is called cutoff Region because the Current is nearly Zero Amperes because of the Reverse Bias Condition of Emitter Base Junction & Collector Base Junction

⇒ The Region below $I_B = 0$ is cutoff Region, To get $I_B = 0$ we have to provide Reverse Bias at JE which leads to $\boxed{J_E, J_C = R \cdot B}$

Saturation Region:

⇒ The Region before $V_{CE} = 0.2V$ is called Saturation Region, Becoz Both the Junctions are in Forward Bias condition

In CE $J_E = F \cdot B$, $J_C = R \cdot B$



$V_{BE} = F \cdot B$ & $V_{CE} = 0.2$ across J_C which is very negligible R.B Voltage

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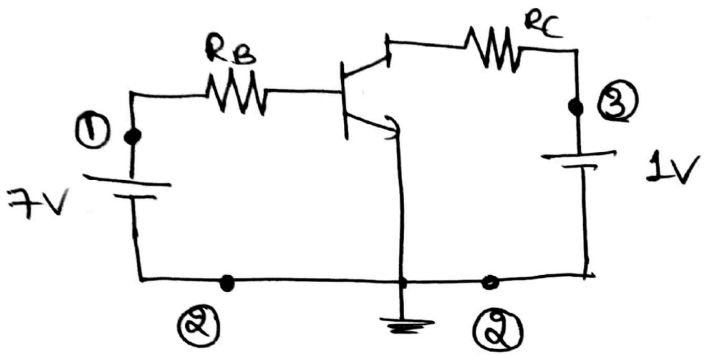
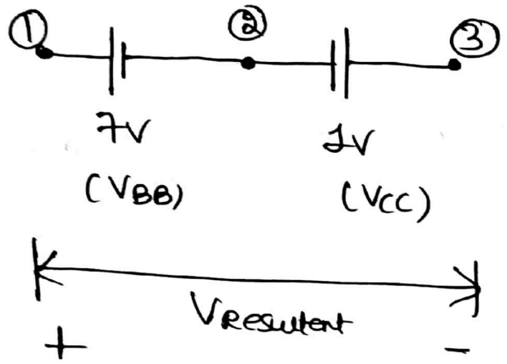
For suppose $V_{BE} = 5V$ (To give $V_{BE}=5V$, V_{BB} must be $> 5V$)

So let us assume $V_{BB} = 7V$ & to provide $V_{CE} = 0.2\,V$

V_{CC} must be > 0.2, so consider $V_{CE} = 1V$ (or) around $1V$





$$-V_{Resultant} + 7V - 1V = 0$$

$V_{Resultant} = 6V \simeq 7V$ (V_{BB} is dominating V_{CC})

$\Rightarrow$ V_{BB} is dominating $\Rightarrow V_{CE}$ (when its very small only) then it seems that V_{BB} is Present at "J_C" which is a Forward Bias condition so Both J_E & J_C Forward Biased

So the Region behind $0.2V$ is Saturation Region

($0.2V$ is the Practically observed value obtained from V-I c/s)

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$V_{CE(sat)} = 0.2V \Rightarrow$ For silicon

$V_{CE(sat)} = 0.1V \Rightarrow$ For Germanium

The condition for saturation is

$$\boxed{I_{B(min)} \geq \frac{I_C}{\beta}}$$

In Linear Region (or) Active Region the equation $I_C = \beta I_B$

~~is~~ i.e I_C is greter than "I_B" (or) equal to I_B

since $I_C = \beta I_B + I_{CEO}$

$$I_C \geq \beta I_B$$

But In saturation Region that condition will become

Reverse ie $I_C \leq \beta I_B$ (where $I_B = (I_B)min$)

$$\Rightarrow I_C \leq \beta I_{B(min)}$$

$$\boxed{I_{B(min)} \geq \frac{I_C}{\beta}} \Rightarrow \text{Saturation Region condition}$$

Linear Region (or) Active Region:-

⇒ The Region after 0.2V is a Linear Region. It is called Linear Region because output (I_C) varies linearly in accordance with the input (I_B)

As we are ↑ I_B, I_C ↑ linearly with a slope called β (or) gain

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

⇓

($I_C = \beta I_B$

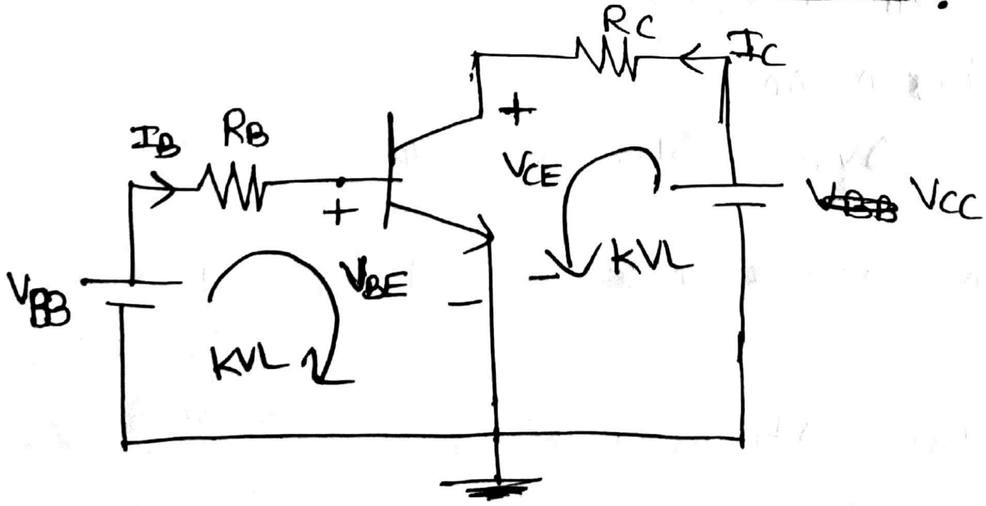
$y = mx$ form)

⇒ we are also calling this Region as Active Region because the transistor acts as an Amplifier in this Region

☆☆☆☆ VIMP

How the transistor acts as an Amplifier?

⇒

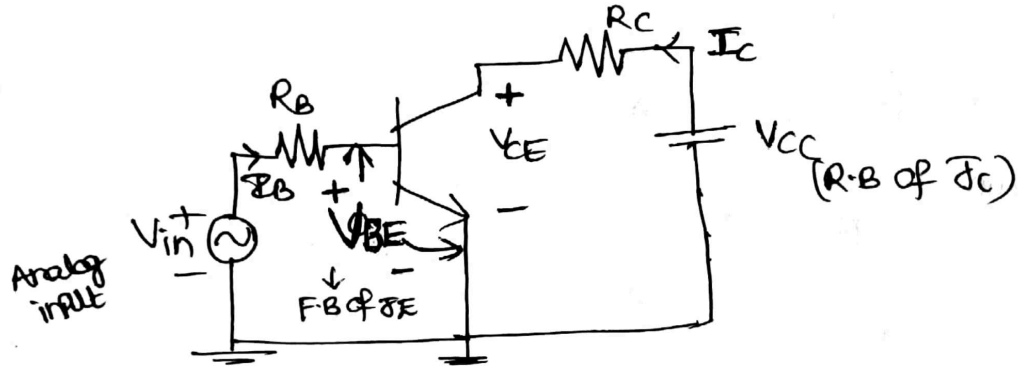


⟹ This is the Common Emitter Amplifier with "DC" Voltages (Biasing)

⇒ But Amplifier is the one which amplifies the Analog input (Human voice, music etc,,,.) ⇒ DC is not an input, it is just a Biasing voltage which is used to set the Q-point. (V_{CE}, I_C) to make the transister to acts as an Amplifier.

⇒ Amplifier Amplifies the input Analog signal, so the input to be given is Analog input which is applied across the Emitter & Base terminals for common emitter configuration.

⇒



Apply KVL at i/p side

$$-V_{in} + I_B R_B + V_{BE} = 0$$

$$V_{in} = I_B R_B + V_{BE}$$

Change in Vin

$$\Delta V_{in} = \Delta I_B R_B + \Delta V_{BE}$$

V_{BE} = Base to emitter DC Voltage to overcome Barrier Potential = 0.7V (F.B of J_E)

$$\Delta V_{in} = \Delta I_B R_B + \Delta(0.7)$$

$$\Delta V_{in} = \Delta I_B R_B + 0V$$

$$\Delta V_{in} = \Delta I_B R_B$$

$$\Delta V_{in} = \Delta I_B R_B \rightarrow (A)$$

Apply KVL at output side

$$-V_{CC} + I_C R_C + V_{CE} = 0$$

$$V_{CC} = I_C R_C + V_{CE}.$$

V_{CE} = output voltage measured $= V_0$

$$\Delta V_{CC} = \Delta I_C R_C + \Delta V_{CE}$$

$$0 = \Delta I_C R_C + \Delta V_{CE}$$

$$\Delta V_{CE} = -\Delta I_C R_C$$

(or)

$$\Delta V_0 = -\Delta I_C R_C \rightarrow (B)$$

$$\frac{(B)}{(A)} = \frac{\Delta V_0}{\Delta V_{in}} = \frac{-\Delta I_C R_C}{\Delta I_B R_B}$$

$$\Rightarrow A_V = \text{Voltage gain} = \frac{\Delta V_0}{\Delta V_{in}} = -\frac{\Delta I_C R_C}{\Delta I_B R_B}$$

So, $\boxed{A_V = -\beta \frac{R_C}{R_B}}$

$$\left(\because \beta = \frac{I_C}{I_B} \text{ (or) } \frac{\Delta I_C}{\Delta I_B}\right.$$

$$\frac{\Delta V_0}{\Delta V_{in}} = -\beta \frac{R_C}{R_B}$$

$$\boxed{\Delta V_0 = \left(-\beta \frac{R_C}{R_B}\right) \Delta V_{in}}$$

$\Rightarrow$ o/p varies linearly with respect to input in linear region, ie when J_E = F.B

J_C = R.B

$\Delta V_o \Rightarrow$ change in output

$\Delta V_{in} \Rightarrow$ change in input

output is 180° phaseshift with input → gain ⇒ so amplified output

$$\boxed{\Delta V_o = \left(-\beta \frac{R_C}{R_B}\right) \Delta V_{in}} \rightarrow \text{(C)}$$

180° phase shift

Why CE Amplifier is having 180° phase shift:

$$\Delta V_o = -\beta \frac{R_C}{R_B} \Delta V_{in}$$

The output of the amplifier ΔV_o is out of phase from the above equation.

we know than the gain ~~β ≈ 99 to 100~~ $\beta \simeq 50-200$

(For high frequency low power BJT $\beta \simeq 1000$)

∴ (wkt $\alpha = 0.98$

$$\beta = \frac{\alpha}{1-\alpha} \Rightarrow \frac{0.98}{1-0.98} \Rightarrow \frac{0.98}{0.02} \Rightarrow 49 \simeq 50$$

So From eq (C)

$$\Delta V_o = \underbrace{-50}_{\text{(minimum } \beta)} \times \frac{R_C}{R_B} \Delta V_{in}$$

$$\text{Voltage Gain } A_v = \frac{\Delta V_o}{\Delta V_{in}} = -50 \times \frac{R_C}{R_B}$$

$$Gain = A_V = -50 \times \frac{R_C}{R_B}$$

* gain with 180° phase shift has been produced in CE Amplifier. Hence CE Amplifier acts as an Amplifier

⇒ Similarly ~~~~ CB & CC also acts as amplifiers

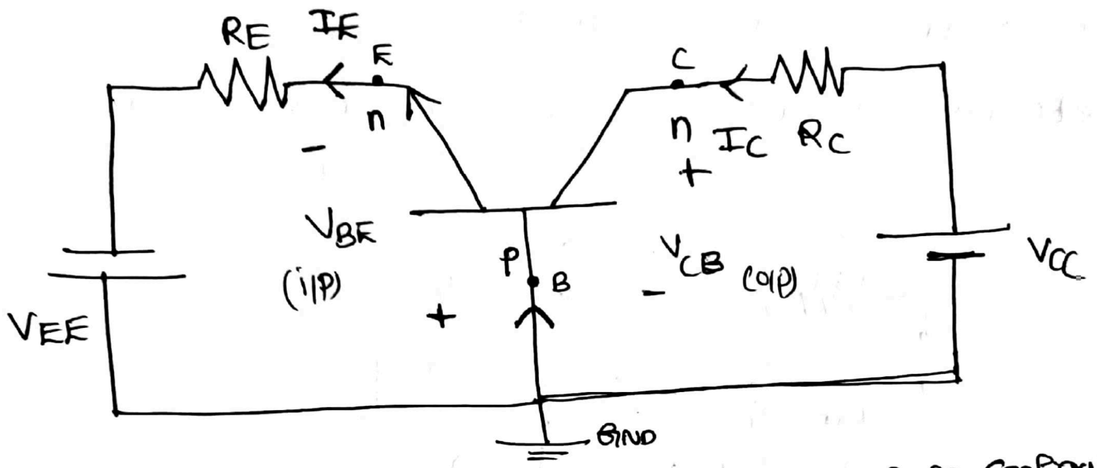
Common Base $\xrightarrow{\text{acts as}}$ Voltage Amplifier

Common emitter ⟹ Power Amplifier

Common collector ⟹ Current Amplifier
★ (Emitter follower)

Common Base configurations-

Base is common to Both i/p & o/p, so called common Base Configuration



Fig@ Common Base Configuration ckt

⇒ RE = input Resistance , RC = O/P Resistance

⇒ Base is grounded & is common to Both Emitter (i/p), Collector (o/p).

⇒ From KCL for the above CKt

$$\boxed{I_E = I_B + I_C}$$

⇒ The gain (or) DC gain of the ckt configuration is "α"

$$\alpha = \frac{\text{output of the collector ie } (I_{PC})}{\text{input current } I_E}$$

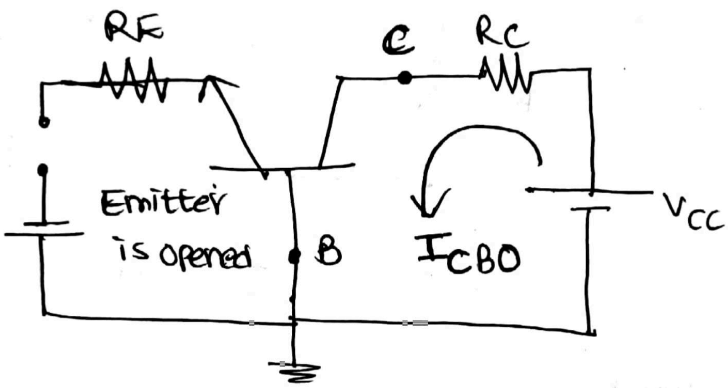
$$\boxed{\alpha = \frac{I_{PC}}{I_E} \quad \text{(or)} \quad \alpha \simeq \frac{I_C}{I_E} \quad \text{(or)} \quad \frac{\Delta I_C}{\Delta I_E}}$$

wkt

$$I_C = I_{PC} + I_{CO}$$

$$I_C = \alpha I_E + I_{CO} \quad \left(\text{since } \frac{I_{PC}}{I_E} = \alpha\right)$$

I_{CO} :- Reverse saturation current, which is measured in between Collector & Base, when Emitter is opened ($\downarrow$ ci/p)

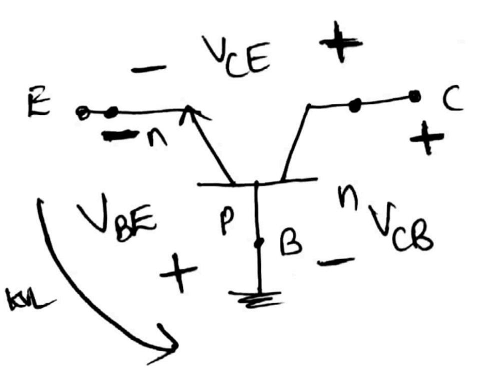


$$I_C = I_{CO} = I_{CBO}$$ | when $I_E = 0$, emitter is opened

when we will input I_E, the output current equation is

$$\boxed{I_C = \alpha I_E + I_{CBO}}$$

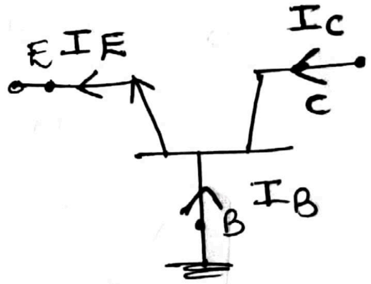
KVL in CB



$$-V_{BE} - V_{CB} + V_{CE} = 0$$

$$\boxed{V_{CE} = V_{BE} + V_{CB}}$$

KCL in CB



$$\boxed{I_E = I_B + I_C}$$

VI characteristics of CB Amplifier:

h-parameters for CB Amplifier is

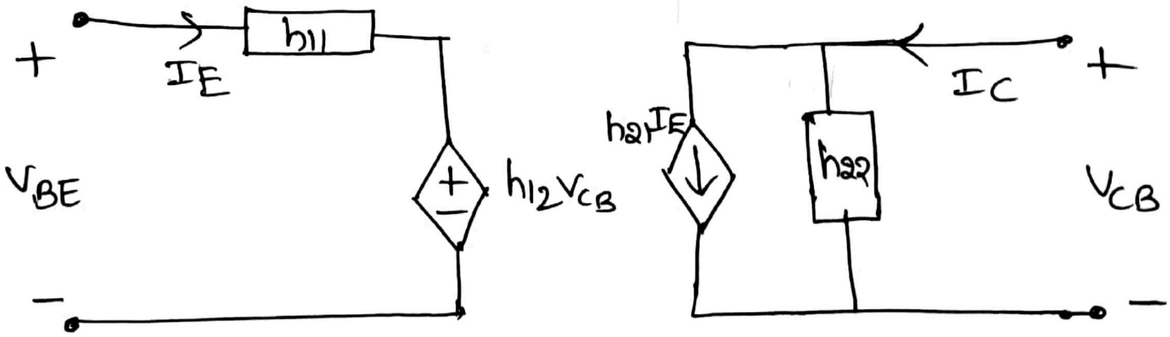
$V_1 = h_{11} I_1 + h_{12} V_2$ $\qquad$ V_1, V_2 = i/p & o/p voltage

$I_2 = h_{21} I_1 + h_{22} V_2$ $\qquad$ I_1, I_2 = i/p & o/p currents

$V_1 = V_{BE}$, $V_2 = V_{CB}$: $I_1 = I_E$, $I_2 = I_C$

so

$$\boxed{\begin{aligned} V_{BE} &= h_{11} I_E + h_{12} V_{CB} \\ I_C &= h_{21} I_E + h_{22} V_{CB} \end{aligned}}$$



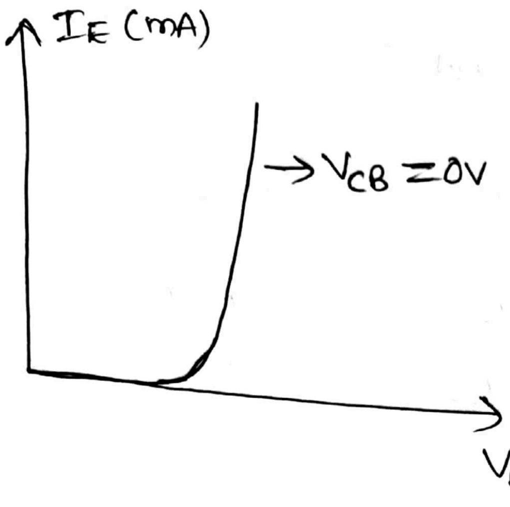
Input V-I Characteristics of ~~Ba~~ CB Configuration:

Graph between V_{BE} and I_E when V_{CB} is constant

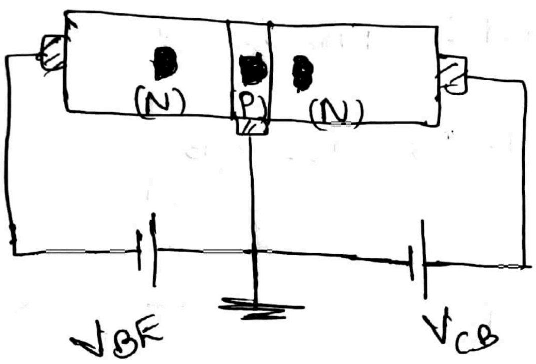
$V_{BE} = h_{11} I_E + h_{12} V_{CB}$ constant

Case(i) when $V_{CB} = 0V$

I_E varies with V_{BE} same as in PN Diode after 0.7V



Case(ii) :- when $V_{CB} = 1V, 10V$ - - -



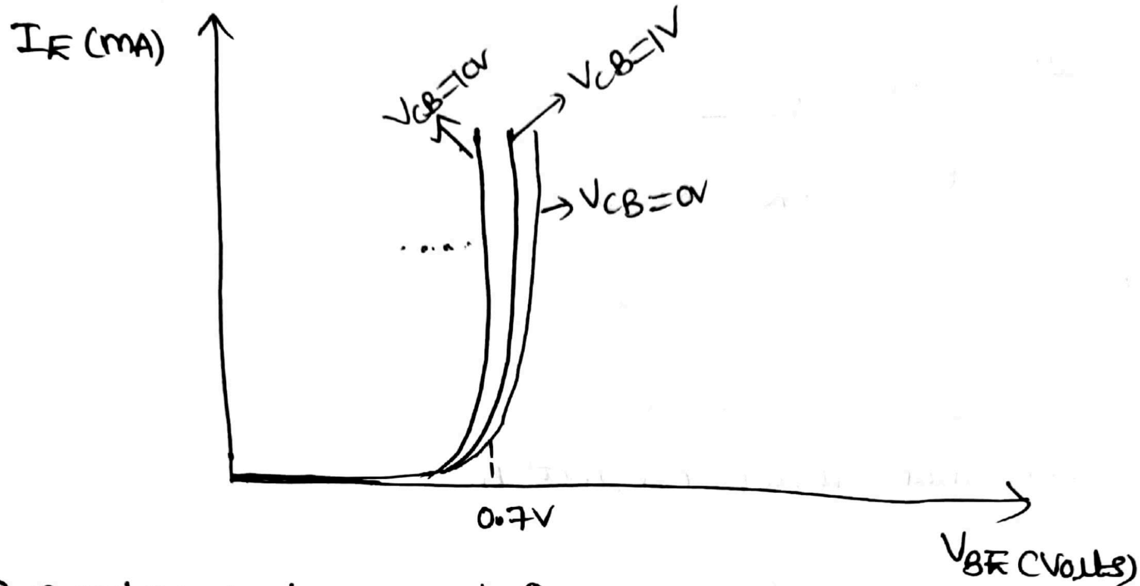
⇒ when V_{CB} is given a non-zero value, then the Reverse Bias across the Collector Base Junction increases, then width of the depletion Region increases which causes reduction in Base width

⇒ The Recombination current ⇓ because of the reduction in Base width, ie the concentration of "Charge carriers in Base Region ⇓" so Charge flow in Base Region w.r.to time ⇓ then I_B ⇓.

★★ The concentration of charge carriers ⇑, compared to in high width of Base, Before early effect, Because of the reduction in Base width, the base allows less no of charge carriers than earlier so the more charge carriers remained in emitter Region which causes the increase in current in emitter Region (I_E ⇑)

⇒ when V_{CB} ⇑, Depletion Region width ⇑, Effective Base width ⇓

I_B ⇓ then I_E ⇑



Parameters to be obtained from i/p c/s

$$\frac{V_{BE}}{I_E} = h_{11} = R_i = \text{Input Resistance}$$

$$\frac{V_{BE}}{V_{CB}} = h_{12} = \text{Reverse voltage gain}$$

Output VI characteristics of CB configuration:

The output V-I c/s will be obtained when input current I_E is constant

$$I_C = h_{21} \underbrace{I_E}_{\text{input current constant.}} + h_{22} \cdot V_{CB}$$

output characteristics are drawn between output voltage & output current.

$$\boxed{I_C = \alpha I_E + I_{CBO}} \rightarrow (A)$$ output current equation of CB Amplifier

Case(i) :- when $I_E = 0$

$$I_C = \alpha I_E + I_{CBO}$$

$$I_E = 0, \quad I_C = 0 + I_{CBO}$$

$$\boxed{I_C = I_{CBO}}$$

From common emitter configuration

$$I_C = \beta I_B + I_{CEO}$$

$$I_C = \beta I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$$

$$I_{CEO} = \frac{1}{(1-\alpha)} (I_{CBO})$$

$$\boxed{I_{CEO} = (1+\beta) I_{CBO}}$$

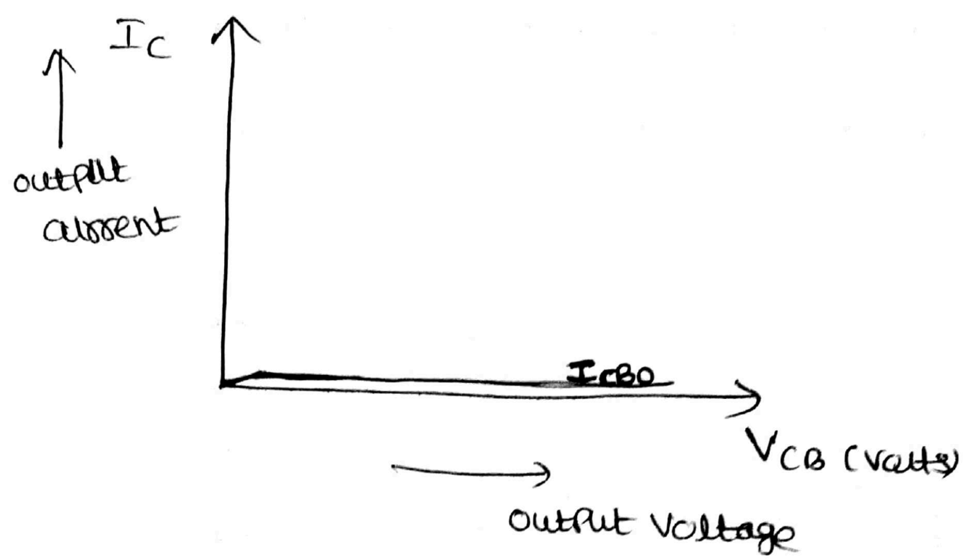
where $\frac{1}{1-\alpha} = 1+\beta = 1 + \frac{\alpha}{1-\alpha} = \frac{1-\cancel{\alpha}+\cancel{\alpha}}{1-\alpha} = \frac{1}{1-\alpha}$

$$\boxed{I_{CEO} = (1+\beta) I_{CBO}} \rightarrow \text{In CE}$$

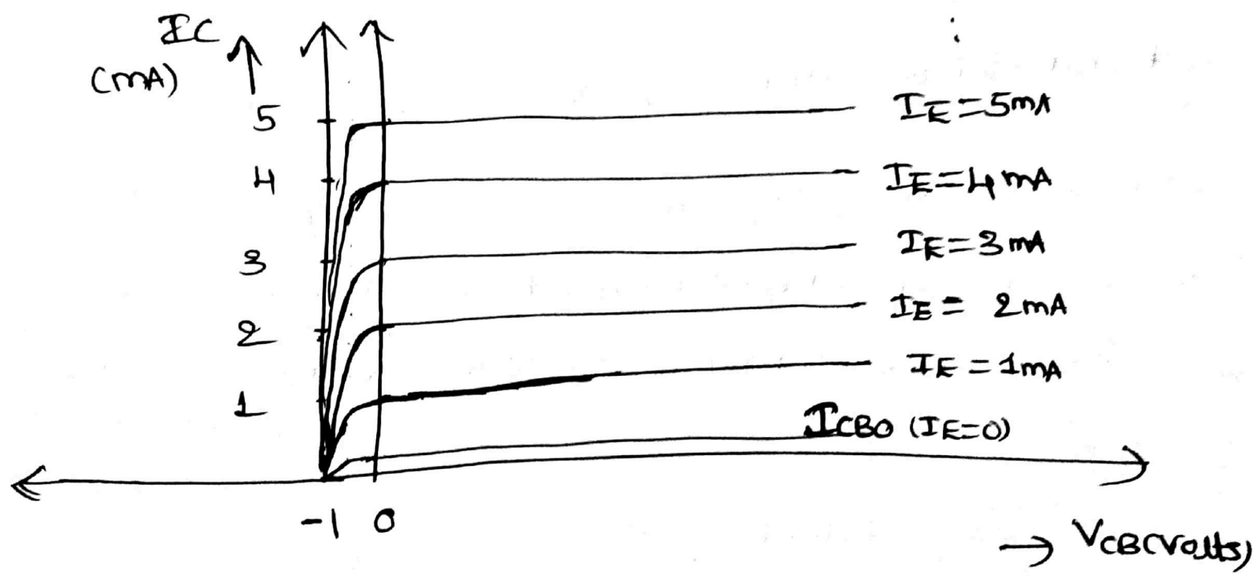
so

$$\boxed{I_{CEO} >> I_{CBO}}$$ Reverse saturation current in CE is greater than CB

SO $I_{CBO} << I_{CEO}$



Case(ii) when $I_E \neq 0$, 1mA, 2mA ----

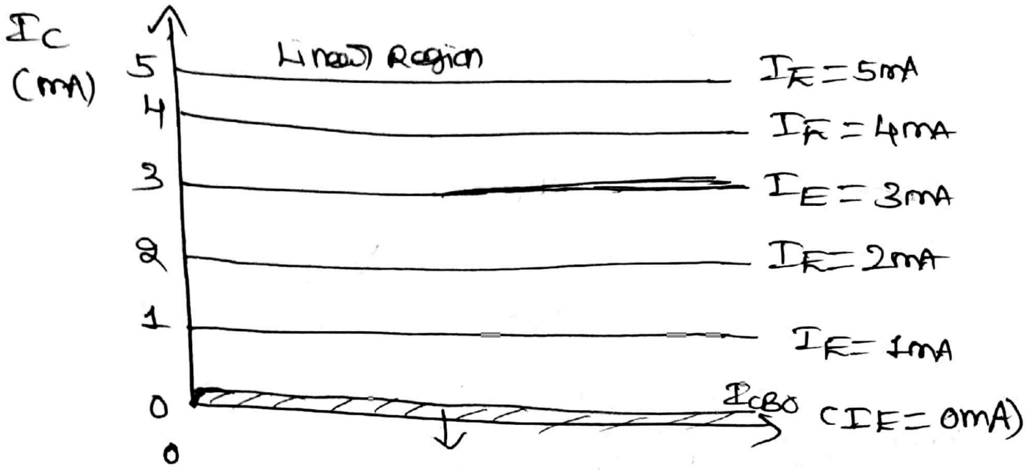


⇒ when I_E is a non zero value, the collecter current Varies Linearly with "I_E", because the gain "α" in common Base configuration is almost 1 (or) 0.995 to 0.998 Practically ie

$$\alpha \simeq 1 \quad (or) \quad \alpha = 0.995 - 0.998$$

SO $\boxed{I_C \cong I_E}$

⇒ As α is almost "1" I_C is almost equal to "I_E" when it is operated in Active mode (Fwd active mode :- J_E :- F-B, J_C :- R-B)

⇒ 

Output characteristics when $-1 < V_{CB} < 0V$? :-

⇒ when V_{CB} = -ve value, the J_C ⇒ Collector Base Junction is also in Forward Biased condition, we know that the J_E ⇒ Emitter Base Junction is already in Forward Bias condition so, now

J_E = Forward Bias

J_C = Forward Bias

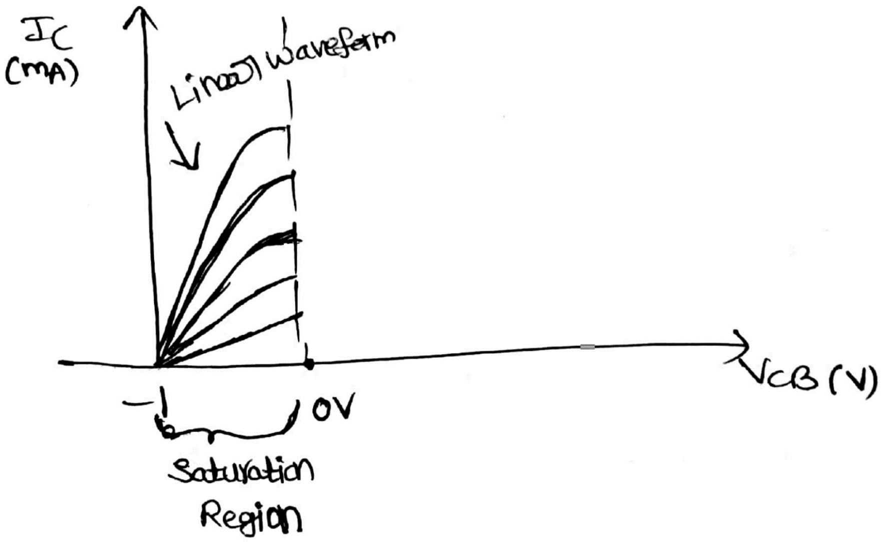
If Both the Junctions are in Forward Bias condition, then the collector current I_C is not a function of I_E

$$\boxed{I_C \neq f(I_E)}$$

In saturation Region I_C & I_E varies Independently

⇒ I_C varies linearly with V_{CB} and I_E varies linearly with V_{BE}, But the variations are not dependent

so In O/P V-I characteristics, I_C varies linearly with V_{CB} But does not depend on "I_E"



⇒ Regions of operation:-

cutoff Region:-

⇒ The Region below $I_E = 0mA$ is called cutt-off Region

⇒ To get $I_E = 0mA$ $V_{BE} = 0V$, which makes the emitter base junction Reverse Bias. As we already know that J_C is in Reverse bias condition, so Both the junctions are in Reverse Bias condition and the transister is said to be in cutoff Region

Saturation Region:-

⇒ The J_E is already in F.B condition, If we apply V_{CB} -ve, then J_E is in F.B

⇒ we know that, we are operating the transistor in Forward active mode to make it to act as a transistor so J_E is in Forward Bias condition and If V_{CB} is -ve ie $V_{CB} < 0V$, then J_C is also in Forward Bias condition

⇒ when Both the Junctions are in Forward Bias Condition, then the transistor is said to be in Saturation Region.

Active Region:

⇒ when ~~Both~~ $J_E = F.B$, $J_C = R.B$, then the transistor acts as an Amplifier and the Region of operation is Active Region (or) Linear Region

⇒ In this Region input current (I_E) and output current (I_C) are in Linear Relation ie output current (I_C) varies Linearly with input current (I_E) with a slope "α" also called gain

$$I_C = f(I_E)$$

$$\boxed{I_C \simeq \alpha I_E} \Rightarrow \boxed{y = mx} \text{ form}$$

$y = o/p$, $m = $ slope, $x = $ input

Linear Region means, the Region where output current varies Linearly with input current. Then we can use the transistor as an Amplifier in this Region

⇒ The lines in Active Region, ie the output V-I c/s of CB

c/s in Active Region are STRAIGHT LINES, because the gain α is not high, it is almost equal to "1", so we will get straight lines.

But in CE configuration, the V-I c/s of CE amplifier are not straight lines because of the gain $\beta = \frac{I_C}{I_B}$, since "β" is high, the lines are not stright lines ⇒ β is 50 to 400 and α is 0.995 to 0.998 practically

NOTE:

⇒ $\boxed{\text{h- Parameters are Valid in Active Region (or) Linear Region only.}}$

TRANSISTOR BIASING:

- The basic function of a transistor is to do amplification. The process of raising the strength of a weak signal without any change in its shape is known as faithful amplification.
- The proper maintenance of zero signal collector current (I_{CQ}) and collector-emitter voltage (V_{CEQ}) in transistor circuit during the passage of AC signal is considered as 'biasing'.
- When a transistor is not properly biased, it provides unfaithful amplification and produces distortion in the output signal.
- In order to produce distortion-free output in amplifier circuits, the supply voltages and the passive elements in the circuit must be suitably chosen.
- The supply voltage and resistances in a transistor biasing circuit establish a set of DC voltage V_{CEQ} and current I_{CQ} to operate the transistor at a desired point called operating point or Quiescent point or Q-point in the active region.

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Requirements of Biasing

1. **Active region of operation**

   → FB at J_E

   → RB at J_C

2. **Operating point (Q-pt) establishment**

   Q-Point:

   A point in the active region at which, a BJT provides faithful amplification against the weak input signal applied and delivers undistorted output signal is called as operating point or Quiescent point or Q point.

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Note 2: In an amplifier circuit, if the operating point is established near to the cut off region (Q_2 in fig.6) some portion of the amplified output signal will be clipped off in the negative half cycle i.e certain amount of information may be lost in the output signal.

Note 3: In an amplifier circuit if the operating point is established at the middle of DC load line or at the centre of active region (Q in fig.6), the amplifier provides faithful amplification against the small or weak AC input signal applied and delivers undistorted output signal.

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signal.

3. Q-point Stability:

There are two factors which are responsible for the instability of operating point. They are:

- The transistor parameters are temperature dependent.
- When a transistor is replaced by another transistor of same type, there is a wide spread in the values of transistor parameters due to manufacturing errors.

Therefore stabilization of the Q-point is necessary against

(a) Variations of minority carrier current, I_{CO} with temperature ($I_C \rightarrow I_{co} \rightarrow$ Minority carrier concentration $\rightarrow$ Temp).

(b) Variations of β in case of replacement of transistors ($I_c \rightarrow \beta \rightarrow \alpha \rightarrow$ Base width $\rightarrow$ manufacturing errors).

(c) Variations of junction voltage of the transistor, V_{BE} with temperature ($I_c \rightarrow I_B \rightarrow V_{BE} \rightarrow$ Temp).

Temperature dependence of I_C:

- The instability of I_C is principally caused by the following three sources:
- The I_{CO} doubles for every $10^{\circ}C$ rise in temperature.
- Increase of β with increase of temperature.
- The V_{BE} decreases about 2.5mV per $^{\circ}C$ increase in temperature.

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4. Stability Factor:

It is the measure of the stability of operating point in a transistor amplifier circuit.

(a) Stability factor, S:

The variation of collector current with the variations in reverse saturation current I_{CO} in a BJT at constant β and V_{BE} is considered as stability factor, S.

$$S = \left(\frac{\partial I_c}{\partial I_{co}} \right) \text{ with } \beta \text{ and } V_{BE} \text{ Constant}$$

(b) Stability factor, S^1:

The variation of I_C with the variation in β at a constant I_{CO} and V_{BE} is considered as stability factor S^1.

$$S^1 = \left(\frac{\partial I_C}{\partial_\beta} \right) \text{ with } I_{CO} \text{ and } V_{BE} \text{ constant.}$$

(c) Stability factor S^{11} :

The variation of I_C with the variations in V_{BE} at a constant I_{CO} and β is considered as S^{11}.

$$S^{11} = \left(\frac{\partial I_C}{\partial V_{BE}} \right) \text{ with } I_{CO} \text{ and } \beta \text{ Constant.}$$

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Derivation of Stability Factor (S):

Consider the collector current equation of a BJT in CE configuration:

$I_c = \beta I_B + (1+\beta) I_{CO}$ -----------(1)

Differentiating equation (1) w.r.t. I_C

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta)\frac{\partial I_{CO}}{\partial I_c}$$

$$\frac{\partial I_{co}}{\partial I_c} = \frac{1-\beta\left(\frac{\partial I_b}{\partial I_c}\right)}{(1+\beta)}$$

$$\Rightarrow \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

$$\therefore S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\left[\frac{\partial I_B}{\partial I_C}\right]} ---(2)$$

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Biasing Circuits

1. Fixed Bias :

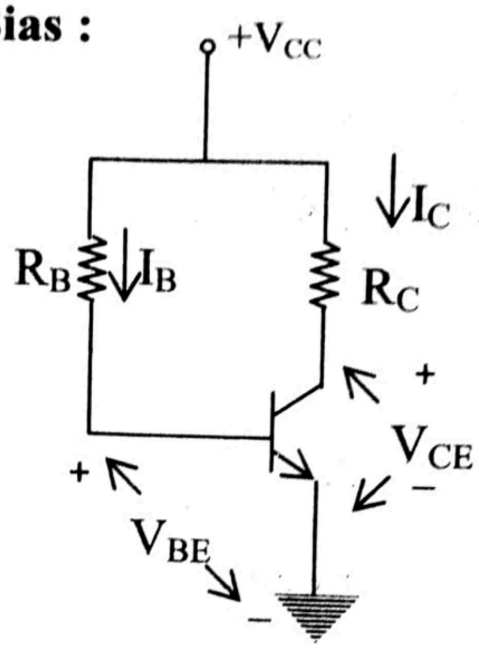

Figure.7

Q- Point establishment:

Step 1: KVL for input section

$$V_{cc} - I_B R_B - V_{BE} = 0 \quad \text{-----} \ (1)$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B} \quad \text{----------} \ (2)$$

$$\therefore I_{CQ} = \beta I_B = \beta \left[\frac{V_{cc} - V_{BE}}{R_B} \right] \text{-----} \ (3)$$

Step 2: KVL for output section

$$V_{CC} - I_C R_C - V_{CE} = 0 \ \text{--------} \ (4)$$

$$\therefore V_{CEQ} = V_{CC} - I_{CQ} R_C \ \text{--------} \ (5)$$

$$\therefore Q = \left[V_{CEQ} \quad I_{CQ} \right] \text{--------} \ (6)$$

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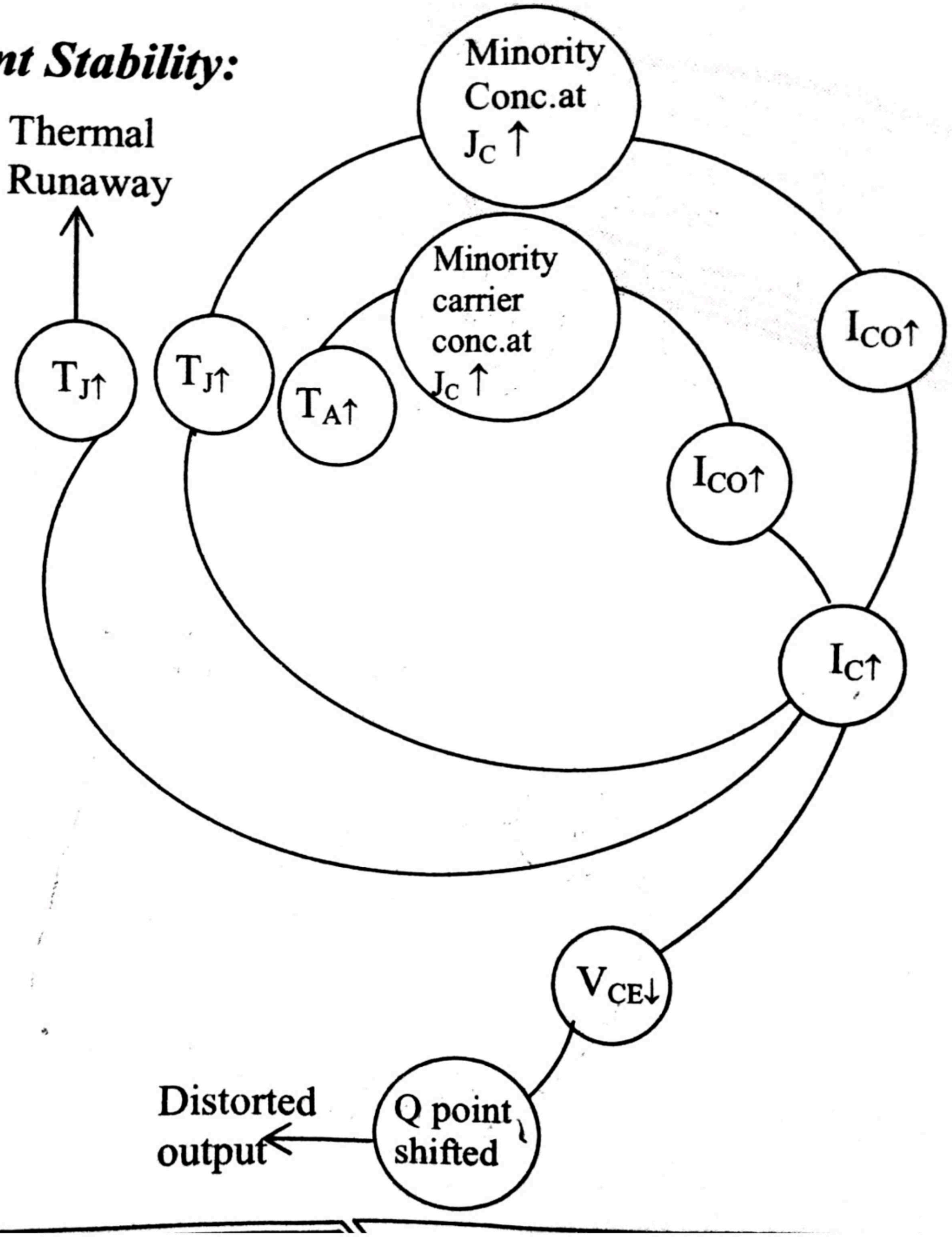
Q- point Stability:



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Stability factor, S:

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\left[\frac{\partial I_B}{\partial I_C}\right]} ---(1)$$

KVL for the input section of fig.7

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} ---(2)$$

$$\Rightarrow \frac{\partial I_B}{\partial I_C} = 0 ---(3)$$

$$\therefore S = 1+\beta \text{ -----(4)}$$

Draw backs:

- Operating point is unstable with the variations in temperature and β.
- Possibility of thermal runaway.

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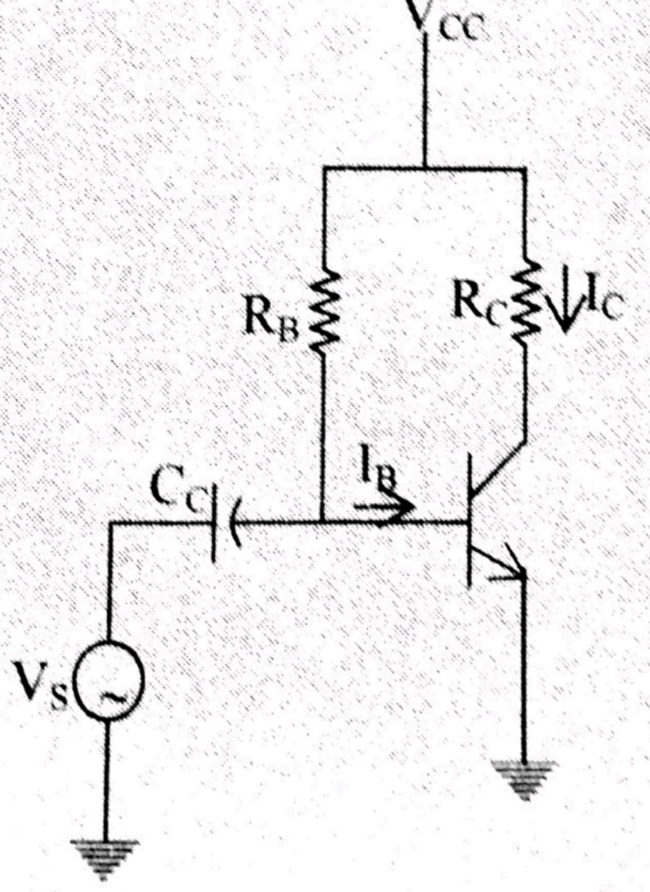
Example.1:

For the circuit shown below, find the value of R_B & R_C required to establish a Q- point of 6 V & 1mA.Given $V_{CC} = 12$ V,$\beta = 100$ $V_{BE} = 0.7$ V



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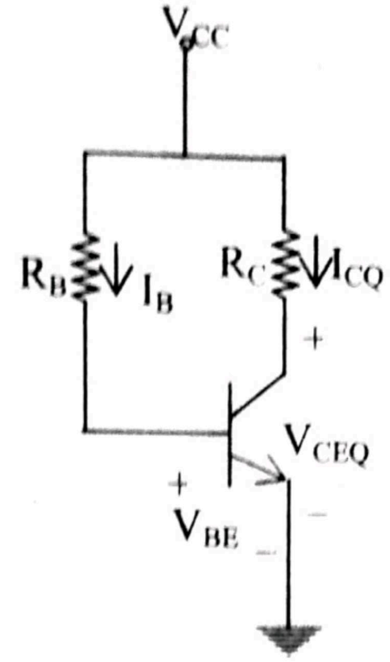
Sol: *Consider the DC equivalent of the given circuit*



Step.1: KVL to output loop:

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow R_C = (V_{CC} - V_{CE})/\ I_C = 6\ K\Omega$$

Step.2: $$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1x10^{-3}}{100} = 10\mu A$$

Step.3: Applying KVL to input loop

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_{BQ}}$$

$$= \frac{12 - 0.7}{10 x 10^{-6}}$$

$$= \frac{11.3}{10} x\ 10^6$$

$$\therefore R_B = 1.13\ M\Omega$$

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2. Collector-to- Base bias or Collector feedback bias

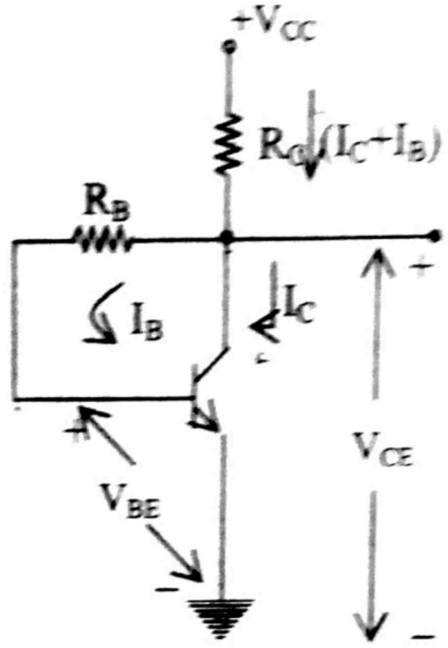

Figure.8

Q–point establishment:

Step1: KVL for the input,

$$V_{CC} - (I_C+I_B)R_C - I_BR_B - V_{BE} = 0 \quad ---(1)$$

$$V_{CC} - (1+\beta)I_BR_C - I_BR_B - V_{BE} = 0 \quad ---(2)$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C} \quad ---(3)$$

$$I_{CQ} = \beta\left[\frac{V_{CC} - V_{BE}}{R_B + (1+\beta)R_C}\right] \quad -----(4)$$

Step2: KVL for the output,

$$+V_{CC} - (I_C+I_B)R_C - V_{CE} = 0 \quad ----(5)$$

$$V_{CEQ} \approx V_{CC} - I_{CQ}R_C \quad ----(6)$$

$$\therefore Q = [V_{CEQ}, I_{CQ}] \quad -----(7)$$

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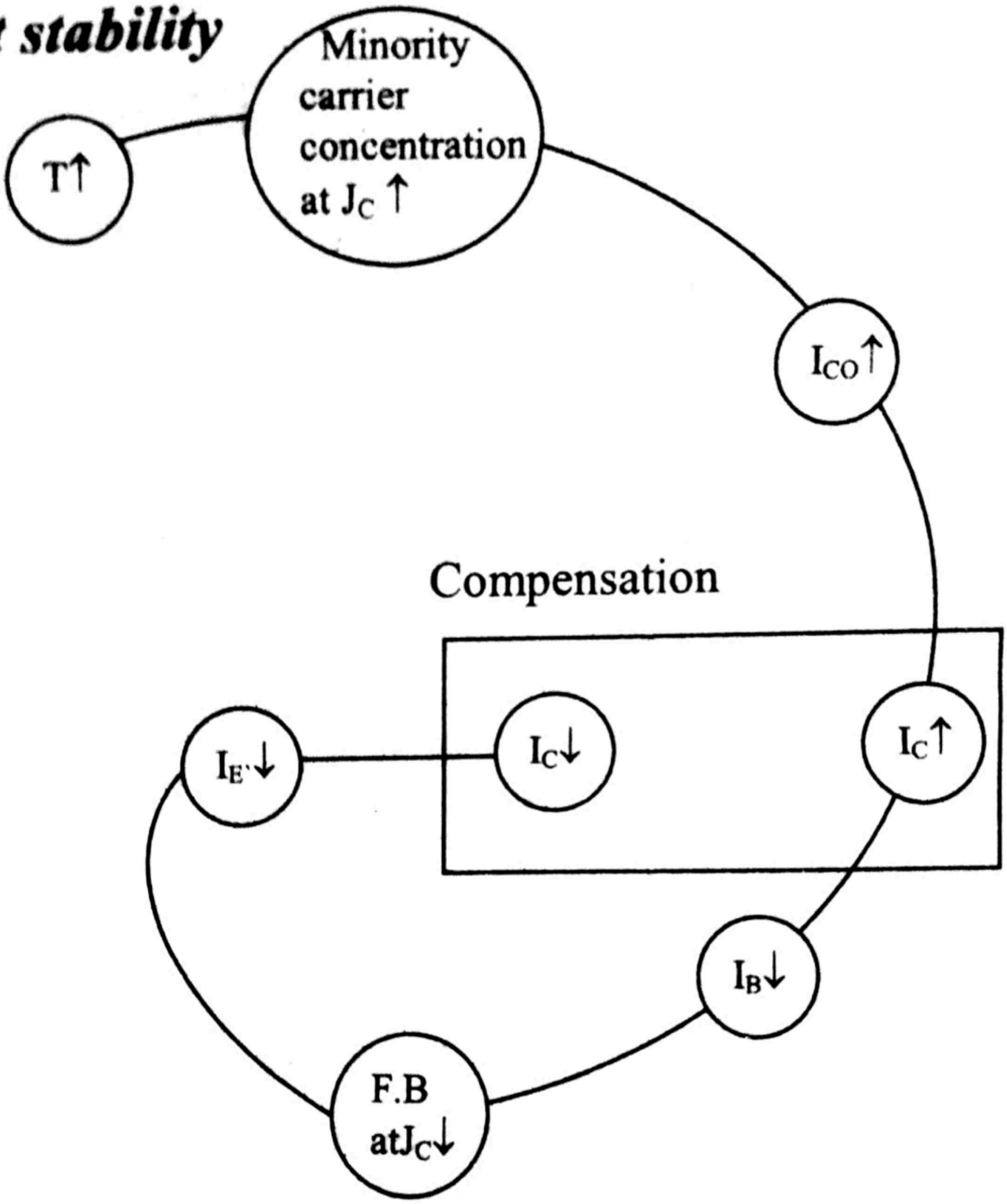
Q Point stability



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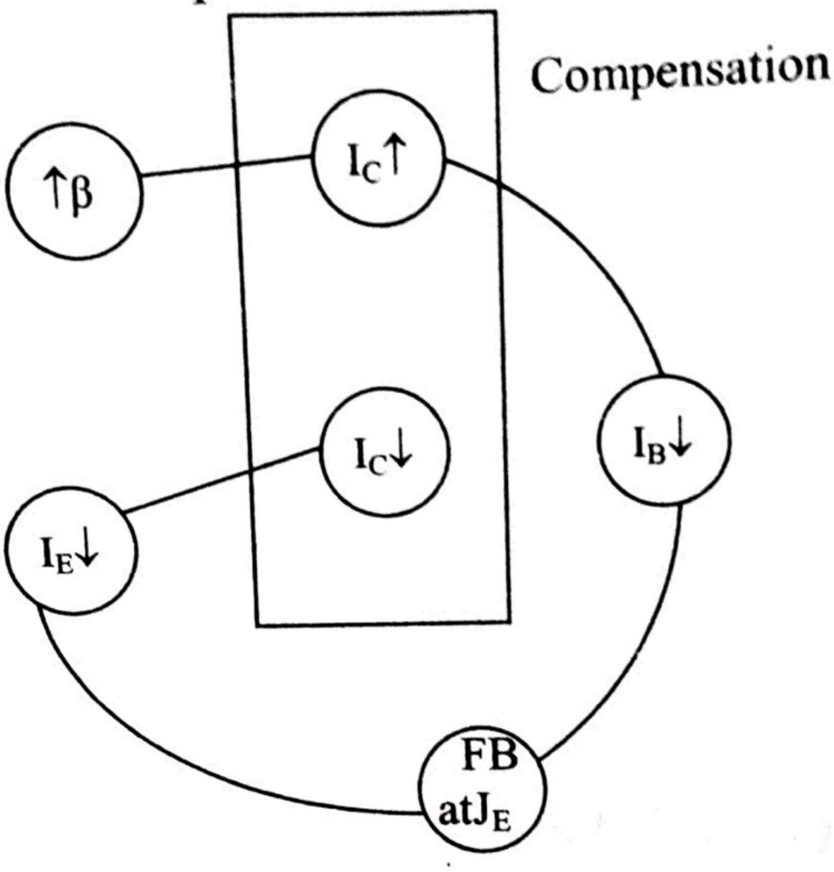
Note: The increase in I_C due to the increase in I_{CO} is compensated by the decrease in I_C due to the decrease in base current (I_B) of the circuit during the temperature variations.



Note: The increase in I_C due to increase in β of the transistor is compensated by the decrease in I_C due to the decrease in base current of the circuit.

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circuit.

Stability factor, S:

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\left[\dfrac{\partial I_B}{\partial I_C}\right]} ---(1)$$

KVL for the input section of fig.8

$$V_{CC}-(I_C+I_B)R_C-I_BR_B-V_{BE}=0----------(2)$$

$$\Rightarrow V_{CC}-I_CR_C-I_B(R_C+R_B)-V_{BE}=0---(3)$$

$$\Rightarrow I_B = \frac{V_{CC}-V_{BE}-I_CR_C}{R_C+R_B} ----------(4)$$

$$\Rightarrow \frac{\partial I_B}{\partial I_C} = \frac{-R_C}{R_C+R_B} -----(5)$$

$$\therefore S = \frac{1+\beta}{1+\beta\left(\dfrac{R_C}{R_C+R_B}\right)} ----(6)$$

Drawback:

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Drawback:

The resistor R_B connected between collector and base in a collector to base bias circuit, not only provides DC stabilization to the operating point

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but also causes AC negative feedback at the input section of the amplifier, which will in turn reduce the overall AC gain of the amplifier.

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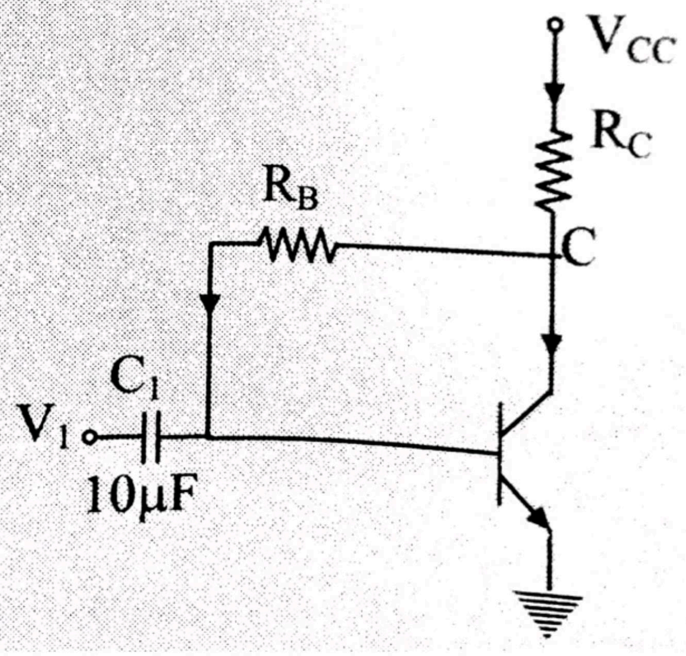
Example.2:

In a common emitter circuit an N-PN transistor having a value of $\beta = 50$ is used with $V_{CC} = 10V$ and $R_C = 2K\Omega$. If a $100K\Omega$ resistor is connected between collector and base and $V_{BE} = 0$, determine.

(i) the position of quiescent point and

(ii) stability factor S.



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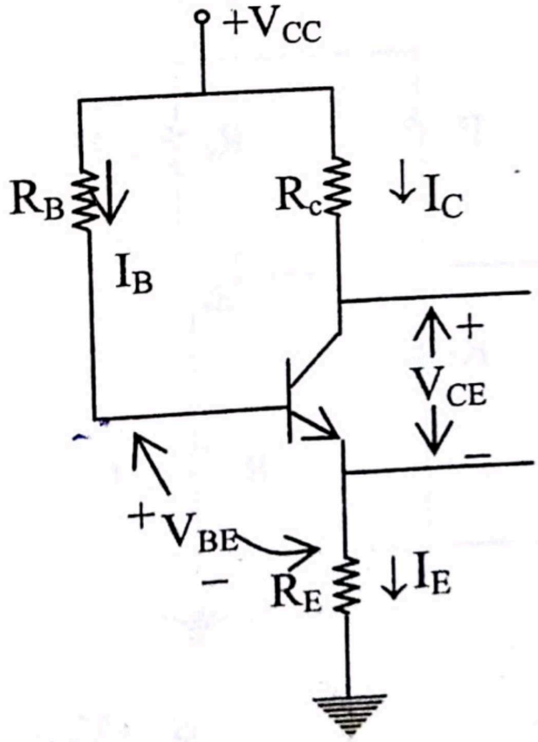
3. Fixed bias with emitter resistor or Emitter Bias



Q- Point Establishment:

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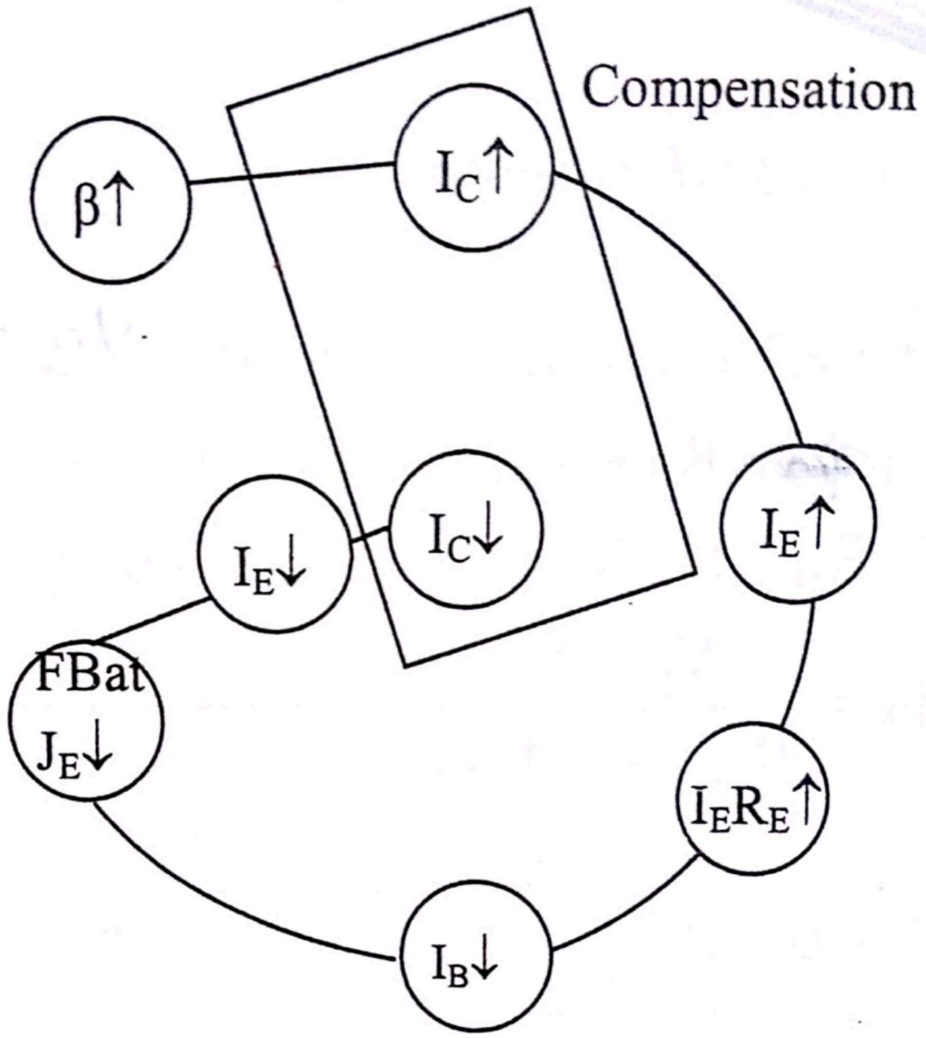
Q–Point stability:



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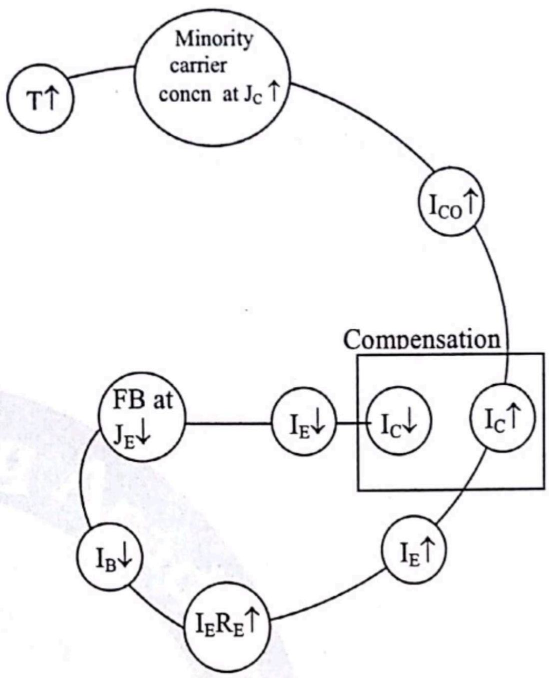
Emitter

Note: The increases in I_C due to the increase in β is compensated by the decrease in I_C due to the increase in $I_E R_E$



Note: The increase in I_C due to the increase in I_{CO} is compensated by the decrease in I_C due to the increase in voltage drop across R_E during the variations in temperature.

Stability Factor, S:

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\left[\dfrac{\partial I_B}{\partial I_C}\right]}$$

$I_E]$

KVL for the input section of fig.9

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \text{ --------------(1)}$$

$$\Rightarrow V_{CC} - I_B R_B - V_{BE} - I_C R_E - I_B R_E = 0 \text{ -----(2)}$$

[Since $I_E = I_C + I_B$]

on

$$\Rightarrow I_B = \frac{V_{cc} - V_{BE} - I_c R_E}{R_E + R_B} \text{ ------------------(3)}$$

$$\Rightarrow \frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_B + R_E} \text{ ------------------------(4)}$$

)

$$\therefore S = \frac{1+\beta}{1+\beta\left[\dfrac{R_E}{R_E + R_B}\right]} \text{ ---------------------(5)}$$

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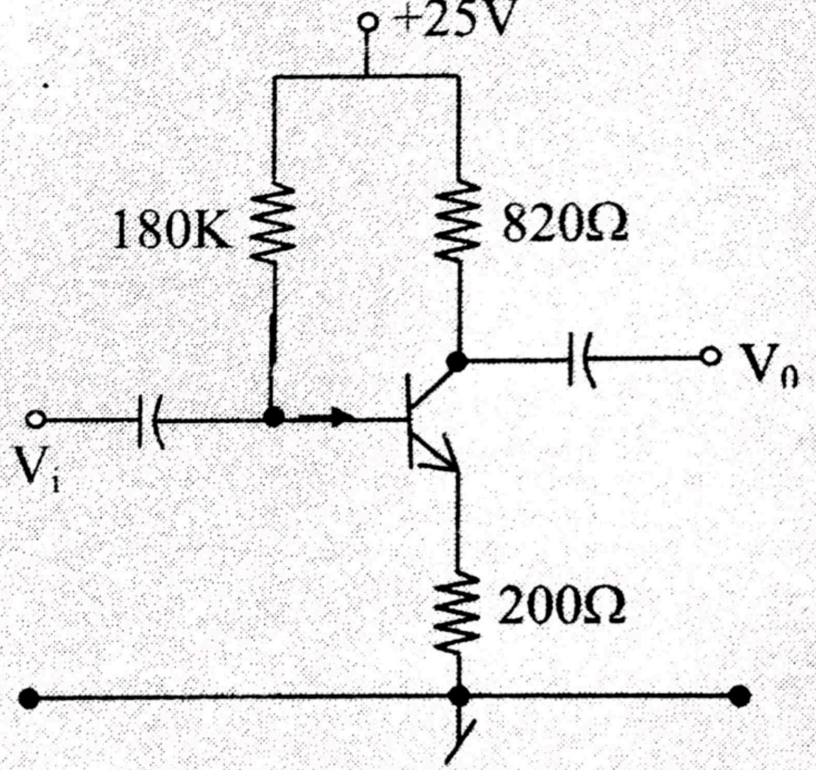
Example.3:

Find I_C and V_{CE} for the following circuit of $\beta = 80$ for BJT.



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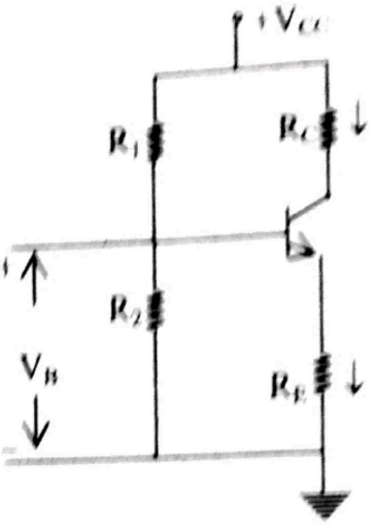
4. Voltage-divider bias or self-bias:



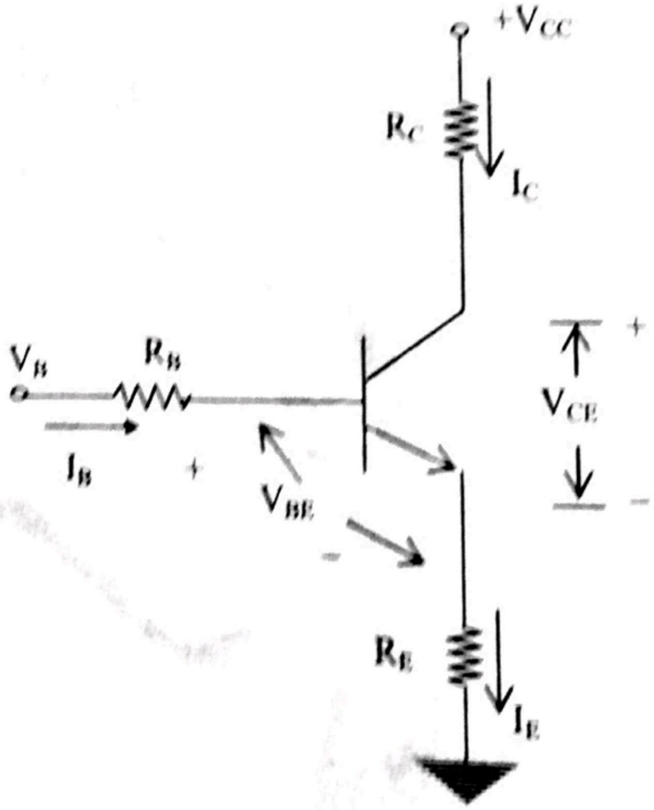


Figure.11: Thevenin equivalent of self-bias ckt

Where $V_B = V_{Th} = \dfrac{V_{CC}\ R_2}{R_1 + R_2}$

And $R_B = R_{Th} = \dfrac{R_1\ R_2}{R_1 + R_2}$

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Q- Point Establishment:

Step 1 : KVL for the I/P section $V_B - I_B R_B - V_{BE} - I_E R_E = 0$

$$V_B - I_B R_B - V_{BE} - I_E R_E = 0 \text{ ------ } (1)$$

$$I_B R_B - (1+\beta) I_B R_E = V_B + V_{BE} \text{ ---- } (2)$$

$$I_B = \frac{V_B + V_{BE}}{R_B + (1+\beta)R_E} \text{ ------------ } (3)$$

$$\therefore I_{CQ} = \beta \left[\frac{V_B + V_{BE}}{R_B + (1+\beta)R_E} \right] \text{ -------- } (4)$$

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Step 2: KVL for the O/P section

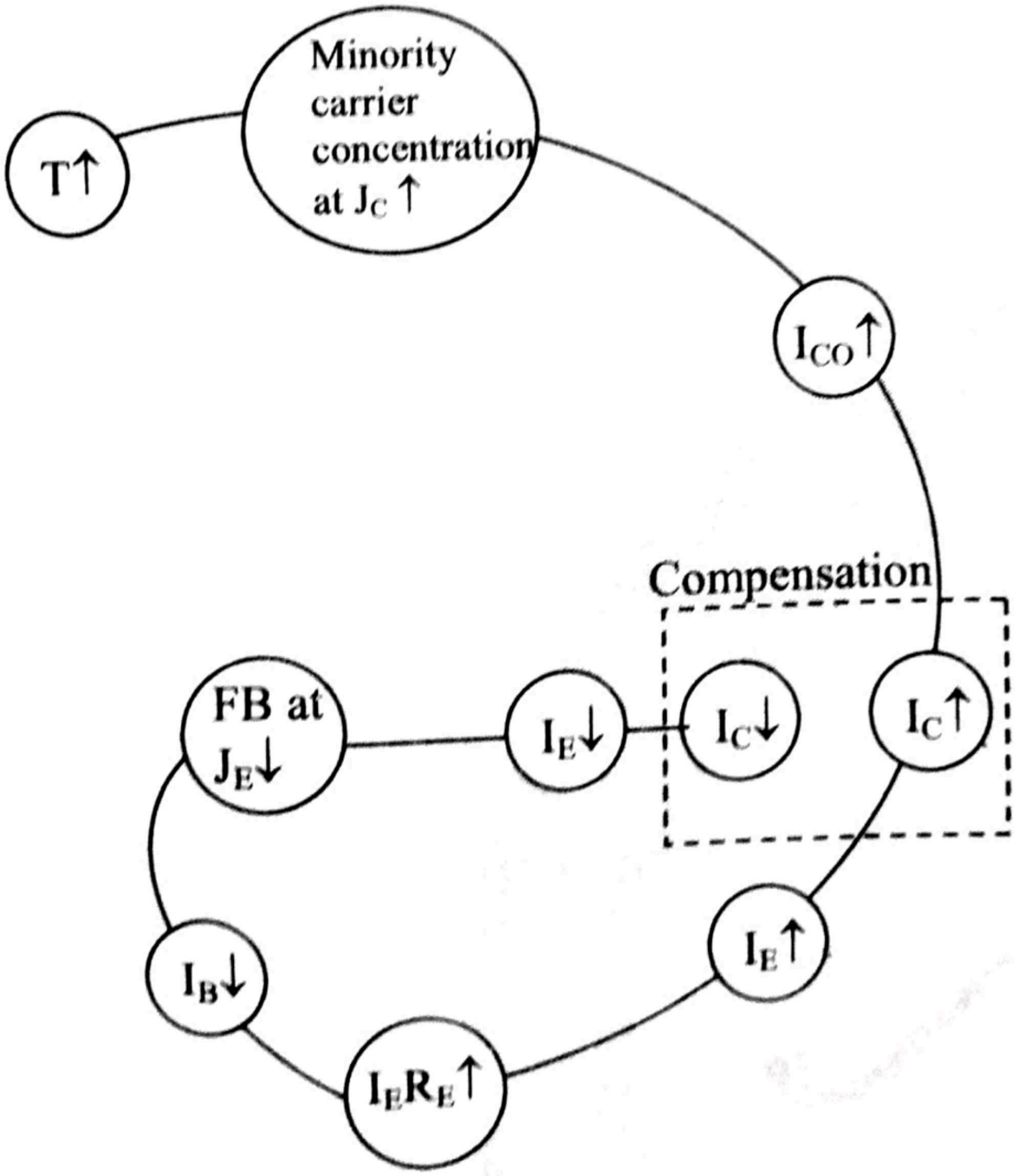
$$V_{CC} - I_C R_C - V_{CE} - R_E I_E \text{ ------------(5)}$$

$$\therefore V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E) \text{----- (6)}$$

$$\therefore Q = [V_{CEQ}, I_{CQ}] \text{ ---------------------(7)}$$

Q- Point stability:

(a)



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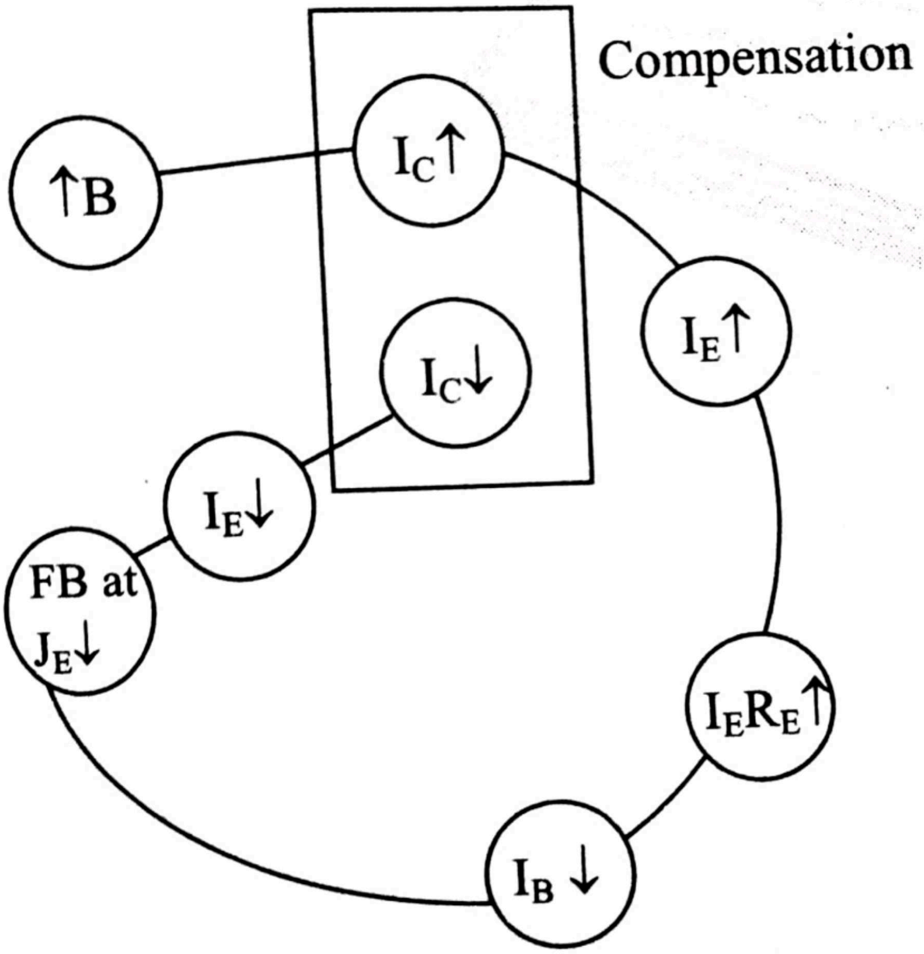
Note: The Increase in I_C Due to the increase in I_{CO} is compensated by the decrease in I_C due to increase in voltage drop across R_E during temperature variations.

b)



Note: The increase in I_C due to the increase in β is compensated by the decrease in I_C due to the increase in voltage drop across R_E.

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Stability Factor, S:

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\left[\frac{\partial I_B}{\partial I_C}\right]} \text{------------------(1)}$$

KVL for the input section of fig.11

$$V_B - I_B R_B - V_{BE} - I_E R_E = 0 \text{ -------------(2)}$$

$$V_B - I_B R_B - V_{BE} - I_C R_E - I_B R_E = 0 \text{ ----(3)}$$

$$I_B = \frac{V_B - V_{BE} - I_C R_E}{R_E + R_B} \text{------------------(4)}$$

$$\frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_E + R_B} \text{--------------------------(5)}$$

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E + R_B}\right)} \text{-----------------(6)}$$

Note: For the reasonable values of R_1, R_2 & R_E the Stability factor of a self bias circuit can be less than 10.

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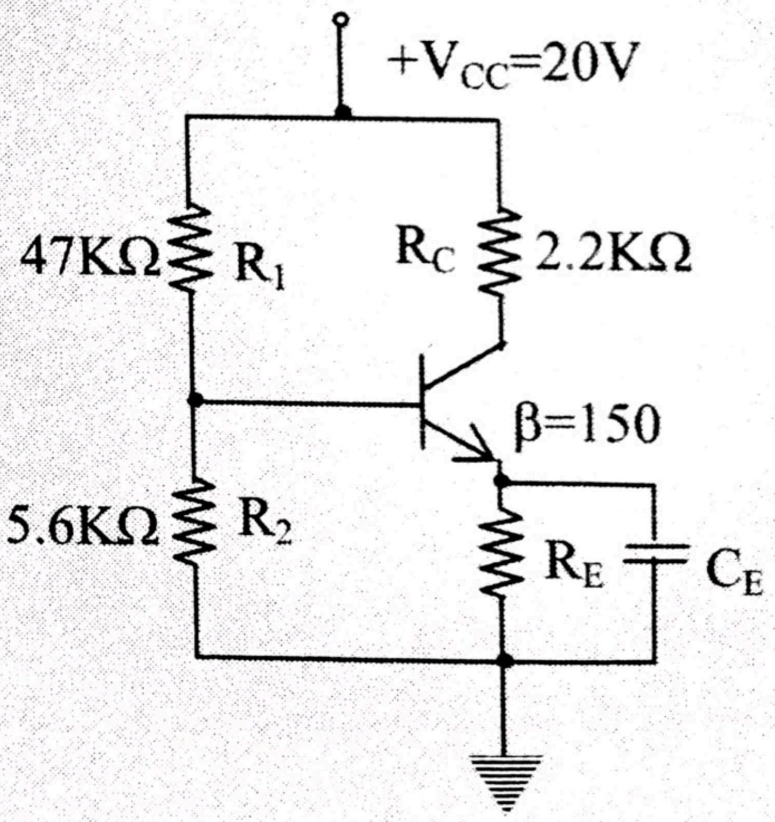
Example.5:

For a voltage divider biasing circuit shown below. Find I_C, V_{CE}, I_B, V_E and V_B.



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Example.6:

In a self-bias circuit, a BJT with $h_{fe} = 100$, $V_{BE} = 0.7V$ and $I_{CO} = 0$ is used. Calculate the values of R_1 and R_C such that it's $I_C = 1mA$ and $V_{CE} = 2.5V$

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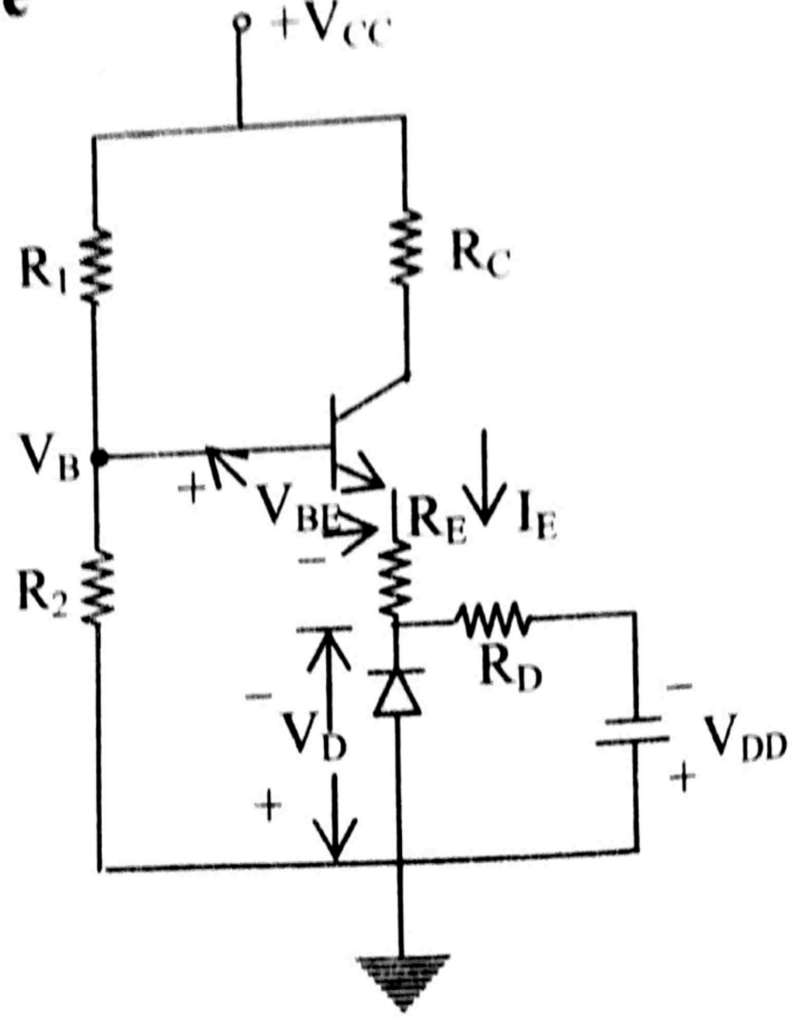
1. Diode compensation for V_{BE} variations with temperature



KVL for Base- Emitter Loop

$V_B - V_{BE} - I_E R_E + V_D = 0$ ------(1)

$$\therefore I_E = \frac{V_B - V_{BE} + V_D}{R_E} \quad \text{------ (2)}$$

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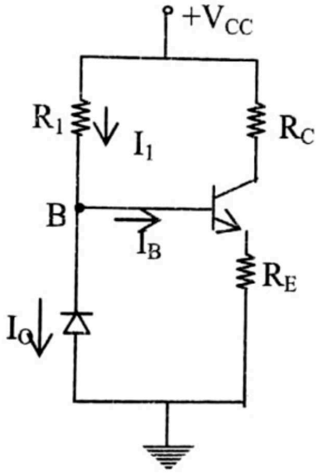
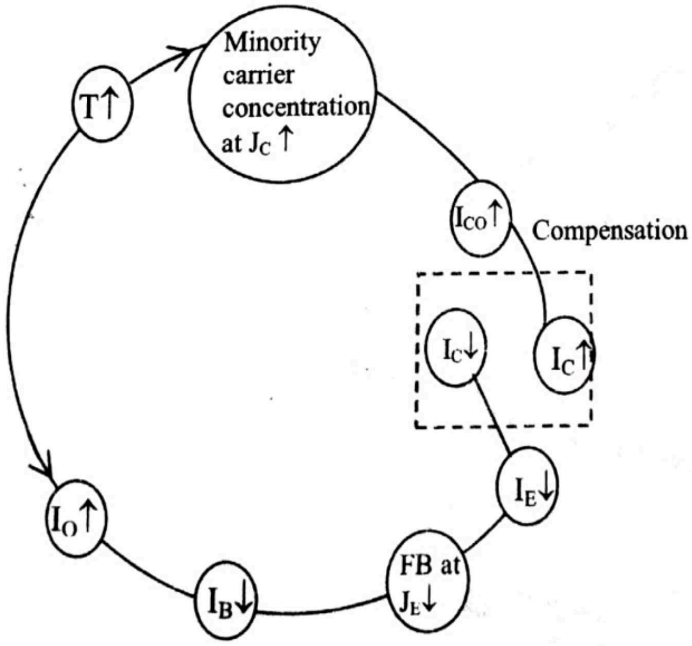
Note: The variations in I_E due to the variations in the junction voltage of BJT, V_{BE} are compensated by the corresponding variations in junction voltage of the diode, V_D during temperature variations.

2. Diode compensation for I_{CO} variations with temperature



KCL at node B

$I_1 = I_B + I_O \Rightarrow I_B = I_1 - I_O$ ----(1)



Note: The increase in I_C due to the increase in I_{CO} is compensated by the corresponding increase in reverse saturation current, I_O in the diode during temperature variations.

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Thermistor compensation for I_{CO} variations with temperature:

Thermistor is a temperature dependant resistance which has got negative temperature coefficient. i.e the resistance of a thermistor varies inversely with the variations in temperature.

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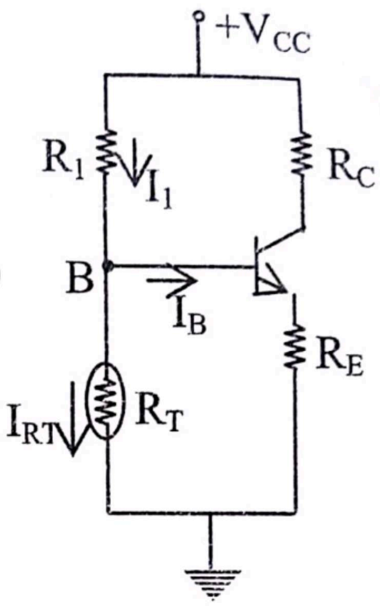
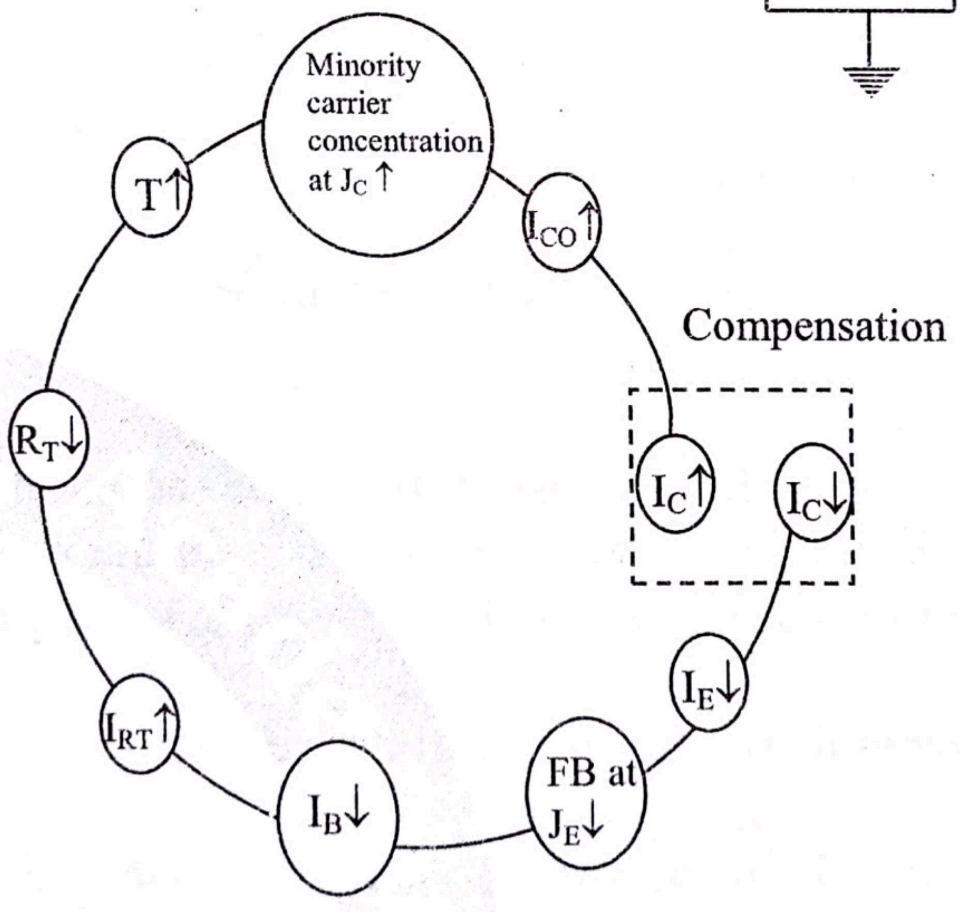
KCL at node B

$I_1 = I_B + I_{RT} \Rightarrow I_B = I_1 - I_{RT}$ ----(1)





Note: The Increase in I_C due to increase I_{CO} is compensated by decrease in the resistance of Thermistor during increase in temperature.

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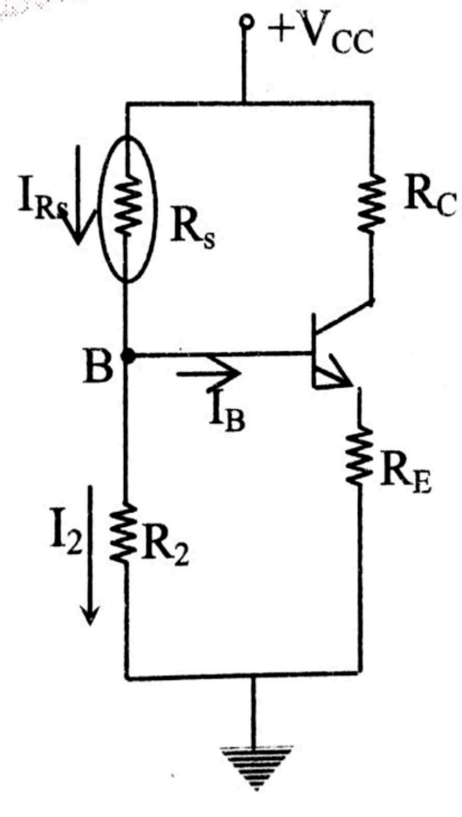
4. Sensistor compensation for I_{CO} variations with temperature:

Sensistor is variable resistor or temperature dependant resistor which has got positive temperature coefficient. i.e the resistance of sensistor varies in proportional with the variations in temperature.



KCL at B

$I_{RS} = I_B + I_2 \Rightarrow I_B = I_{RS} - I_2$ -----(1)

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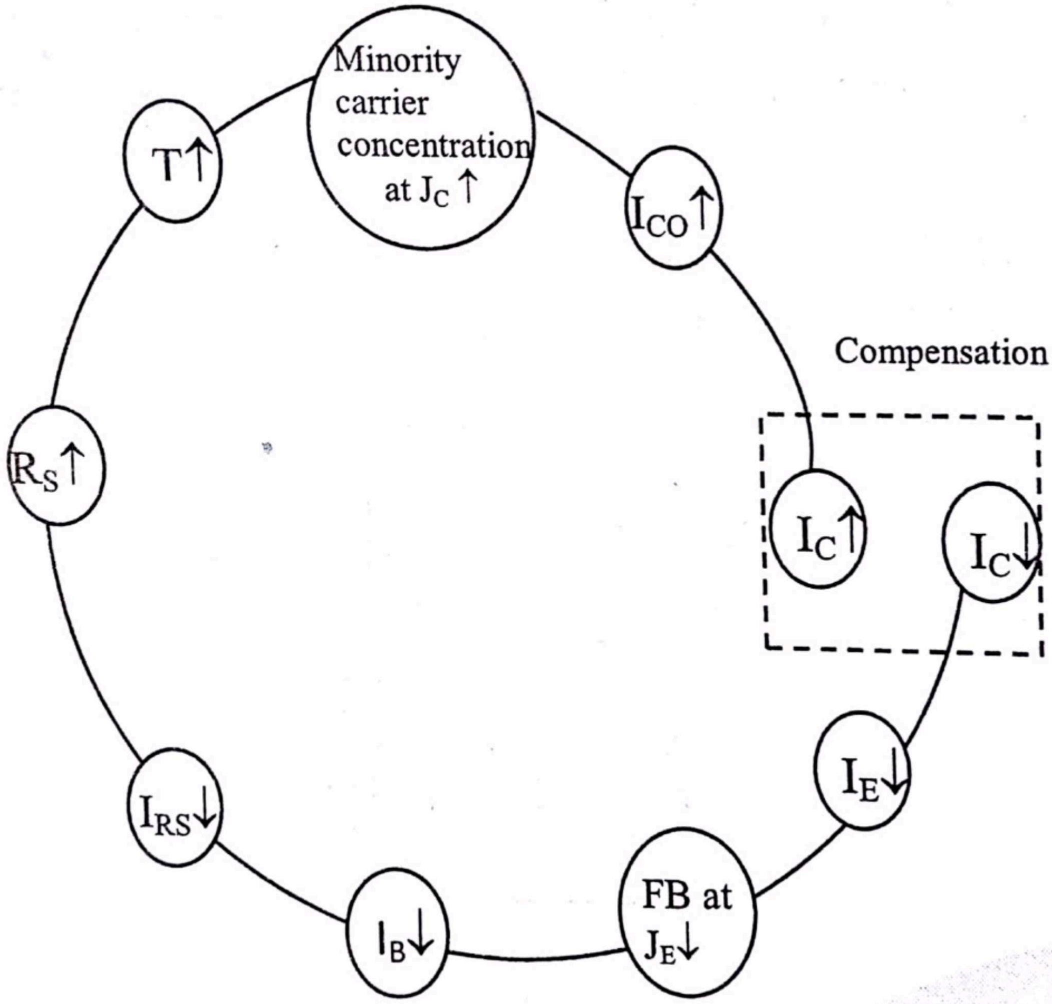

Note: The increase in I_C due to the increase I_{CO} is compensated by the increase in the resistance of sensistor during the increase in temperature.

Thermal stability in electronic devices:

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Thermal stability in electronic devices:

- Let $T_A{}^oC$ be the ambient temperature i.e., the temperature of surroundings air around transistor and $T_j{}^oC$, the temperature of collector-base junction of the transistor. Then

$$\boxed{T_J - T_A \propto P_D \text{ ----- } (1)}$$

Where P_D is the power released at a reverse biased p-n junction of an electronic device under steady state condition.

$\Rightarrow T_J - T_A = \Theta P_D$ ----- (2)

Where Θ is the thermal resistance of an electronic device expressed in ^OC / Watt.

Note:

- For a low power, low cost transistor, the thermal resistance Θ is around 1000^0 C/Watt
- For a high power quality transistor thermal resistance Θ is 0.02^0 C /watt.

Assuming the ambient temperature in equation (2) as constant,

$\partial T_j = \Theta \, \partial P_D$ ----- (3)

$$\boxed{\Rightarrow \frac{\partial P_D}{\partial T_j} = \frac{1}{\Theta} - - - (4)}$$

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- Let P_C is the power released at the reverse bias collector junction of a BJT during its real time operation.

$$\therefore \frac{\partial P_C}{\partial T_j} < \frac{\partial P_D}{\partial T_J} \text{ ---------------- (5)}$$

$$\boxed{\therefore \frac{\partial P_C}{\partial T_J} < \frac{1}{\Theta} \text{---(6)}}$$

This is the condition to prevent thermal runaway in transistors.

- From Fixed bias circuit,
  $V_{CE} = V_{CC} - I_C R_C$ ------------ (7)

- The power dissipation at the collector junction of a BJT is given by

  $P_C = V_{CE}\, I_C$ ------------------- (8)

  $= V_{CC} . I_C - I_C^2 R_C$ ----------- (9)

$$\boxed{\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C R_C \text{---(10)}}$$

From equation (4): $\frac{\partial P_C}{\partial T_j} < \frac{1}{\Theta}$

$$\frac{\partial p_C}{\partial I_C} \times \frac{\partial I_C}{\partial T_J} < \frac{1}{\Theta} \text{------------- (11)}$$

- Since $\frac{\partial I_C}{\partial T_j}$ is the positive and $\frac{1}{\Theta}$ is approximately zero for low power transistor, $\frac{\partial P_C}{\partial I_C}$ should be negative

$$\Rightarrow \frac{\partial P_C}{\partial I_C} = V_{CC} - 2\, I_C\, R_C < 0 \text{ -- (12)}$$

$$\Rightarrow I_C \geq \frac{V_{CC}}{2R_C} \text{ ---------------------- (13)}$$

- Substituting equation (13) in (7)

$$\boxed{\therefore V_{CE} \leq \frac{V_{CC}}{2}} \text{-------------------- (14)}$$

Note: This is the condition for thermal stability in transistors

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