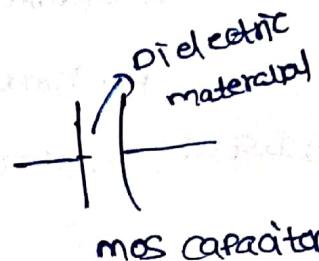
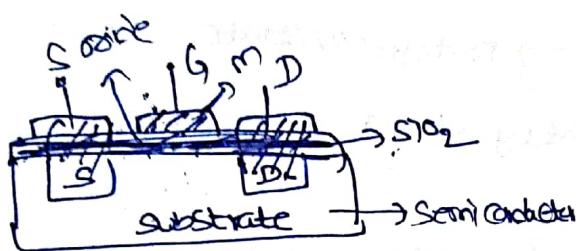


## MOSFET

m - metal  
 o - oxide  
 s - semiconductor  
 f - Field  
 E - Effect  
 T - Transistor

BJT  
↓  
Bipolar



$$C = \frac{\epsilon A}{d}$$

Electric Field

**H & E**

$I_{DS} \Rightarrow$  Single Polarity

$$C = \frac{\epsilon_{ox} \cdot A}{d} \quad \epsilon_{ox} = 10^{-9} \frac{3.6 \text{ fF}}{\text{fm}}$$

$$E = E_{ox} \times E_0$$

BJT

MOSFET

$\Rightarrow$  Bipolar device

$n|p|n$

$\Rightarrow$  less I/P Resistance

$$R = \frac{V}{I}$$

$\Rightarrow$  A symmetrical device

E & C - unequal doping

$\Rightarrow$  High power dissipation

$\Rightarrow$  high speed device

$\Rightarrow$  used in low power applications

where speed is a factor

$\Rightarrow$  Current controlled device

$\Rightarrow$  Base  $\Rightarrow$  control terminal

$\Rightarrow$  Unipolar device, C small in size

$\Rightarrow$  High I/P Resistance

$[SiO_2 \Rightarrow$  Insulator]

$\Rightarrow$  Symmetrical device

S & D  $\Rightarrow$  same doping

$\Rightarrow$  Low Power dissipation

$\Rightarrow$  Low speed device

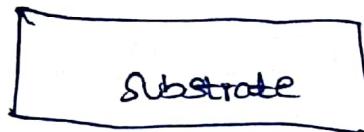
$\Rightarrow$  used in High power application

$\Rightarrow$  Voltage controlled device

$\Rightarrow$  Gate  $\Rightarrow$  control terminal

## Construction of MOSFET :

### Step ① → Formation of substrate



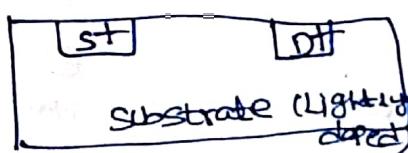
$n$ -Channel  $\Rightarrow$   $p$ -type substrate

$p$ -Channel  $\Rightarrow$   $n$ -type substrate

Substrate  $\Rightarrow$  Lightly doped

### Step ② Formation of source & drain

$S, D \Rightarrow$  Heavily Doped



For  $n$ -channel  $S, D = n$  type

$p - " S, D = p$  type

Interchange  $\rightarrow$   $S \& D$  terminals

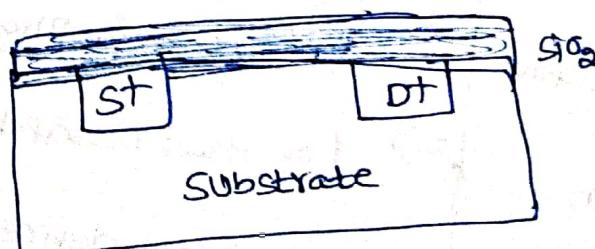
Symmetrical device

### Step ③ : Formation of oxide layer

$1000 - 1200^{\circ}\text{C}$

dry oxidation

(or)  
wet oxidation

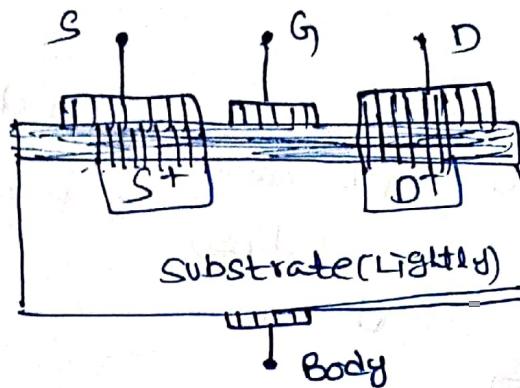


Because of  
oxide Layer  $\Rightarrow$   
(Insulator)

MOSFET IS having  
high  $1/p$  resistance

\$

Step(4) : Formation of metal contacts to source & drain & gate, Body



S, D - Photomasking tech

G - Chemical vapor deposition

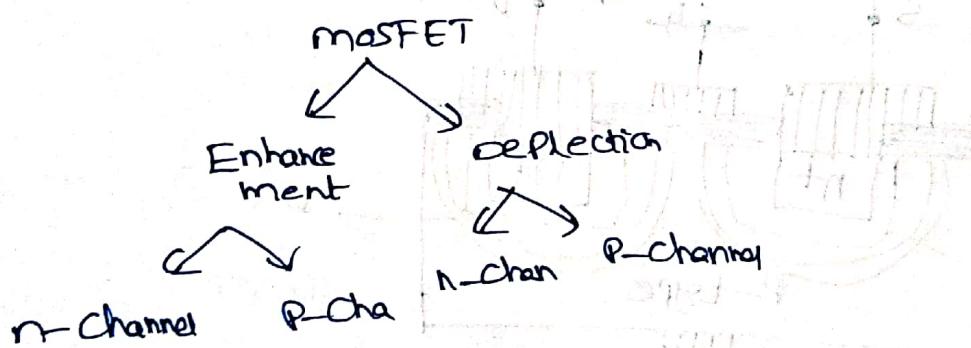
Body - To eliminate Body effect terminal

metal contacts - To supply voltage

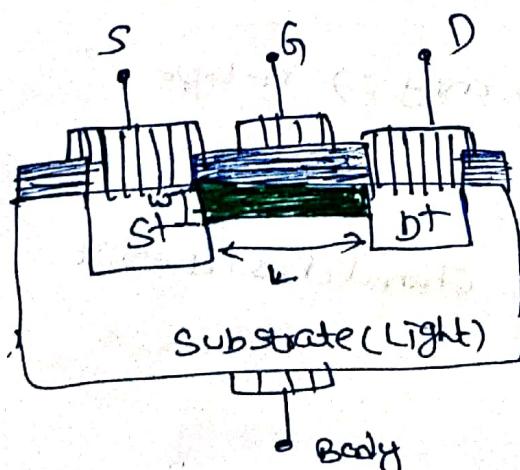
To provide  $\Rightarrow$  modern - Silicon gate Tech  
gate terminal

Polarization - To Form gate electrode

Step(5) : Fabrication of Channel [depletion type]



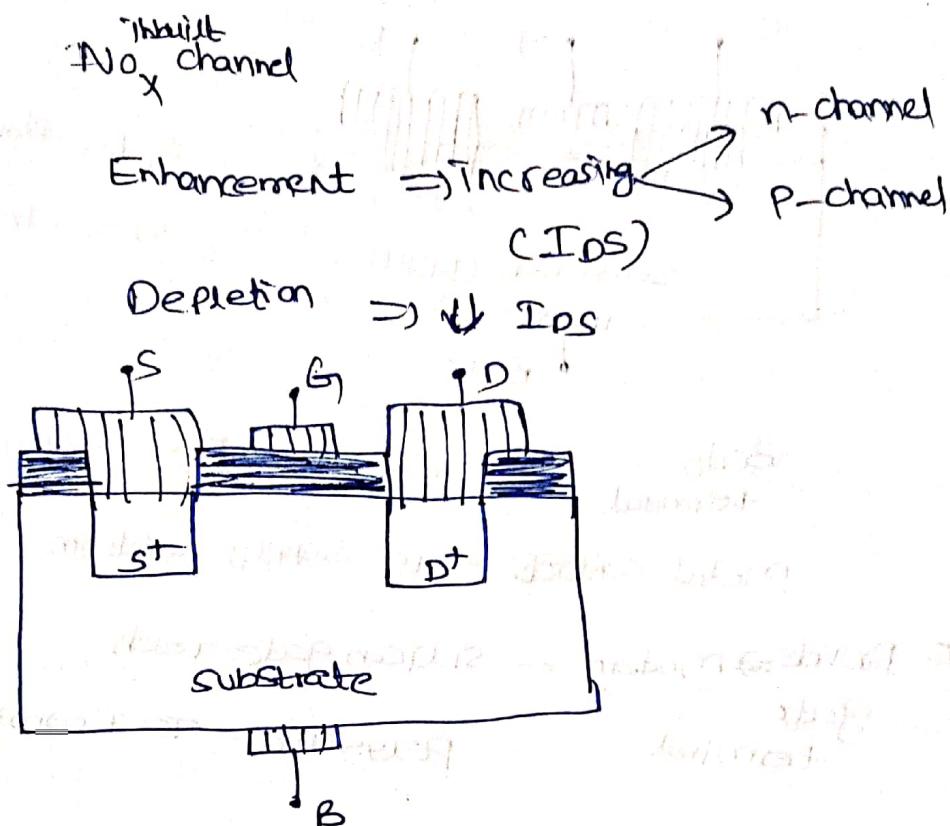
Depletion mosFET



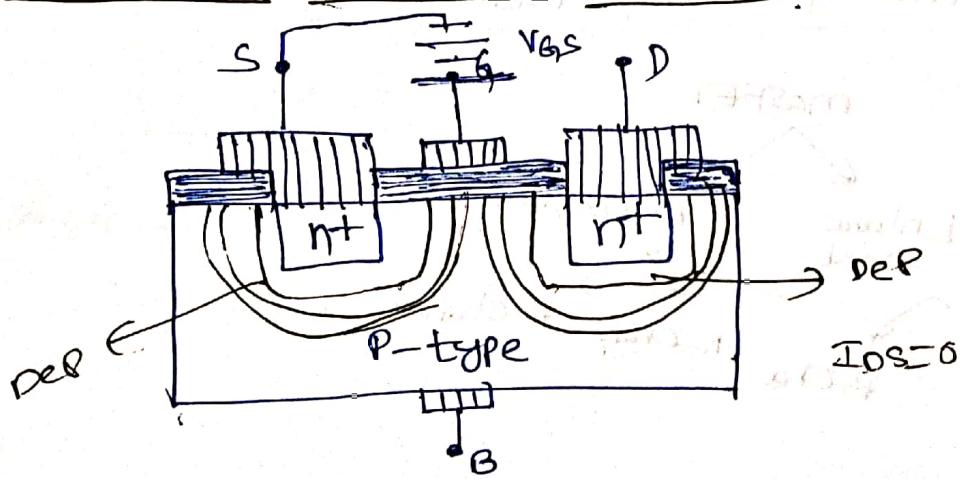
$$L = 0.03 \text{ nm to } 1 \text{ nm}$$

$$w = 0.1 \text{ nm to } 160 \text{ nm}$$

## Working of Enhancement mosFET:



## N-Channel Enhancement mosFET:



## Channel Creation for current flow:

Channel  $\Rightarrow$  e<sup>-</sup>s only  $\Rightarrow$  n-type

$$V_{GS} = +ve$$

case  
(1)

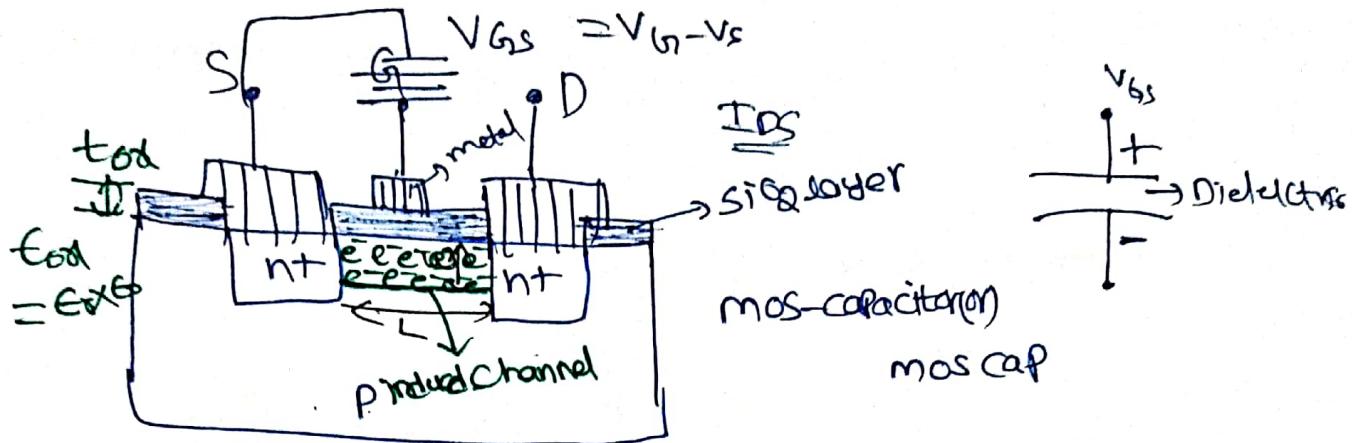
If  $V_{GS} = 0$ , channel does not exist

$$I_{DS} = 0$$

Case(ii)

63

$$V_{GS} = +ve$$



Threshold voltage ( $V_T$ ) :

minimum  $V_{GS} \Rightarrow$  to form a conducting channel

since  $V_{GS} = +ve$

$V_T$  = positive in n-channel Enhancement  
mosFET

$$V_T = 0.3V \text{ to } 1V$$

$$V_{GS} - V_T = V_{\text{overdrive}}$$
 (overdrive voltage)

magnitude of e- charge in a channel

$$Q = C \times V_{\text{overdrive}}$$

$$C = C_{ox} \times wL$$

$$\downarrow \\ F/m^2 \times m^2 = \text{farads}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$Q = (C_{ox} \times wL) \times (V_{GS} - V_T)$$

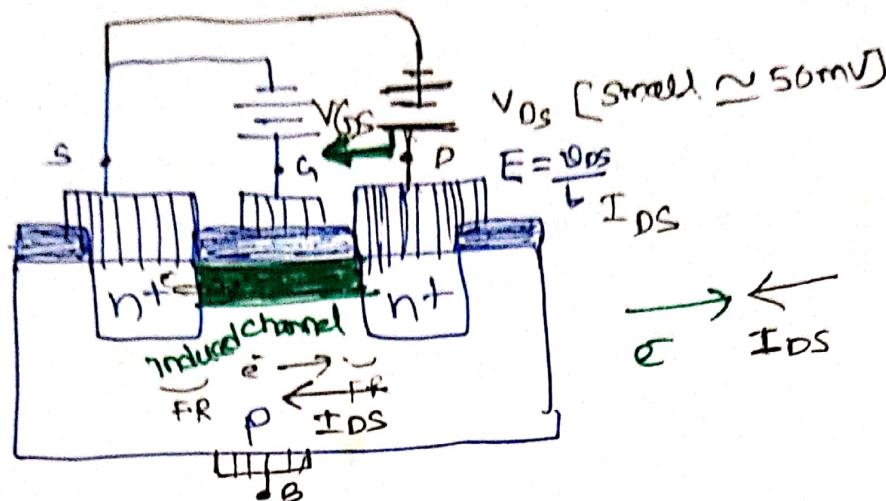
$$C_{ox} = \frac{\epsilon_{ox}}{d} \text{ (or) } \frac{\epsilon_{ox}}{t_{ox}}$$

distance b/w  
two plates

Distance b/w the plates (or)  
Gate & +ve plate (channel)

Apply  $V_{DS}$  to collect current  $I_{DS}$

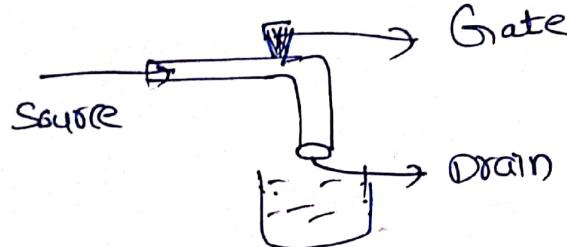
Case@ Applied small  $V_{DS}$  ( $\because V_{DS} = \text{small}$ )



S - giving  $e^-$   $\simeq$  Emitter

G - controlling the  $e^-$  flow  $\simeq$  Base

D - Collecting  $e^-$   $\simeq$  collector



$I_{\text{drift}}$

$$E = \frac{V_{DS}}{L}$$

$e^-$  drift velocity ( $U_d$ ) =  $\mu_n E$

$$(U_d) = \mu_n \left( \frac{V_{DS}}{L} \right)$$

$$I_{DS} = I_D = \frac{Q}{t}$$

$$I_D = \frac{(C_{ox} \times \omega L) \times (V_{GS} - V_T)}{\text{time}}$$

$$\text{time} = \frac{\text{displacement}}{\text{velocity}}$$

$$\text{displacement} = L$$

$$\text{velocity} = 2Ld$$

$$\text{time} = \frac{L}{2Ld} = \frac{L}{\mu_n E} = \frac{L}{\mu_n \times \frac{V_{DS}}{L}} = \frac{L^2}{\mu_n \times V_{DS}}$$

$$I_D = \frac{(\text{Co}_x \times W) \times (V_{GS} - V_T)}{\left( \frac{L^2}{\mu_n \times V_{DS}} \right)}$$

$$I_D = \frac{\mu_n \times V_{DS} \times \text{Co}_x \times W \times (V_{GS} - V_T)}{L}$$

$$I_D = \mu_n \times \text{Co}_x \times \left( \frac{W}{L} \right) \times (V_{GS} - V_T) \times V_{DS}$$

↓  
V<sub>DS</sub> (small)

For Small

$$V_{DS} \Rightarrow I_D = m_d \Rightarrow \text{controlled by } V_{GS} - V_T$$

$$I_D = \left[ \mu_n \text{Co}_x \left( \frac{W}{L} \right) (V_{GS} - V_T) \right] V_{DS}$$

$$g_{DS} = \text{Conductance} \quad \left( \frac{I_D}{V_{DS}} \right) = \underbrace{\mu_n \times \text{Co}_x \times \frac{W}{L}}_{k_n} (V_{GS} - V_T)$$

$\mu_n \times \text{Co}_x \Rightarrow$  MOSFET Fabrication (or) Process Technology

unitless  $\left( \frac{W}{L} \right)$   $\Rightarrow$  Process transconductance parameter  $\frac{g_{DS}}{V_{DS}} = \frac{I_D}{V_{DS}^2}$

$$k_n = \frac{\mu_n \times \text{Co}_x}{2} \times \frac{W}{L} = \frac{Amp \times V^2}{Amp \times V^2}$$

$$K_n' = \mu_n \times C_{ox} \text{ Amp/V}^2$$

Aspect Ratio  $\frac{W}{L}$

MOSFET transconductance parameter  $K_n$

$$K_n = K_n' \times \frac{W}{L}$$

$$K_n = \mu_n \times C_{ox} \times \frac{W}{L} \text{ Amp/V}^2$$

Units of  $K_n' \Rightarrow \text{m}^2/\text{V}\cdot\text{sec} \times \text{F/m}^2$

$$K_n' = \frac{\text{Amp}}{\text{V}\cdot\text{sec}} \times \frac{C}{V} \times \frac{1}{\text{m}^2}$$

$$K_n' = \frac{it}{V^2 \cdot \text{sec}} = \frac{\text{Amp} \times \text{sec}}{V^2 \cdot \text{sec}}$$

$$K_n' = \text{Amp/V}^2$$

$$K_n = \text{Amp/V}^2$$

For  $V_{DS} = \text{small} \Rightarrow \text{channel length is almost uniform}$

MOSFET  $\Rightarrow$  Linear device

Linear Resistance

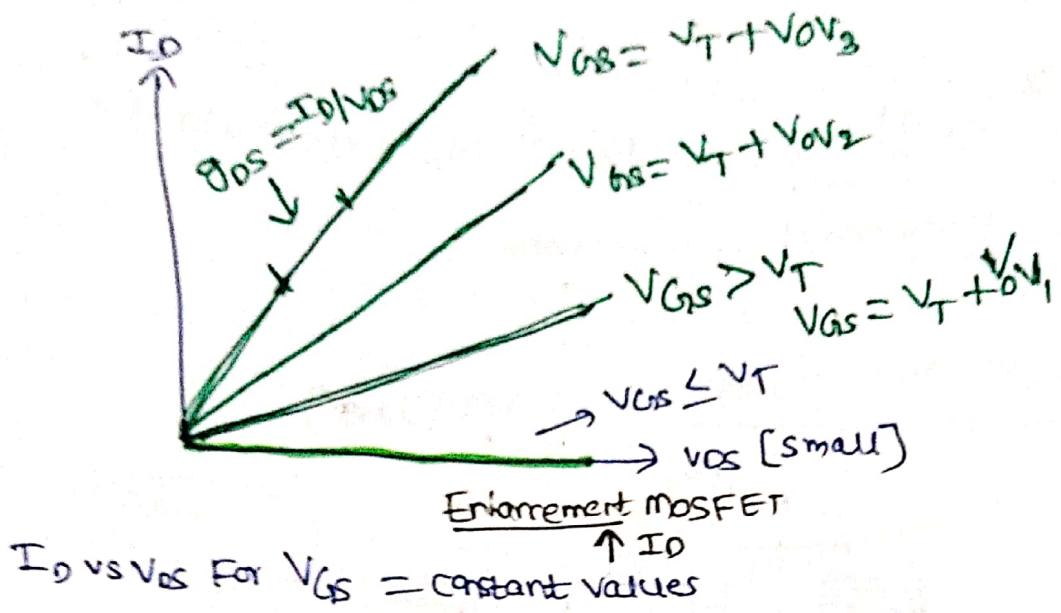
$$r_{DS} = \frac{1}{g_{DS}}$$

Linear Region

Voltage  
Controlled  
Resistance

$$r_{DS} = \frac{1}{(\mu_n C_{ox}) \left( \frac{W}{L} \right) (V_{GS} - V_T)}$$

$V_{ov}$



$$V_{GS} > V_T \Rightarrow \text{channel exist}$$

$V_{GS} \leq V_T \Rightarrow$  Channel does not exist

$$r_{DS} = \frac{1}{g_{DS}} = \underbrace{1}_{\left( k_n C_o \right) \left( \frac{W}{L} \right) \left( V_{GS} - V_T \right)}$$

high resistance  $\Rightarrow I_D = 0$

$$\tau_{ds} \propto \frac{1}{N_{GS} - N_f}$$

$$\gamma ds \propto \frac{1}{\sqrt{ov}} \uparrow$$

$I_D \uparrow$   $V_{DS}$  vs  $I_D$  for  $V_{GS}$

$$V_{Gg} > v_f$$

$$\underbrace{V_{GS} - V_T}_{> 0V}$$

1, 2, etc -

V<sub>ov</sub>

Vay

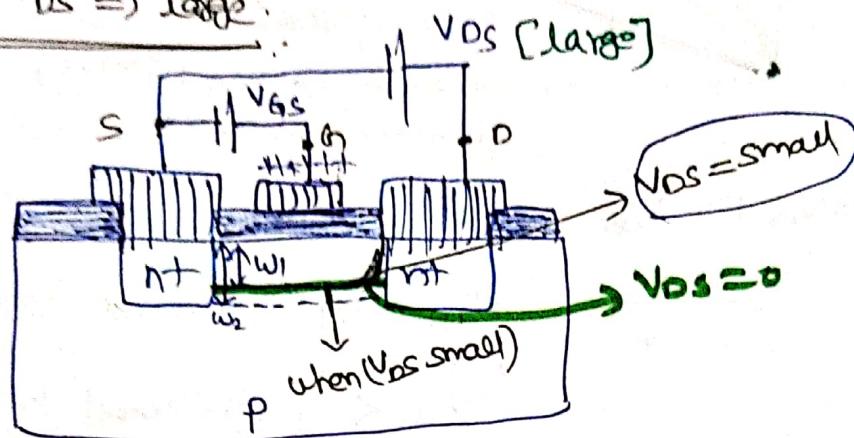
100

$$V_{\beta s} = V_T + V_{0VJ}$$

$$V_{GS} = V_T + V_{OV_2}$$

Note! By  $\uparrow V_{GS}$ ,  $I_{DS} \uparrow$ , that is the reason for enhancement MOSFET name

Case (iv)  $V_{DS} \Rightarrow$  large



$$V_{GS} > V_T$$

$$V_{GS} - V_T > 0$$

$$V_{ov}$$

To increase width of the channel

$$V_{GS} = V_T + V_{ov}$$

$$(V_{GS} = V_T + V_{DS} - V_T)$$

Channel width

$$(w) \propto V_{ov}$$

due to  $V_{GS}$  only

$$V_{GD} = V_G - V_D$$

$$V_{GD} = \underbrace{V_G - V_S}_{V_{GS}} + V_S - V_D$$

$$V_{GD} = V_{GS} - [V_D - V_S]$$

$$V_{GD} = V_{GS} - V_{DS}$$

$$V_{GD} = V_T + (V_{ov} - \frac{V_{DS}}{0.05})$$

$V_{ov} \downarrow$  will reduce the channel length

A

Channel uniform

B

$$V_{GD} = V_T + V_{ov} - V_{DS}$$

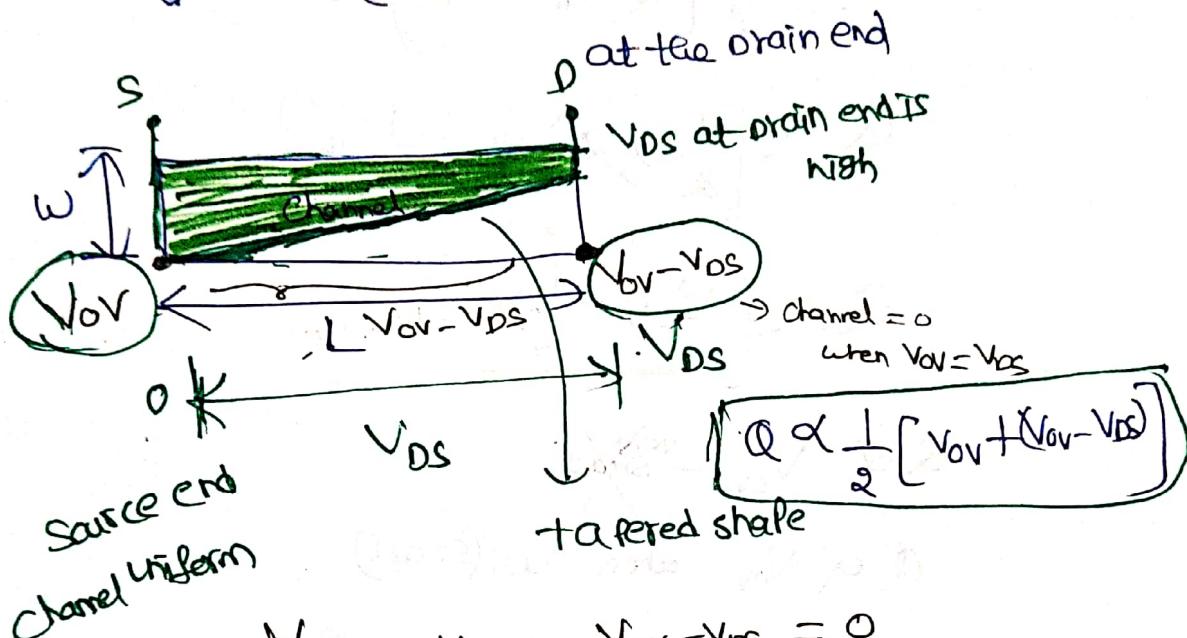
(large)

↓      ↓      ↓

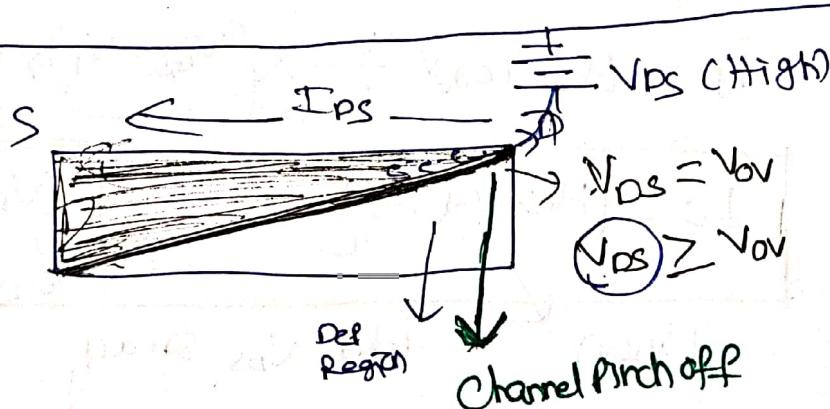
4V      2V

$$V_T + (4-2) = 2V$$

$\downarrow V_{ov} \propto$  channel width  $\downarrow$



$$V_{DS} = V_{ov} \Rightarrow V_{ov} - V_{DS} = 0$$



For  $V_{DS} > V_{ov} \Rightarrow$  No effect on channel

$I_{DS} \Rightarrow$  constant  $\Rightarrow$  saturates

$$V_{GD} = V_T$$

$$V_{GD} = V_T + V_{ov} - V_{DS}$$

$$V_{DS} = V_{ov}$$

$$V_{GD} = V_T \Rightarrow$$

The current equation is

$$i_D = ?$$

$$Q \propto \frac{1}{2} [V_{ov} + (V_{ov} - V_{DS})]$$

$$Q \propto \frac{1}{2} [2V_{ov} - V_{DS}]$$

$$Q \propto \frac{1}{2} \times 2V_{ov} - \frac{1}{2} V_{DS}$$

$$Q \propto \underline{\underline{V_{ov} - \frac{1}{2} V_{DS}}}$$

$$Q \propto V_{ov} - \frac{V_{DS}}{\text{small}}$$

$$Q \propto V_{ov} \text{ when } V_{DS} \text{ (small)}$$

The current eqn when  $V_{DS}$  (small) Regions

$$i_D = \mu_n \times C_{ox} \times \frac{w}{l} \times \underbrace{(V_{GS} - V_T)}_{\text{Linear}} \times V_{DS}$$

$$i_D = \left[ \mu_n \times C_{ox} \times \frac{w}{l} \times V_{ov} \right] \times V_{DS}$$

Linear when  $V_{DS}$  small (Linear Region)

when  $V_{DS}$  (large)

$$i_D = \mu_n \times C_{ox} \times \frac{w}{l} \times \underline{\underline{V_{ov} - \frac{1}{2} V_{DS}}} V_{DS}$$

$$i_D = \mu_n \times C_{ox} \times \frac{w}{l} \times \left[ (V_{GS} - V_T) - \frac{1}{2} V_{DS} \right] V_{DS}$$

$$i_D = K_n \times \left( \frac{w}{l} \right) \times \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$i_D = k_n' \times \left(\frac{w}{L}\right) \times \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \rightarrow \textcircled{A}$$

Current equation when  $V_{DS} \Rightarrow$  large

TO obtain current eqn in saturation Region

$$V_{DS} \geq V_{OV} \Rightarrow \text{channel Pinch off occurs}$$

$$V_{DS} \geq V_{GS} - V_T \Rightarrow \text{current will saturates}$$

$$V_{DS} = V_{OV}$$

$$V_{DS} = V_{GS} - V_T \rightarrow \textcircled{B} \quad \text{For saturation Region}$$

Sub  $\textcircled{B}$  in  $\textcircled{A}$

$$i_D = k_n' \times \left(\frac{w}{L}\right) \times \left[ (V_{GS} - V_T) (V_{GS} - V_T) - \frac{1}{2} (V_{GS} - V_T)^2 \right]$$

$$i_D = k_n' \times \left(\frac{w}{L}\right) \times \left[ (V_{GS} - V_T)^2 - \frac{1}{2} (V_{GS} - V_T)^2 \right]$$

$$i_D = k_n' \times \left(\frac{w}{L}\right) \times \left[ \frac{1}{2} (V_{GS} - V_T)^2 \right]$$

$$i_D = \frac{1}{2} \times k_n' \times \left(\frac{w}{L}\right) \times [V_{GS} - V_T]^2$$

$$i_D = \frac{1}{2} \times k_n \times [V_{GS} - V_T]^2$$

}  
Saturation Region

V-V<sub>Imp</sub>

$$k_n = k_n' \times \frac{w}{L} ; k_n' = n_n \times \rho_{sd}$$

Linear & Triode Regions

$$V_{DS} \Rightarrow$$

Very small  
Linear  
Region

$$V_{DS} < V_{OV}$$

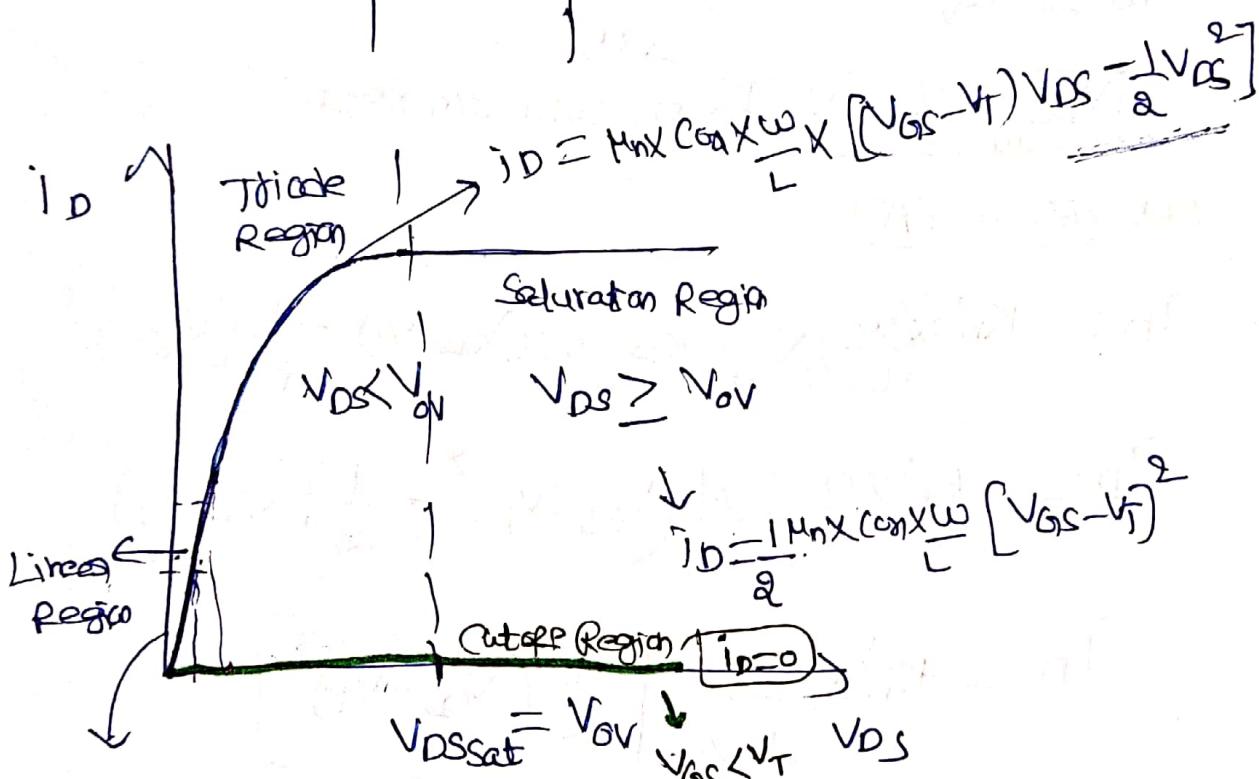
$$V_{DS} < V_{GS} - V_T$$

Saturation Region

$$V_{DS,sat} = V_{GS} - V_T$$

$$V_{DS} \geq V_{OV}$$

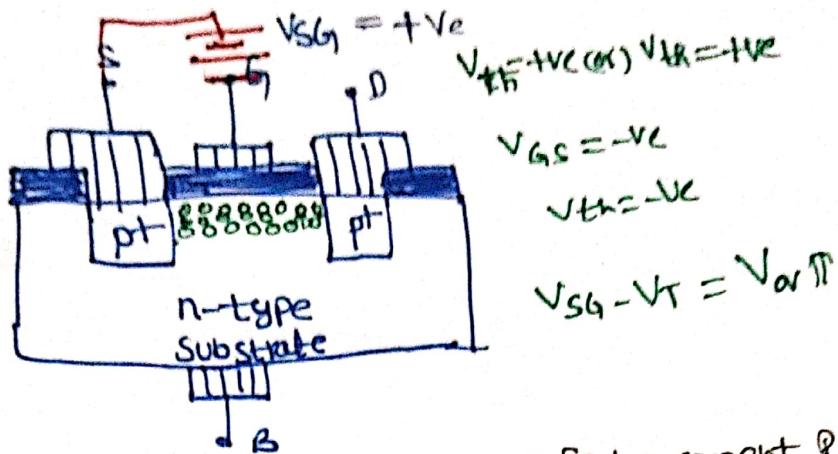
$$V_{DS} \geq (V_{GS} - V_T)$$



$$i_D = M_n \times \text{Con} \times \left( \frac{W}{L} \right) \times (V_{GS} - V_T) V_{DS}$$

Fig @ OIP characteristics of E-mos of n-channel

## P-channel Enhancement MOSFET



Fig@ construction of PMOS Enhancement PMOS

## Channel creation (P channel)

## Charge carriers in P-channel - holes

$$H_b < H_e$$

$$N_A = 3K_h$$

C whole

Case(i) If  $V_{GS} = 0$ , channel does not exist

$$vsG = 0 \quad I = 0$$

$$\underline{\text{Case (ii)}} \quad \underline{V_{SG} = +ve} \quad (01) \quad (V_{GS} = -ve)$$

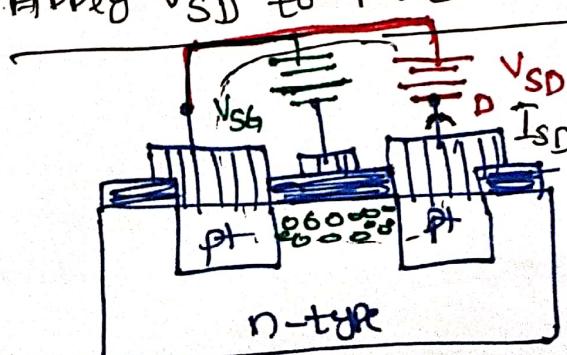
$$V_S > V_G$$

$$V_{\text{bf}} = V_{\text{th}} = V_{\text{re}}$$

$$V_{GS} = -V \quad V_{th} = -V$$

Induced Channel width  $N$  when  $V_{ATP}$

Case (ii): Apply  $V_{SD}$  to ~~to~~ collect current  $I_{SD}$



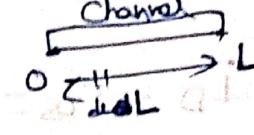
$$u_d = \mu_d E$$

$$E = \frac{V_{SD}}{L}$$

$$E = -\frac{dV_{SD}}{dL}$$

$$E = -\frac{dV_{SD}}{dL}$$

$$V_d = \mu_p \times E$$

$$\frac{dL}{dt} = V_d = \mu_p \times \frac{d(V_{SD})}{dL}$$


$$V_d = \frac{\text{displacement}}{\text{time}} = \frac{dL}{dt}$$

$$\frac{dL}{dt} = -\mu_p \frac{d(V_{SD})}{dL}$$

$$I = \frac{dq}{dt} = \frac{dq}{dL} \times \frac{dL}{dt}$$

$$dq = C \times V_{\text{overdrive voltage}}$$

$$dq = C_o \times w \cdot dL \times [V_{SG} - V_T - \frac{V_{SD}}{2}]$$

$$\frac{dq}{dt} = C_o \times w \times [V_{SG} - V_T - \frac{V_{SD}}{2}]$$

$$\frac{dq}{dL} = C_o \times w \times [V_{SG} - V_T - \frac{V_{SD}}{2}]$$

$$I = \frac{dq}{dL} \times \frac{dL}{dt}$$

$$I = C_o \times w \times [V_{SG} - V_T - \frac{V_{SD}}{2}] \times -\mu_p \times \frac{d(V_{SD})}{dL}$$

$$I_{dL} = -C_o \times w \times [V_{SG} - V_T - \frac{V_{SD}}{2}] \times \mu_p \times d(V_{SD})$$

$$I_{dL} = - \int C_o \times w \times \mu_p \times [V_{SG} - V_T - \frac{V_{SD}}{2}] d(V_{SD})$$

$$I_{\cancel{dL}} = -C_o \times \mu_p \times w \times [V_{SG} - V_T - \frac{V_{SD}}{2}] \frac{d(V_{SD})}{2}$$

$$I = -\mu_p \times C_o \times w \times (V_{SG} - V_T) V_{SD} - \frac{V_{SD}(L)}{2}$$

$$I = -M_p \times C_{ox} \times \frac{W}{L} \times \left[ (V_{SG} - V_T) V_{SD} - \frac{V_{SD}^2}{2} \right]$$

$$\frac{I}{S_D} = -M_p \times C_{ox} \times \frac{W}{L} \left[ (V_{SG} - V_T) V_{SD} - \frac{V_{SD}^2}{2} \right]$$

$$I_D = I_{DS} = -I_{SD}$$

$$I_D = I_{DS} = M_p \times C_{ox} \times \frac{W}{L} \left[ (V_{SG} - V_T) V_{SD} - \frac{V_{SD}^2}{2} \right]$$

Triode Region

Linear Region

$$V_{DS} = V_{DS,small}$$

$$I_D = M_p \times C_{ox} \times \frac{W}{L} \left[ (V_{SG} - V_T) V_{SD} - \frac{V_{SD}^2}{2} \right]$$

$$I_D = M_p \times C_{ox} \times \frac{W}{L} \left[ (V_{SG} - V_T) V_{SD} \right]$$

Saturation Region

$$V_{DS} \geq V_{DS,0} - V_T$$

$$I_D = M_p \times C_{ox} \times \frac{W}{L} \left[ (V_{SG} - V_T) (V_{SG} - V_T) - \frac{(V_{SG} - V_T)^2}{2} \right]$$

$$I_D = \frac{1}{2} M_p \times C_{ox} \times \frac{W}{L} [V_{SG} - V_T]^2$$

$$I_D = \frac{1}{2} M_p \times C_{ox} \times \frac{W}{L} [V_{SG} - V_T]^2$$

For n-channel E-MOS

$$I_D = M_n \times C_{ox} \times \frac{W}{L} (V_{GS} - V_T) \Rightarrow \text{Linear Region}$$

Pmos

$$V_{GS} = -ve$$

$$V_T = -ve$$

$$I_D = \frac{N_p \times C_{ox} \times W}{L} \left[ (V_{GS} - V_T) \frac{V_{DS} - \frac{V_{DS}^2}{2}}{2} \right]$$

PMOS  $I_D = N_p \times C_{ox} \times \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$

$$V_{GS} = -ve$$

$$V_T = -ve$$

$$V_{DS} = -ve$$

$$I_D = \frac{N_p \times C_{ox} \times W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Saturation Region  $I_D = \frac{N_p \times C_{ox} \times W}{L} (V_{GS} - V_T)^2$

PMOS  $V_{GS} = -ve$

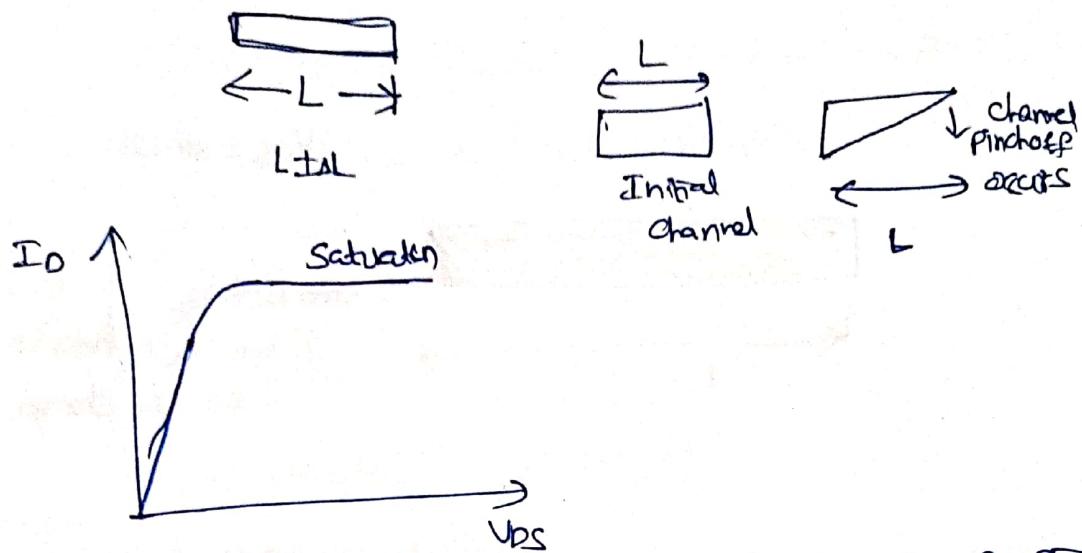
$$V_T = -ve$$

$$I_D = N_p \times C_{ox} \times \frac{W}{L} \left[ \underbrace{(V_{GS} - V_T)^2}_{N_{SV}} \right]$$

## Channel length modulation • [occurs in saturation region]

1

Change in length of the channel, becos of  $\uparrow$  in  $V_{DS}$  ( $V_{DS} > V_{OV}$ )

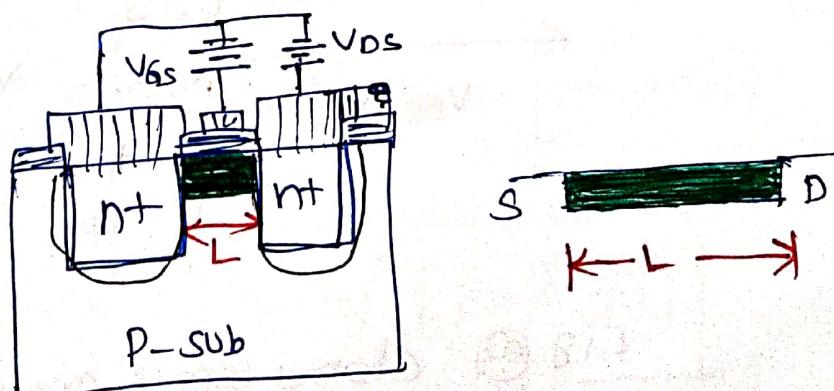


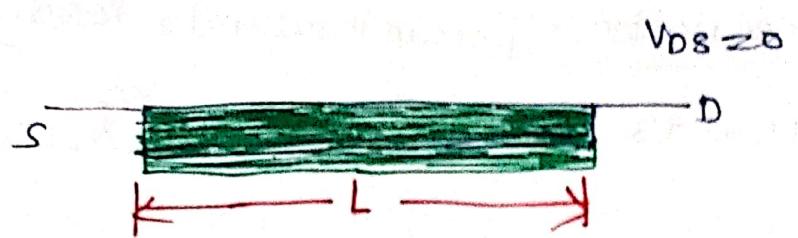
DC current,  $I_D$ , is independent of  $V_{DS}$  in saturation region  
becoz of Channel Pinchoff at the drain end

$$\left. \begin{array}{l} \Delta V_{DS} \implies \Delta I_D = 0 \\ (I_D = \text{constant}) \\ d(I_D) = 0 \\ d(\text{constant}) = 0 \end{array} \right\} \text{Saturation Region}$$

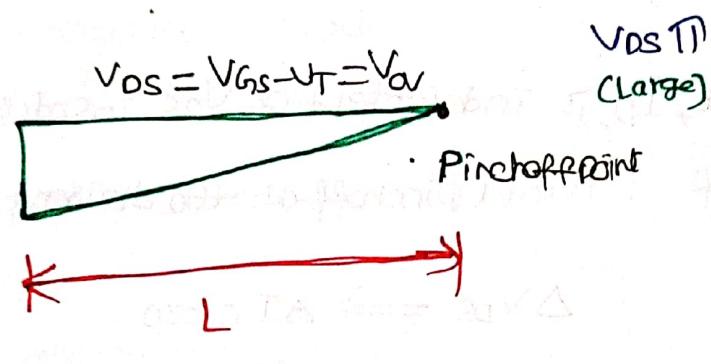
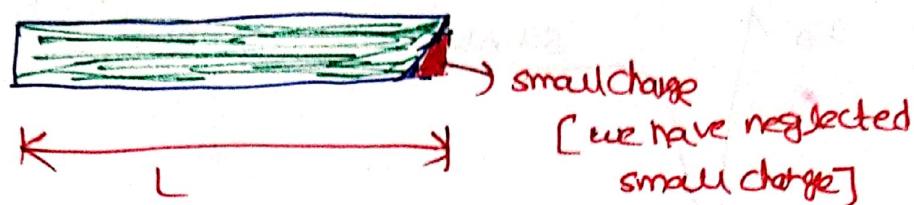
$$\delta d(\text{or}) r_o = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{(\Delta V_{DS})}{0} \Rightarrow \infty$$

Practically, there will be some change in drain current





$V_{DS} = \text{small}$



$V_{DS} > V_{ov}$

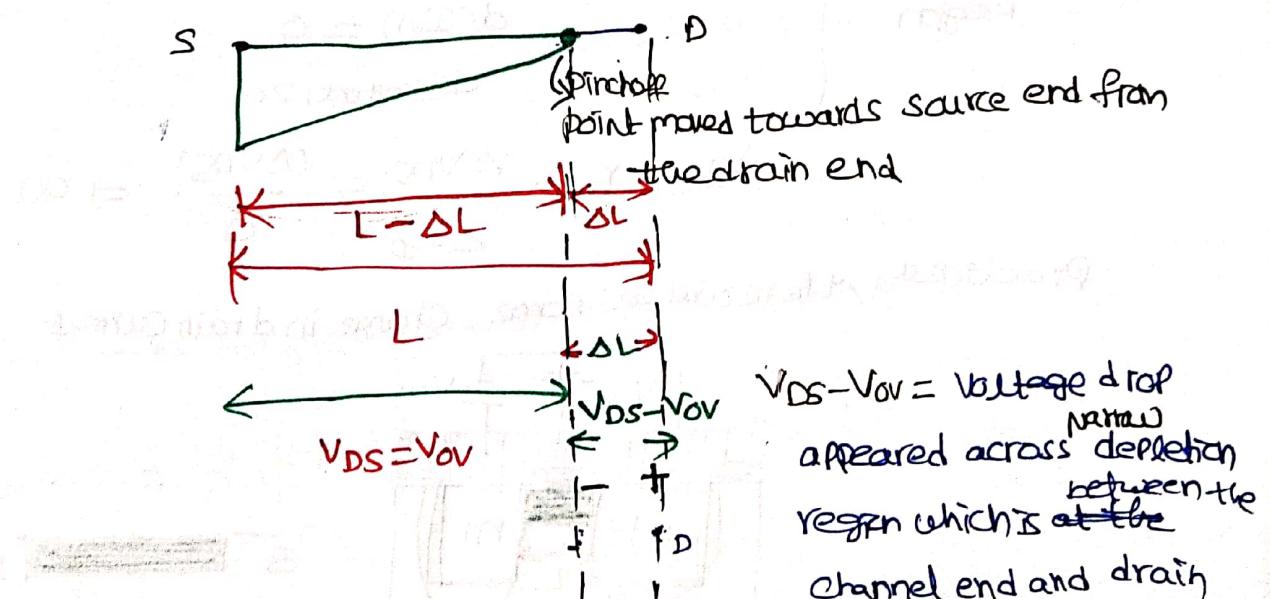


Fig ② Channel length modulation

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T]^2 \Rightarrow \text{saturation Region}$$

$V_{DS} > V_{ov} \Rightarrow$  Channel length modulation occurs in saturation region  
 $[\because V_{DS} \geq V_{ov} \Rightarrow \text{saturation Region}]$

From eq ①

$$I_D \propto \frac{1}{L}$$

channel length  $\downarrow \Rightarrow I_D \uparrow$

$\begin{cases} \text{in channel length modulation} \\ \text{channel length } \downarrow \end{cases}$

$\Rightarrow$  Channel length modulation causes  $\uparrow$  in drain current

$\because I_D \uparrow$

with  $\uparrow V_{DS}$

$\therefore \uparrow \text{in } V_{DS} \xrightarrow{\text{causes}} \text{channel length modulation} \xrightarrow{\text{causes}} \uparrow \text{in } I_D$

$\uparrow \text{in } I_D \text{ with } \uparrow V_{DS}$

$\Rightarrow$  The channel length modulation effect can be accounted for in

the expression of  $I_D$  by  $\times$   $\left[ 1 + \lambda [V_{DS} - V_T] \right]$  (or) simply  $\left[ 1 + \lambda V_{DS} \right]$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T]^2 \cdot [1 + \lambda V_{DS}]$$

$I_D$  after channel length modulation occurs

$\lambda = \text{Device parameter } (V^{-1})$

$$I_D = \frac{1}{2} M_n \cos \frac{w}{L} [V_{GS} - V_T]^2 [1 + \lambda V_{DS}]$$

The above current equation is obtained from the channel length modulation  $\underline{[L \Rightarrow L - \Delta L]}$

The current equation before channel length modulation is

$$\Rightarrow I_D = \frac{1}{2} M_n \cos \frac{w}{L} [V_{GS} - V_T]^2$$

After Channel length modulation

$$I_D = \frac{1}{2} M_n \cos \frac{w}{L - \Delta L} [V_{GS} - V_T]^2$$

$$I_D = \frac{1}{2} M_n \cos \frac{w}{L} \left(1 - \frac{\Delta L}{L}\right)^{-1} [V_{GS} - V_T]^2$$

$$I_D = \frac{1}{2} M_n \cos \frac{w}{L} \left(1 - \frac{\Delta L}{L}\right)^{-1} [V_{GS} - V_T]^2$$

$$(1 - \alpha)^{-1} = 1 + \alpha + \frac{\alpha^2}{2!} + \frac{\alpha^3}{3!} + \dots$$

$$\alpha = \frac{\Delta L}{L} \ll 1 \quad (\alpha \ll 1)$$

$$\Delta L \ll L \Rightarrow \frac{\Delta L}{L} \ll 1$$

$$(1 - \alpha)^{-1} = 1 + \alpha = \left(1 + \frac{\Delta L}{L}\right)$$

$$I_D = \frac{1}{2} M_n \cos \frac{w}{L} \left(1 + \frac{\Delta L}{L}\right) [V_{GS} - V_T]^2$$

$$I_D = \frac{1}{2} \mu n C_{ox} \frac{\omega}{L} \left[ 1 + \frac{\Delta L}{L} \right] [V_{GS} - V_T]^2$$

$$\frac{\Delta L}{L} \propto V_{DS} - V_{OV}$$

$$\frac{\Delta L}{L} \propto V_{DS} - V_{OV} \rightarrow ①$$

$$L \propto \frac{1}{(V_{DS} - V_{OV})} \rightarrow ②$$

$$V_{DS} - V_{OV} \propto \frac{1}{L}$$

$$\frac{\Delta L}{L} \propto (V_{DS} - V_{OV}) \rightarrow ③$$

$$\frac{\Delta L}{L} = \lambda (V_{DS} - V_{OV})$$

$$I_D = \frac{1}{2} \mu n C_{ox} \frac{\omega}{L} \left[ 1 + \frac{\Delta L}{L} \right] [V_{GS} - V_T]^2$$

$$I_D = \frac{1}{2} \mu n C_{ox} \frac{\omega}{L} \left[ 1 + \lambda (V_{DS} - V_{OV}) \right]$$

$$[V_{GS} - V_T]^2$$

$$\begin{aligned} \text{units of } \lambda &= \frac{\Delta L \times 1}{L \times V_{DS} - V_{OV}} \\ &= \frac{m}{m} \times \frac{1}{V_{DS} - V_{OV}} \end{aligned}$$

$$\lambda = \frac{1}{V_{DS} - V_{OV}}$$

$$\lambda = \frac{1}{V_{DS}} = \text{volt}^{-1}$$

$$I_D = \frac{1}{2} \mu n C_{ox} \frac{\omega}{L} \left[ 1 + \lambda V_{DS} \right] [V_{GS} - V_T]^2$$

$$I_D = \frac{1}{2} \mu n C_{ox} \frac{\omega}{L} \left[ 1 + \frac{V_{DS}}{V_A} \right] [V_{GS} - V_T]^2$$

$$I_D = \frac{1}{2} \mu n \cos \theta (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$\lambda$  = device parameter [V<sup>-1</sup>]

$$[V_{DS}^{-1} = \frac{1}{V_{DS}} = V^{-1}]$$

$$1 = \frac{1}{V_A} \quad \& \quad V_{DS} = -V_A$$

[to indicate  $I_D = 0$  for -ve  $V_{DS}$ ]

$V_A$  = positive voltage = device parameter

$[1 + \lambda V_{DS}] \Rightarrow$  to indicate linear dependence of  $I_D$  on  $V_{DS}$

$$I_D \propto V_{DS}$$

$$I_D = \frac{1}{2} \mu n \cos \theta (V_{GS} - V_T)^2 \left[ 1 + \frac{V_{DS}}{V_A} \right]$$

$V_{DS} = +ve$  to get  $I_D$

$V_A = +ve$  to get high  $I_D$

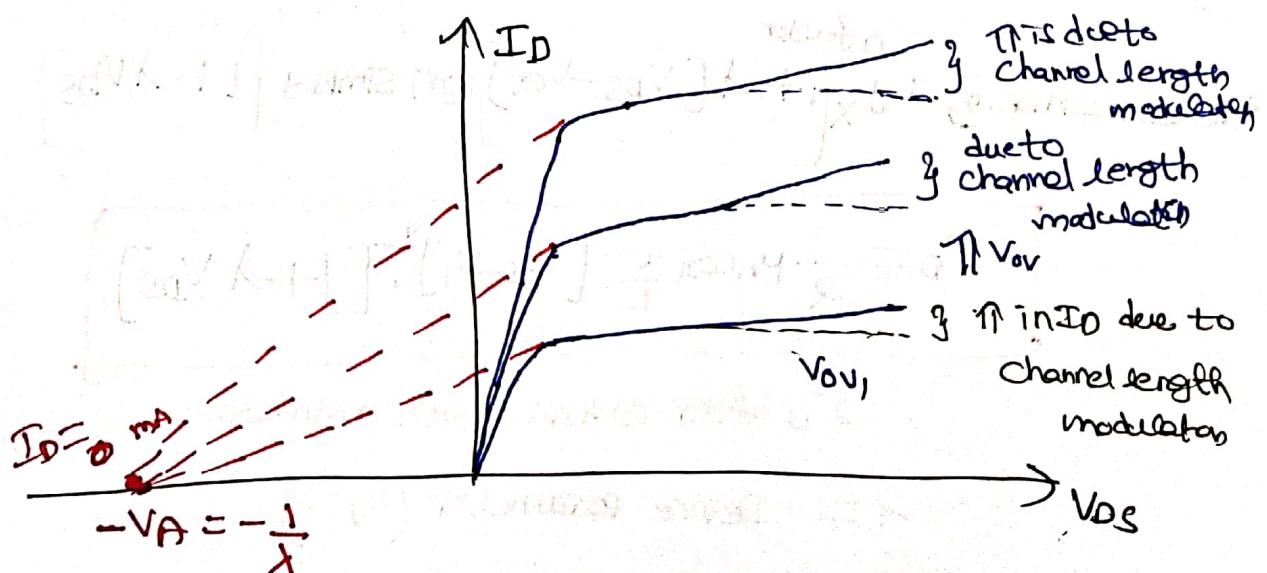
If  $V_{DS} = -ve$  then  $I_D$  should be zero

$$I_D = 0$$

$$I_D = \frac{1}{2} \mu n \cos \theta (V_{GS} - V_T)^2 \left[ 1 + \frac{(-V_A)}{V_A} \right] = 0$$

$$V_{DS} = -V_A$$

V-I CLS when channel length modulation is considered



## Parameters of Enhancement MOSFET

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad \text{Triode Region}$$

$$I_D = K_n \frac{W}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$I_D = K_n \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$I_D = K_n \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad \text{Triode region}$$

Linear (or) Deep Triode Region

$$I_D = K_n [V_{GS} - V_T] V_{DS}$$

$$I_D = \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T] V_{DS}$$

Saturation Region

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T]^2$$

$$I_D = \frac{1}{2} K_n [V_{GS} - V_T]^2$$

### Parameters

① Drain ON Resistance (or) ON Resistance (or) Drain to Source Resistance

Resistance offered by MOSFET in Linear Region.

$$I_D = \text{for small } V_{DS} \text{ values}$$

$$I_D = \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T] V_{DS}$$

$$r_{ds(on)} \text{ (or) } R_{DS} \text{ (or) } r_{ds(on)}$$

$$\gamma_{ds(on)} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{\frac{\Delta I_D}{\Delta V_{DS}}}$$

$$I_D = \mu_n \cos \frac{w}{L} [V_{GS} - V_T] V_{DS}$$

$$\gamma_{ds(on)} = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}}$$

$$\frac{\partial I_D}{\partial V_{DS}} = \mu_n \cos \frac{w}{L} [V_{GS} - V_T] \quad (1)$$

$$\left( \frac{1}{\gamma_{ds(on)}} \right) = \frac{\partial I_D}{\partial V_{DS}} = \mu_n \cos \frac{w}{L} [V_{GS} - V_T]$$

$$\gamma_{ds(on)} = \left( \frac{\partial I_D}{\partial V_{DS}} \right)^{-1} = \frac{1}{\mu_n \cos \frac{w}{L} [V_{GS} - V_T]}$$

Linear Region

In Linear Region

$$\gamma_{ds(on)} @ R \propto \frac{1}{\left( \frac{w}{L} \right) \text{ aspect ratio}}$$

R  $\propto$  aspect ratio  $\left( \frac{w}{L} \right)$

## ② Transconductance ( $g_m$ ) [ $g_m$ is used for Amplifiers ]

$$g_m = \frac{OIP \text{ current}}{OIP \text{ voltage}} \quad [ g_m \Rightarrow \text{Insaturation Region} ]$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \text{slope of Transfer C.S. of mos FET}$$

$g_m \Rightarrow$  Transfer C.S. of mos FET

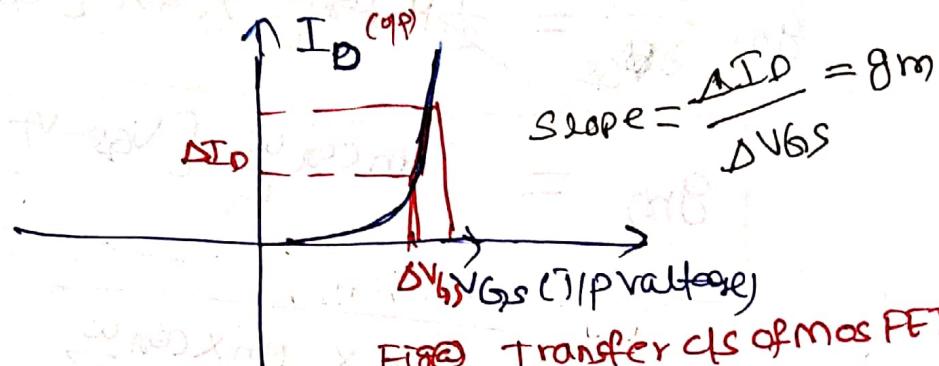


Fig 2 Transfer C.S. of mos FET

n-channel  $\Rightarrow V_{GS} = +ve$



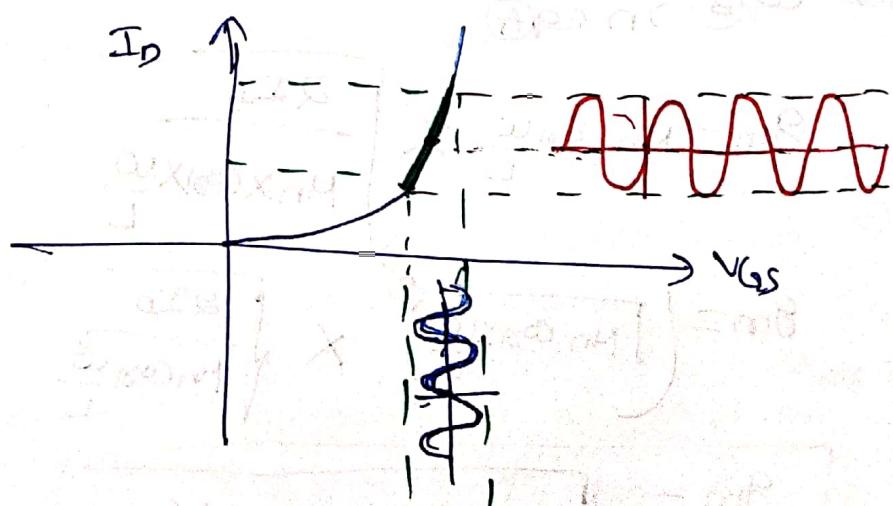
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T]^2 \quad I_D \propto (V_{GS} - V_T)$$

Saturation Region  $I_D \propto V_{GS}$

$V_{GS} \Rightarrow$  Supply voltage

$V_{GS}$  AC

$$V_{GS} = V_{GS,DC} + V_{GS,AC}$$



Current

$$\text{Linear Region } I_D = \frac{\mu_n C_{ox} W}{L} (V_{GS} - V_T) V_{DS}$$

$$I_D \propto (V_{GS}, V_{DS})$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad |_{V_{DS} \text{ constant}}$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \times [V_{GS} - V_T]^2$$

$$g_m \frac{\Delta I_D}{\Delta V_{GS}} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \times 2 \times [V_{GS} - V_T]$$

$$g_m = \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T] \rightarrow (A)$$

$$g_m = \sqrt{2 I_D \times \mu_n C_{ox} \frac{W}{L}}$$

$$W \cdot K \cdot t I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \times [V_{GS} - V_T]^2$$

$$V_{GS} - V_T = \sqrt{\frac{2 I_D}{\mu_n C_{ox} \frac{W}{L}}} \rightarrow (B)$$

Sub eq(B) in eq(A)

$$g_m = \mu_n C_{ox} \frac{W}{L} \times \frac{2 I_D}{\mu_n C_{ox} \frac{W}{L}}$$

$$g_m = \left( \sqrt{\mu_n C_{ox} \frac{W}{L}} \right) \times \frac{2 I_D}{\mu_n C_{ox} \frac{W}{L}}$$

$$g_m = \sqrt{2 I_D \times \mu_n C_{ox} \frac{W}{L}} \quad |_{\text{Amp} / \text{vaff}} \rightarrow (C)$$

$$g_m = \frac{2I_D}{V_{GS} - V_T}$$

$$\text{From eq (B)} \left( \frac{1}{\mu_n \cos \frac{\omega}{L}} \right) = \frac{(V_{GS} - V_T)^2}{2I_D}$$

$$\mu_n \cos \frac{\omega}{L} = \frac{2I_D}{(V_{GS} - V_T)^2} \rightarrow (D)$$

Sub eq (D) in (C)

$$g_m = \sqrt{2I_D \times \frac{2I_D}{(V_{GS} - V_T)^2}}$$

$$g_m = \frac{2I_D}{V_{GS} - V_T}$$

(3) Drain Resistance (or) Output Resistance  $[r_d \text{ (or) } r_o]$   
 It is the resistance offered by the MOSFET  
 in saturation region

$$r_d \text{ (or) } r_o = \frac{\Delta V_{DS}}{\Delta I_D} \quad | V_{GS} = \text{constant}$$

$$r_o = \frac{1}{\text{Slope of } \Delta I_D / \Delta V_{DS}} \quad | V_{GS} = \text{constant}$$

$\lambda$  = Channel length  
 modulation parameter

$V_A$  = Early voltage

$$r_o = \frac{V_A}{I_D} \text{ (or) } \frac{1}{A I_D} \quad | \lambda = \frac{1}{V_A}$$

When ~~early~~ channel length  
 modulation

Current

$$\text{after channel } \Delta I_D = \frac{1}{2} \mu n \cos \frac{\omega}{L} [V_{GS} - V_T]^2 \times [0 + \Delta V_{DS}]$$

length modulation

$$\frac{\Delta I_D}{\Delta V_{DS}} = \frac{1}{2} \mu n \cos \frac{\omega}{L} [V_{GS} - V_T]^2$$

$$r_o = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{\lambda} \times \frac{1}{\frac{1}{2} \mu n \cos \frac{\omega}{L} [V_{GS} - V_T]^2}$$

$$r_o = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{\lambda} \times \frac{1}{I_D}$$

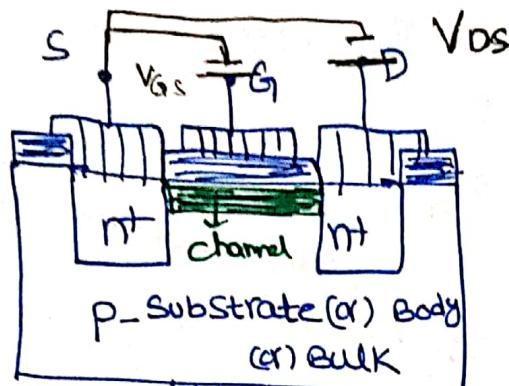
$$r_o = \frac{1}{\lambda I_D}$$

con

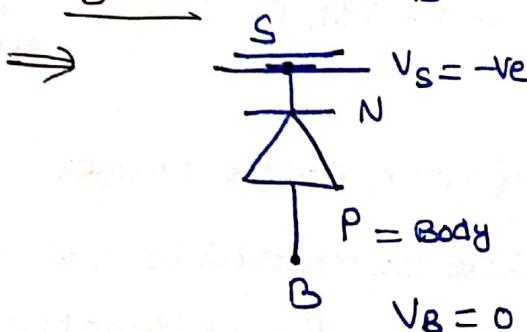
$$r_o = \frac{V_A}{I_D}$$

length modulation

## Body effect or Back gate effect:



Case(i)  $V_B > V_S$

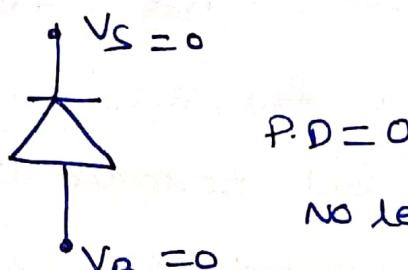


$V_B > V_S$

$V_{SB} < 0$

⇒ leakage current flows from Body to Source

Case(ii)  $V_S = V_B = 0$  X (  $V_S$  must be "ve" to make the to flow from S-D to create repulsive force)



to flow from S-D

to create repulsive force)

No leakage current flows from Body to Source

Clue

$\checkmark V_S = V_B \quad P.D = 0$   
No leakage from  $B \rightarrow S$

NOTE:

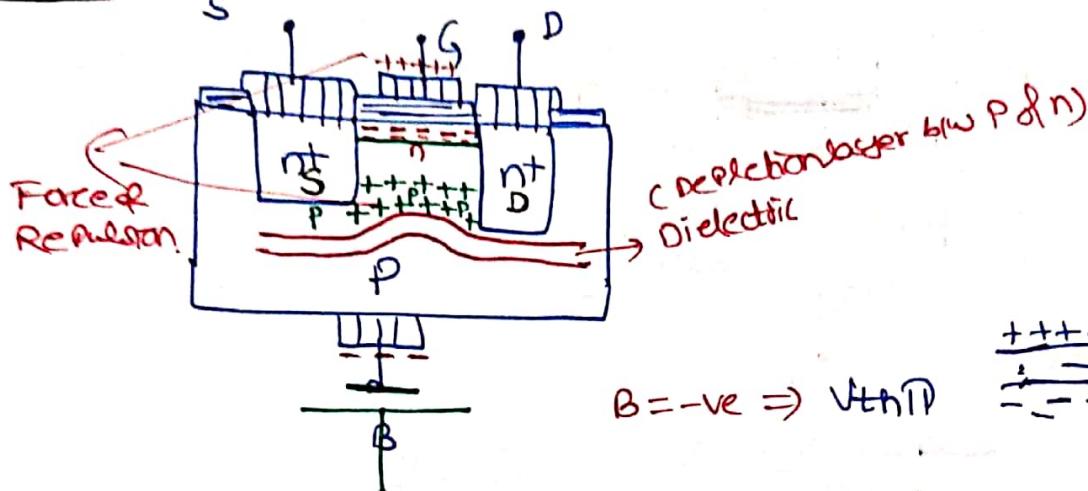
TO get zero leakage current from Body to Source

we are taking  $V_S = V_B$ , Source & Body terminals are tied to the same potential

Case(iii)

② Body = -ve

$$V_{SB} > 0 \Rightarrow V_S > V_B \quad (V_{SB} = +ve)$$



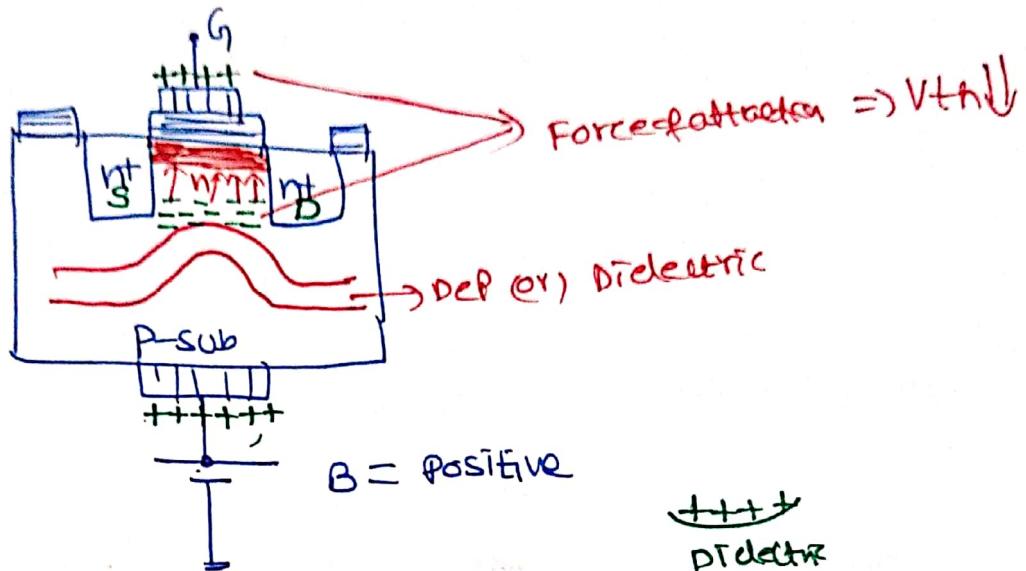
→ -ve terminal of Body is forming some positive charges across depletion Region (OR) Dielectric material becoz of Capacitor action, The positive charges formed due to the Capacitor action due to -ve bulk terminal will accumulate in b/w S & D. Due to this, force of repulsion has been established in b/w the gate & +ve charges in b/w S & D so to attract  $e^-$  from P-sub we need to apply more potential across Gate terminal which is nothing but  $V_{GS}$  to induce the channel which causes  $\uparrow$  in  $V_{th}$  (OR)  $V_T$

Note :

$V_{th}$  or  $V_T \uparrow$  on has to be increased to overcome the repulsive force in b/w positive charges accumulated on Gate & positive charges in b/w S & D (If Body = -ve)  $\Rightarrow (V_{SB} > 0) \Rightarrow V_T \uparrow$

Case IV  $V_{SB} < 0$  (or)  $V_{SB} = -ve$  (on Body = positive)  $V_S < V_B$

Body  $\Rightarrow$  Positive



$\begin{array}{c} + + + \\ \text{P-dielectric} \\ - - - \end{array}$

Note:

$V_T$  (or)  $V_{th}$   $\downarrow$  ie  $V_{GS}$  to be applied to attract

$e^-$  from P-sub decreases bcoz of ~~the~~ positive charges on Gate terminal & negative charges in b/w S&D

C If Body = +ve) when ( $V_{SB} < 0$ )  $\Rightarrow V_T \downarrow$

Note

Body terminal acts as a Gate (ie it is forming the +ve & -ve charges based on capacitor action) so this effect is called **BACK gate effect**

When

$$V_S \Rightarrow V_{SB} < 0 \Rightarrow V_T \downarrow$$

$$V_{SB} > 0 \Rightarrow V_T \uparrow$$

when  $V_{SB} > 0$   $V_T \uparrow$

$V_{SB} < 0$   $V_T \downarrow$

$$V_T' = V_{T_0} + \beta \left[ \sqrt{V_{SB} + \phi_s} - \sqrt{\phi_s} \right]$$

new  
threshold  
voltage becoz of  
body effect

$V_T'$   $\Rightarrow$  new threshold voltage becoz of body effect

$V_{T_0}$   $\Rightarrow$  Threshold voltage when body is not biased

$\beta$   $\Rightarrow$  Body effect parameter

$V_{SB}$  = source to body voltage

$\phi_s$  = surface potential

$$\phi_s = V_t \ln \left( \frac{N_A}{n_i^2 / N_A} \right)$$

$$\phi_s = V_t \ln \left( \left( \frac{N_A}{n_i} \right)^2 \right)$$

$$\phi_s = 2V_t \ln \left( \frac{N_A}{n_i} \right)$$

$$\phi_s = 2\phi_{bulk}$$

NOTE

\* when  $V_{SB} \uparrow$  (true)  $V_T \uparrow$  & when  $V_{SB} \downarrow$  (-ve)  $V_T \downarrow$

$$\text{so } V_T \propto \sqrt{V_{SB} + \dots}$$

$$V_T^I = V_{TO} + \mu \left[ \sqrt{V_{SB} + \varphi_S} - \sqrt{\varphi_S} \right]$$

when  $V_{SB} = 0V$

$$V_S = V_B$$

so Body are tied to the same potential

$$V_T^I = V_{TO} + \mu \left[ \sqrt{0 + \varphi_S} - \sqrt{\varphi_S} \right]$$

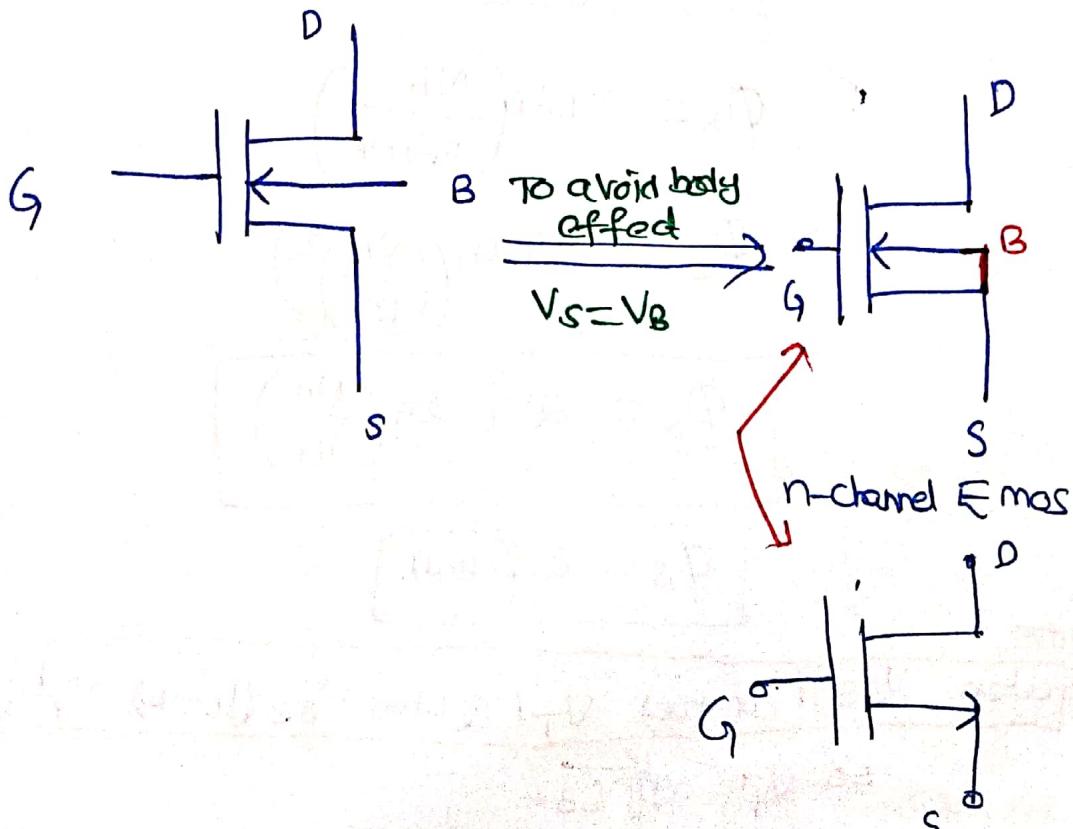
$$V_T^I = V_{TO} + \mu \left[ \sqrt{\varphi_S} - \sqrt{\varphi_S} \right]$$

$$V_T^I = V_{TO}$$

Note!

while manufacturing IC's so Bulk are tied together to the same potential to avoid charges (Q)

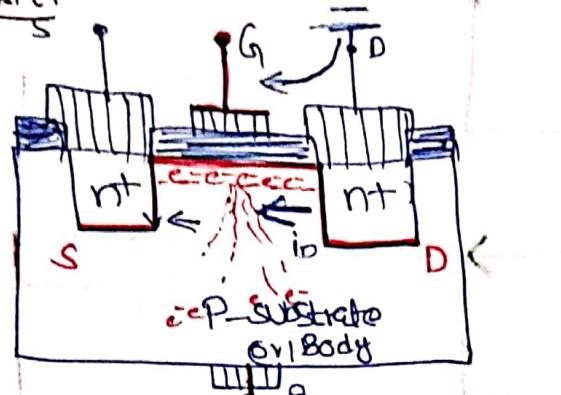
Variations in  $V_T$



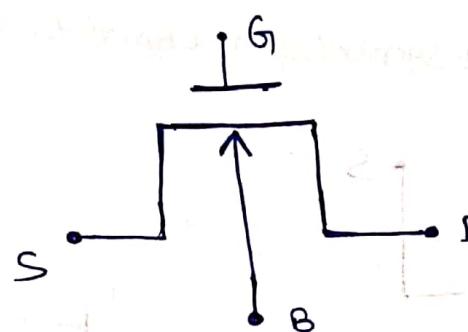
# Circuit symbol (or) Schematic diagram of MOSFET

1

Enhancement mosFET

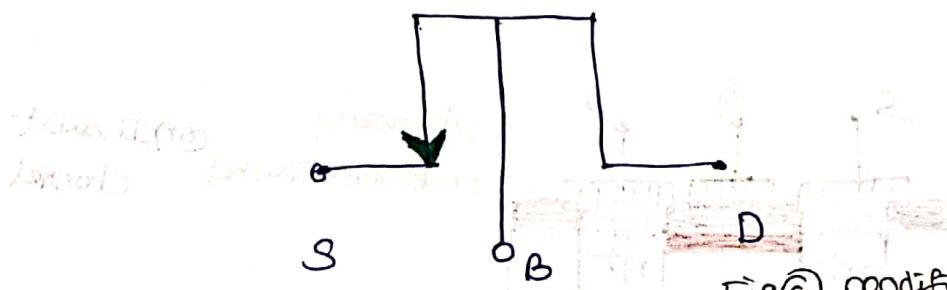


Fig@ h Emos (or) n-channel Enhancement mos

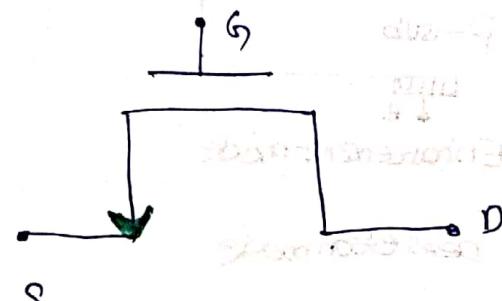


Fig@ n-channel E mos ckt symbol

Arrow head on Body line indicates  $\Rightarrow$  Type of channel or Type of Substrate & also indicates the Channel is n-type



Fig@ modified symbol



Fig@ Finalized symbol of n-Emos

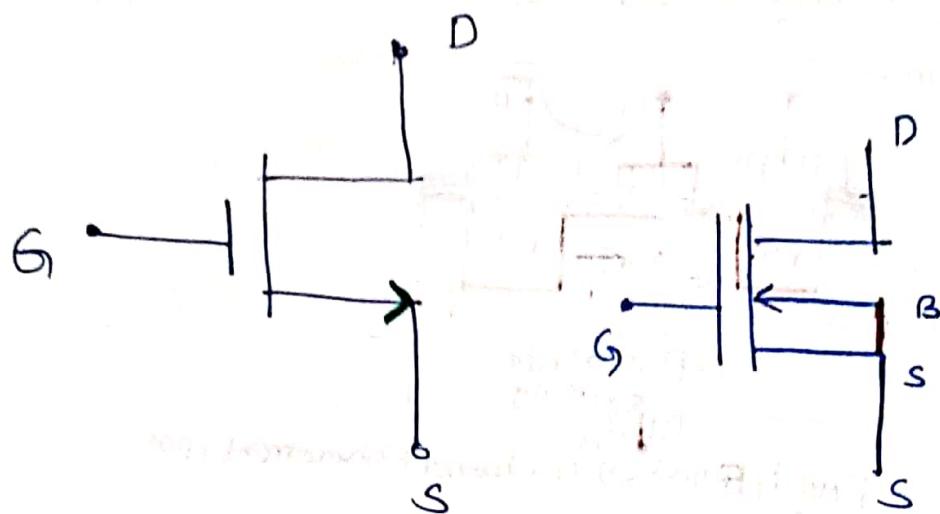


Fig ⑥ : ckt symbol of n-channel Enhancement MOSFET

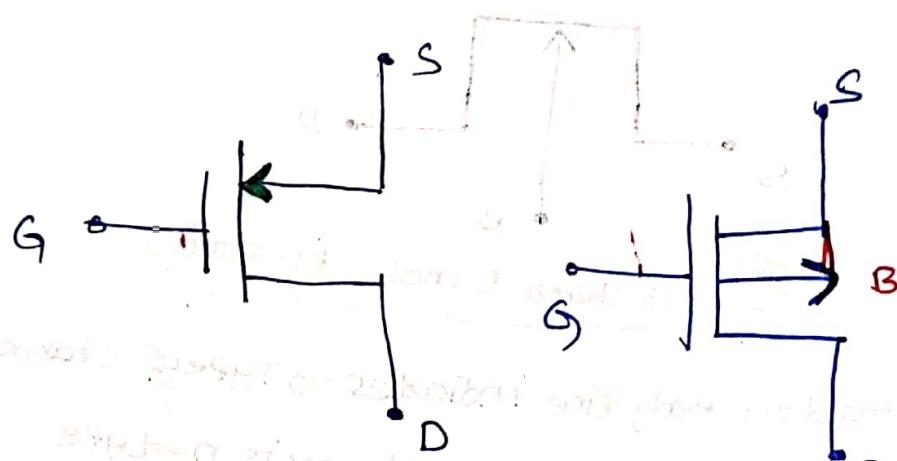
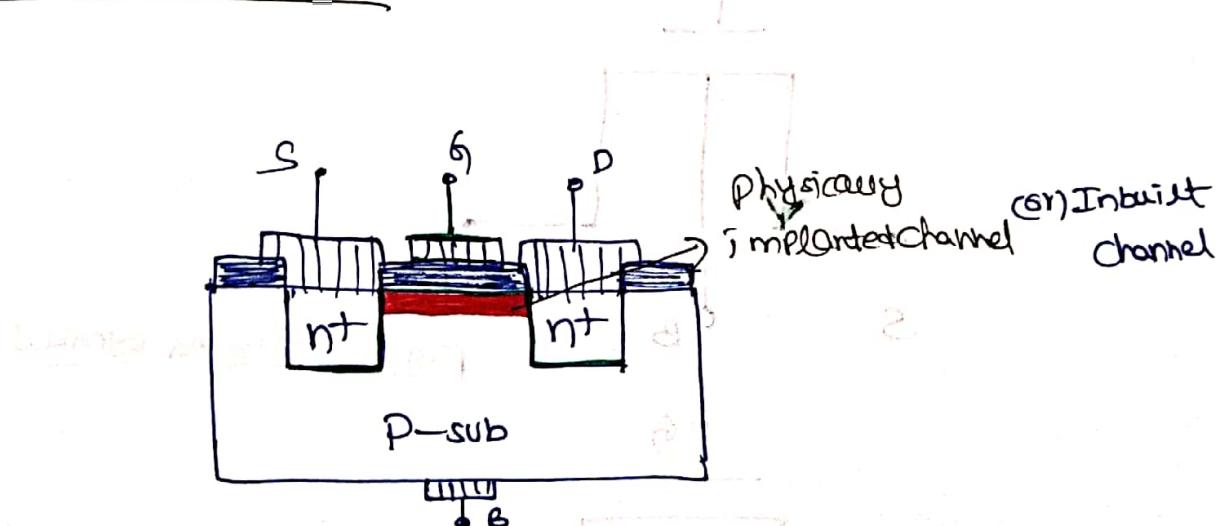


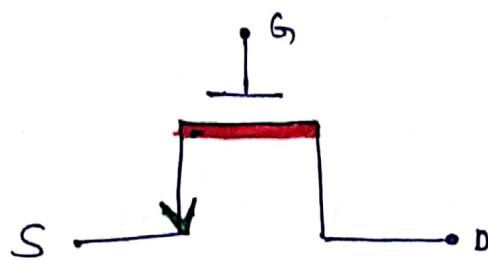
Fig ⑦ : ckt symbol of p-channel Enhancement MOSFET

### Depiction type of MOSFET

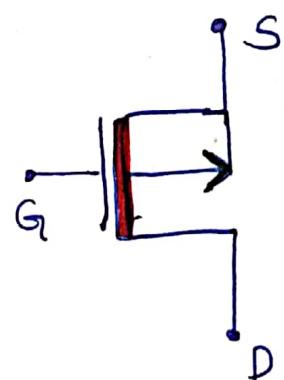
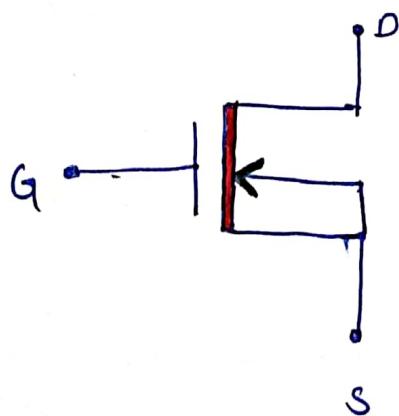
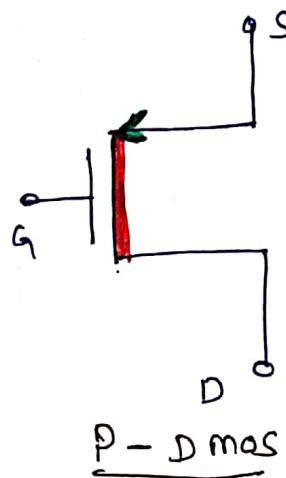
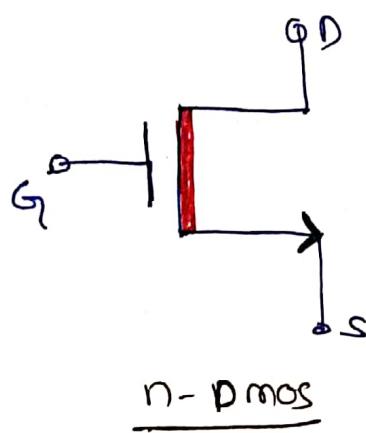


$V_{GS} = +ve \Rightarrow$  Enhancement mode

$V_{GS} = -ve \Rightarrow$  depletion mode



FIG(A) ckt symbol for n-channel DMos



## Biasing of MOSFETs

⇒ Applying zero signal voltage (or) DC voltage to set a Q-Point (or) Operating point (or) Quiescent point

MOSFET - Q( $V_{DSQ}$ ,  $I_{DQ}$ )

Q( $V_{CEQ}$ ,  $I_{CQ}$ )  $\Rightarrow$  BJT

S - E

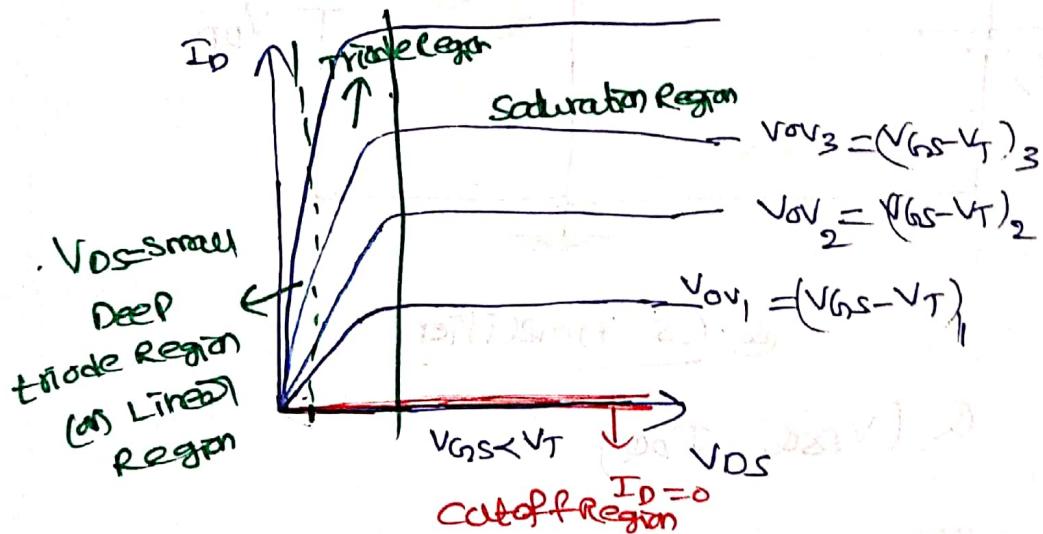
G - B

D - C

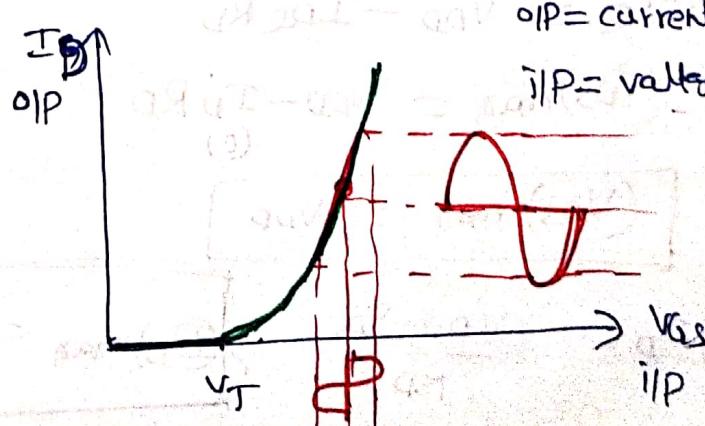
⇒ Q-Point is to make the MOSFET to act as an Amplifier

⇒ ~~MOSFET acts as an Amplifier in Saturation Region~~

⇒ MOSFET ~~as a Switch in Linear Region & Cutoff Region~~



⇒ MOSFET acts as a constant current source in saturation region [In the absence of channel length modulation]



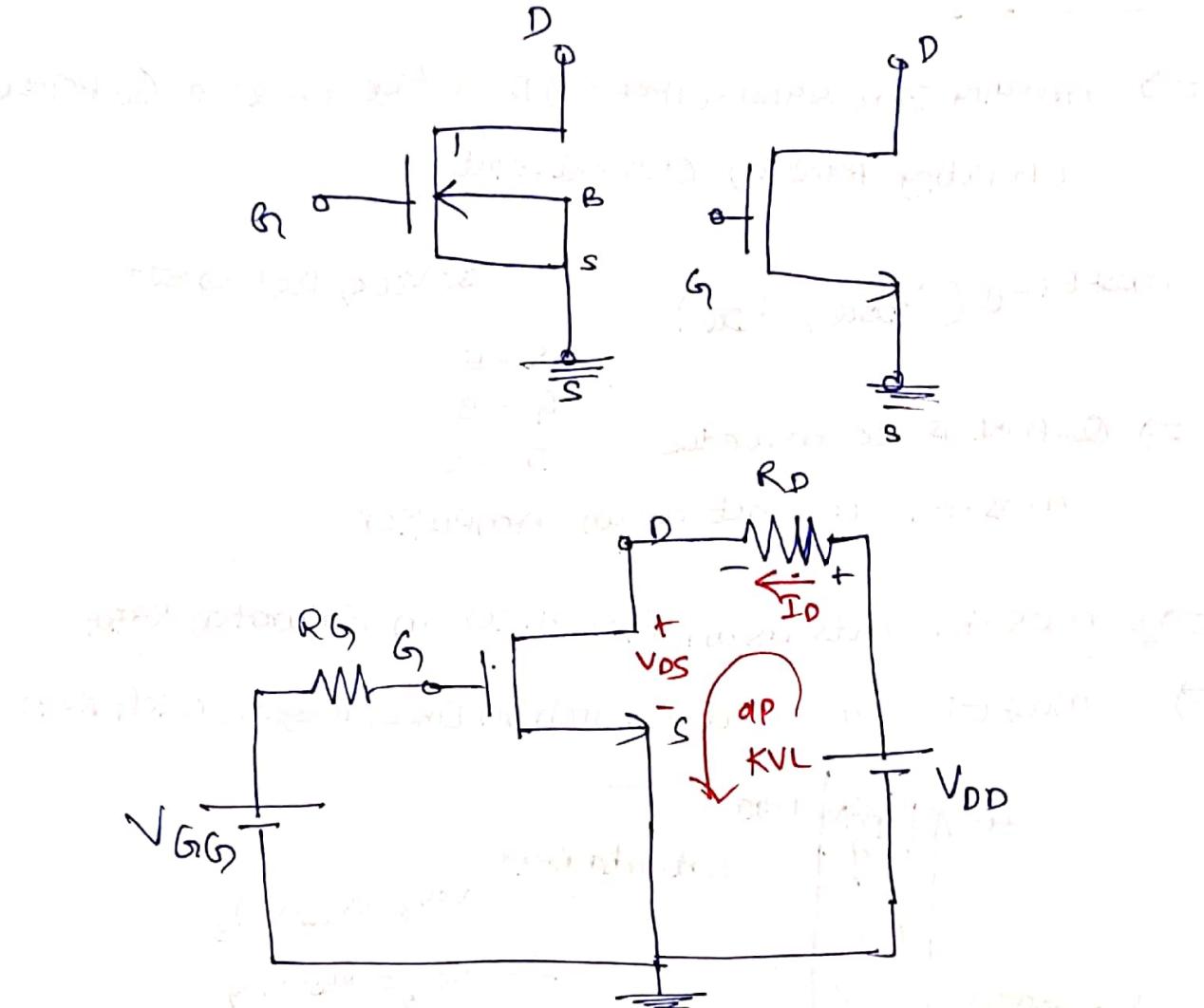
$\text{I}_{OP} = \text{current} = C_S$

$\text{V}_{IP} = \text{voltage} = V_C$

**VCCS**

Voltage  
controlled  
current  
source

## 2) FET as an amplifier



### ② CS Amplifier

Q ( $V_{DSQ}$ ,  $I_{DQ}$ )

O/P KVL

$$-V_{DD} + I_D R_D + V_{DS} = 0 \rightarrow \textcircled{1}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{DSQ} = V_{DD} - I_{DQ} R_D$$

$$(V_{DS})_{max} = V_{DD} - I_D R_D \quad \text{(i)}$$

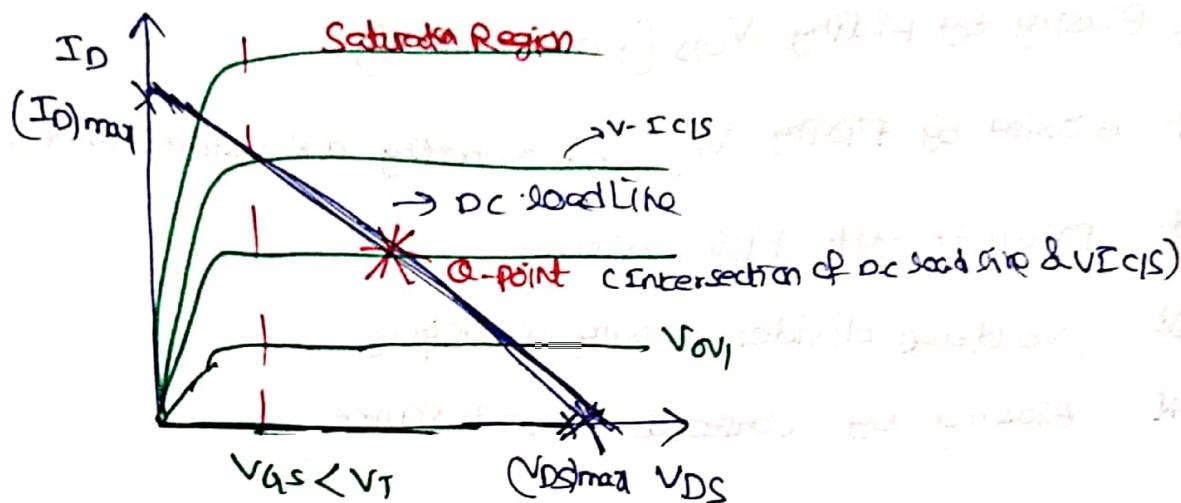
$$(V_{DS})_{max} = V_{DD}$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D}$$

$$(I_D)_{max} = \frac{V_{DD}}{R_D}$$

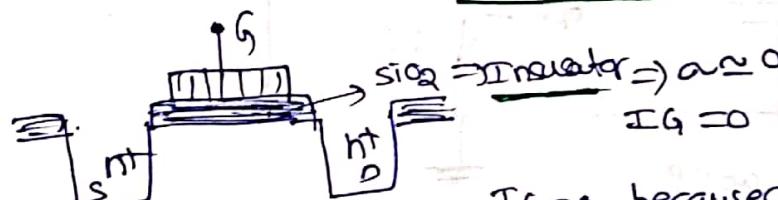
## DC load Line of MOSFET

2



⇒ MOSFET is a unipolar device  $\Rightarrow I_D$  due to  $e^-$  s only  
 Reverse saturation current = 0

⇒ Gate current of MOSFET  $I_G = 0$



In MOSFET

⇒ Thermal stability is high compared to BJT  
 (we do not have minority charge carriers)

⇒ MOSFET  $V_T$  &  $\mu_n$  depends on Temperature  
 $(\beta, I_C, V_{BE} \text{ depends on Temp})$

$$V_T \& \mu_n \Rightarrow f(\text{Temperature})$$

⇒ Size of MOSFET is less compared to BJT & power dissipation is low in MOSFET compared to BJT

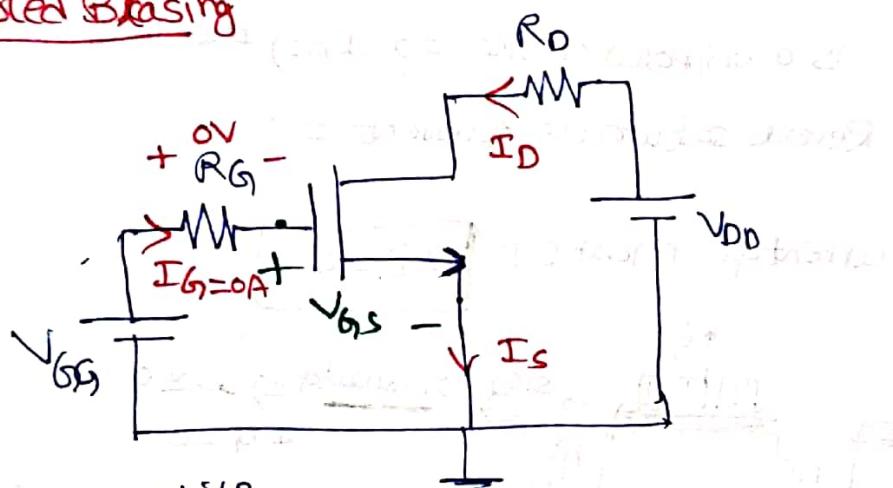
(mosfet  $\Rightarrow$  minority conc. very very low)

power dissipation is low in mosfet

# Biasing Techniques of MOSFET

- \* Biasing by fixing  $V_{GS}$  [Fixed Biasing]
- \* Biasing by fixing  $V_G$  and connecting a resistance in the source
- \* Drain to Gate FIB Resistance
- \* Voltage divider Biasing Technique.
- \* Biasing by constant current source

## Fixed Biasing

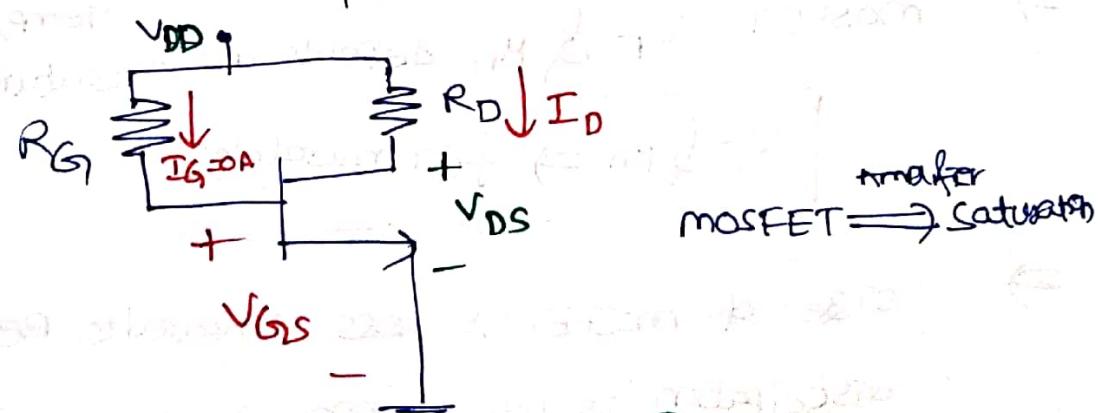


Applying KVL at (P)

$$-V_{GS} + I_G R_G + V_{GS} = 0$$

$$-V_{GS} + 0 + V_{GS} = 0$$

$V_{GS} = V_{GS}$   $\Rightarrow$  Fixed  $V_{GS}$



$$I_D = \frac{1}{2} \mu n C_{ox} W (V_{GS} - V_T)^2$$

$I_D \propto$  (Saturation Region)

MOSFET acts as Amplifier

$$I_D = k_n [V_{GS} - V_T]^2$$

where  $k_n = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \text{Amp/V}^2$

MOSFET Transconductance Parameter

$$I_{DQ} = k_n [V_{GS} - V_T]^2$$

$$V_{DS} \geq V_{GS} - V_T \rightarrow \text{MOSFET in saturation region}$$

$V_{DSQ} \rightarrow$  Apply to top side

$$V_{DD} = I_{DRD} + V_{DS}$$

$$V_{DSQ} = V_{DD} - I_{DQ} R_D$$

$\alpha (V_{DSQ}, I_{DQ})$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T]^2$$

$C_{ox}, \frac{W}{L}, V_T$  vary among the devices

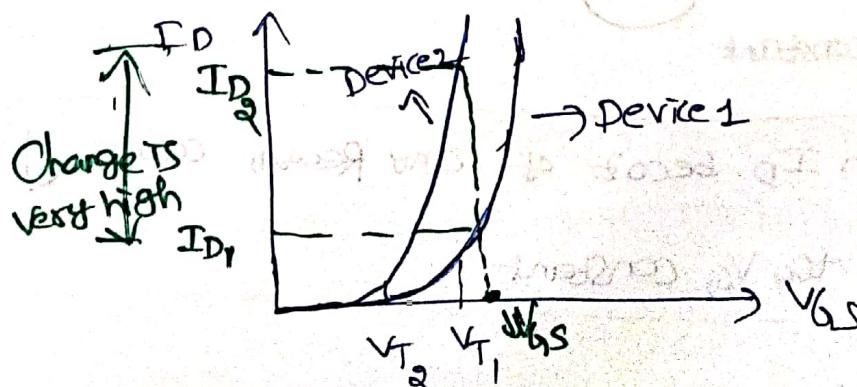
even though they are of same

size & type

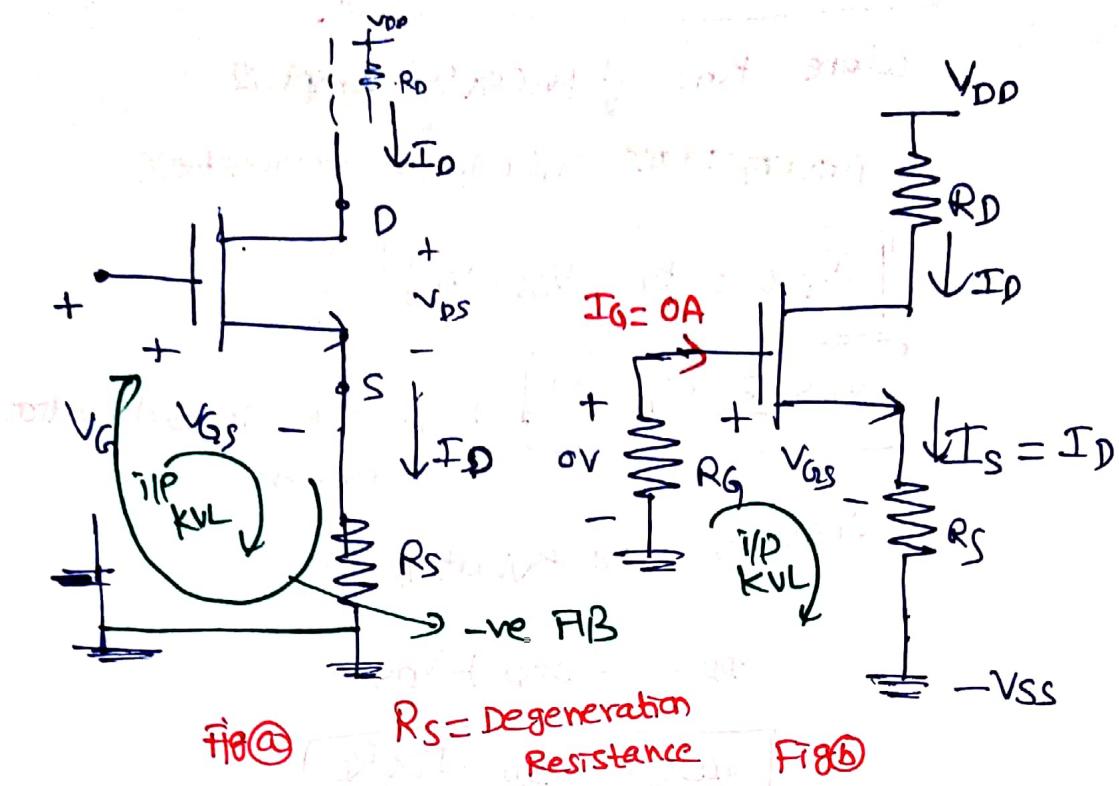
MOSFETs  $\xrightarrow{\text{Fabricated}}$  on different wafers

$\mu_n \& V_T \Rightarrow$  vary w.r.t. temp

$\Rightarrow$  Because of this fixed  $V_{GS} \Rightarrow I_D$  will change among devices



## ② Biasing by Fixing $V_G$ and connecting a Resistance in the source



$$V_{DS} \geq V_{GS} - V_t$$

$$I_D = k_n (V_{GS} - V_t)^2$$

$$V_G = V_{GS} + I_S R_S$$

$$V_G = V_{GS} + I_D R_S$$

Fixed

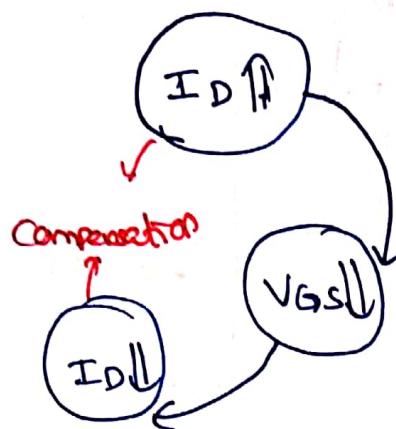
If  $I_D \uparrow$  becoz of any reason (con,  $W_t$ ,  $W$ ,  $M_n$  &  $V_t$ )

$$V_G = V_{GS} + I_D R_S$$

To make  $V_G$  constant

★ Increase in  $I_D$  becoz of any reason causes  $\uparrow$  in  $V_{GS}$  to fix the  $V_G$  constant.

4  
 $\downarrow V_{GS}$  causes  $\rightarrow I_D \downarrow$



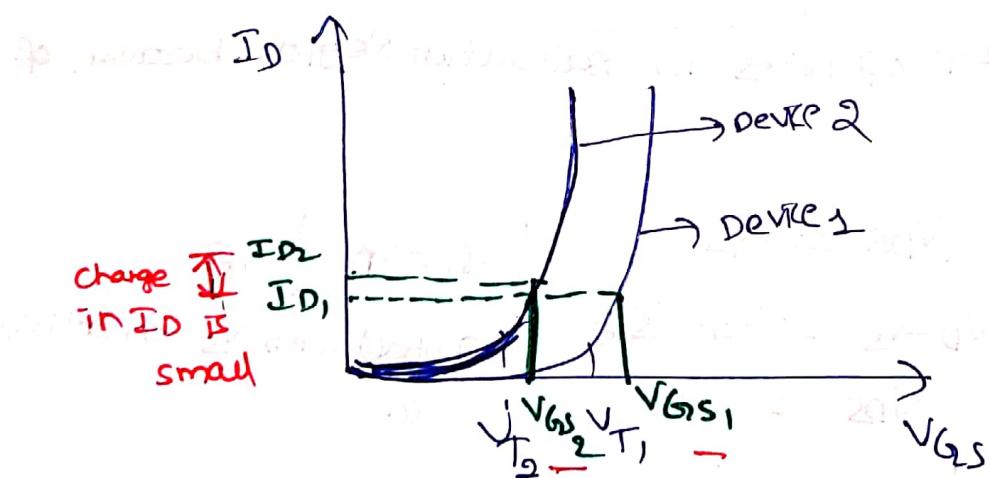
$$V_G = V_{GS} + I_D R_S$$

$$I_{DQ} = \frac{V_G - V_{GS}}{R_S} \rightarrow \text{Regeneration Resistance}$$

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

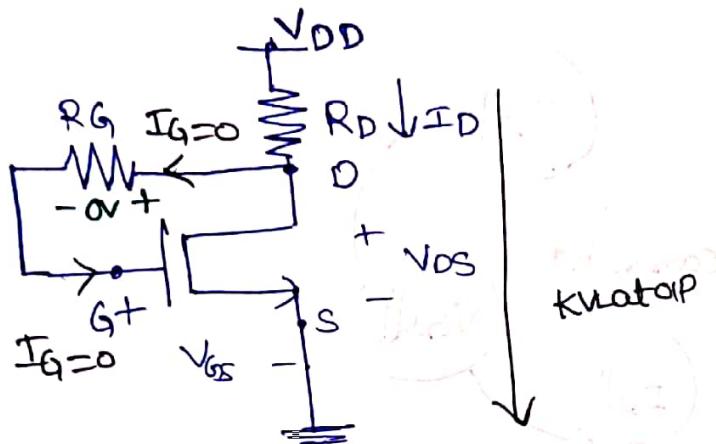
$$V_{DSQ} = V_{DD} - I_{DQ} (R_D + R_S)$$

Q (V<sub>DSQ</sub>, I<sub>DQ</sub>)



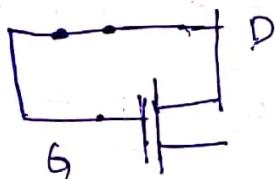
→ Charge in  $I_D$  (or) variation in  $I_D$  is small when  $V_{GS}$  is not constant, so it is preferable technique to bias the MOSFET

③ Biasing with Drain to gate Feedback Resistance:



\*  $I_G = 0$ , because of high input impedance of MOSFET

⇒ Since  $I_G = 0$ ,  $I_G R_G = 0V$ , Gate & drain are connected together because of  $I_G R_G = 0V$



$$V_G = V_D$$

⇒ MOSFET operates in saturation Region because of  $V_G = V_D$

$$V_{DS} = V_{GS}$$

$$V_G = V_D \rightarrow \textcircled{A}$$

$$V_D - V_S = V_G - V_S \leftarrow \text{subtract with } V_S \text{ on both sides}$$

$$V_{DS} = V_{GS}$$

\textcircled{A}

$V_{GS} < V_T \Rightarrow$  cutoff Region

MOSFET operates in  
Saturation Region

$V_{DS} < V_{GS} - V_T$ ; Linear Region

$V_{DS} \geq (V_{GS} - V_T)$  Saturation Region

NOTE :

Whenever the gate & drain terminals are connected together then MOSFET operates in saturation Region

$$I_D = K (V_{GS} - V_T)^2$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

$$I_{DQ} = K (V_{GS} - V_T)^2$$

$$V_{DSQ} = ?$$

By applying KVL at op side

$$V_{DD} = I_D R_D + V_{DS}$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_{DSQ} = V_{DD} - I_{DQ} R_D$$

$$V_{DS} = V_{GS} = V_{DD} - I_{DQ} R_D$$

$$V_D = V_G \Rightarrow V_{DS} = V_{GS}$$

$$Q (V_{DSQ}, I_{DQ})$$

$$V_{DD} = I_D R_D + V_{GS}$$

↓  
constant

$$I_P \quad I_D \uparrow \downarrow$$

$$V_{GS} \uparrow \downarrow$$

$$I_D \uparrow \downarrow$$

Compensated

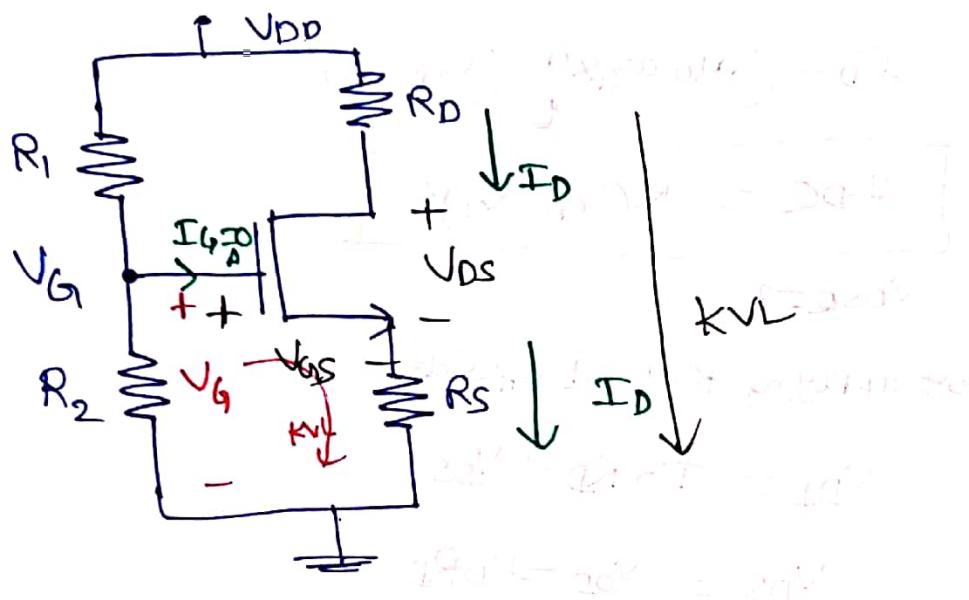
the effect of  
↑ in  $I_D$  by  
↓  $V_{GS}$

NOTE :  $R_G$  ( $D - G$ ) = FIB Resistor, provided the Compensation  
for ↑ in  $I_D$  (or)  $R_G$  works to keep the  $I_D$  constant

## Drawback of D-G FET Resistor

⇒ OIP voltage swing is limited

### ④ Voltage divider biasing Technique:-



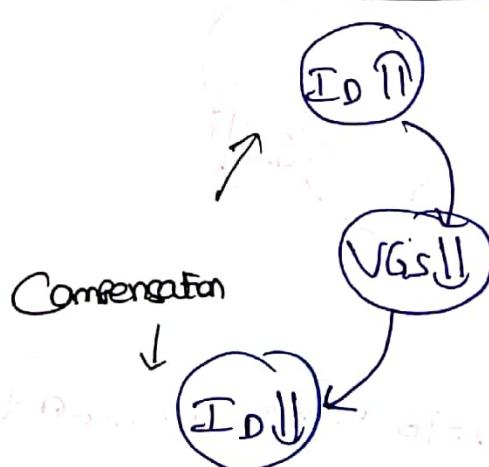
$$V_G = \frac{V_{DD} \times R_2}{R_1 + R_2}$$

$$V_G = V_{GS} + I_D R_S$$

$$I_D = K(V_{GS} - V_t)^2$$

$$I_{DQ} = K(V_{Gr} - V_t)^2$$

$$I_D = \frac{V_G - V_{GS}}{R_S}$$



(To make  $V_G$  constant)

$V_G \approx$  constant becoz of  
 $V_{DD}$  supply)

By KVL at O/P side

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

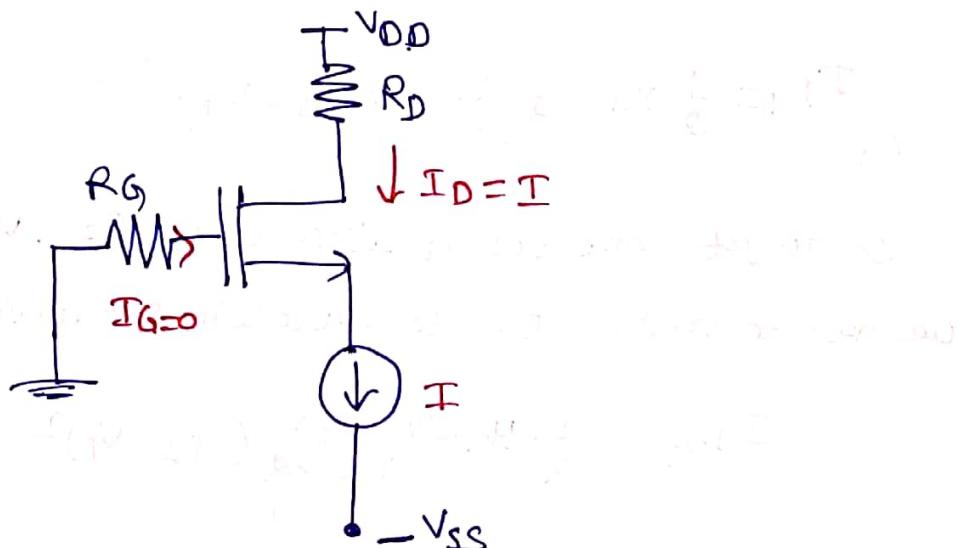
$$V_{DD} = I_D (R_D + R_S) + V_{DS}$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

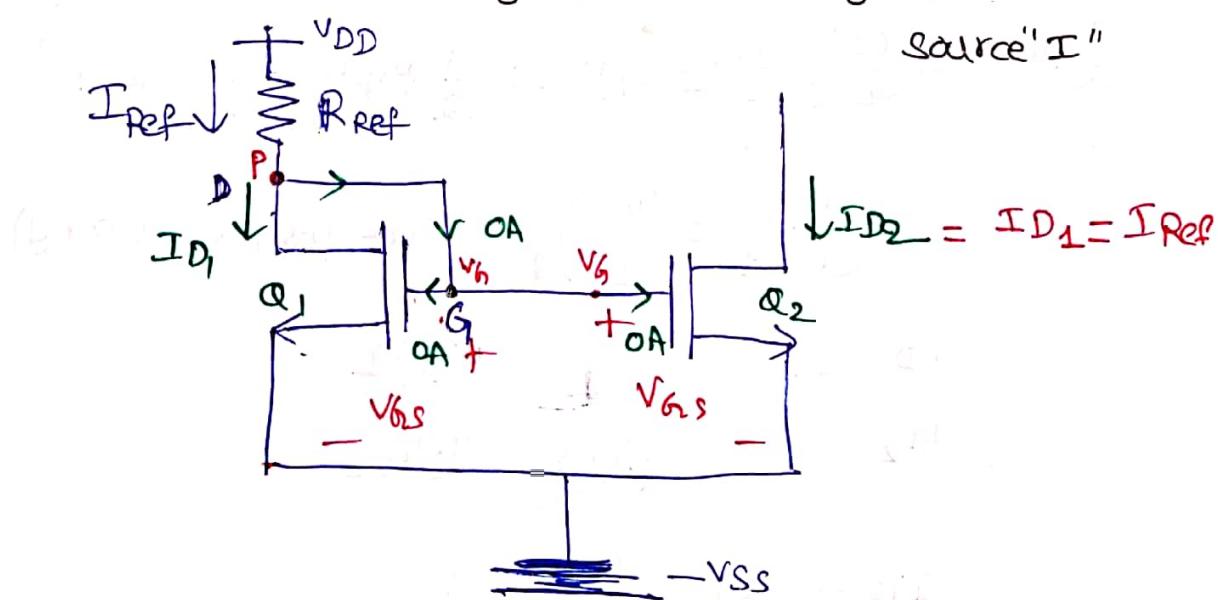
$$V_{DSQ} = V_{DD} - I_D (R_D + R_S)$$

$$Q(V_{DSQ}, I_DQ)$$

④ Biasing by using a constant current source



Fig@ Biasing the MOSFET using a constant current source 'I'





$I_{Ref} = I_{D1}$ , because 'OA' Gate current flowing through MOSFETs  $Q_1$  &  $Q_2$

APPLY KCL at P

$$+I_{D1} \leftarrow I_{Ref} + OA = 0$$

$$\boxed{I_{Ref} = I_{D1}}$$

$Q_1$  operates in saturation region, since we have tied gate & drain terminals  $V_{GS} = V_D$

$$I_{D1} = \frac{1}{2} \mu_n \cos\left(\frac{w}{L}\right)_1 (V_{GS} - V_T)^2$$

So to get same current at the drain of  $Q_2$  as  $Q_1$ , then we have to make  $Q_2$  to operate in saturation region

$$I_{D2} = \frac{1}{2} \mu_n \cos\left(\frac{w}{L}\right)_2 (V_{GS} - V_T)^2$$

$$I_{D1} = I_{D2}$$

~~$$\frac{1}{2} \mu_n \cos\left(\frac{w}{L}\right)_1 (V_{GS} - V_T)^2 = \frac{1}{2} \mu_n \cos\left(\frac{w}{L}\right)_2 (V_{GS} - V_T)^2$$~~

$$\left(\frac{w}{L}\right)_1 = \left(\frac{w}{L}\right)_2 \quad (\text{not possible practically})$$

$$\frac{I_{D1}}{I_{D2}} = \frac{\left(\frac{w}{L}\right)_1}{\left(\frac{w}{L}\right)_2} \quad \frac{\left(\frac{w}{L}\right)_1}{\left(\frac{w}{L}\right)_2}$$

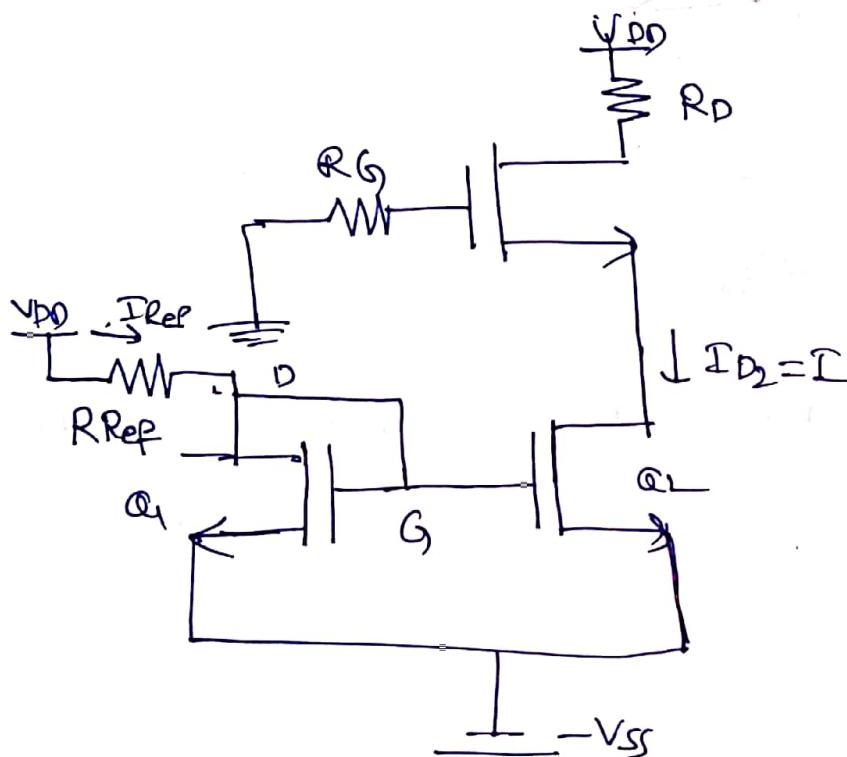
$$I_{D2} = I_{D1} \left( \frac{\left(\frac{w}{L}\right)_2}{\left(\frac{w}{L}\right)_1} \right)$$

$$I_{D2} = I_{D1} \frac{(\omega L)_2}{(\omega L)_1}$$

$$I_{D2} = I$$

$$I_{D1} = I_{Ref}$$

$$-I = I_{Ref} \frac{(\omega L)_2}{(\omega L)_1}$$



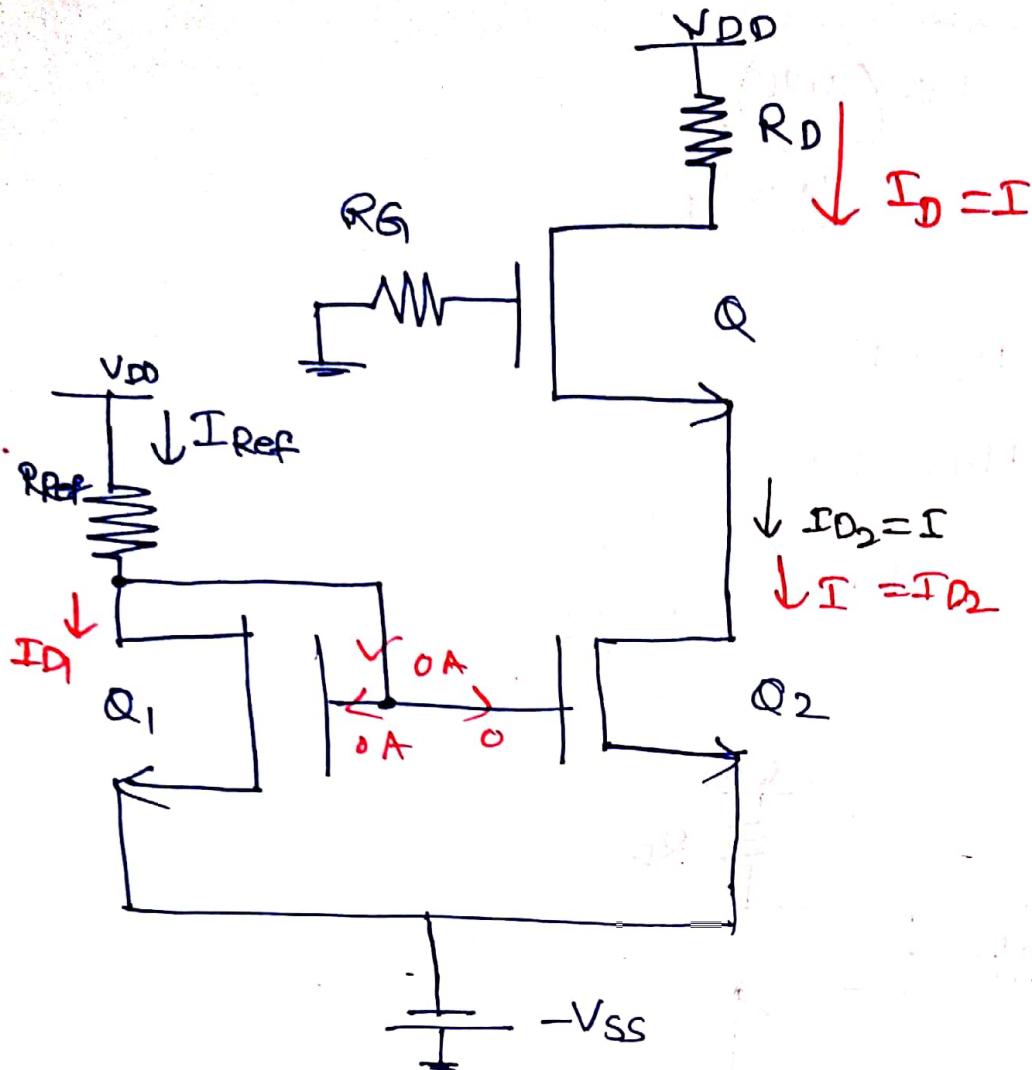


FIG A Biasing of MOSFET using current mirrors

- ⇒ It is an efficient technique to provide biasing to the MOSFET
- ⇒  $I_D$  compensation has been provided & voltage swing at the output will be high
- ⇒ while manufacturing IC, this technique will be used to reduce the power dissipation due to passive loads

## Parameters of Enhancement MOSFET

$$I_D = \mu_n \frac{C_w}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad \text{Triode Region}$$

$$I_D = K_n \frac{C_w}{L} \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$I_D = K_n \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$I_D = K_n \left[ (V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad \text{Triode Region}$$

Linear (or) Deep Triode Region

$$I_D = K_n [V_{GS} - V_T] V_{DS}$$

$$I_D = \mu_n \frac{C_w}{L} [V_{GS} - V_T] V_{DS}$$

Saturation Region

$$I_D = \frac{1}{2} \mu_n \frac{C_w}{L} [V_{GS} - V_T]^2$$

$$I_D = \frac{1}{2} K_n [V_{GS} - V_T]^2$$

### Parameters

① Drain ON Resistance (or) ON Resistance (or) Drain to Source Resistance

Resistance offered by MOSFET in Linear Region.

$I_D$  = For small  $V_{DS}$  values

$$I_D = \mu_n \frac{C_w}{L} [V_{GS} - V_T] V_{DS}$$

$r_{DS(on)}$  (or)  $R_{DS(on)}$  (or)  $r_d$  (or)  $R_d$  (or)  $r_{DS(on)}$

$$\gamma_{ds(on)} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{\frac{1}{\mu_n C_o x} (V_{GS} - V_T)}{\frac{\Delta I_D}{\Delta V_{DS}}}$$

$$I_D = \mu_n C_o \frac{w}{L} [V_{GS} - V_T] V_{DS}$$

$$\gamma_{ds(on)} = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}}$$

$$\frac{\partial I_D}{\partial V_{DS}} = \mu_n C_o \frac{w}{L} [V_{GS} - V_T] \quad (1)$$

$$\left( \frac{1}{\gamma_{ds(on)}} \right) = \frac{\partial I_D}{\partial V_{DS}} = \mu_n C_o \frac{w}{L} [V_{GS} - V_T]$$

$$\gamma_{ds(on)} = \left( \frac{\partial I_D}{\partial V_{DS}} \right) = \frac{1}{\mu_n C_o \frac{w}{L} [V_{GS} - V_T]}$$

Linear Region

In Linear Region

$$\gamma_{ds(on)} \propto R \propto \frac{1}{\left( \frac{w}{L} \right) \text{aspect ratio}}$$

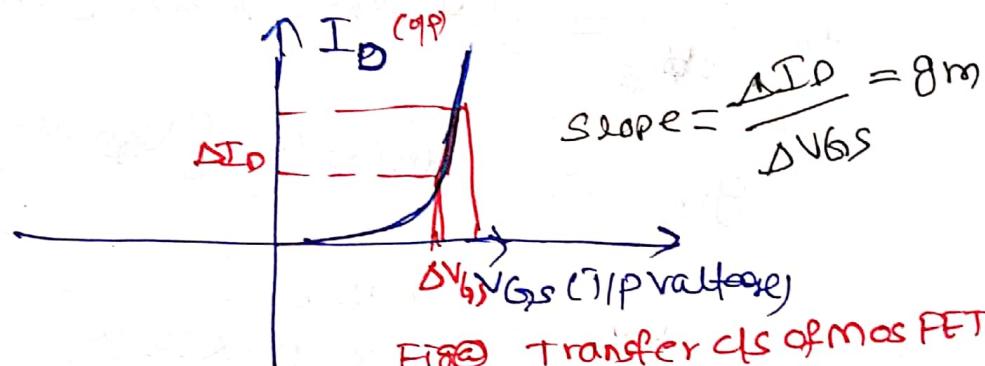
$$R \propto \frac{1}{\text{aspect ratio} \left( \frac{w}{L} \right)}$$

## Q2) Transconductance ( $g_m$ ) [ $g_m$ is used for amplifiers ]

$$g_m = \frac{\text{Output current}}{\text{Input voltage}} \quad [ g_m \Rightarrow \text{Insaturation Region only} ]$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \text{slope of TIF of mosFET}$$

$g_m \Rightarrow$  Transfer I-V of mosFET



n-channel  $\Rightarrow V_{GS} = +ve$



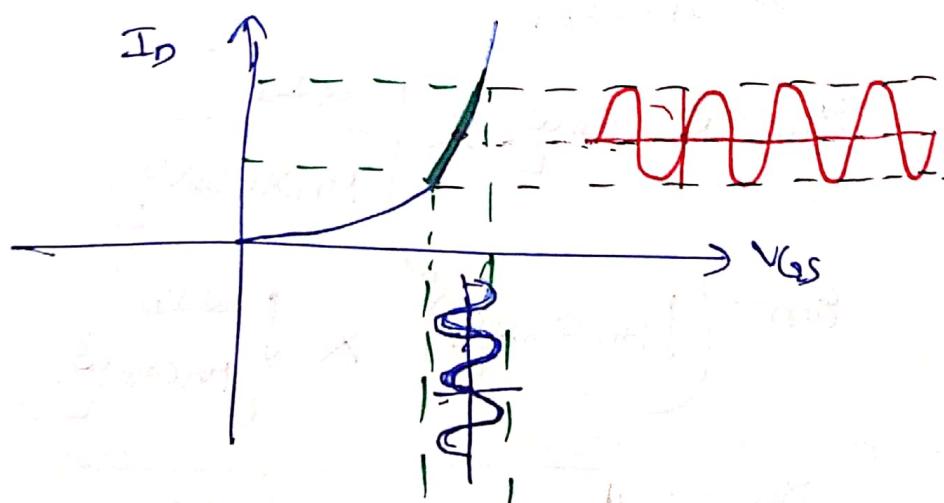
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} [V_{GS} - V_T]^2 \quad [ \text{Saturation Region} ] \quad I_D \propto (V_{GS} - V_T)^2$$

Saturation Region  $I_D \propto V_{GS}$

$V_{GS} \xrightarrow{\text{DC}} \text{Supply voltage}$

$V_{GS} \xrightarrow{\text{AC}}$

$$V_{GS} = V_{GS, \text{DC}} + V_{GS, \text{AC}}$$



Current

$$\text{Linear Region} \quad I_D = \frac{\mu_n C_{ox} W}{L} (V_{GS} - V_T) V_{DS}$$

$$I_D \propto (V_{GS}, V_{DS})$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad | \quad V_{DS} \text{ constant}$$

$$I_D = \frac{1}{2} Mn \cos \frac{w}{L} \times [V_{GS} - V_T]^2$$

$$g_m \frac{\Delta I_D}{\Delta V_{GS}} = \frac{1}{2} Mn \cos \frac{w}{L} \times 2 \times [V_{GS} - V_T]$$

$$g_m = Mn \cos \frac{w}{L} [V_{GS} - V_T] \rightarrow \textcircled{A}$$

$$g_m = \sqrt{2 I_D \times Mn \cos \frac{w}{L}}$$

$$w.k.t I_D = \frac{1}{2} Mn \cos \frac{w}{L} \times [V_{GS} - V_T]^2$$

$$V_{GS} - V_T = \sqrt{\frac{2 I_D}{Mn \cos \frac{w}{L}}} \rightarrow \textcircled{B}$$

Sub eqn \textcircled{B} in eqn \textcircled{A}

$$g_m = Mn \cos \frac{w}{L} \times \frac{2 I_D}{Mn \cos \frac{w}{L}}$$

$$g_m = \left( \sqrt{Mn \cos \frac{w}{L}} \right)^2 \times \sqrt{\frac{2 I_D}{Mn \cos \frac{w}{L}}}$$

$$g_m = \sqrt{2 I_D \times Mn \cos \frac{w}{L}} \quad | \quad \text{amp} | \text{vaff} \rightarrow \textcircled{C}$$

$$g_m = \frac{2I_D}{V_{GS} - V_T}$$

From eq (B)  $\left( \frac{1}{\mu_n \cos \omega_L} \right) = \frac{(V_{GS} - V_T)^2}{2I_D}$

$$\mu_n \cos \omega_L = \frac{2I_D}{(V_{GS} - V_T)^2} \rightarrow (D)$$

Sub eq (D) in (C)

$$g_m = \sqrt{2I_D \times \frac{2I_D}{(V_{GS} - V_T)^2}}$$

$$g_m = \frac{2I_D}{V_{GS} - V_T}$$

③ Drain Resistance (or) Output Resistance ( $r_d$  or)  $r_o$ )  
 It is the resistance offered by the MOSFET  
 in saturation region  $(r_o = \infty = \frac{\Delta V_{DS}}{\Delta I_D} = \infty)$

$$r_d \text{ (or) } r_o = \frac{\Delta V_{DS}}{\Delta I_D} \quad | V_{GS} = \text{constant}$$

$$r_o = \frac{1}{\text{slope of } \text{OIP V/I C/S}} \quad | V_{GS} = \text{constant}$$

$\lambda$  = Channel length

modulation parameter

$V_A$  = Early voltage

$$r_o = \frac{V_A}{I_D} \text{ (or) } \frac{1}{A I_D} \quad \left[ \because \lambda = \frac{1}{V_A} \right]$$

When ~~early~~ channel length  
modulation

Current

$$\text{after channel } \Delta I_D = \frac{1}{2} \mu n \cos \frac{\omega}{L} [V_{GS} - V_T]^2 \times [0 + \Delta V_{DS}]$$

length modulation

$$\cancel{\Delta I_D} = \frac{1}{2} \mu n \cos \frac{\omega}{L} [V_{GS} - V_T]^2$$

$$r_o = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{\lambda} \times \frac{1}{\frac{1}{2} \mu n \cos \frac{\omega}{L} [V_{GS} - V_T]^2}$$

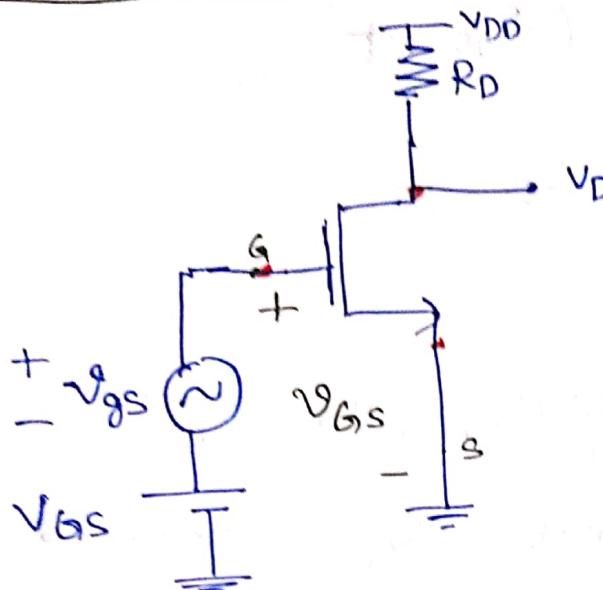
$$r_o = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{\lambda} \times \frac{1}{I_D}$$

$$\boxed{r_o = \frac{1}{\lambda I_D}}$$

con

$$\boxed{r_o = \frac{V_A}{I_D}}$$

## Small signal model of MOSFET :



$v_{gs} = \text{Ac} \cdot \text{ip voltage (or) signal i/p}$

$V_{GS} = \text{D.C voltage (or) DC Bias voltage}$

$v_{GS} = \text{Voltage measured b/w G & S terminals}$

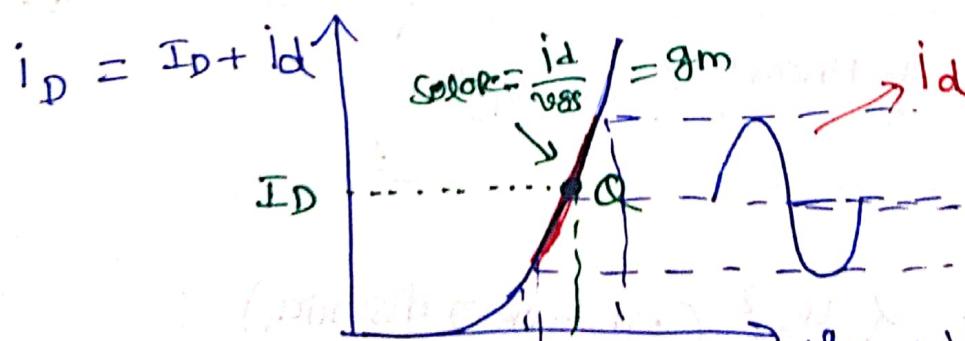
By KVL at ip side

$$-V_{GS} - v_{gs} + v_{GS} = 0$$

$$v_{GS} = v_{gs} + V_{GS}$$

$v_{GS} = \text{A.C + D.C}$

$\Rightarrow$  From the transfer c/s of MOSFET



$$i_D = I_D + i_d$$

$\text{small} = \frac{i_d}{v_{GS}} = g_m$

$$v_{GS} + V_{GS} = v_{GS}$$

$v_{GS} = \text{small}$

$$i_D = \frac{1}{2} \mu_n \cos \frac{\omega}{L} (V_{GS} - V_T)^2 \rightarrow \textcircled{A}$$

$$V_{GS} = V_{DS} + V_{GS} \rightarrow \textcircled{B}$$

Sub eqn  $\textcircled{B}$  in  $\textcircled{A}$

$$i_D = \frac{1}{2} \mu_n \cos \frac{\omega}{L} (V_{GS} + V_{DS} - V_T)^2 \rightarrow \textcircled{C}$$

$i_D$  = Total current  $V_{GS}$  = Total Voltage

$i_d$  = A.c current  $V_{DS}$  = A.c voltage

$I_D$  = D.c current  $V_{GS}$  = D.c voltage

$$i_D = \frac{1}{2} \mu_n \cos \frac{\omega}{L} (V_{GS} - V_T + V_{DS})^2$$

$$i_D = \frac{1}{2} \mu_n \cos \frac{\omega}{L} \left\{ (V_{GS} - V_T)^2 + V_{DS}^2 + 2 \times (V_{GS} - V_T) \times V_{DS} \right\}$$

$$i_D = \underbrace{\frac{1}{2} \mu_n \cos \frac{\omega}{L} (V_{GS} - V_T)^2}_{\text{Term-I}} + \underbrace{\frac{1}{2} \mu_n \cos \frac{\omega}{L} V_{DS}^2}_{\text{Term-II}} + \underbrace{\mu_n \cos \frac{\omega}{L} \times (V_{GS} - V_T) \times V_{DS}}_{\text{Term-III}}$$

X

Term-I

D.c bias current  $i_D = \frac{1}{2} \mu_n \cos \frac{\omega}{L} (V_{GS} - V_T)^2$

Term-II

$i_D \propto V_{DS}^2$  (non-linear distortion)

To reduce the non-linear distortion introduced by MOSFET, the input signal should be kept small

Term - III

$$M_n C_o x \frac{W}{L} (V_{GS} - V_T) \times V_{GS}$$

$$i_o \propto V_{GS}$$

$$i_D = K V_{GS}$$

$$K = M_n C_o x \frac{W}{L} (V_{GS} - V_T)$$

Term - II  $\ll$  Term - III  $\Rightarrow$  To reduce Non-Linear distortion

$$\frac{1}{2} M_n C_o x \frac{W}{L} V_{GS}^2 \ll M_n C_o x \frac{W}{L} (V_{GS} - V_T) \times V_{GS}$$

$$\begin{cases} V_{GS} \ll 2(V_{GS} - V_T) \\ V_{GS} \ll 2(V_{ov}) \end{cases}$$

$(V_{ov} = V_{GS} - V_T)$

This condition is called "Small Signal condition"

If small signal conditions satisfied, we can neglect

term - II then  $i_D$  becomes

$$i_D = I_D + 0 + \underbrace{M_n C_o x \frac{W}{L} (V_{GS} - V_T) \times V_{GS}}_{AC current i_d}$$

$$i_D (\text{total current}) = \text{DC current} + \text{AC current}$$

$$i_D = I_D + i_d$$

Total current in MOSFET

$$i_d = M_n C_o x \frac{W}{L} (V_{GS} - V_T) \times V_{GS}$$

$$i_d = Mn \cos \frac{w}{L} (V_{GS} - V_T) V_{GS}$$

A.C  
current

$$g_m = \frac{i_d}{V_{GS}} = Mn \cos \frac{w}{L} (V_{GS} - V_T)$$

mosFET

→ transconductance

I

$$g_m = Mn \cos \frac{w}{L} (V_{ov}) \quad \left[ \because V_{ov} = V_{GS} - V_T \right]$$

II

$$g_m = \sqrt{2I_D \times Mn \cos \frac{w}{L}} \quad \text{Amp/Volt}$$

III

$$g_m = \frac{2I_D}{V_{GS} - V_T}$$

$g_m$  = small signal parameter

Drain Resistance (small signal parameter when Channel length modulation is considered)

$$r_o = \frac{\Delta V_D}{\Delta I_D} = \frac{\Delta V_D}{0} \Rightarrow \infty \quad \text{(when channel length modulation is not considered)}$$

$$r_o = \frac{V_A \text{ (or) } 1}{I_D \lambda I_D}$$

$$I_D = \frac{1}{2} \mu_n \cos \frac{w}{L} [1 + \lambda V_{DS}] [V_{GS} - V_T]^2$$

$$r_o = \frac{\Delta V_{DS}}{\Delta I_D}$$

$$\frac{dI_D}{dV_{DS}} \text{ (or)} \frac{\Delta I_D}{\Delta V_{DS}} = \frac{1}{2} \mu_n \cos \frac{w}{L} [0 + \lambda(1)] [V_{GS} - V_T]^2$$

$$= \left( \frac{1}{2} \mu_n \cos \frac{w}{L} (V_{GS} - V_T)^2 \right) \lambda$$

$$y_{r_o} = \frac{\Delta I_D}{\Delta V_{DS}} = I_D \times \lambda$$

$$r_o = \frac{1}{I_D \times \lambda}$$

$$\left( \lambda = \frac{1}{V_A} \right)$$

$$r_o = \frac{V_A}{I_D}$$

NOTE!

Since  $g_m, r_o$  are small signal parameters,  
we can include  $g_m \& r_o$  in small signal eq. model of MOSFET

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad r_o = \frac{\Delta V_{DS}}{\Delta I_D}$$

$$y = mx$$

$$y = my$$

Linear Segment Line

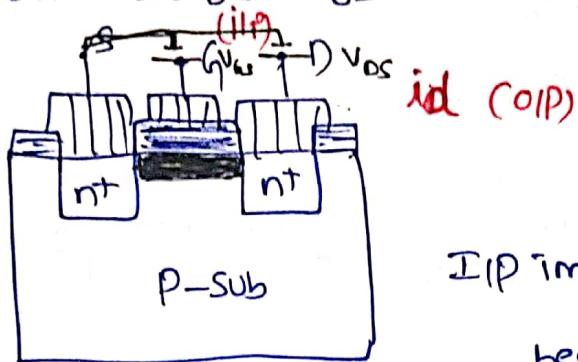


if  $V_{DS} = \text{signal} \Rightarrow V_{DS} \Rightarrow \text{Very small}$

$\Rightarrow$  Small Signal Analysis

## Small signal equivalent model of MOSFET

In this  
 $\Rightarrow$  The small signal voltage  $V_{gs}$  is small

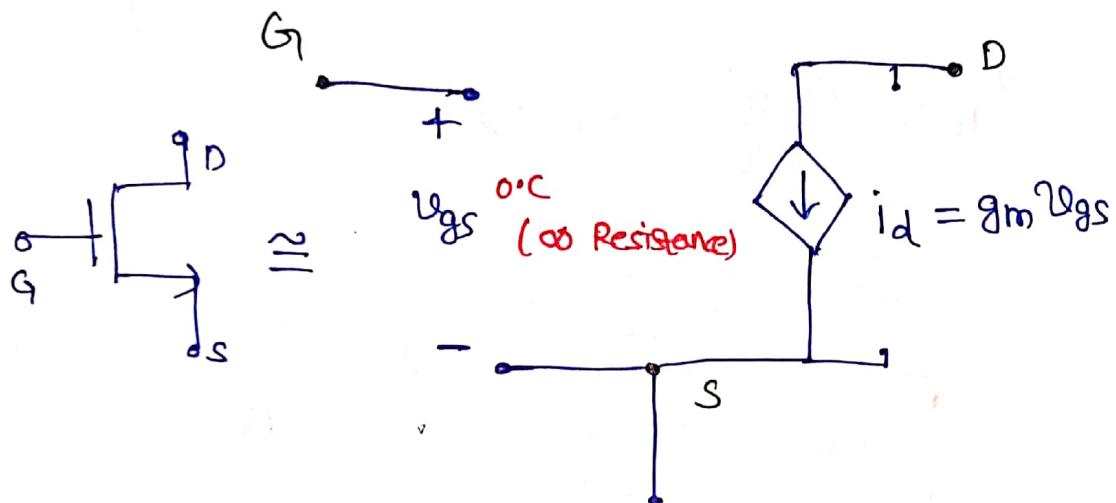


Small signal voltage  $V_{gs}$  is small

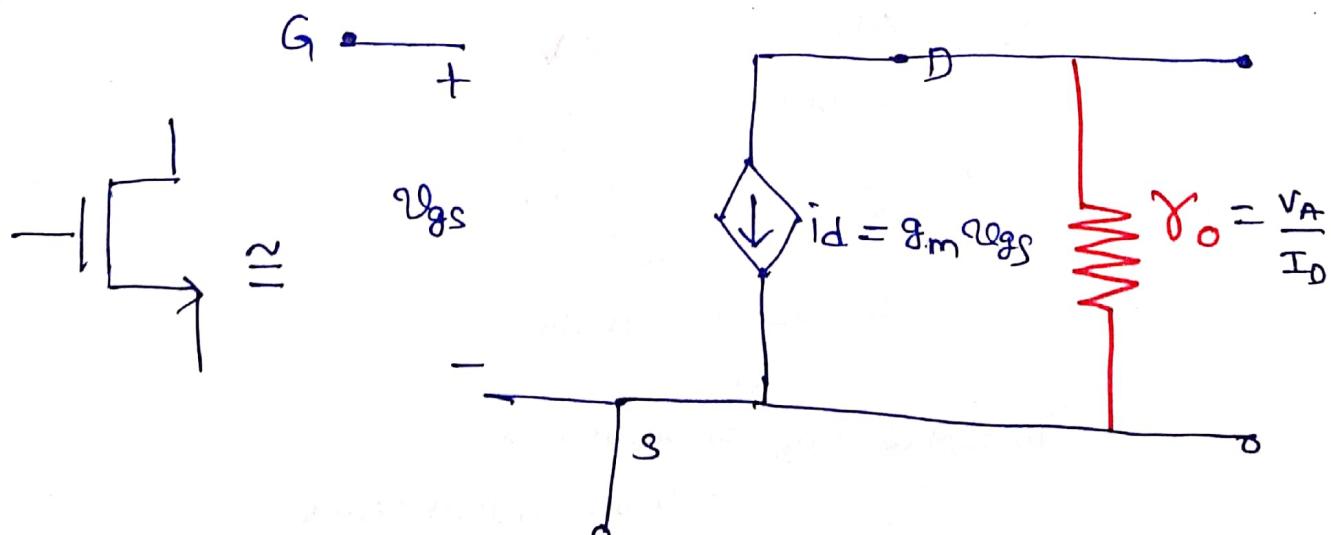
because  $\text{SiO}_2$  layer

$\therefore \text{SiO}_2 \Rightarrow$  Dielectric

(a) insulating material



Fig② Small signal equivalent model of MOSFET  
 when channel length modulation effect is not considered



Fig③ Small signal equivalent model of MOSFET when channel length modulation effect is considered

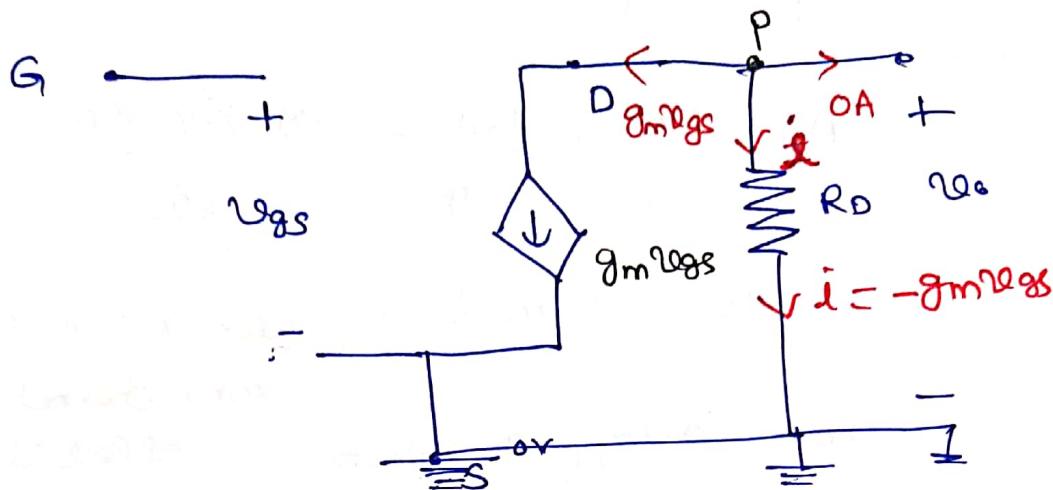


FIG D Small signal eq model For common source amplifier

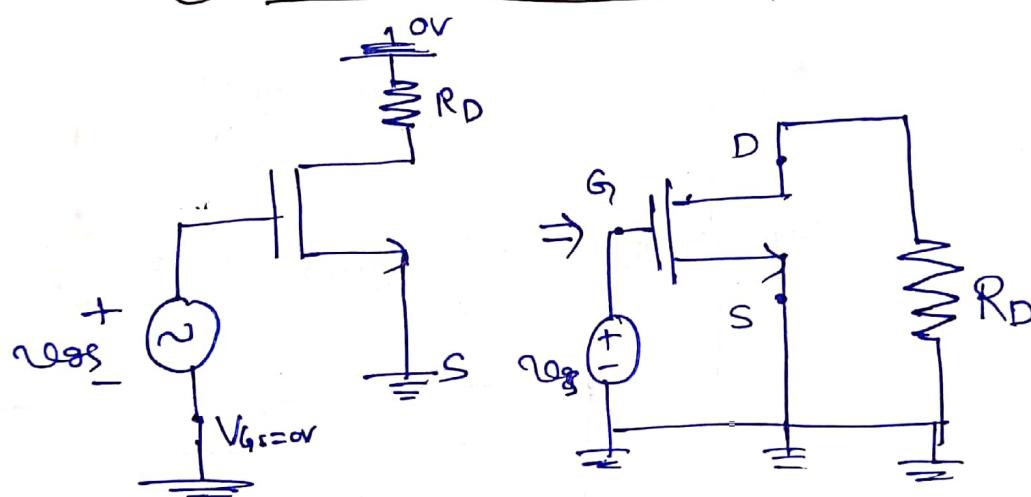


FIG O AC equivalent Ckt of MOSFET

### (i) Voltage gain (AV)

$$AV = \frac{V_o}{V_{in}} = \frac{V_o}{V_{gs}} \text{ (or)} \frac{V_d}{V_{gs}}$$

Apply KCL at Node P

$$+gm * V_{gs} + OA + i = 0$$

$i = -gm * V_{gs}$

$$V_o = i R_D$$

$$V_o = -g_m V_{GS}$$

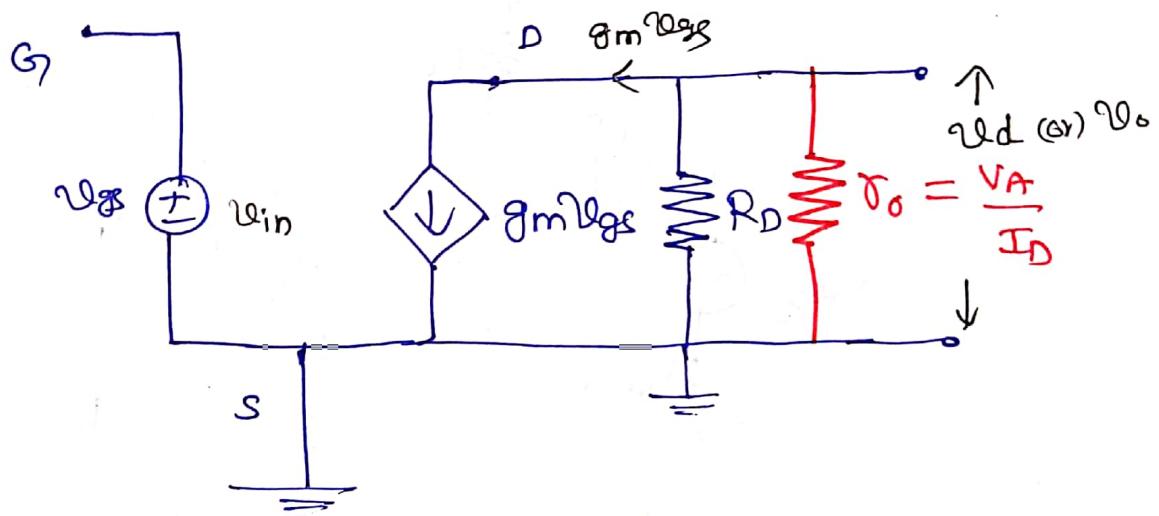
$$V_{in} = V_{GS}$$

$$A_V = \frac{V_o}{V_{in}} = \frac{V_d}{V_{GS}} = -\frac{g_m V_{GS} R_D}{r_{DS}}$$

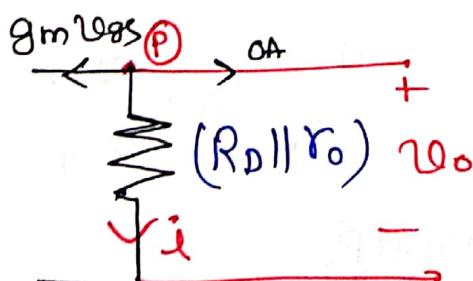
$$A_V = -g_m R_D$$

( when "r<sub>o</sub>" is not considered)  
(or) channel length modulation effect is not considered)

$$A_V = 20 \log (-g_m R_D) \text{ dB}$$



$$A_V = \frac{V_o}{V_{in}} = \frac{V_d}{V_{GS}} = -\frac{g_m V_{GS} (R_D \parallel r_o)}{r_{DS}} = -g_m (R_D \parallel r_o)$$



By applying KCL at (P)

$$g_m V_{GS} + i_A + i = 0$$

$$i = -g_m V_{GS}$$

$$V_o = V_d = i (R_D \parallel r_o)$$

$$V_o = V_d = -g_m V_{GS} (R_D \parallel r_o)$$

$$A_V = -g_m (R_D || r_o)$$

(when  $r_o$  is considered)

$$r_o = \frac{V_A}{I_D}$$

(Or) channel length modulation

( $r_o = \text{finite}$ ) effect is considered

→ Because of finite Resistance ( $r_o$ ),  $A_V \downarrow$ , which is a better approximation (or) approach practically

Input Resistance:  $(R_{in})^{(a)}$  ( $Z_{in}$ )

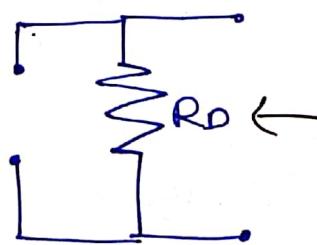
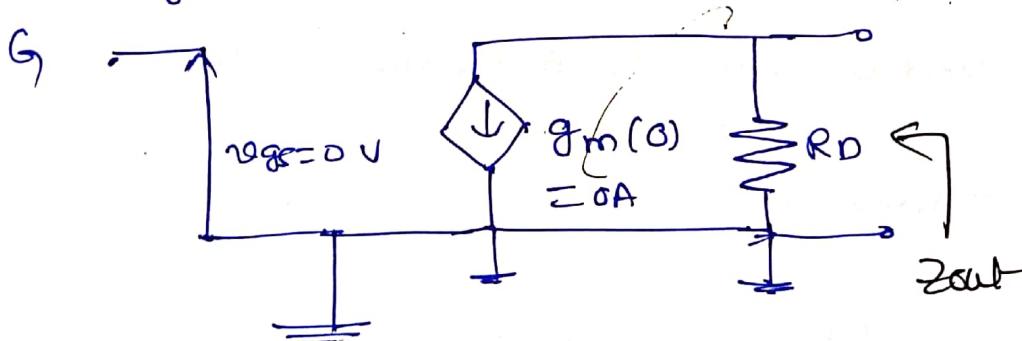
$$Z_{in} = R_{in} = \infty$$

$$R_{in} = (\infty) \parallel R_G = R_G \quad (\text{If } R_G \text{ is included})$$

Output Resistance ( $R_o$ ) ( $Z_{out}$ )

(1)  $r_o = \infty$  (channel length modulation effect is not considered)

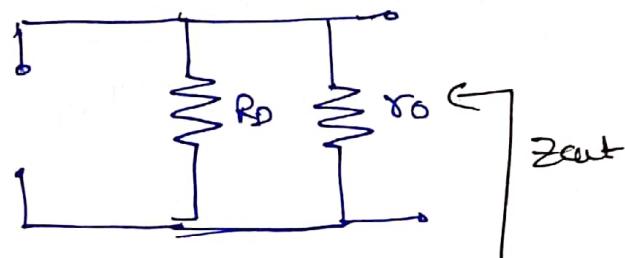
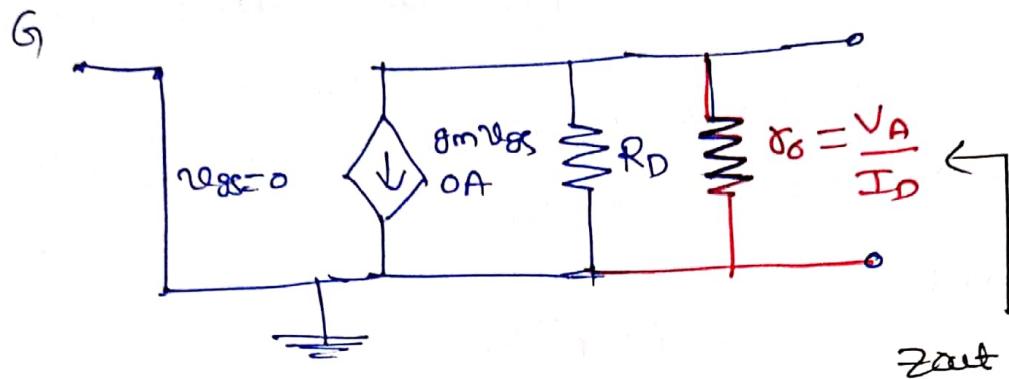
$$V_{GSS} = 0$$



$$Z_{out} = R_D$$

(ii)  $r_o = \text{Finite}$  ( Channel length modulation effect is considered)

$$r_o = \frac{V_A}{I_D}$$



$$Z_{\text{out}} = R_D \parallel r_o$$

NOTE:

- \* The output impedance  $Z_{\text{out}}$  is decreasing because of "r\_o"
- \* The voltage gain  $A_V$  is decreasing because of "r\_o"

$A_I$   $\Rightarrow$  current gain

$$A_I = \frac{I_{\text{out}}}{I_{\text{in}}} \Rightarrow \frac{i_d}{i_g}$$

$$A_I = \frac{i_d}{i_g = 0A} \Rightarrow A_I = \infty$$

$$i_g = 0A \Rightarrow Z_{\text{in}} = \infty$$

## Large signal model of mosFET

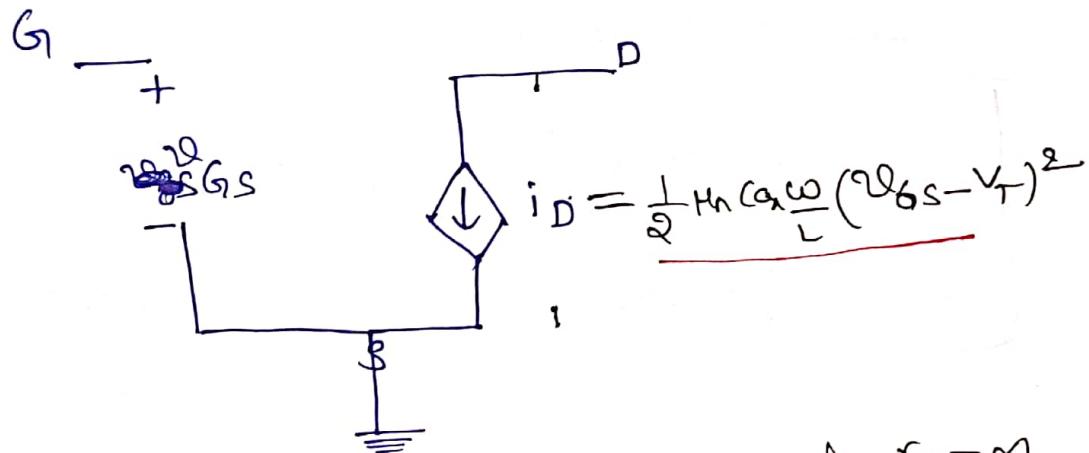
⇒ The input A.c voltage  $V_{GS}$  is large, which makes the drain current non-linear

In small signal model  $\Rightarrow V_{GS}$  is small

$$i_D = g_m V_{GS} \text{ (Linear)}$$

In large signal model  $\Rightarrow V_{GS}$  is large

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad ( \text{Non-Linear} )$$



Fig@ Large signal model of mosFET when  $r_o = \infty$   
(Channel length modulation is not considered)

$$(V_{GS} = V_{GS}^{AC} + V_{GS}^{DC})$$

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \quad (\text{Total})$$

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} + V_{GS} - V_T)^2$$

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left\{ (V_{GS} - V_T) + V_{GS} \right\}^2$$

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left\{ (V_{GS} - V_T)^2 + V_{GS}^2 + 2(V_{GS} - V_T) \times V_{GS} \right\}$$

$$i_D = \frac{1}{2} \mu_n \cos \frac{\omega}{L} \left\{ (V_{GS} - V_T)^2 + 2V_{GS}^2 + 2(V_{GS} - V_T) \times 2V_{GS} \right\}$$

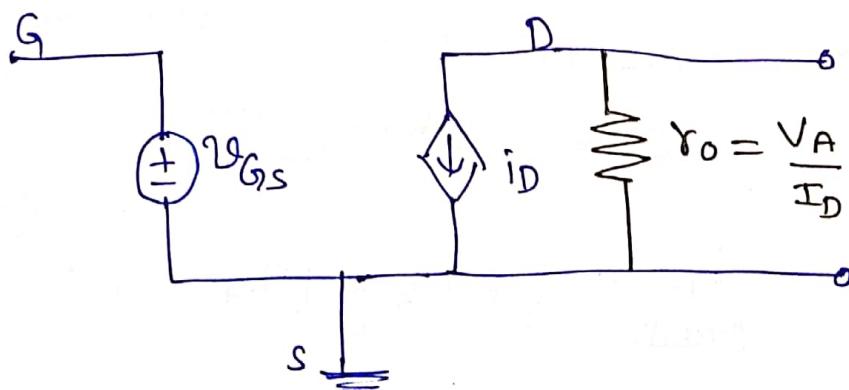
$$i_D = \frac{1}{2} \mu_n \cos \frac{\omega}{L} \left\{ V_{GS} - V_T \right\}^2 + \frac{1}{2} \mu_n \cos \frac{\omega}{L} 2V_{GS}^2 + \frac{1}{2} \mu_n \cos \frac{\omega}{L} \times 2(V_{GS} - V_T) \times 2V_{GS}$$

$$i_D = \underbrace{I_D}_{\text{D.C}} + \underbrace{\frac{1}{2} \mu_n \cos \frac{\omega}{L} \left\{ 2V_{GS}^2 + 2(V_{GS} - V_T) \times 2V_{GS} \right\}}_{\text{A.C}} \\ i_D = I_D + i_d$$

$$i_{D\text{total}} = I_D + i_d$$

$$I_D = \frac{1}{2} \mu_n \cos \frac{\omega}{L} \left\{ V_{GS} - V_T \right\}^2$$

$$i_d = \frac{1}{2} \mu_n \cos \frac{\omega}{L} \left\{ 2V_{GS}^2 + 2(V_{GS} - V_T) \times 2V_{GS} \right\}$$



Fig(b) Large signal equivalent model when  $r_0 = \text{Finite}$   
Channel length modulation effect is considered

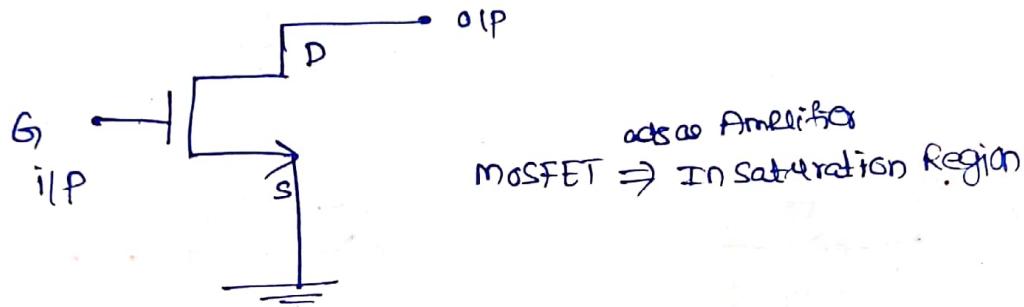
$$r_0 = \frac{V_A}{I_D} = \frac{1}{\lambda I_D} = \frac{1}{\lambda \left( \frac{1}{2} \mu_n \cos \frac{\omega}{L} (V_{GS} - V_T)^2 \right)}$$

## Common Source amplifier (By using constant current source Biasing)

⇒ Source is common to both iIP & oIP (iIP = Gate oIP = Drain)

⇒ CS - iIP  $\Rightarrow$  Gate terminal  
oIP  $\Rightarrow$  Drain terminal

$$\begin{aligned} C_E &= C_S \\ C_B &= C_G \\ C_C &= C_D \end{aligned}$$



⇒ MOSFET acts as an Amplifier in Saturation Region, so we must set a Q-Point in Saturation Region by using DC Biasing Techniques.

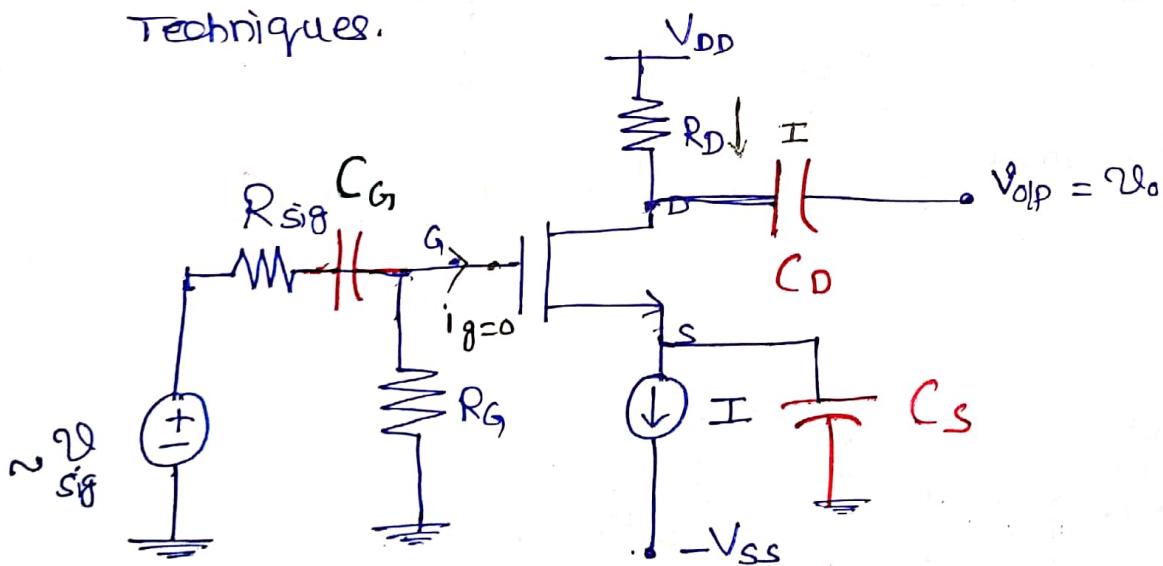


Fig @ Common Source amplifier Ckt diagram by using constant current source Biasing

$i_g = 0$  Amp  $\Rightarrow$  Because of High iIP Impedance due to dielectric  $\sigma_d$

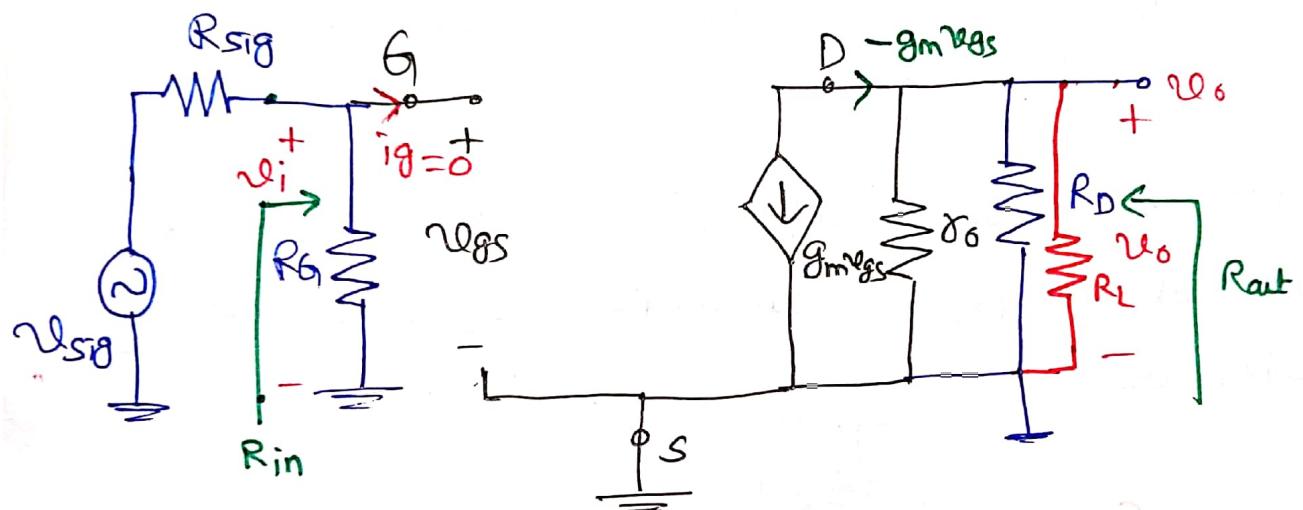
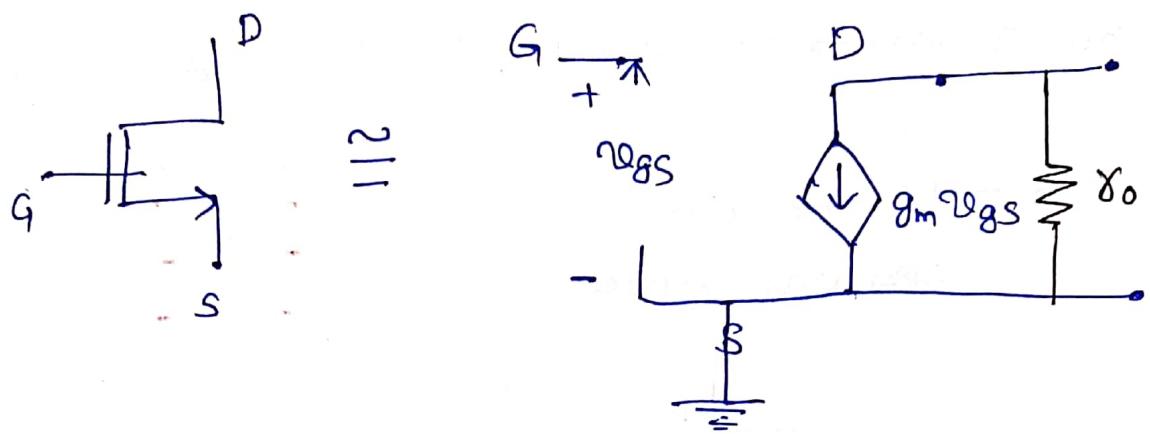


Fig (a) Small signal equivalent model of MOSFET

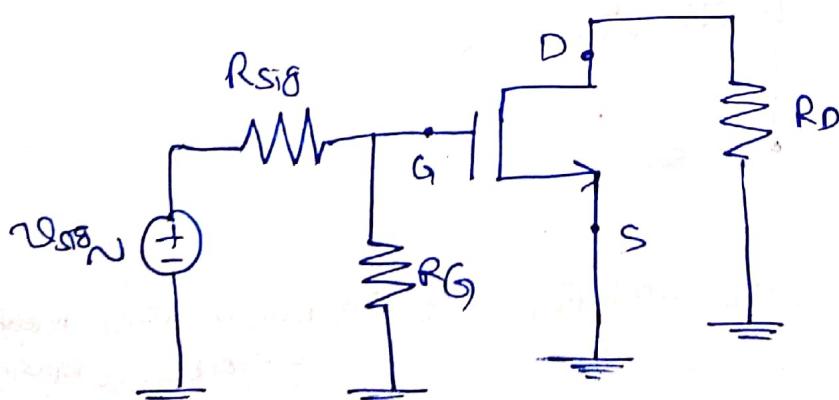


Fig (b) AC Analysis of MOSFET

## Parameters of common Source Amplifier

2

### (i) Input Impedance

from the small signal equivalent Ekt diagram

$$R_{in} = R_G$$

$$u_i = \frac{u_{sig} \times R_G}{R_G + R_{sig}} ; u_i = u_{gs}$$

$$u_i = \frac{u_{sig} \times R_{in}}{R_{in} + R_{sig}} \Rightarrow u_{sig} = \frac{u_i \times R_G}{R_G + R_{sig}}$$

### (ii) Voltage gain ( $A_v$ )

$$A_v = \frac{\text{O/P voltage}}{\text{I/P voltage}}$$

$$A_v = \frac{u_o}{u_i} = \frac{-g_m u_{gs} (r_o \parallel R_D)}{u_{gs}}$$

$$A_v = -g_m (r_o \parallel R_D)$$

when  $R_L$  is considered  $\Rightarrow A_v = \frac{u_o}{u_i} = \frac{-g_m u_{gs} (r_o \parallel R_D \parallel R_L)}{u_{gs}}$

$$A_v = -g_m (r_o \parallel R_D \parallel R_L)$$

$$A_{v0} = -g_m r_o (R_D) \quad (R_L = \infty)$$

$A_{v0} \Rightarrow$  This is called the open circuit voltage gain since we have not considered  $u_{sig}$  into account

## ⑤ Overall voltage gain (G<sub>v</sub>)

$$G_{vo} = \frac{O/P \text{ voltage}}{I/P \text{ signal voltage}}$$

$$G_{vo} = \frac{v_o}{v_{sig}} \rightarrow ⑥$$

$$v_o = -g_m v_{sig} (r_o \parallel R_o \parallel R_L)$$

$$v_{sig} = ?$$

$$v_i = \frac{v_{sig} R_G}{R_G + R_{sig}}$$

$$v_{sig} = \frac{v_i (R_G + R_{sig})}{R_G} = v_i \left( \frac{R_{in} + R_{sig}}{R_{in}} \right) \rightarrow ⑥$$

$$G_{vo} = \frac{-g_m v_{sig} (r_o \parallel R_o \parallel R_L)}{v_i \left( \frac{R_{in} + R_{sig}}{R_{in}} \right)}$$

$$G_{vo} = \frac{-g_m v_{sig} (r_o \parallel R_o \parallel R_L)}{v_{sig} \left( \frac{R_{in} + R_{sig}}{R_{in}} \right)} \quad (v_i = v_{sig})$$

$$G_{vo} = \frac{-g_m (r_o \parallel R_o \parallel R_L)}{R_{in} + R_{sig}} \times R_{in}$$

$$G_{vo} = \frac{R_{in}}{R_{in} + R_{sig}} \left( -g_m (r_o \parallel R_o \parallel R_L) \right) \underbrace{\left( -g_m (r_o \parallel R_o \parallel R_L) \right)}_{A_v}$$

$$G_{vo} = \frac{R_o}{R_{int} R_{sig}} (A_{vo})$$

$G_{vo}$  = overall voltage gain from the signal source to the load

$A_{vo}$  = open circuit voltage gain

$$G_{vo} = \frac{R_o}{R_o + R_{sig}} (A_{vo})$$

(iii) Output Resistance :

$$R_{out} = R_o \parallel R_D \parallel R_L$$

$$R_{out} = R_o \parallel R_D$$

Common Source Amplifier with a Source Resistance

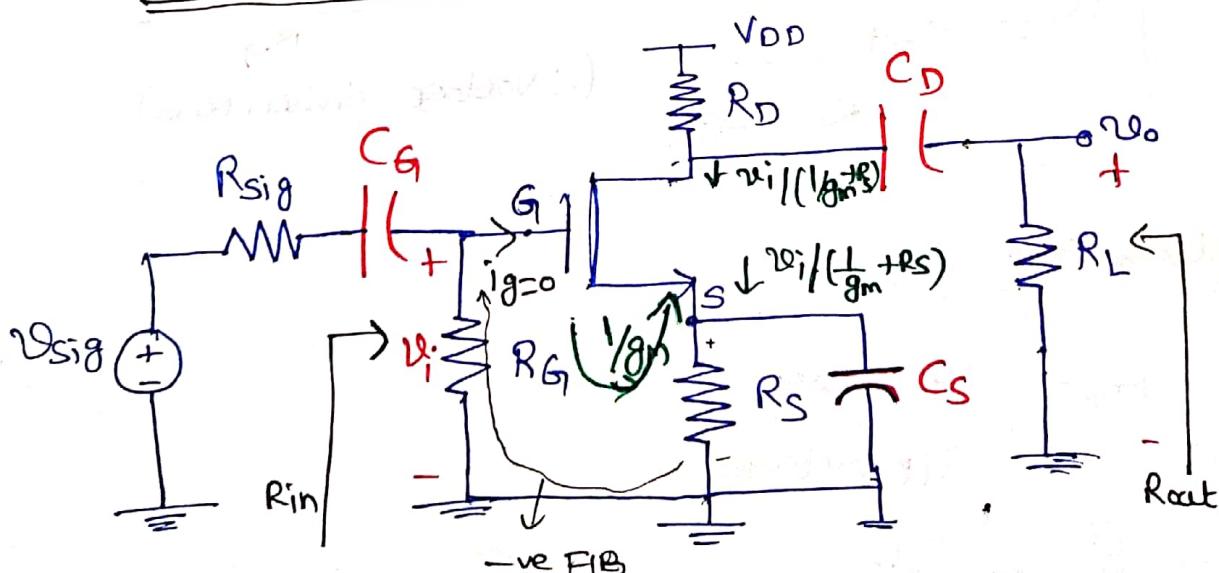


Fig @ Common source amp with a source resistance  $R_s$

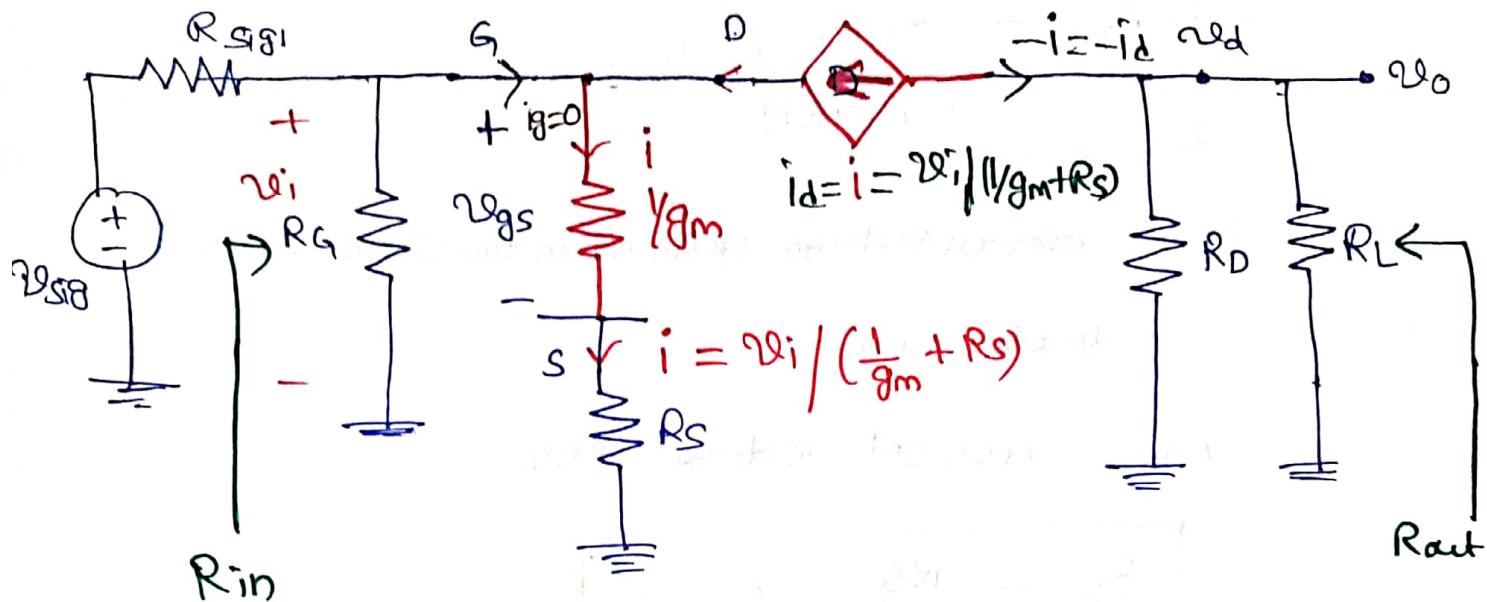


FIG 6 Small signal equivalent model of common source amplifier with source resistance  $R_s$

parameters of common source amplifier with "R<sub>s</sub>"

(i) Input Impedance

$$R_{in} = R_g$$

$$v_i = v_{sig} \frac{R_g}{R_g + R_{sig}}$$

$$v_{sig} = v_i \times (R_g + R_{sig})$$

( $\because$  voltage division rule)

(ii) Voltage gain A<sub>vo</sub>

$$A_{vo} = \frac{\text{O/p voltage}}{\text{I/p voltage}}$$

$$A_{vo} = \frac{v_o}{v_i}$$

$$v_o = -i (R_o \parallel R_L)$$

$$v_o = -i_d (R_o \parallel R_L)$$

For suppose if  $\gamma_o$  is included then

$$v_o = -i (R_o \parallel R_o \parallel R_L) \rightarrow @$$

$$i = v_i / \left( \frac{1}{g_m} + R_s \right) \rightarrow b$$

Sub  $b$  ineq @ then  $v_o$  becomes

$$v_o = - \frac{v_i}{\left( \frac{1}{g_m} + R_s \right)} (R_o \parallel R_o \parallel R_L)$$

$$v_o = - \frac{v_i (R_o \parallel R_L)}{\left( \frac{1}{g_m} + R_s \right)}$$

$$v_o = - \frac{v_i (R_o \parallel R_L) \times g_m}{1 + g_m R_s}$$

$$A_v = \frac{v_o}{v_i} = - \frac{g_m (R_o \parallel R_L)}{1 + g_m R_s}$$

If

$$R_L = \infty \Rightarrow \frac{\text{absence of } "R_L"}{\text{open circuit}} \quad A_v = - \frac{g_m (R_o \parallel \infty)}{1 + g_m R_s}$$

open circuit

$R_L$  gives  $A_v = \text{open circuit}$

voltage gain

Voltage gain of CS amplifier using 'Rs'

$$A_{vD} = \frac{-g_m R_D}{1 + g_m R_S} \rightarrow \textcircled{A}$$

The gain of common source amplifier by using constant DC current source biasing is

$$A_{vD} = -g_m R_D \rightarrow \textcircled{B}$$

$$A_{vD} = -g_m (R_{oL} \parallel R_D)$$

$$A_{vD} = -g_m (R_{oL} \parallel R_D \parallel R_L)$$

By comparing eq  $\textcircled{A}$  &  $\textcircled{B}$

Gain of common source amplifier  $\downarrow$  by a factor of

$1 + g_m R_S$ . Because of its action in reducing the gain,

$R_S$  is called "source degeneration resistance"

[ The reduction in gain is due to negative F/B provided by source resistance "Rs" ]

Common source amplifier  
with constant current source

Common source amplifier with  
source resistance 'Rs'

$$\Rightarrow R_{in} = R_G$$

$$\Rightarrow R_{in} = R_G$$

$$\Rightarrow * A_{vD} = -g_m R_D$$

$$\Rightarrow * A_{vD} = \frac{-g_m R_D}{1 + g_m R_S}$$

$$\Rightarrow G_{vD} = \frac{R_S}{R_G + R_S} (A_{vD})$$

$$\Rightarrow G_{vD} = \frac{R_S}{R_G + R_S} (A_{vD})$$

$$\Rightarrow R_{out} = R_{oL} \parallel R_D \parallel R_L$$

$$\Rightarrow R_{out} = R_{oL} \parallel R_D \parallel R_L$$

(b) Overall voltage gain  $G_{12}$

$$G_{12} = \frac{U_o}{U_{SIG}}$$

$$G_{12} = \frac{\frac{-g_m(R_D || R_L)}{1 + g_m R_S} V_i}{\frac{V_i (R_G + R_{SIG})}{R_G}}$$

$$G_{12} = \frac{R_G}{R_G + R_{SIG}} \cdot \frac{-g_m (R_D || R_L)}{1 + g_m R_S}$$

$$G_{12} = - \frac{R_G}{R_G + R_{SIG}} \left( \frac{g_m (R_D || R_L)}{1 + g_m R_S} \right)$$

$$G_{12} = \frac{R_G}{R_G + R_{SIG}} (Ans)$$

(iii) Output Resistance

$$R_{out} = R_D || R_L$$

If we include  $r_o$

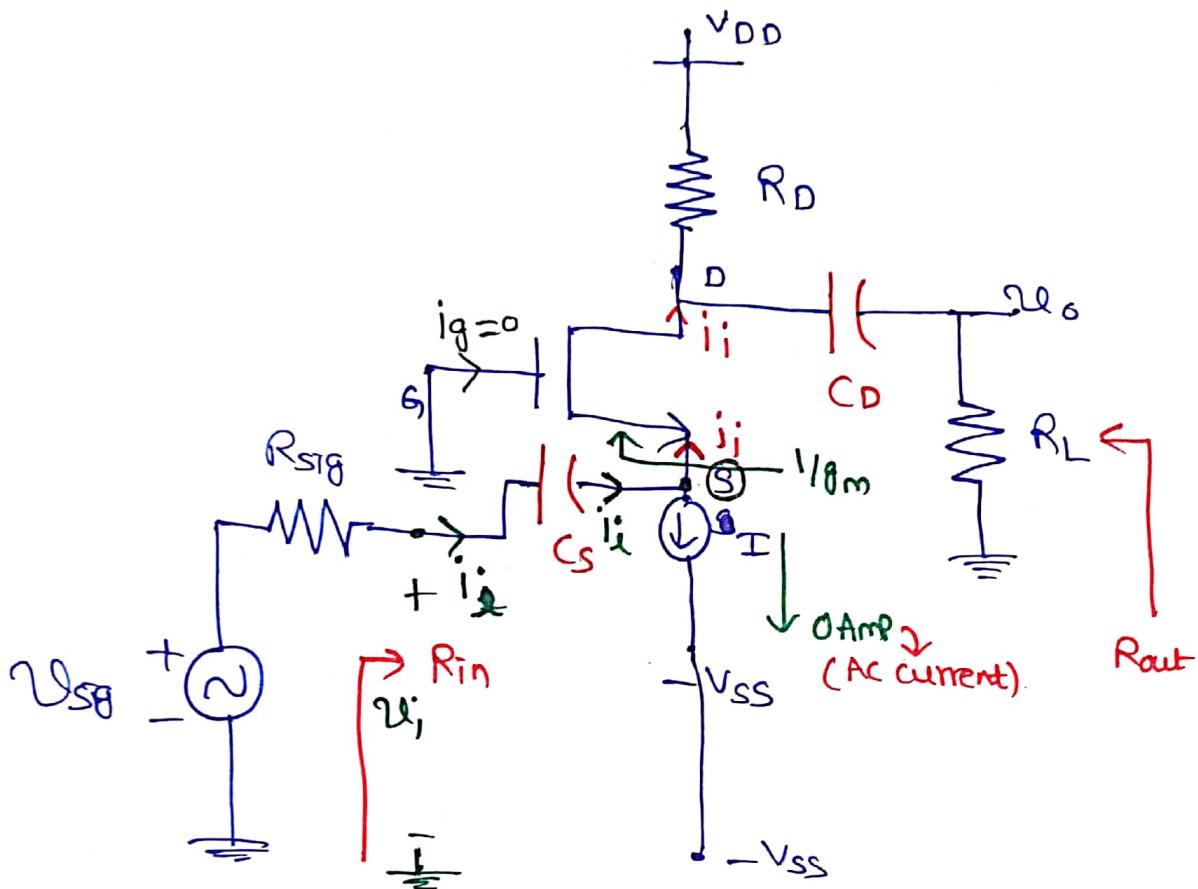
$$R_{out} = r_o || R_D || R_L$$

$$R_L = \infty$$

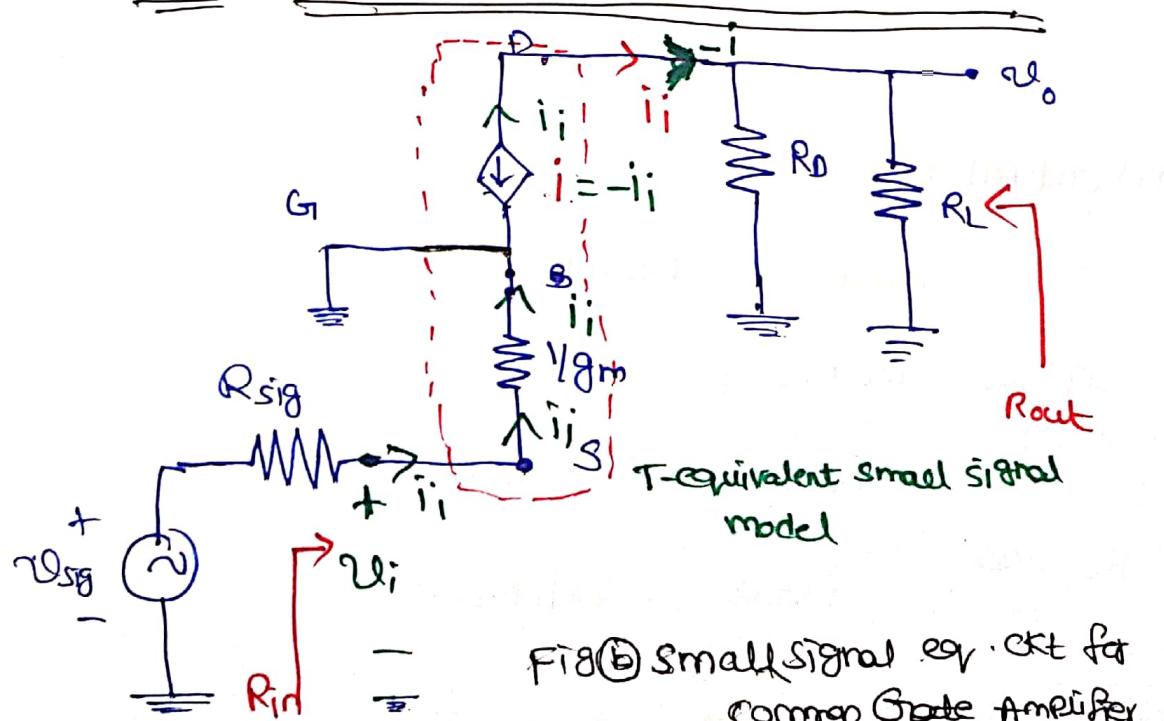
$$R_{out} = r_o || R_D$$

## Common gate Amplifier (CG)

- ⇒ Gate  $\Rightarrow$  common to both  $iP(s)$  &  $oP(D)$ , i.e. Gate is grounded
- ⇒ In common gate configuration source is  $iP$  terminal & drain is  $oP$  terminal



## Fig@ CKT diagram of Common gate Amplifier



Fig(B) Small Signal eq. ckt for  
Common Gate Amplifier

## Parameters of common gate amplifier

⇒ (i) Input Resistance or Impedance :

$$V_i = V_s \text{ (from source terminal to Gate terminal)}$$

$V_i$  = Voltage drop across  $Y_m$

$$V_i = i_s \times Y_m$$

$$R_{in} = \frac{\text{i/p voltage}}{\text{i/p current}} = \frac{V_i}{i_s} = Y_m$$

$$R_{in} = Y_m$$

$$\left. \begin{array}{l} \text{we know that} \\ Y_m \approx 1 \text{ mA/V} \\ R_{in} = Y_m = 1 \text{ k}\Omega \end{array} \right\} \text{approximately}$$

$$V_i = \frac{V_{sig} \times Y_m}{Y_m + R_{sig}} = \frac{V_{sig} \times R_{in}}{R_{in} + R_{sig}}$$

$$V_i = \frac{V_{sig} \times (1/Y_m)}{1 + Y_m R_{sig}} = V_{sig} \times \frac{1}{1 + Y_m R_{sig}}$$

$$V_i = \frac{V_{sig}}{1 + Y_m R_{sig}}$$

⇒ Since  $R_{in}$  is very low in common gate configuration, compared to CS amplifier, less because of this low  $R_{in}$  loss of signal strength can occur in coupling the signal to the i/p of the CG amplifier

$$R_{sig} \ll Y_m$$



$$R_{sig} \ll \frac{1}{g_m}$$

To reduce loss of signal strength

$$R_{sig} \ll R_{in}$$

(ii) Voltage gain  $A_v$ :

$$A_v = \frac{v_o}{v_i} \Rightarrow v_o = -i (R_{o\parallel R_L})$$

$$v_o = -i (r_{o\parallel R_o\parallel R_L})$$

$$i = -i_i \rightarrow \textcircled{P}$$

$$v_i = (g_m) i_i$$

$$i_i = v_i \times g_m \rightarrow \textcircled{Q}$$

Sub eqn  $\textcircled{Q}$  in eqn  $\textcircled{P}$

$$i = -v_i \times g_m$$

$$v_o = -(-v_i \times g_m) (r_{o\parallel R_o\parallel R_L})$$

$$v_o = v_i \times g_m (r_{o\parallel R_o\parallel R_L})$$

$$v_o = v_i \times g_m (R_o\parallel R_L)$$

$$A_v = \frac{v_o}{v_i} = g_m (R_o\parallel R_L)$$

$A_v$  becomes open circuit voltage gain when  $R_L = \infty$  (or) open circuited

$$A_v = g_m R_o$$

open circuit voltage gain

⑤ Overall voltage gain ( $G_{vo}$ ) :

⑦

$$G_{vo} = \frac{V_o}{V_{sig}}$$

$$V_o = V_i \times g_m (R_{ol} \| R_L) \rightarrow R$$

$$V_i = \frac{V_{sig}}{1 + g_m R_{sig}} \rightarrow S$$

Sub eqn S in eqn R

$$V_o = \frac{V_{sig}}{1 + g_m R_{sig}} \times g_m (R_{ol} \| R_L)$$

$$G_{vo} = \frac{V_o}{V_{sig}} = \frac{g_m (R_{ol} \| R_L)}{1 + g_m R_{sig}}$$

$$G_{vo} = \frac{g_m (R_{ol} \| R_L)}{1 + g_m R_{sig}}$$

$$G_{vo} = \frac{1}{1 + g_m R_{sig}} (A_{vo})$$

$$G_{vo} = \frac{A_{vo}}{1 + g_m R_{sig}}$$

(iii) output resistance:

$$R_{out} = R_{ol} \| R_L$$

$$R_{out} = R_o$$

$$R_{out} = R_{ol} \| R_D$$

⇒

CS

⇒ OIP  $\Rightarrow$  Inverting ( $180^\circ$  phase)

$$V_o = -g_m (R_{\text{load}} R_D)$$

$$V_o = -g_m R_D$$

⇒ Input Resistance is very high

$$R_{\text{in}} = R_G \text{ (Gate resistance)}$$

$$R_{\text{in}} = R_G \text{ (Input } 10^6 \text{ ohms)}$$

$$\Rightarrow A_{\text{voltage}} = \frac{R_G}{R_G + R_{\text{load}}} \text{ (Av)}$$

CG

⇒ OIP  $\Rightarrow$  Non-inverting

$$V_o = g_m (R_{\text{load}} R_D)$$

$$V_o = g_m R_D$$

⇒ Input Resistance of CG amplifier is low ( $R_{\text{in}}$ )

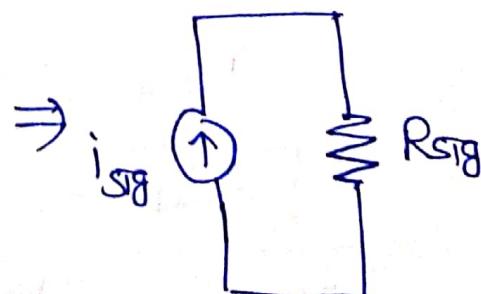
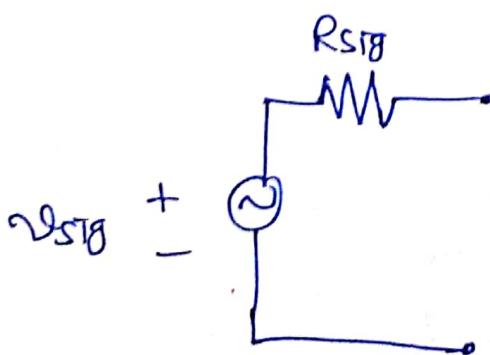
$$R_{\text{in}} = 1/g_m \quad (\because g_m \approx 1 \text{ mA/V})$$

$$R_{\text{in}} \approx 1 \text{ k}\Omega$$

$$\Rightarrow A_{\text{voltage}} = \frac{1}{1 + g_m R_{\text{load}}} \text{ (Av)}$$

Av is  $\downarrow$  by factor of  $1 + g_m R_{\text{load}}$

⇒ Compared to CS amplifier, the CG do not show any particular advantage, so to improve performance we are going to replace the voltage signal source with the current signal source



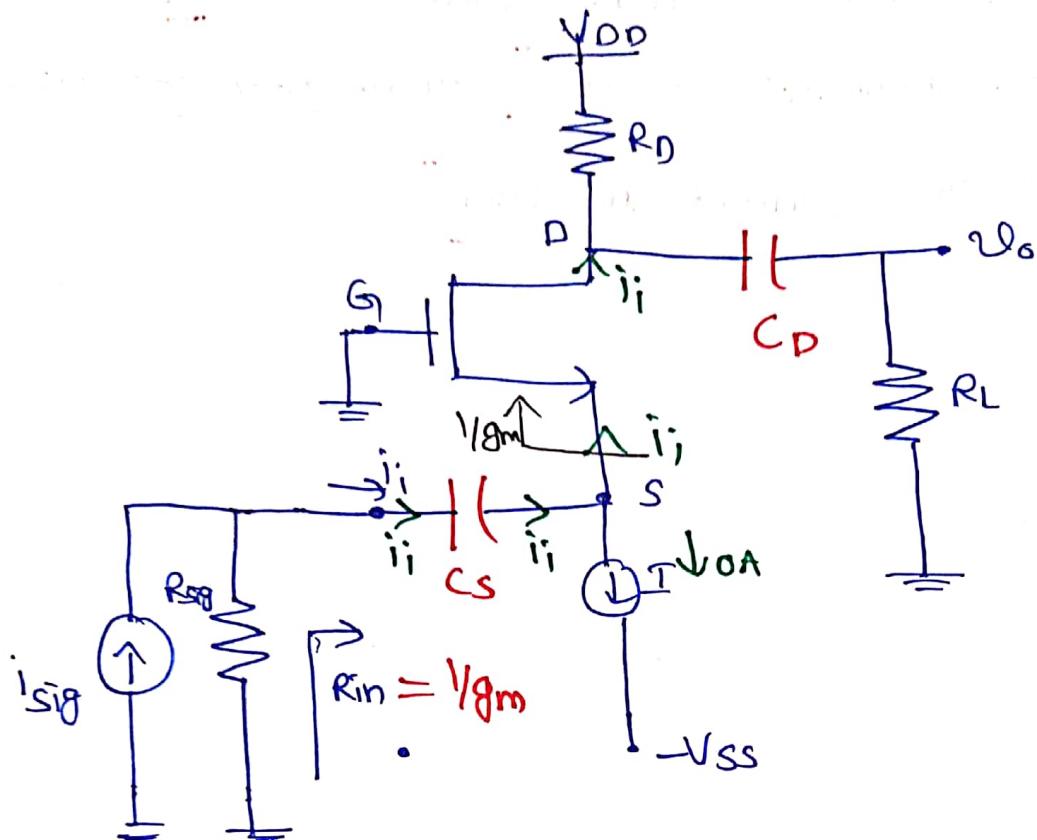
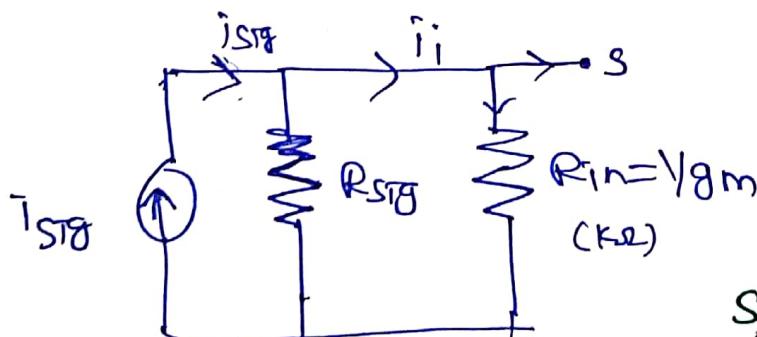


Fig ⑧ Common gate Amplifier fed with current signal i<sub>sig</sub>

$$R_{in} = 1/gm$$

$$i_i = \frac{i_{sig} \times R_{sig}}{R_{sig} + R_{in}} = \frac{i_{sig} \times R_{sig}}{R_{sig} + 1/gm}$$



$$R_{sig} \gg 1/gm$$

$$i_i \approx i_{sig}$$

$$i_i = \frac{i_{sig} \times R_{sig}}{R_{sig} + 1/gm}$$

Special Application due to i<sub>sig</sub>

In CG  $\Rightarrow i_D \approx i_s$

Current follower

(or) unity gain current

amplifier  $A_i = \frac{i_D}{i_s} \approx 1$

NOTE: By providing current signal source  $i_{sig}$ , the Common Gate Amplifier acts as "Current Amp follower" OR unity-gain current amplifier"