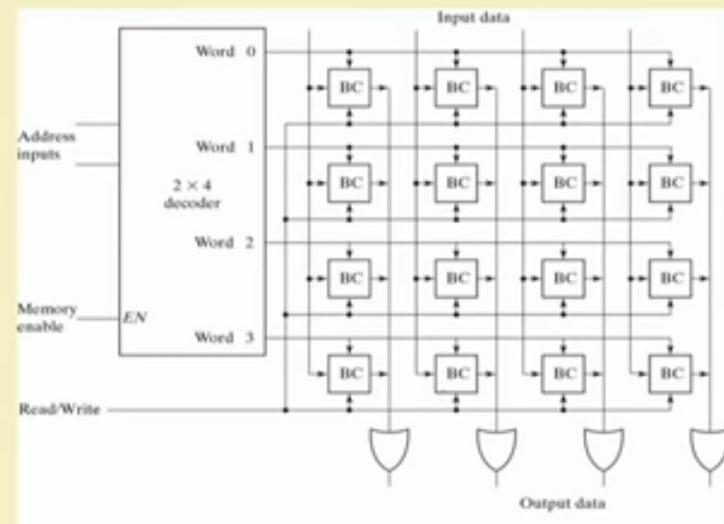


## 4X4 RAM

- There is a need for **decoding circuits** to select the memory word specified by the input address.
- During the **read operation**, the four bits of the selected **word go through OR gates** to the output terminals.
- During the **write operation**, the data available in the input lines are transferred into the four binary cells of the selected word.
- A memory with  $2^k$  words of  $n$  bits per word requires  $k$  address lines that go into  $k \times 2^k$  decoder.



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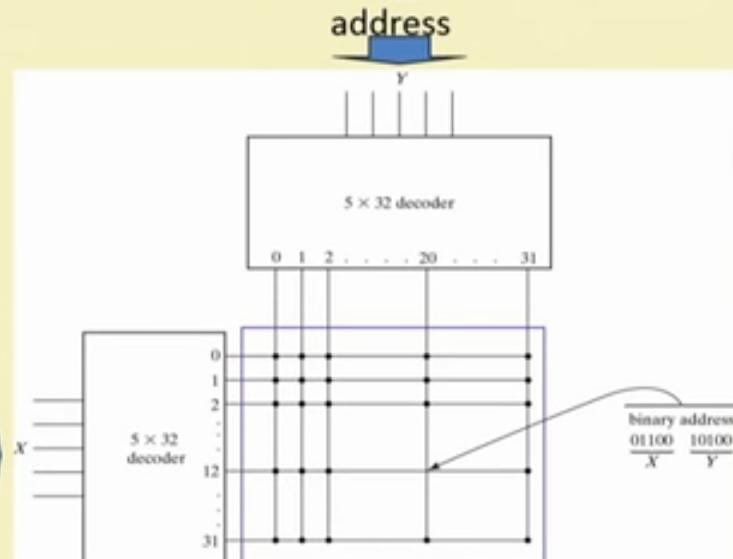


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# Coincident decoding

- A decoder with  $k$  inputs and  $2^k$  outputs requires  $2^k$  AND gates with  $k$  inputs per gate.
- Two decoding in a two-dimensional selection scheme can reduce the number of inputs per gate.
- 1K-word memory, instead of using a single **10X1024 decoder**, we use two **5X32 decoders**.



Two-Dimensional Decoding Structure for a 1K-Word Memory



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# Address multiplexing

- DRAMs typically have four times the density of SRAM.
- The cost per bit of DRAM storage is three to four times less than SRAM. Another factor is lower power requirement.



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# Address multiplexing

- DRAMs typically have four times the density of SRAM.
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# Address multiplexing

- Address multiplexing will reduce the number of pins in the IC package.
- In a two-dimensional array, the address is applied in two parts at different times, with the row address first and the column address second. Since the same set of pins is used for both parts of the address, so can decrease the size of package significantly.



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## Address multiplexing for 64K DRAM

- After a time equivalent to the **settling time of the row selection**, RAS goes back to the 1 level.
- **Registers** are used to store the addresses of the row and column.
- **CAS** must go back to the 1 level before initializing another memory operation.



Address Multiplexing for a 64K DRAM



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## Error detection and correction

- It is protecting the occasional errors in storing and retrieving the binary information.
- Parity can be used to check the error, but it can't be corrected.
- An error-correcting code generates multiple parity check bits that are stored with the data word in memory.



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# Hamming Code

- One of the most **commonly used** in RAM was devised by R. W. Hamming (called Hamming code).
- In Hamming code:
  - k** = parity bits in n-bit data word,
  - forming a new word of **n + k** bits. Those positions numbered as a power of 2 are reserved for the parity bits.
  - the remaining bits are the data bits.



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# Hamming Code

**Ex.** Consider the 8-bit data word 11000100. we include four parity bits with it and arrange the 12 bits as follows:

Bit position: 1 2 3 4 5 6 7 8 9 10 11 12

P<sub>1</sub> P<sub>2</sub> 1 P<sub>4</sub> 1 0 0 P<sub>8</sub> 0 1 0 0

$$P_1 = \text{XOR of bits}(3,5,7,9,11) = 1 \oplus 1 \oplus 0 \oplus 0 \oplus 0 = 0$$

$$P_2 = \text{XOR of bits}(3,6,7,10,11) = 1 \oplus 0 \oplus 0 \oplus 1 \oplus 0 = 0$$

$$P_4 = \text{XOR of bits}(5,6,7,12) = 1 \oplus 0 \oplus 0 \oplus 0 = 1$$

$$P_8 = \text{XOR of bits}(9,10,11,12) = 0 \oplus 1 \oplus 0 \oplus 0 = 1$$



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# Hamming Code

- The data is stored in memory together with the parity bit as 12-bit composite word.

Bit position:      1 2 3 4 5 6 7 8 9 10 11 12  
                      0 0 1 1 1 0 0 1 0 1 0 0

- When read from memory, the parity is checked over the same combination of bits including the parity bit.

$$C_1 = \text{XOR of bits}(3,5,7,9,11)$$

$$C_2 = \text{XOR of bits}(3,6,7,10,11)$$

$$C_4 = \text{XOR of bits}(5,6,7,12)$$

$$C_8 = \text{XOR of bits}(9,10,11,12)$$



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# Error-Detection

- A **0** check bit designates an **even parity** over the checked bits and a **1** designates an **odd parity**.
- Since the bits were stored with even parity, the result,  $C = C_8C_4C_2C_1 = 0000$ , indicates that no error has occurred.
- If  **$C \neq 0$** , then the 4-bit binary number formed by the check bits gives the position of the erroneous bit.



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# Example

Bit position: 1 2 3 4 5 6 7 8 9 10 11 12

0 0 1 1 1 0 0 1 0 1 0 0 No error

1 0 1 1 1 0 0 1 0 1 0 0 Error in bit 1

0 0 1 1 0 0 0 1 0 1 0 0 Error in bit 5

- Evaluating the XOR of the corresponding bits, get the four check bits

	$C_8$	$C_4$	$C_2$	$C_1$
For no error:	0	0	0	0
with error in bit 1:	0	0	0	1
with error in bit 5:	0	1	0	1



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## Hamming Code

- The Hamming Code can be used for data words of any length.
- Total bit in Hamming Code is  $n + k$  bits, the syndrome value C consists of  $k$  bits and has a range of  $2^k$  value between 0 and  $2^k - 1$ . The range of  $k$  must be equal to or greater than  $n + k$ , giving the relationship

$$2^{k-1} \geq n + k$$

*Range of Data Bits for  $k$  Check Bits*

<b>Number of Check Bits, <math>k</math></b>	<b>Range of Data Bits, <math>n</math></b>
3	2-4
4	5-11
5	12-26
6	27-57
7	58-120



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## Single-Error correction, Double-Error detection

- The Hamming Code can detect and correct only a single error.
- By adding another parity bit to the coded word, the Hamming Code can be used to correct a single error and detect double errors. Becomes  $001110010100P_{13}$ .

$001110010100 P_{13} \rightarrow 001110010100 \text{ 1}$   
 $P = \text{XOR}(001110010100 \text{ 1})$

if  $P = 0$ , the parity is correct (even parity), but if  $P = 1$ , then the parity over the 13 bits is incorrect (odd parity).

the following four cases can occur:



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## Single-Error correction, Double-Error detection

1. If  $C = 0$  and  $P = 0$ , no error occurred
2. If  $C \neq 0$  and  $P = 1$ , a single error occurred that can be corrected
3. If  $C \neq 0$  and  $P = 0$ , a double error occurred that is detected but that cannot be corrected
4. If  $C = 0$  and  $P = 1$ , an error occurred in the  $P_{13}$  bit



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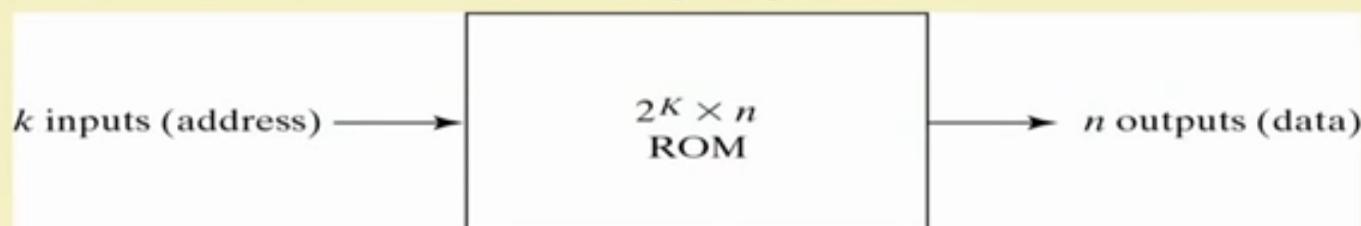


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## Read-Only Memory

- A block diagram of a ROM is shown below. It consists of  $k$  address inputs and  $n$  data outputs.
- The number of words in a ROM is determined from the fact that  $k$  address input lines are needed to specify  $2^k$  words.



ROM Block Diagram



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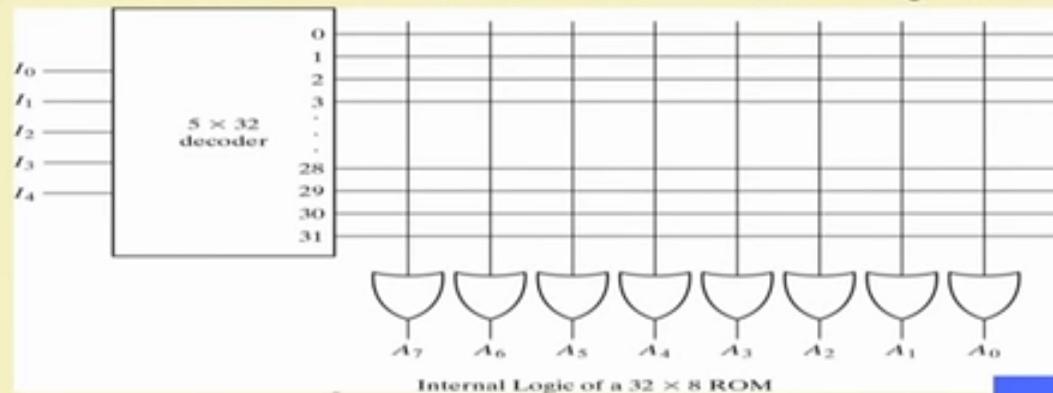


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## Construction of ROM

- Each output of the decoder represents a memory address.
- Each OR gate must be considered as having 32 inputs.
- A  $2^k \times n$  ROM will have an internal  $k \times 2^k$  decoder and  $n$  OR gates.



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## Truth table of ROM

- A programmable connection between two lines is logically equivalent to a switch that can be altered to either be close or open.
- Intersection between two lines is sometimes called a cross-point.

*ROM Truth Table (Partial)*

Inputs					Outputs							
I4	I3	I2	I1	I0	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
⋮					⋮							
1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1



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## Example

- Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number.

Derive truth table first

*Truth Table for Circuit*

Inputs			Outputs						Decimal
$A_2$	$A_1$	$A_0$	$B_5$	$B_4$	$B_3$	$B_2$	$B_1$	$B_0$	
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49



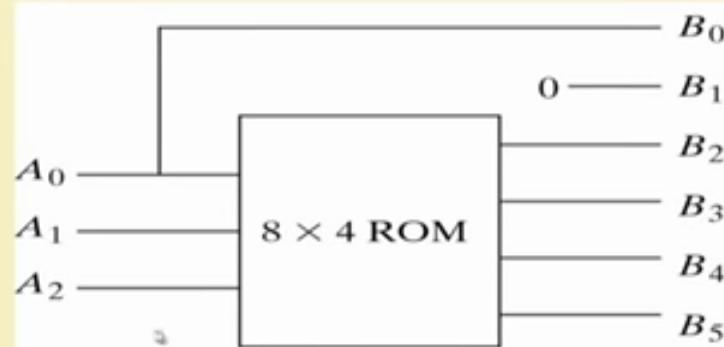
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# Example



(a) Block diagram

$A_2$	$A_1$	$A_0$	$B_5$	$B_4$	$B_3$	$B_2$
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

(b) ROM truth table

## ROM Implementation



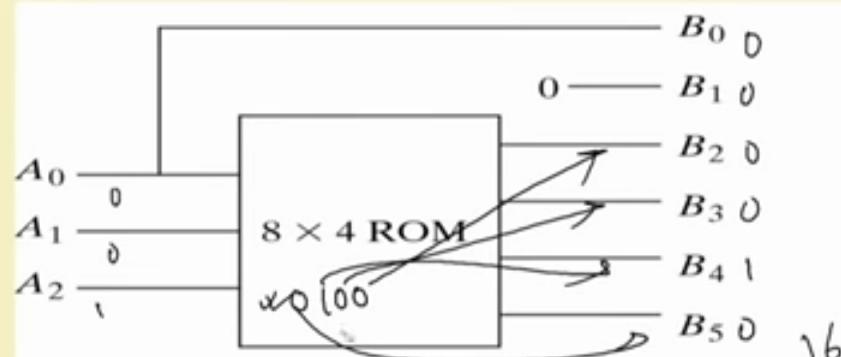
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# Example



(a) Block diagram

$A_2$	$A_1$	$A_0$	$B_5$	$B_4$	$B_3$	$B_2$
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

(b) ROM truth table

## ROM Implementation



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# Types of ROMs

- The required paths in a ROM may be programmed in four different ways.
  1. Mask programming: fabrication process
  2. Read-only memory or PROM: blown fuse /fuse intact
  3. Erasable PROM or EPROM: placed under a special ultraviolet light for a given period of time will erase the pattern in ROM.
  4. Electrically-erasable PROM(EEPROM): erased with an electrical signal instead of ultraviolet light.



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# Combinational PLDs

- A **combinational PLD** is an integrated circuit with **programmable** gates divided into an **AND array** and an **OR array** to provide an **AND-OR sum of product** implementation.
- **PROM**: fixed AND array constructed as a decoder and programmable OR array.
- **PAL**: programmable AND array and fixed OR array.
- **PLA**: both the AND and OR arrays can be programmed.



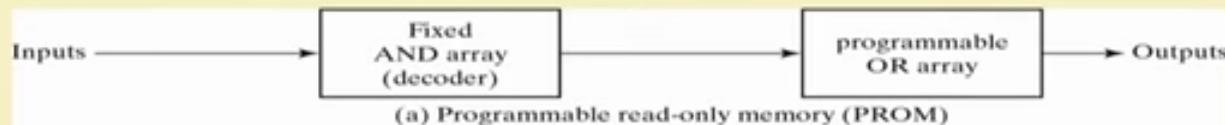
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## Combinational PLDs



Basic Configuration of Three PLDs



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## Programmable Logic Array

- The decoder in PROM example can be replaced by an array of AND gates that can be programmed to generate any product term of the input variables.
- The **product terms** are then **connected to OR gates to provide the sum of products** for the required Boolean functions.
- The **output is inverted when the XOR input is connected to 1 (since  $x \oplus 1 = x'$ )**. The **output doesn't change and connect to 0 (since  $x \oplus 0 = x$ )**.



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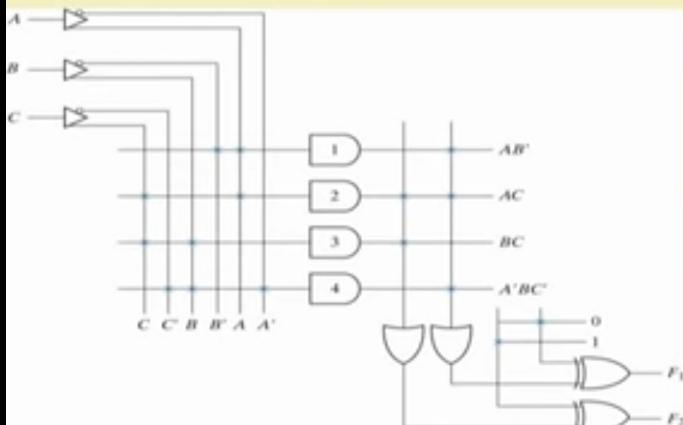
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# PLA

$$F_1 = AB' + AC + A'BC'$$

$$F_2 = (AC + BC)'$$



PLA with 3 Inputs, 4 Product Terms, and 2 Outputs

PLA Programming Table

Product Term		Inputs			Outputs	
		A	B	C	(T)	(C)
AB'	1	1	0	-	1	-
AC	2	1	-	1	1	1
BC	3	-	1	1	-	1
A'BC'	4	0	1	0	1	-



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# Programming Table

1. First: list the product terms numerically
2. Second: specify the required paths between inputs and AND gates
3. Third: specify the paths between the AND and OR gates
4. For each output variable, we may have a T(ure) or C(complement) for programming the XOR gate



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# Simplification of PLA

- Careful investigation must be undertaken in order to reduce the number of distinct product terms, PLA has a finite number of AND gates.
- Both the true and complement of each function should be simplified to see which one can be expressed with fewer product terms and which one provides product terms that are common to other functions.



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## Example

Implement the following two Boolean functions with a PLA:

$$F_1(A, B, C) = \sum(0, 1, 2, 4)$$

$$F_2(A, B, C) = \sum(0, 5, 6, 7)$$

The two functions are simplified in the maps shown.

		BC		B	
		00	01	11	10
		A	0	1	0
A	0	1	1	0	1
	1	1	0	0	0

1 elements  $F_1 = A'B' + A'C' + B'C'$

0 elements  $F_1 = (AB + AC + BC)'$

		BC		B	
		00	01	11	10
		A	0	1	0
A	0	1	0	0	0
	1	0	1	1	1

$$F_2 = AB + AC + A'B'C'$$

$$F_2 = (A'C + A'B + AB'C)'$$



## PLA table by simplifying the function

- Both the **true** and **complement** of the functions are simplified in **sum of products**.
- We can find the same terms from the group terms of the functions of  $F_1$ ,  $F_1'$ ,  $F_2$  and  $F_2'$  which will make the minimum terms.

$$F_1 = (AB + AC + BC)'$$

$$F_2 = AB + AC + A'B'C'$$

Product term	Inputs			Outputs	
	A	B	C	(C)	(T)
$AB$	1	1	1	-	1
$AC$	2	1	-	1	1
$BC$	3	-	1	1	-
$A'B'C'$	4	0	0	0	-



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