ECE 525 Final Exam July 2019

EXAMINATION RULES

1. This is an open-book/open-note take-home exam.
2. I can e-mail a MathCAD file with the exam problems to you if you would like a copy.
3. Do your own work on this examination. You are on your honor. Therefore, you will neither give nor receive aid on this examination, except from the *course* instructor. If you violate this trust, you will receive the grade of zero for this examination.
4. Show all of your work! Make it neat. *No* partial credit will be given if I can not easily follow your work.
5. You have 3 days to complete the exam the exam from the time you receive it from your proctor.
6. Pease read and sign the following statement when you finish the exam:
7. I certify that I have neither given nor have I received any help on this examination, except from the course instructor.

SIGNED: _____

PRINTED NAME:_____

DATE:_____

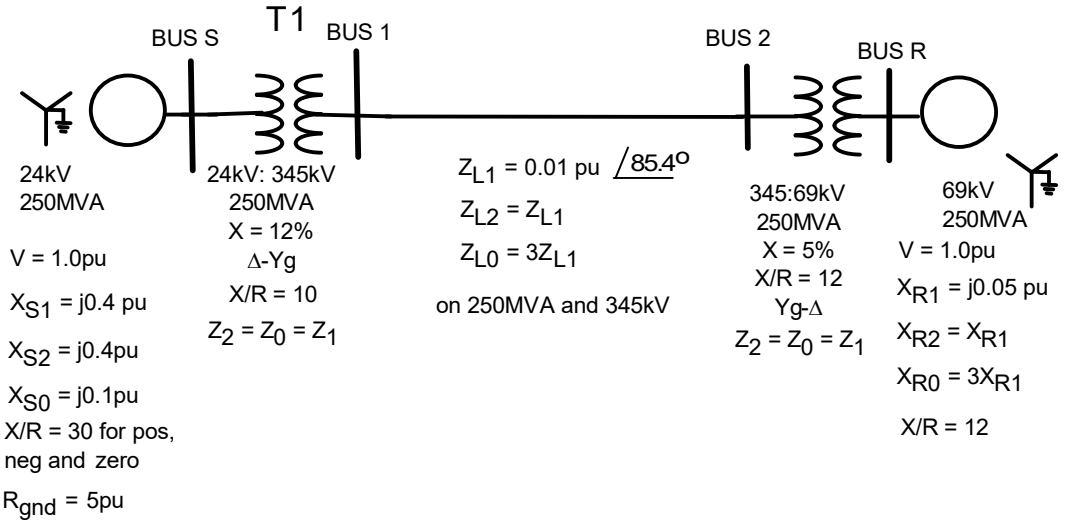
1. _____/46 pts

2. _____/36 pts

3. _____/18 pts

Total: _____/100 pts

1. (46 pts) Given the simple power system below, consider transformer protection options for T1.



A. Assuming the transformer, T1, above is connected to meet the standard ANSI phase shift, show how the windings are connected with a sketch and supporting description as needed. Include CT connections, first assuming you have electromechanical relays and second assuming you have a microprocessor relay. Also determine CT ratios for the microprocessor relay case.

B. Calculate the TAP settings to for the primary and secondary windings and choose appropriate connection compensation matrices for a differential protection scheme in a microprocessor relay.

C. Suggest a setting for an unrestrained overcurrent. What would you base this setting on?

D. Explain the difference between harmonic restraint and harmonic blocking in transformer differential protection. Recommend settings for each. When should these be acting?

E. Suppose you are instructed to choose a slope setting, assuming the relay can make a decision prior to CT saturation. The transformer also has a tap changer on the HV winding, with limits of +10% and -10%. Incorporate this in the slope setting (show your work).

F. Using the results of the earlier parts of the problem, calculate the IOP and IRT currents for the following external events. Will the element be secure using a slope setting of 40%. Currents in primary Amps

Case 1: Rated load, with nominal tap position:

$$\left|I_{HV\_F1}\right| = \begin{pmatrix} 418.37 \\ 418.37 \\ 418.37 \end{pmatrix} A \qquad \arg\left(I_{HV\_F1}\right) = \begin{pmatrix} -175.84 \\ 64.16 \\ -55.84 \end{pmatrix} deg \qquad \left|I_{LV\_F1}\right| = \begin{pmatrix} 6014.06 \\ 6014.06 \\ 6014.06 \end{pmatrix} A \qquad \arg\left(I_{LV\_F1}\right) = \begin{pmatrix} -25.84 \\ -145.84 \\ 94.158 \end{pmatrix} deg$$

Case 2: Rated load, with off nominal tap position on HV side (LV doesn't change):

$$\left|I_{HV\_F2}\right| = \begin{pmatrix} 469.504 \\ 469.504 \\ 469.504 \end{pmatrix} A \qquad \arg\left(I_{HV\_F2}\right) = \begin{pmatrix} -175.84 \\ 64.16 \\ -55.84 \end{pmatrix} deg \qquad \left|I_{LV\_F2}\right| = \begin{pmatrix} 6224.557 \\ 6224.557 \\ 6224.557 \end{pmatrix} A \qquad \arg\left(I_{LV\_F2}\right) = \begin{pmatrix} -25.84 \\ -145.84 \\ 94.158 \end{pmatrix} deg$$

Case 3: Phase open condition on the transmission line

$$\left|I_{HV\_F3}\right| = \begin{pmatrix} 134.270 \\ 0 \\ 136.266 \end{pmatrix} A \qquad \arg\left(I_{HV\_F3}\right) = \begin{pmatrix} -129.79 \\ 100.62 \\ -43.052 \end{pmatrix} deg \qquad \left|I_{LV\_F3}\right| = \begin{pmatrix} 1580.052 \\ 1141.957 \\ 1158.921 \end{pmatrix} A \qquad \arg\left(I_{LV\_F3}\right) = \begin{pmatrix} 3.132 \\ -129.79 \\ 136.948 \end{pmatrix} deg$$

Case 4: External SLG

$$\left|I_{HV\_F4}\right| = \begin{pmatrix} 1296.862 \\ 341.511 \\ 341.511 \end{pmatrix} A \qquad \arg\left(I_{HV\_F4}\right) = \begin{pmatrix} 94.049 \\ 97.217 \\ 97.217 \end{pmatrix} deg \qquad \left|I_{LV\_F4}\right| = \begin{pmatrix} 8106.92 \\ 8106.92 \\ 0 \end{pmatrix} A \qquad \arg\left(I_{LV\_F4}\right) = \begin{pmatrix} -87.074 \\ 92.926 \\ 104.036 \end{pmatrix} deg$$

Case 5: Repeat case 4, with only 20% of the current coming from the Phase A CT on the HV side.

2. (36 pts) Short Answer:

(a) (12 pts) Low impedance bus differential protection scheme:
(1) Explain how CT saturation could impact performance for faults internal to the zone
(2) Explain how CT saturation could impact performance for faults external to the zone. Which is more of a concern, internal or external
(3) What could be modified to create a bus protection scheme be set up to reduce the effect of saturation on security (list and describe at least 2 options).

(b) (8 pts) Describe how you would set up a bus protection scheme for a configuration that doesn't lend itself to differential protection, such as a ring bus.

(c) (8 pts) Describe the basic concept of a breaker failure scheme and create and describe a simple application example with a failure at a transmission bus.

(d) (8 pts) Suppose a station has two transformers in parallel, each with tap changers. How would a protection and control scheme be implemented to minimize circulating currents between the two transformers

3. (18 pts) You are given a bus with 3 incoming lines, as shown in the figure below. Each as a 1200/5, C600 CT with the charactersitic shown on the next page. Assumine a resistance of 0.0024 ohm/turn. The lead resistance is 0.81 ohm. from any CT to the junction point. Determine the settings for a high impedance bus differential relay which has a stabilizing resistance of 2000 ohms. Assume VLLrated = 230kV, Sbase = 100 MVA

The maximum fault external fault currents seen at any CT are as follows:

- Three phase fault: 45 kA
- SLG fault: 40 kA
- LL fault: 37 kA

Do the following:

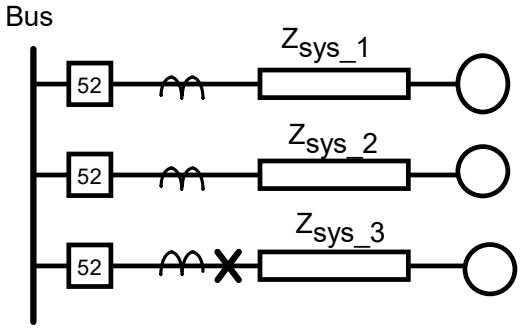
A. Determine the voltage set point using the equation (1) below (slightly modified from Lecture 23 and also equations (1) and (2) from the paper "Considerations for Using High-Impedance or Low-Impedance Relays for Bus Differential Protection" linked from lecture 24).

B. Determine the minimum primary internal fault current this relay can detect using equation (2) below (also equation (3) from the paper above).

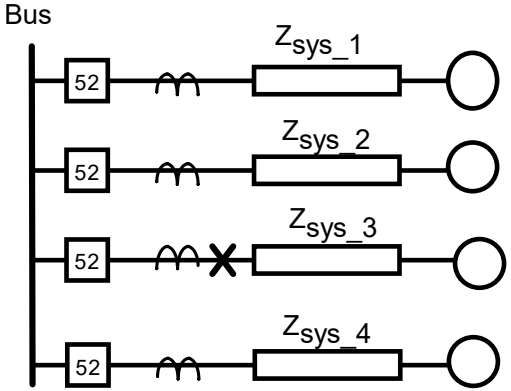
C. Repeat **A** and **B** if the stabilizer resistor is 1200 ohm

D. Repeat parts A and B if an additional feeder is added to the circuit, wth a CT identical to the others. The available fault currents increase to 50 kA for the 3 phase fault, 45 kA for the SLG and 39 kA for LL.

System Diagram for Parts A-C:



System Diagram for Part D:



$$V_R = 1.5\left(R_{CT} + k \cdot R_{Lead}\right) \cdot \frac{I_{Fmax}}{CTR} \qquad (1)$$

Where: $k = 1$ for a 3 phase fault, and $k = 2$ for unbalanced faults.

$$I_{min} = \left(n \cdot I_e + I_{relay} + I_m\right) \cdot CTR \qquad (2)$$

Where: I_e is the CT excitation current for the voltage across the magnetizing branch

n is the number of CTs in parallel

I_{relay} the current through the relay for the applied voltage (in this case, to determine the minimum fault current, use the setpoint voltage, V_R, divided by the stabilizing resistance

I_m MOV leakage current at the applied voltage (0A in the minimum fault detectable fault current case.

CT data

CT Data: C600 class, 1200/5

ORIGIN := 1

CT Excitation Curve

$$excitation := \begin{pmatrix} .001 & 0.09 \\ .04 & 90 \\ .1 & 428 \\ .12 & 520 \\ .14 & 600 \\ .2 & 700 \\ .3 & 780 \\ .4 & 800 \\ 40 & 927 \end{pmatrix}$$

TAPS

$$t := \begin{pmatrix} 240 \\ 200 \\ 180 \\ 160 \\ 120 \\ 100 \\ 80 \\ 60 \\ 40 \\ 20 \end{pmatrix}$$

$$v_t(N2) := \left(\frac{N2}{t_1}\right) \cdot \text{excitation}^{\langle 2 \rangle} \qquad Im_t(N2) := \left(\frac{t_1}{N2}\right) \cdot \text{excitation}^{\langle 1 \rangle}$$