CS451/CS551/ECE441/ECE541 - SECOND EXAM
Fall 2019

Name (Please print):_____

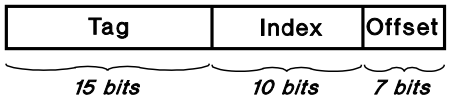
Take home exam. I don't want the "wikipedia" or internet answer, I want *your* answer. Be concise with your answers - excessive wording will result in a loss of points. Show your work for full credit. You may not consult anyone else (except the instructor) regarding answers to this test.

By signing your name below, you swear that you have not received help from anyone else (besides the instructor) in writing this test:

Name (Please Sign):_____

There are 10 questions to this test.

1. (15 pts) The 32 bit address generated by a certain processor is divided up as shown to access its cache:



If this address is used to access a *4-way set associative* cache, answer the following questions. If you cannot determine the answer to a question from the information given, then so state. Assume the memory is byte addressable.

- What is the cache line (block) size in bytes?

- How many sets are in the cache?

- How many blocks are in the cache?

- Is the cache a virtually addressed or physically addressed cache?

- What is the total cache size in bytes?

2. (9 pts) When designing a cache memory, a designer can choose several different parameters for that cache - total cache size, cache line (block) size, and associativity. For a given set of these parameters, explain what you would need to do to reduce the following types of cache misses:

a) Compulsory misses

b) Capacity misses

c) Conflict misses

3. (9 pts) We used several terms to describe memory in a modern processor. Describe each term below - be sure to distinguish each term from the others.

- Physical Memory

- Logical Memory

- Virtual Memory

4. (4 pts) Explain the purpose of the TLB in a virtual memory system.

5. (4 pts) Some processors implement *data prefetch* instructions. Explain how these can speed up overall memory access.

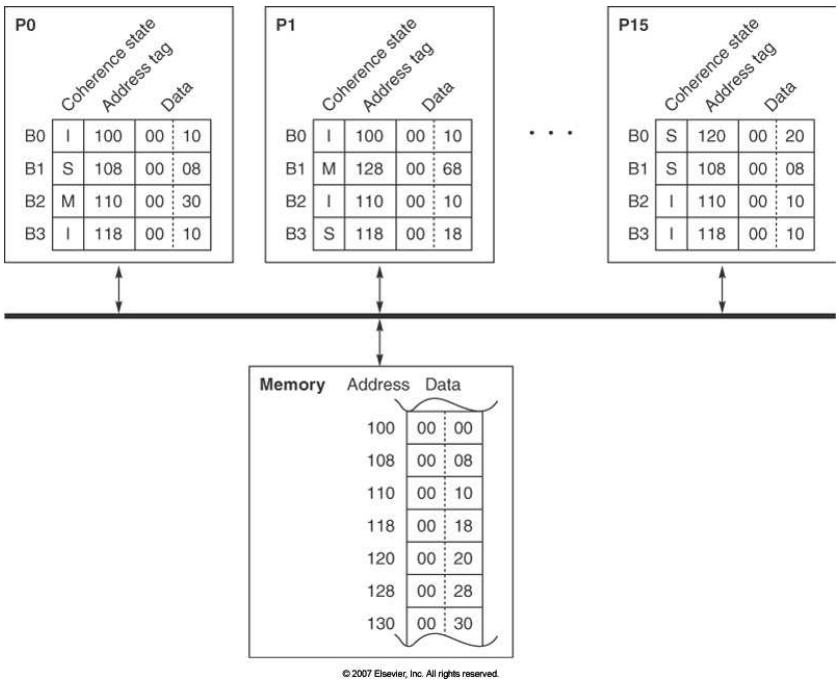
6. (8 pts) Both write through and write back caches are in common use, which would suggest that there are pros and cons for each. List one advantage and one disadvantage for each type.

7. (5 pts) Explain what a *victim buffer* does.

8. (6 pts) With virtual memory, it is not necessary for the *virtual address space* to be the same as the *physical address space*. For example, the larger models of the 16-bit PDP11 processor had a 4 mB (22 bit) physical address space. Conversely, several models of the 64-bit Alpha processor have a 44-bit physical address. Explain how this is done.

9. (20 pts) You currently have a processor with a direct-mapped, L1 cache. Its hit rate is 90%, and the miss penalty to main memory is 80 cycles. You are considering adding an off-chip L2 cache. This cache will be sized so that its hit rate is 96%. The hit time in this cache is 8 cycles, and its miss penalty to main memory is 90 cycles. Determine the speedup you can expect to gain (if any) with this cache, if the base CPI of the processor is 1.5, with an instruction mix that includes 20% loads and 10% stores.

10. (20 pts) The figure below represents the current status of a bus-based multiprocessor that uses a snooping protocol similar to that described in the textbook. The local caches of processors **P0**, **P1**, etc. and main memory are shown. Each cache has room for 4 blocks (**B0** thru **B3**), and each block holds 2 32-bit values. The current status of each block in the cache is shown in the figure (`I` - Invalid, `S` - for shared, and `M` - for Exclusive as described in the textbook). For each part below, assume that the initial cache state is as shown in the figure - that is, the operations are *not* cumulative. Describe what the state of the system will be as a result of the following CPU operations:



- a) CPU **P0** reads address 120

- b) CPU **P0** writes the value 80 into address 120

- c) CPU **P15** writes the value 80 into address 120

- d) CPU **P0** reads address 110

- e) CPU **P0** write the value 48 into address 108