

**Muhammad Junaid Saleem Qadri**

**70003**

**Solution:-**

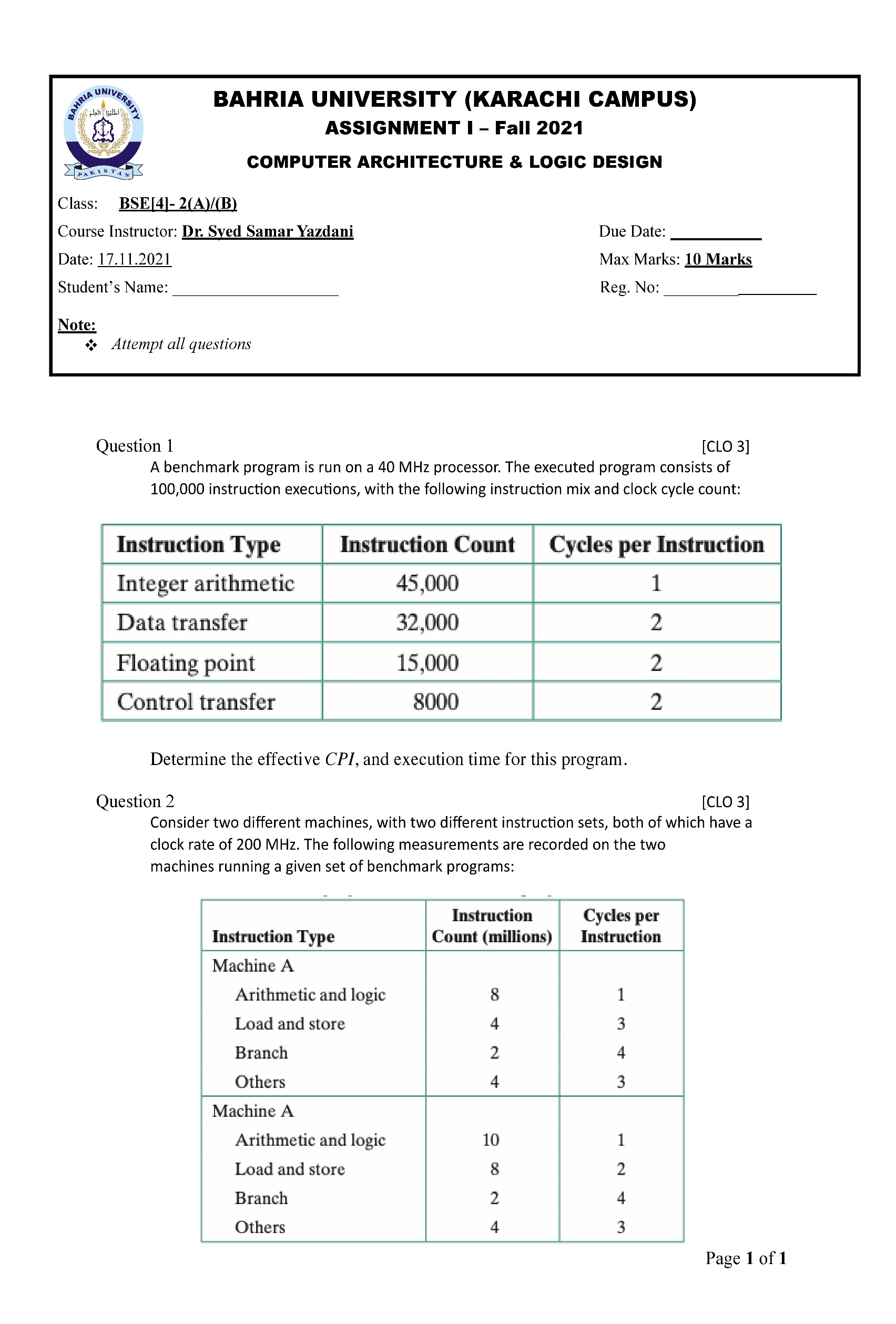
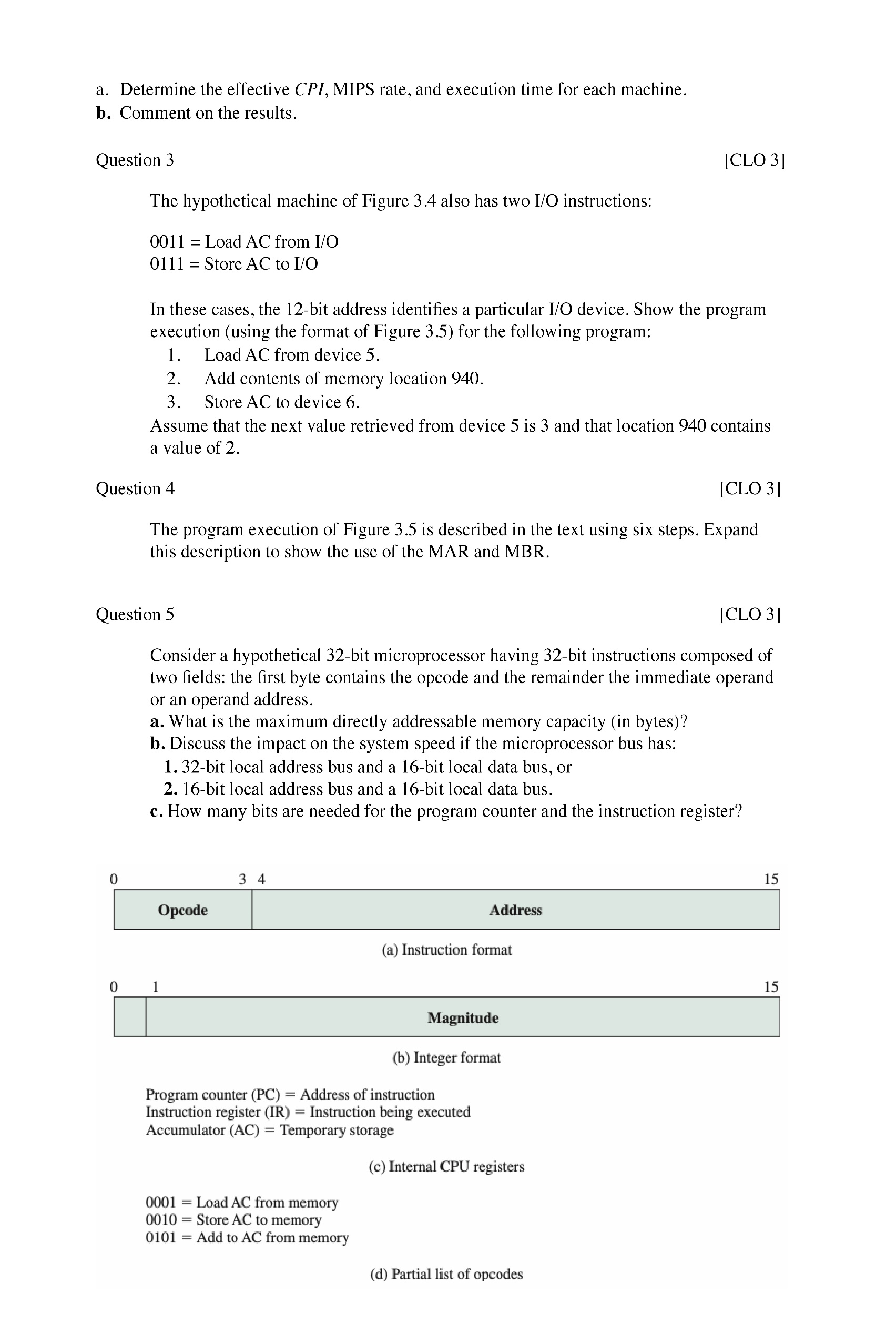
CPI (average Clocks per instructions) =

45000 + (2\*32000) + (2\*15000) + (8000\*2) / (100 000) = 155 / 100 = **1.55**

MIPS =40 M clocks / sec \* (1/1.55 clocks per instruction) = 40 / 1.55 / 1000000 = **25.8 MIPs**

Execution time = (100 000 instructions) \* 1.55 CPI = 155 000 cyles \* 1/40M sec = **3.87 ms**

Stallings: CPI = 1.55; MIPS rate = 25.8; Execution time = 3.87 ms.

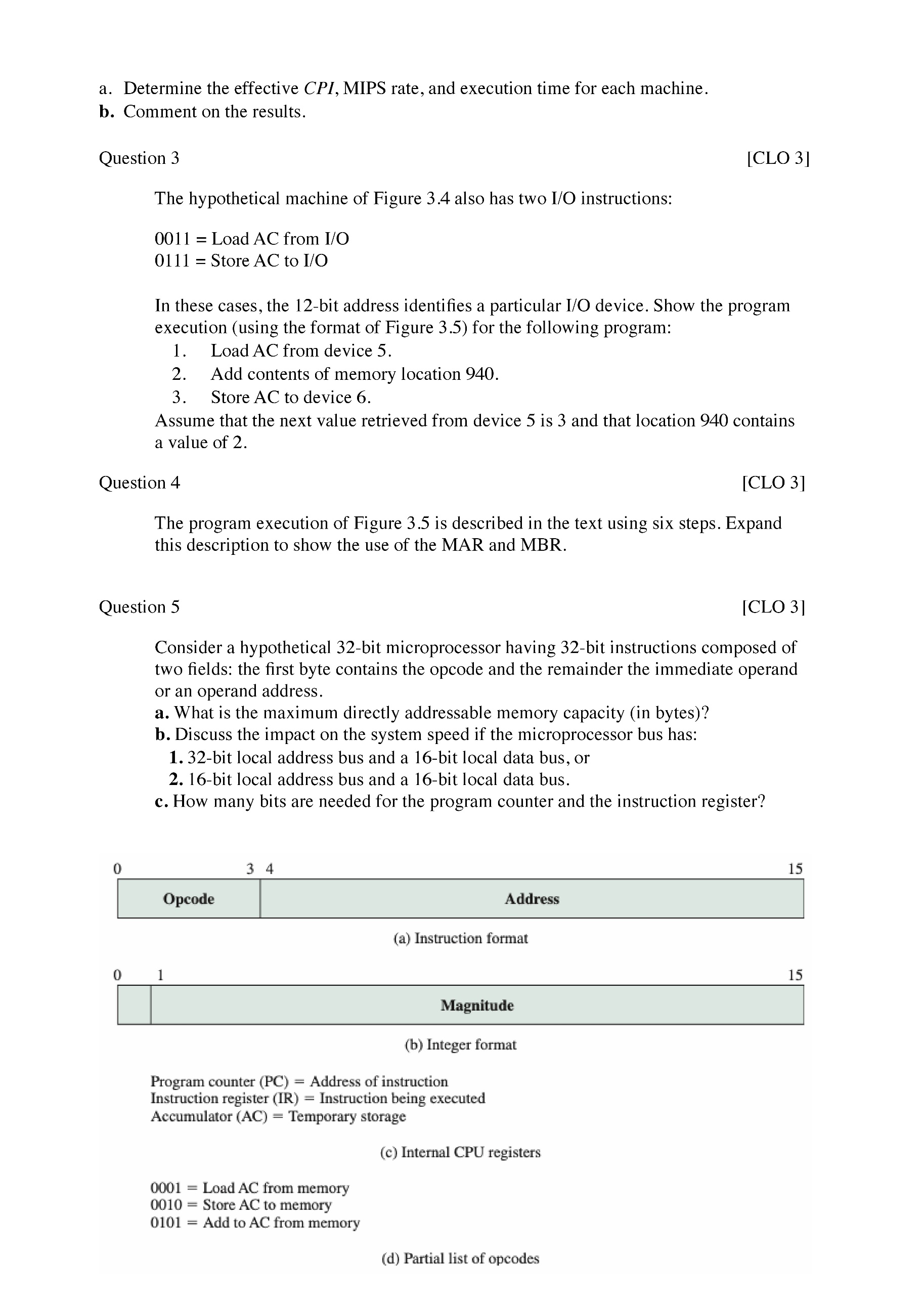


**Solution:-**

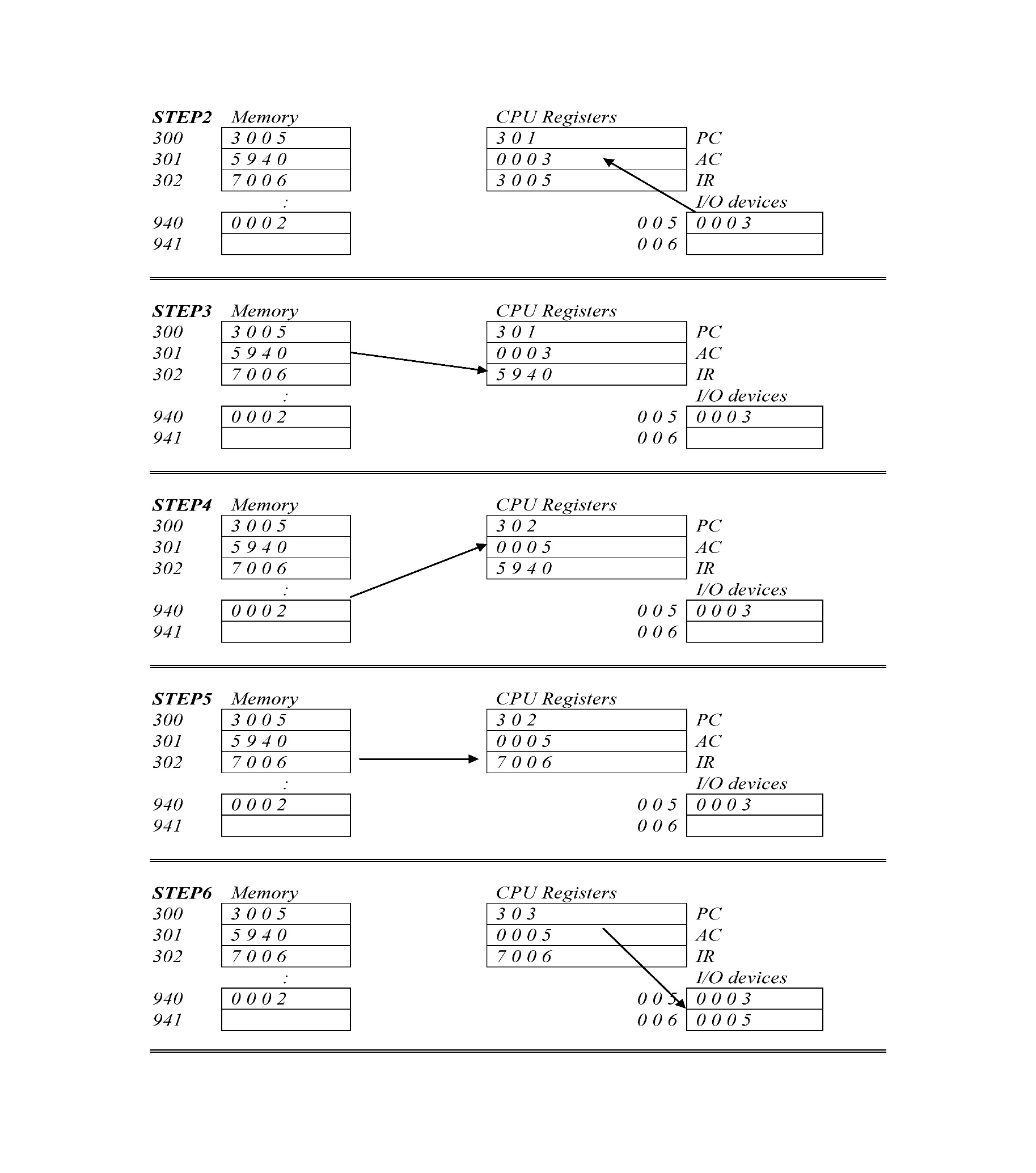
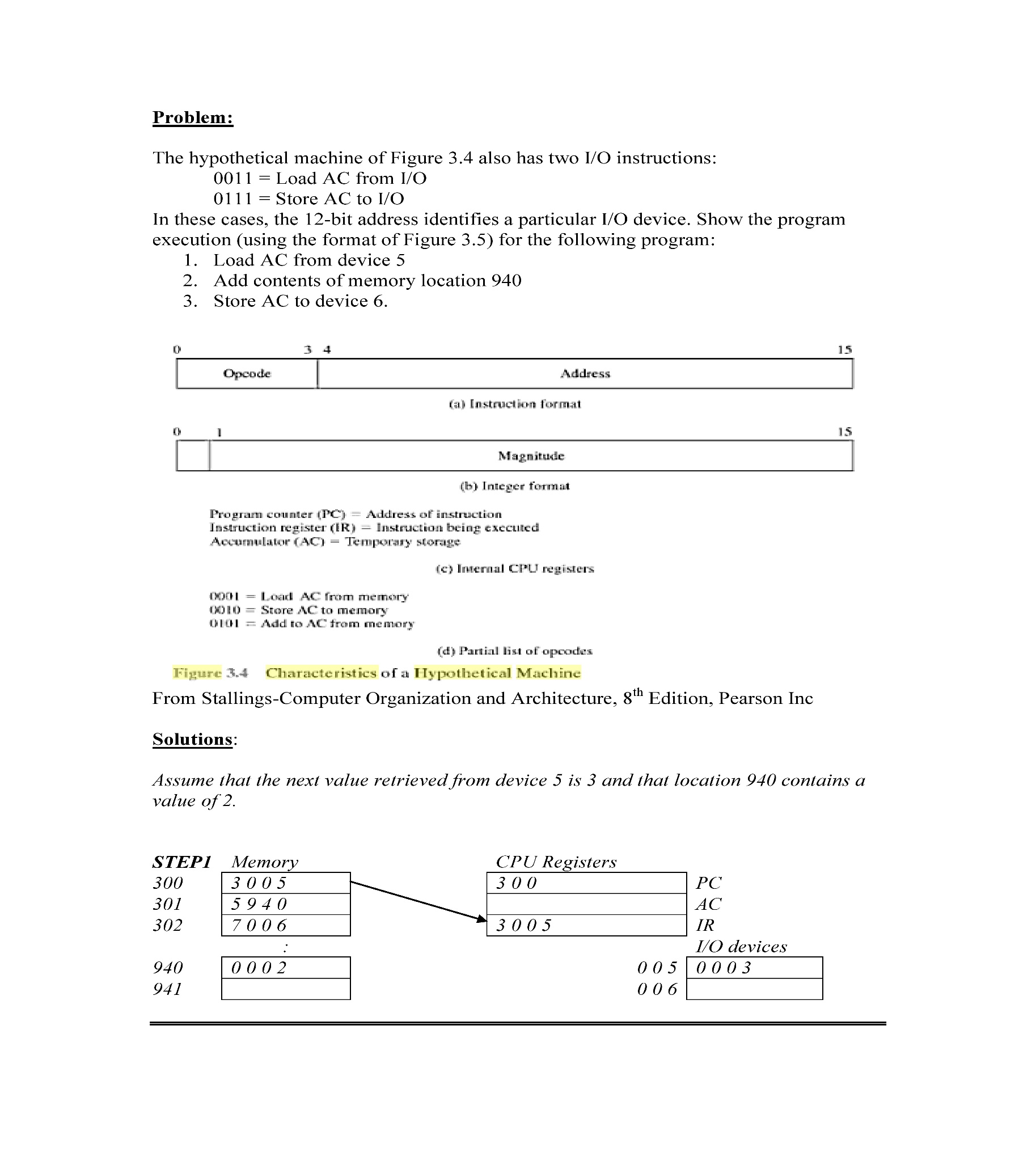


**a)**

**b)** Even though, machine B has a higher MIPS than machine A, it needs a longer CPU time to execute the similar set of benchmark programs (instructions).



**Solution :-**



**Table

Description automatically generated**

**Solution :-**

**STEP 1:**

A) The PC contains 300, the address of the first instruction. This value is loaded in to the MAR.

B) The value in location 300 is loaded into the MBR, and the PC is incremented. These two steps can be done in parallel.

C) The value in the MBR is loaded into the IR.

**STEP 2:**

A) The address portion of the IR (940) is loaded into the MAR.

B) The value in location 840 is loaded into the MBR.

C) The value in the MBR is loaded into the AC.

**STEP 3:**

A) The value in the PC (301) is loaded in to the MAR.

B) The value in location 301 is loaded into the MBR, and the PC is incremented.

C) The value in the MBR is loaded into the IR.

**STEP 4:**

A) The address portion of the IR (941) is loaded into the MAR.

B) The value in location 941 is loaded into the MBR.

C) The old value of the AC and the value of location MBR are added and the result is stored in the AC.

**STEP 5:**

A) The value in the PC (302) is loaded into the MAR.

B) The value in location 302 is loaded into the MBR, and the PC is incremented.

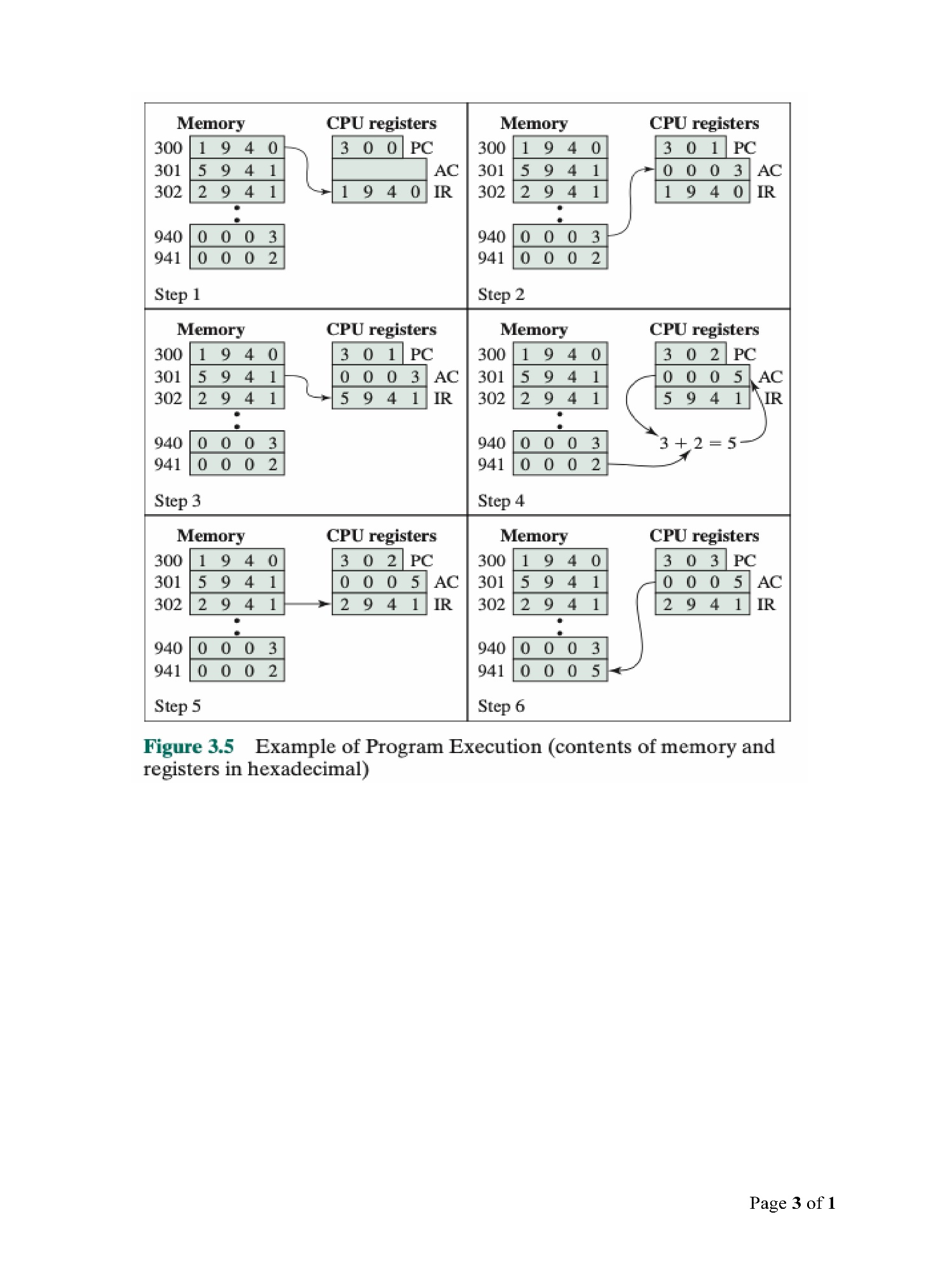
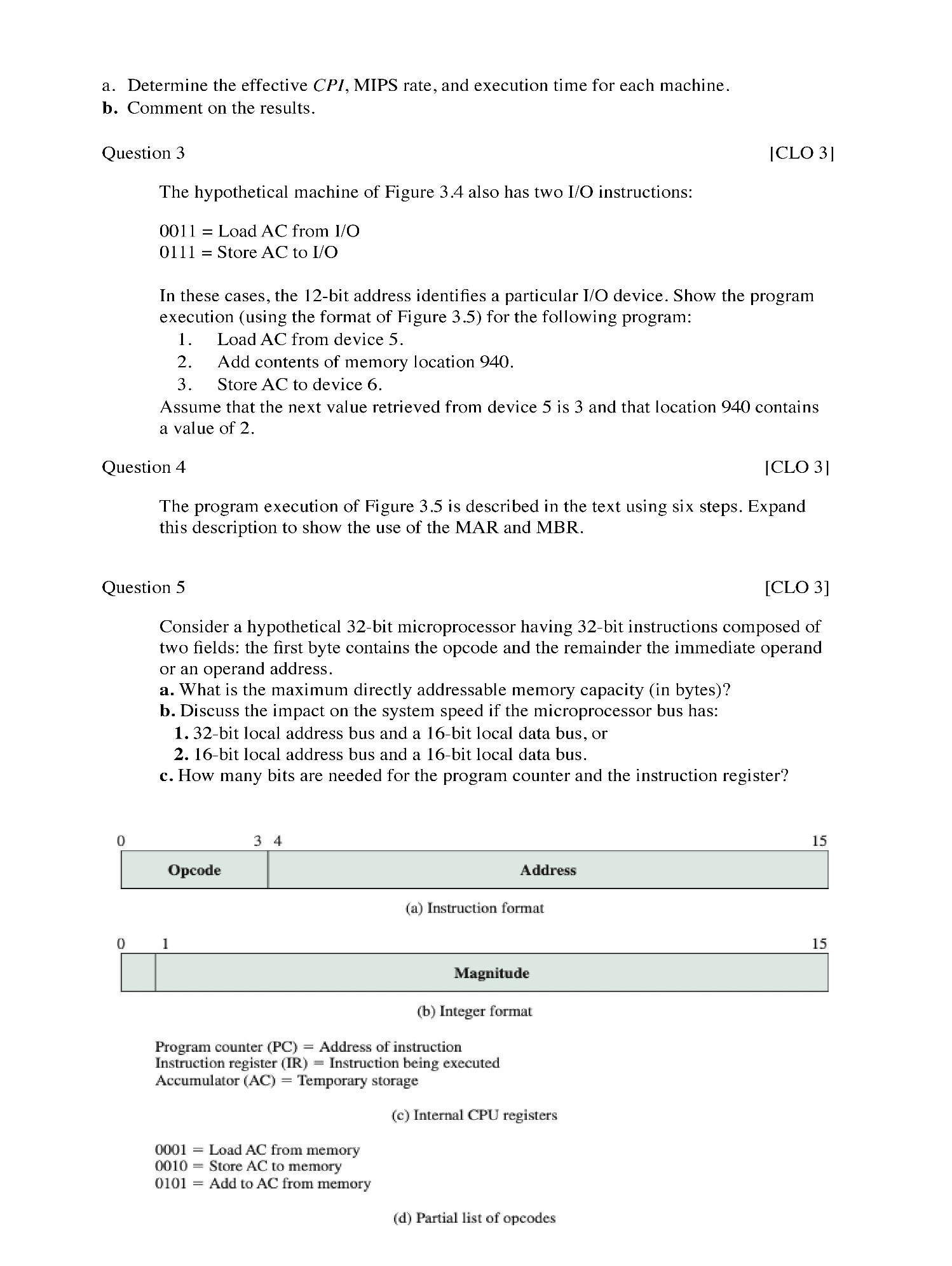
C) The value in the MBR is loaded into the IR.

**STEP 6:**

A) The address portion of the IR (941) is loaded into the MAR.

B) The value in the AC is loaded into the MBR.

C) The value in the MBR is stored in location 941.



**Solution :-**

**a)**  2(32-8) = 224 = 16,777,216 bytes = 16 MB ,(8 bits = 1 byte for the opcode).

**b,1)** A 32-bit local address bus and a 16-bit local data bus. Instruction and data transfers would take three bus cycles each, one for the address and two for the data. Since If the address bus is 32 bits, the whole address can be transferred to memory at once and decoded there; however, since the data bus is only 16 bits, it will require 2 bus cycles (accesses to memory) to fetch the 32-bit instruction or operand.

**b,2)** A 16-bit local address bus and a 16-bit local data bus. Instruction and data transfers would take four bus cycles each, two for the address and two for the data. Therefore, that will have the processor perform two transmissions in order to send to memory the whole 32-bit address; this will require more complex memory interface control to latch the two halves of the address before it performs an access to it. In addition to this two-step address issue, since the data bus is also 16 bits, the microprocessor will need 2 bus cycles to fetch the 32-bit instruction or operand.

**c)** For the PC needs 24 bits (24-bit addresses), and for the IR needs 32 bits (32-bit addresses).

The End