Intel core 13:

The processor is a personal computer or embedded in a small device is often called microprocessor. This means the elements are contained on a single ontegrated chip TSL.

lore IB is a desktop/waptop processor with INTEL

Applications'

- 1) Laptop
- 2) computer
- 3) Android cellphones
- W AT -700 W
- 5) Simulation

Specifications: There are various versions and generations of the Intel core 13. Thus the specifications can vary based on the generation.

The power regularement range from 55 w to 90 W

- + Here es a general overview:
 - 1) Address Bus: Typically they have a 64-61+ address
 - 3) Data Bus: The data bus is also a 64-67+ one.
 - 3) Clock speed; The base clock speeds depend on the generation. They can vary from D. MGHZ to 4.0 GHZ
 - 4) Cache memory:

L1 eache -32kB per core (64kB total).

a cache - 256kB per core (512 KB en +0 tal). L3 cache - 3 to 8 MB . shared between the cores

some other features of core 13:

i) They have 4 processing threads for multithreading. and multitasking

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- For Kimm process
- 3) Intel HO Emaphies

like other *86 Architechture CPU's they have varrety of registers, General purpose registers (16), segment registers, instruction pointers, flags register, floating point and SIMD registers

The CPU works with dary 1 dary dype memory. Overall, all these elements work together in tandem to Prorease efficiency.

238050255 Y. Mohan Kalyan.

7 The core 15 features a more advanced architecture compared to core 13.

The 95 series · meroprocessors -are built on various architures Nehalem, sandy Bordge, Skylake and many more.

They typically have 4-6 cores depending on model generation and architecture. The newer ones also support hyper-threading

· Registers- Registers in 15 are similar to 13 but enhanced. of They ware to war this comes to be truncated to but it

- 1) General purpose Régisters
 - 2) Segment registers
 - 3) Instruction pointers. 3101 6 4 0 4 18 - 17 , 2926; 16
 - 4) Hag Registers.
- न्यान अवस्था किया रहार -) This data bus is typically by bit loide.
- -) Address is also to By-6it bys.

cache: L1 -> 32 KB per core L2 -> 256 KB per core. L3 -> 3-1 12 MB Shared among all cores

23BDS0255 Y. Mohan Kalyan.

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- 7 Address is also & BU-59+ 645.

Cache: L1 -> 32 KB per core

L2 -> 256 KB per core

L3 -> 3-> 12 MB Shared among all core)

Intel core 17:-

- by Indigo.
 - Sandy bridge, skylate etc.
 - Tristruction set: x86-84 (64bit). With support
- The clock speed ranges from 20142 54HZ ranging on generation & model.
- -) Intially fabricated at 45 NM but now at 10/14nm.
- # Modern : 75 use a 64 bit address . bit & a64 bit wide data bus.

The bus interface is quickpath or DMI

cache: L1 - 31kB per core

La -> 256 KB per core

L3 -> HAB- 25MB. depending on model.

The power ranges from 35W to 125W.

-) .97 Ps well · Suited for · high performance · tasks such as gaming, was · Video - editing, AI Workloadsek.

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