

AHB-Lite Protocol Verification

EE-595f SoC System Verilog

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Introduction to the Device-Under-Test (DUT)

AMBA3 AHB-lite Protocol

Introduction

AMBA AHB-Lite addresses the requirements of high-performance synthesizable designs. It is a bus interface that supports a single bus master and provides high-bandwidth operation. AHB-Lite implements the features required for high-performance, high clock frequency systems including:

- burst transfers
- single-clock edge operation
- non-tristate implementation
- wide data bus configurations, 64, 128, 256, 512, and 1024 bits.

The most common AHB-Lite slaves are internal memory devices, external memory interfaces, and high bandwidth peripherals. Although low-bandwidth peripherals can be included as AHB-Lite slaves, for system performance reasons they typically reside on the AMBA Advanced Peripheral Bus (APB). Bridging between this higher level of bus and APB is done using a AHB-Lite slave, known as an APB bridge.

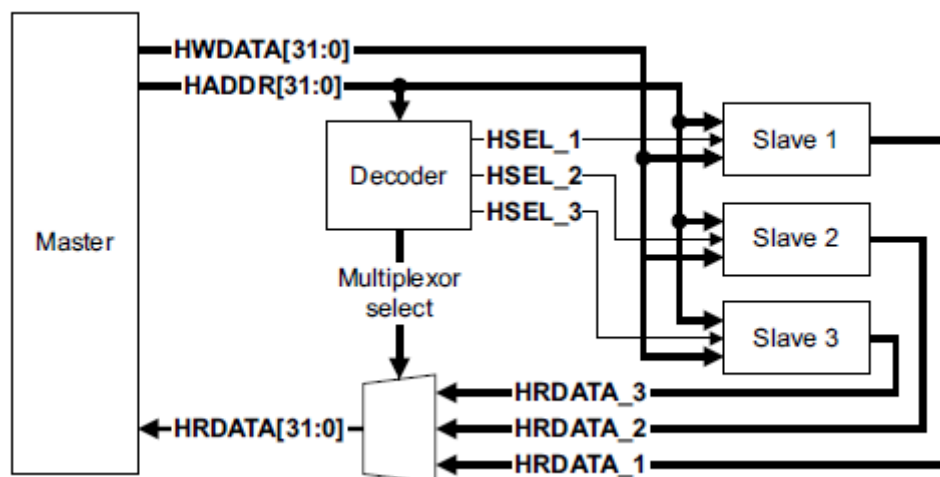


Figure 1 AHB lite block diagram

Components

1. Master

In order to perform read and write operations on slaves, the master gives the necessary information. When presenting the arbitration, each slave is chosen via a selection signal as explained below (HSEL). For example, the slave can now clearly distinguish between when it is being stimulated and when it is not. Additionally, it gets two response signals from the slaves, HRESP and HREADY, to determine whether or not a transfer has been completed successfully (HRESP) and whether or not an extension of the data phase is necessary (HREADY).

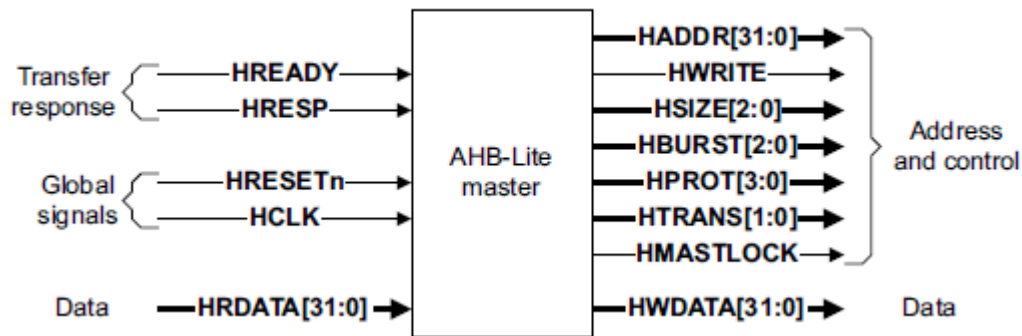


Figure 2 Master interface

2. Slave

Whenever a master in the system initiates a transfer, an AHB-Lite slave responds. HSELx select signals from the decoder are used to determine when a bus transfer occurs for the slave. The slave informs the master of the data transfer's success, failure, or delay.

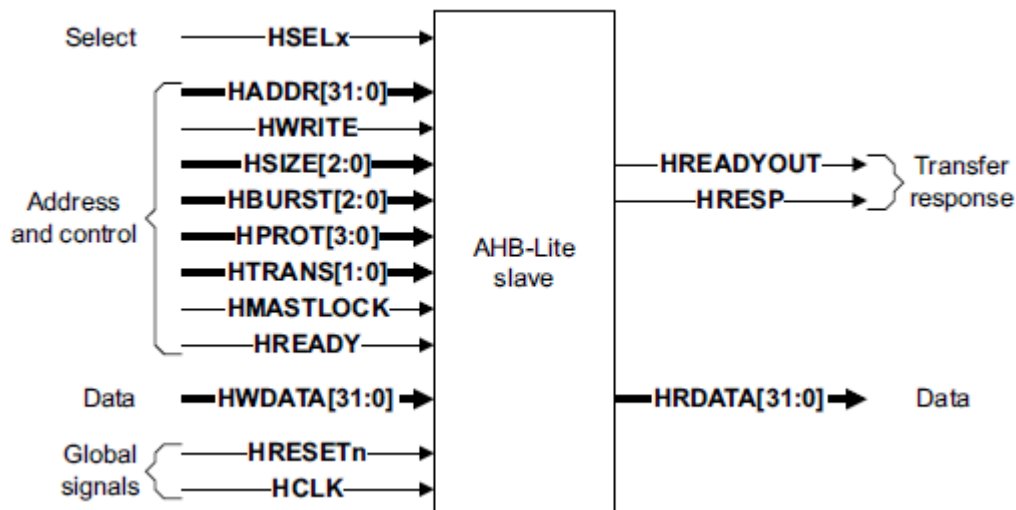


Figure 3 Slave interface

3. Decoder

The address of each transfer is decoded by this component, and a select signal is provided for the slave that is involved. The multiplexor receives a control signal from it as well. All AHB-Lite implementations that make use of two or more slaves must have a single centralised decoder.

4. MUX

There must be a multiplexer between the slaves and the master in order to multiplex the read data and response signals. The multiplexor is controlled by the decoder. All AHB-Lite implementations employing two or more slaves must make use of a single centralised multiplexor.

Working operation

The master starts a transfer by driving the address and control signals. These signals provide information about the address, direction, width of the transfer, and indicate if the transfer forms part of a burst. Transfers can be:

- single
- incrementing bursts that do not wrap at address boundaries

- wrapping bursts that wrap at particular address boundaries.

The write data bus moves data from the master to a slave, and the read data bus moves data from a slave to the master. Every transfer consists of:

- Address phase one address and control cycle
- Data phase one or more cycles for the data.

A slave cannot request that the address phase is extended and therefore all slaves must be capable of sampling the address during this time. However, a slave can request that the master extends the data phase by using HREADY. This signal, when LOW, causes wait states to be inserted into the transfer and enables the slave to have extra time to provide or sample data. The slave uses HRESP to indicate the success or failure of a transfer.

Signals

Global signals

Name	Source	Description
HCLK	Clock source	The bus clock times all bus transfers. All signal timings are related to the rising edge of HCLK.
HRESETn	Reset controller	The bus reset signal is active LOW and resets the system and the bus. This is the only active LOW AHB-Lite signal.

Master signals

Name	Destination	Description
HADDR [31:0]	Slave and decoder	The 32-bit system address bus.
HBURST [2:0]	Slave	The burst type indicates if the transfer is a single transfer or forms part of a burst. Fixed length bursts of 4, 8, and 16 beats are supported. The burst can be incrementing or wrapping. Incrementing bursts of undefined length are also supported.
HMASTLOCK	Slave	When HIGH, this signal indicates that the current transfer is part of a locked sequence. It has the same timing as the address and control signals.
HPROT [3:0]	Slave	The protection control signals provide additional information about a bus access and are primarily intended for use by any module that wants to implement some level of protection. The signals indicate if the transfer is an opcode fetch or data access, and if the transfer is a privileged mode access or user mode access. For masters with a memory management unit these signals also indicate whether the current access is cacheable or buffer able.
HSIZE [2:0]	Slave	Indicates the size of the transfer, that is typically byte, halfword, or word. The protocol allows for larger transfer sizes up to a maximum of 1024 bits.
HTRANS [1:0]	Slave	Indicates the transfer type of the current transfer. This can be: <ul style="list-style-type: none">• IDLE• BUSY• NONSEQUENTIAL• SEQUENTIAL.
HWDATA [31:0]	Slave	The write data bus transfers data from the master to the slaves during write operations. A minimum data bus width of 32 bits is recommended. However, this can be extended to enable higher bandwidth operation.
HWRITE	Slave	Indicates the transfer direction. When HIGH this signal indicates a write transfer and when LOW a read transfer. It has the same timing as the address signals, however, it must remain constant throughout a burst transfer.

Slave signals

Name	Destination	Description
HRDATA [31:0]	MUX	During read operations, the read data bus transfers data from the selected slave to the multiplexor. The multiplexor then transfers the data to the master. A minimum data bus width of 32 bits is recommended. However, this can be extended to enable higher bandwidth operation.
HREADYOUT	MUX	When HIGH, the HREADYOUT signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
HRESP	MUX	The transfer response, after passing through the multiplexor, provides the master with additional information on the status of a transfer. When LOW, the HRESP signal indicates that the transfer status is OKAY. When HIGH, the HRESP signal indicates that the transfer status is ERROR.

Decoder signals

Name	Destination	Description
HSELx	Slave	Each AHB-Lite slave has its own slave select signal HSELx and this signal indicates that the current transfer is intended for the selected slave. When the slave is initially selected, it must also monitor the status of HREADY to ensure that the previous bus transfer has completed, before it responds to the current transfer. The HSELx signal is a combinatorial decode of the address bus.

MUX signals

Name	Destination	Description
HRDATA [31:0]	Master	Read data bus, selected by the decoder.
HREADY	Master and Slave	When HIGH, the HREADY signal indicates to the master and all slaves, that the previous transfer is complete.
HRESP	Master	Transfer response, selected by the decoder

Verification plan

Sr. No.	Feature	Test Description	Reference	Type	Result	Comments
1	Operation	Initiated signal must give the address, direction and width of transfer	1.2	TR		HRESP is OKAY
2	Extension	Extension of data phase from slave by using HREADY	1.2	TR		HREADY is low, Slave is WAIT and HRESP is OKAY
3	Signals	All master, slave, global, decoder and mux signals are working in range	2	A		HRESP is OKAY
4	Basic read operation	The slave must generate the data on the read data bus	3.1	A		HWRITE is low, HREADY is high
5	Basic write operation	master broadcasts data on the write data bus	3.1	A		HWRITE is high, HREADY is high
6	Simple transfer no wait	Transfer should consist of one address, one cycle, and one data cycle. The address phase of any transfer must occur in during data state of previous transfer	3.1	TR		HWRITE is high when write else low, HREADY is in WAIT and then high
7	Wait state	Insert wait states in any transfer	3.1	TR		HREADY is in WAIT and then high
8	IDLE state	No transfer of data is occurred	3.2	A		HRESP is OKAY, Slave gives WAIT
9	BUSY case-1	Bursts transfer is occurring so next transfer cannot take place immediately	3.2	A		HRESP is OKAY, Slave gives WAIT
10	BUSY case-2	When master uses BUSY , the address and control signals must reflect the next transfer in bursts	3.2	A		HRESP is OKAY, Slave gives WAIT

11	NONSEQ case 1	It must be a single transfer or first transfer of burst, and It must have length one	3.2	A		HRESP is OKAY, Slave gives WAIT
12	SEQ	The control information is identical to previous transfer, the address is related to previous transfer and is equal to previous transfer plus transfer size and In case of wrapping bursts, the address of the transfer wraps at wrapping boundary	3.2	A		HRESP is OKAY
13	HSIZE [2:0]	HSIZE must be 3-bit input	3.4	A		HSIZE is 3 bits
14	Transfer size	Transfer size set by HSIZE must be less than or equal to width of data bus	3.4	A		HRESP is OKAY
15	Address boundary	HSIZE must be used in conjunction with HBURST to determine address boundary for wrapping bursts	3.4	A		Respective HSIZE and HRESP is OKAY
16	Burst transfer	HSIZE must remain constant throughout burst transfer	3.4	A		HSIZE is constant
17	HSIZE [2:0] cases	All eight transfer sizes are covered i.e. Byte, halfword, Word, Doubleword, 4-word line, 8-word line	3.4	TR		Transfer size is <= width of data bus
18	Burst operation	The actual address must be previous + offset size given by HSIZE	3.5	A		For example, INCR4
19	Wrapping bursts	Address boundary must be product of number of beats and size of transfer	3.5	A		For example, four beat wrapping bursts starts with 0x34
20	Transfer size	All transfers must be aligned to the address boundary equal to the size of transfer	3.5	A		For example, halfword must be aligned to halfword boundaries HADRR [0] = b00
21	Fixed length bursts	Each fixed length bursts must terminate with a SEQ type	3.5.1	A		
22	Cancel Bursts	Master can cancel the bursts remaining if slave throws an ERROR	3.5.2	TR		This restriction is not strictly applied

23	IDLE transfer	During waited IDLE transfer, if master changes type to NONSEQ , the address must be constant	3.6.1	A		HREADY is high, HTRANS is constant HBURST is INCR4 and HRDATA reads data
24	Busy transfer with fixed length	Master changes from BUSY to SEQ transfer for fixed length bursts	3.6.1	TR		HREADY is low, HBURST is INCR and HRESP is OKAY
25	No busy transfer on SINGLE bursts	BUSY transfer must be applied between two successive bursts, i.e., INCR4 , INCR8 , INCR16 , WRAP4 , WRAP8 and WRAP 16	3.6.1	A		HRESP is OKAY and HREADY is low
26	Busy transfer: case-1	Master changes from BUSY to IDLE or NONSEQ transfer, and undefined length burst is terminated	3.6.2	TR		HREADY is low, HBURST is INCR and HRESP is OKAY
27	Busy transfer: case-2	Master changes from BUSY to SEQ transfer and undefined length burst is continued	3.6.2	TR		HREADY is low, HBURST is INCR, and Slave is OKAY
28	Busy transfer: case-3	Master changes from IDLE to SEQ transfer	3.6.1	TR		HREADY is low, HBURST is INCR and HRESP is ERROR
29	ERROR response	If slaves throw an ERROR , master changes the address	3.6.2	A		HRESP is ERROR, HREADY is low
30	ERROR response	ERROR must retain for two HCLK cycles	3.6.2	A		HRESP is ERROR, HREADY is low
31	Default slave case-1	If a NONSEQUENTIAL or SEQUENTIAL transfer address location is attempted to a non-existent	4.1.1	A		HRESP is ERROR, HREADY is low
32	Default slave case-2	IDLE or BUSY transfers to non-existent locations	4.1.1	A		HRESP is OKAY, HREADY is low
33	Slave response	A slave must provide a response that indicates the status of the transfer	5.1	A		HRESP should respond

34	HRESP case-1	The transfer has either completed successfully or additional cycles are required for the slave	5.1	A		HRESP is OKAY
35	HRESP case-2	A two-cycle response is required for an error condition with HREADY being asserted in the second cycle.	5.1	A		HRESP is ERROR, HREADY is low
36	Transfer done	A successful completed transfer is signalled	5.1.1	A		HREADY is high, HRESP is OKAY
37	Transfer pending	When a slave inserts a number of wait states prior to completing the response	5.1.2	A		HREADY is low, HRESP is OKAY
38	Latency	Every slave must have a predetermined maximum number of wait states	5.1.2	A		HREADY is low, HRESP is OKAY
39	ERROR case-1	If the slave requires more than two cycles to provide the ERROR response then additional wait states can be inserted at the start of the transfer.	5.1.3	A		HREADY is low, HRESP is OKAY
40	Separate read and write	Separate read and write data buses are required to implement an AHB-Lite system	6.1	A		HRESP is OKAY
41	Correct byte lane	For read write transfers, the receiving module must select the data from the correct byte lane on the bus	6.2	A		HRESP is ERROR, HREADY is high
42	Natural interface	A slave can only accept transfers that are as wide as its natural interface	6.2.1	A		If transfer is wider HRESP is ERROR
43	HCLK	All inputs are sampled at rising edge of HCLK , All output are sampled after rising edge of HCLK	7.1.1	A		HRESP is OKAY
44	HRESETn case-1	It should be asserted asynchronously and deserialized synchronously after rising edge of HCLK	7.1.2	A		HRESP is OKAY
45	HRESETn case-4	During reset all slave must ensure HREADYOUT is HIGH	7.1.2	A		HRESP is OKAY, HTRANS[1:0] is IDLE and HREADYOUT is high

Explanation of Different Fields

No.	The serial number of the test.
Feature	The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level of a user.
Ref.	Reference to the section in the related standard document. The section number as well as page numbers should be described here.
Type	Type of the test. Whether the test is an assertion (A) or a transaction (T) type.
Result	Pass (P) or Fail (F).
Comments	Any other comments about the test or its results that you want to mention.