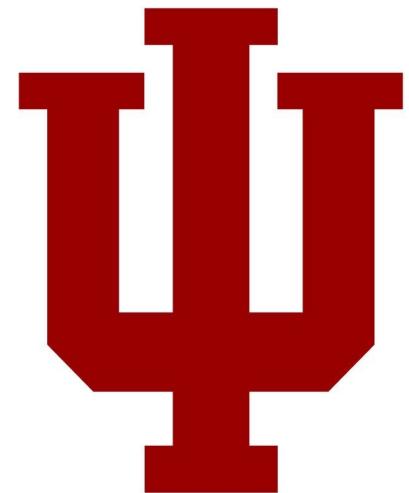


00: Background

E599– Digital Integrated Circuit Design



Website

<https://enr599-ic.github.io>

Let's make a Digital IC. What steps are needed?

Libraries

RTL

Synth

Place & Route

Physical Verification

Timing

Logical Verification

Fill

Software

VLSI (EDA)
CAD

Licensing

\$1

Legal

Manufacturing Run
Reservation

Let's make a Digital IC. What steps are needed?

- Design
 - Blocks / Interfaces
 - IP Block Integration
 - RTL Development
 - Synthesis
 - Place and Route
 - Design-for-Test
 - Logistical Verification
 - Physical Verification
 - Timing Verification
 - Die Seal / Fill
 - Design for Manufacturing
- Legal
 - NDAs
 - License Agreements
- Software:
 - EDA Tools
 - PDK
- Manufacture
 - MPW / Full-Mask
 - Packaging
- Test
 - Power Supplies / Oscilloscopes
 - Testers / JTAG / FPGAs
 - Test/Development boards

And how much does all this cost?



“estimated that ----- spent about \$10 billion in research and development costs.” to develop their latest chip
[\[Link\]](#)

This is a lot of work. Why are we doing this?

- Sell a capability nobody else has

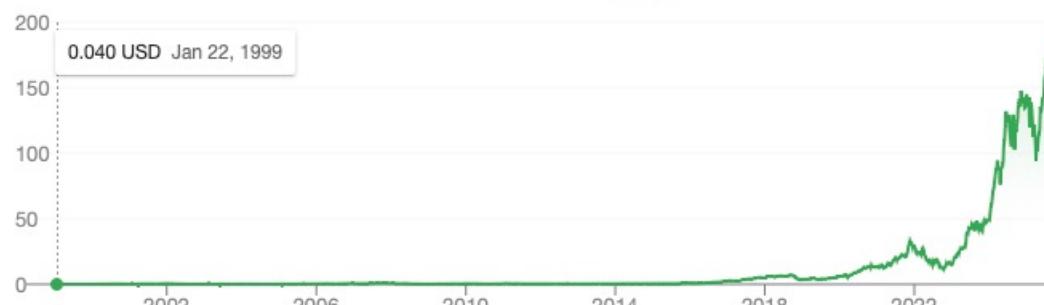
Market Summary > NVIDIA Corp

174.89 USD

+174.85 (437,125.00%) ↑ all time

Aug 21, 12:17 PM EDT • Disclaimer

1D | 5D | 1M | 6M | YTD | 1Y | 5Y | Max



Open	174.85	Mkt cap	4.28T	52-wk high	184.48
High	176.90	P/E ratio	56.32	52-wk low	86.63
Low	173.98	Div yield	0.023%	Qtrly Div Amt	0.010

What happens if you get it wrong?

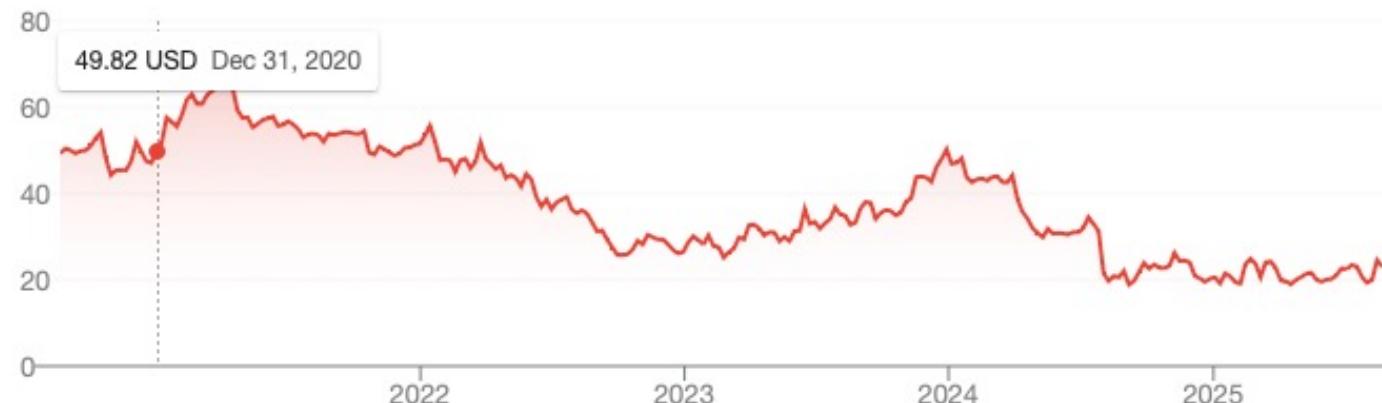
Market Summary > Intel Corp

23.17 USD

-26.11 (-52.99%) ↓ past 5 years

Aug 21, 12:24 PM EDT • Disclaimer

1D | 5D | 1M | 6M | YTD | 1Y | **5Y** | Max

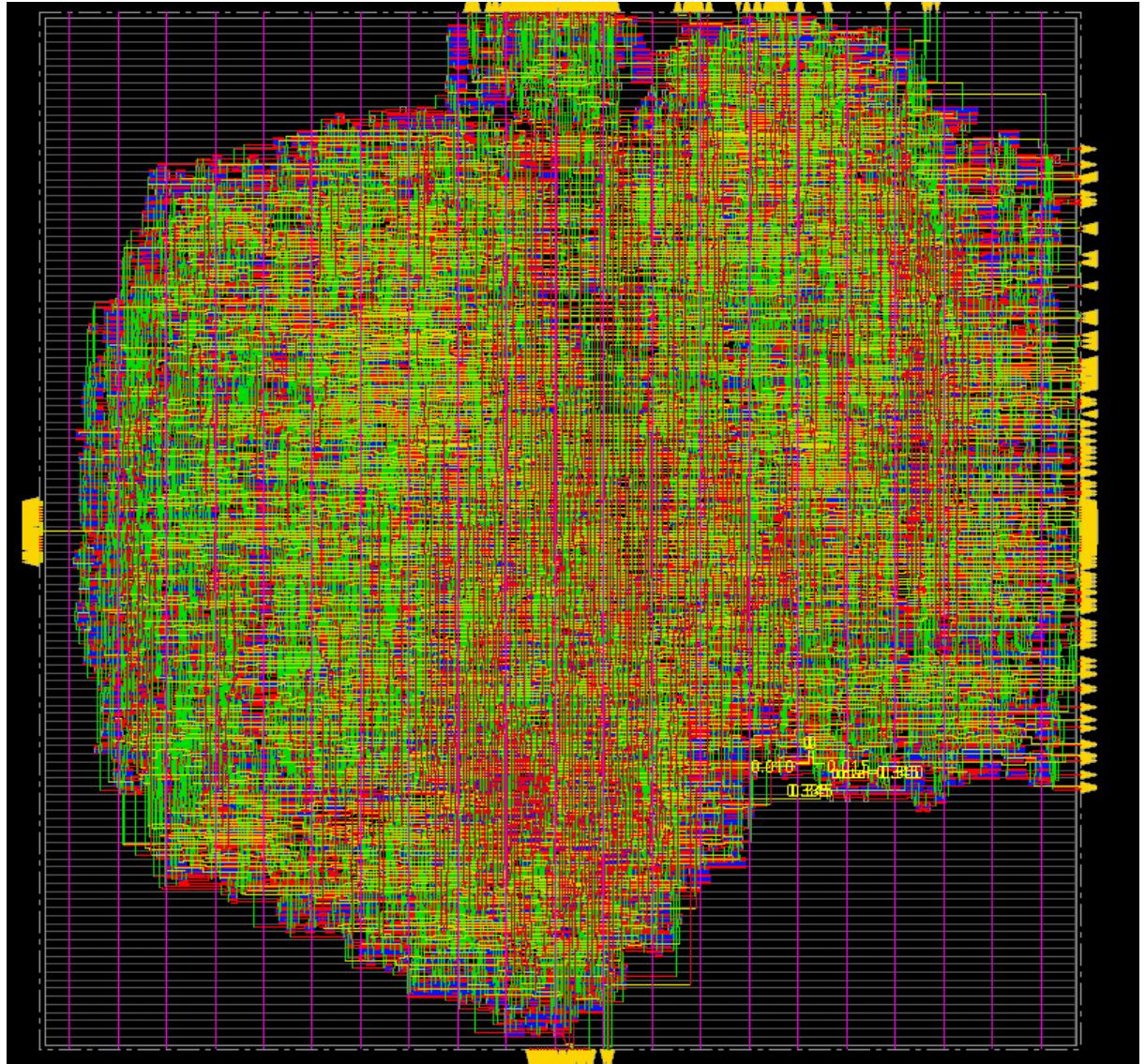


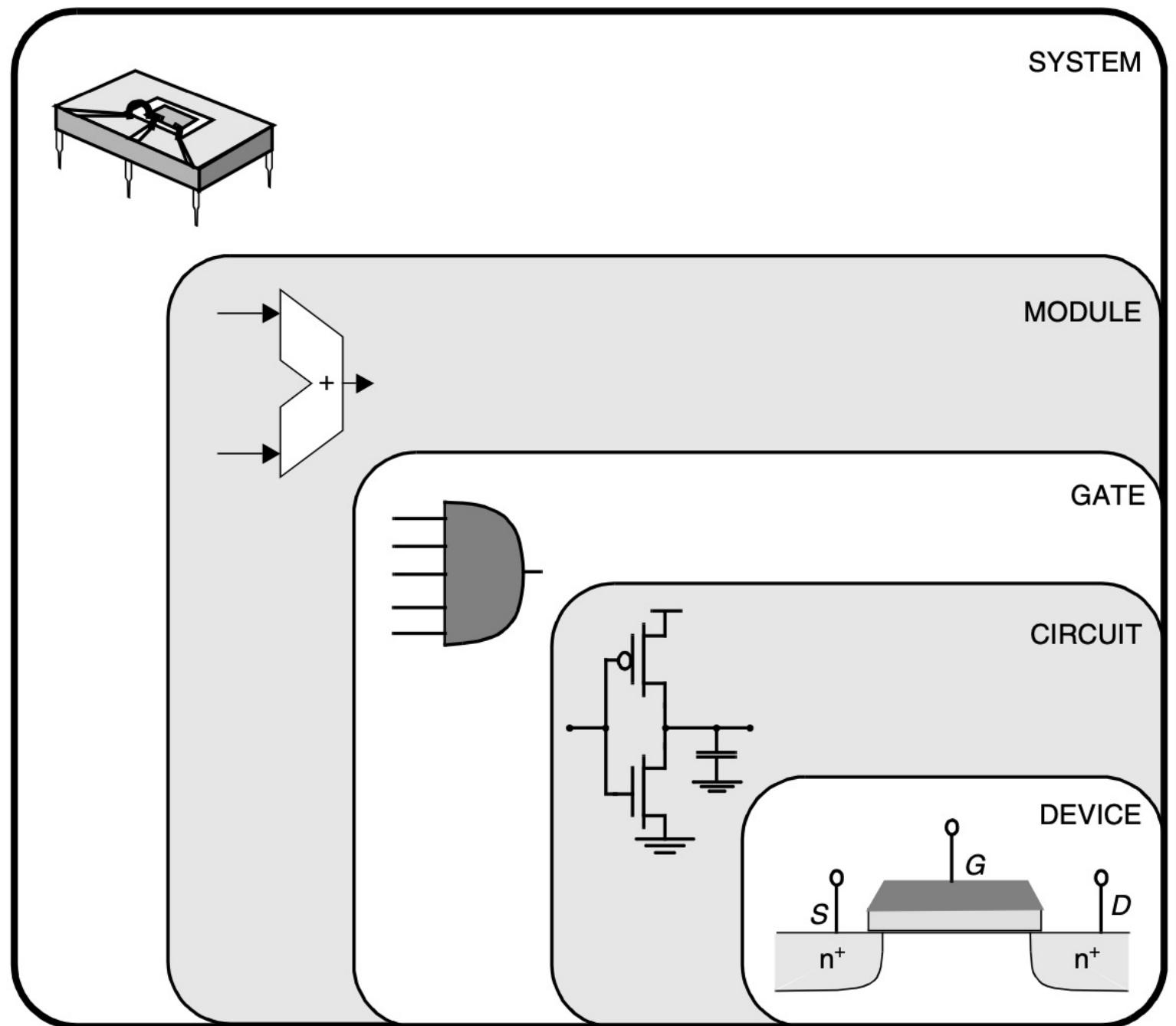
Open	23.52	Mkt cap	101.96B	52-wk high	27.55
High	23.56	P/E ratio	-	52-wk low	17.66
Low	22.78	Div yield	-	Qtrly Div Amt	-

- Can the problem be solved with software?
 - Yes: Use Software
 - No: solution requires hardware
- Can you reuse existing hardware?
 - Yes: Use an FPGA, or DSP, or GPU, etc.
 - No: are you sure you must have custom hardware?
- Are you sure your market is big enough to justify the cost?
 - Yes: Ok, I hope you are right.
 - No: find a better problem to solve

Project 1

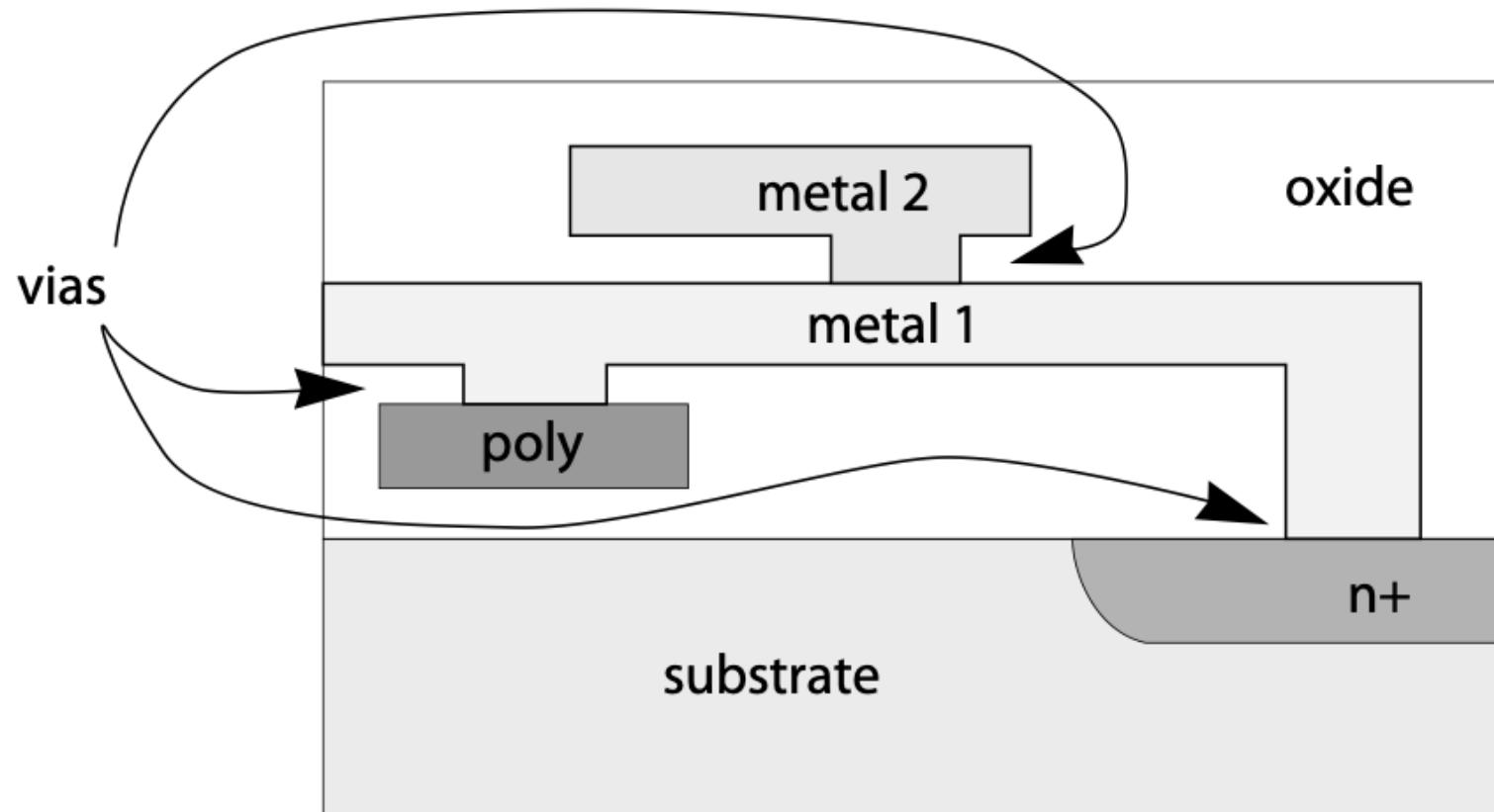
- https://engr599-ic.github.io/P1/run_the_flow.html
- synth



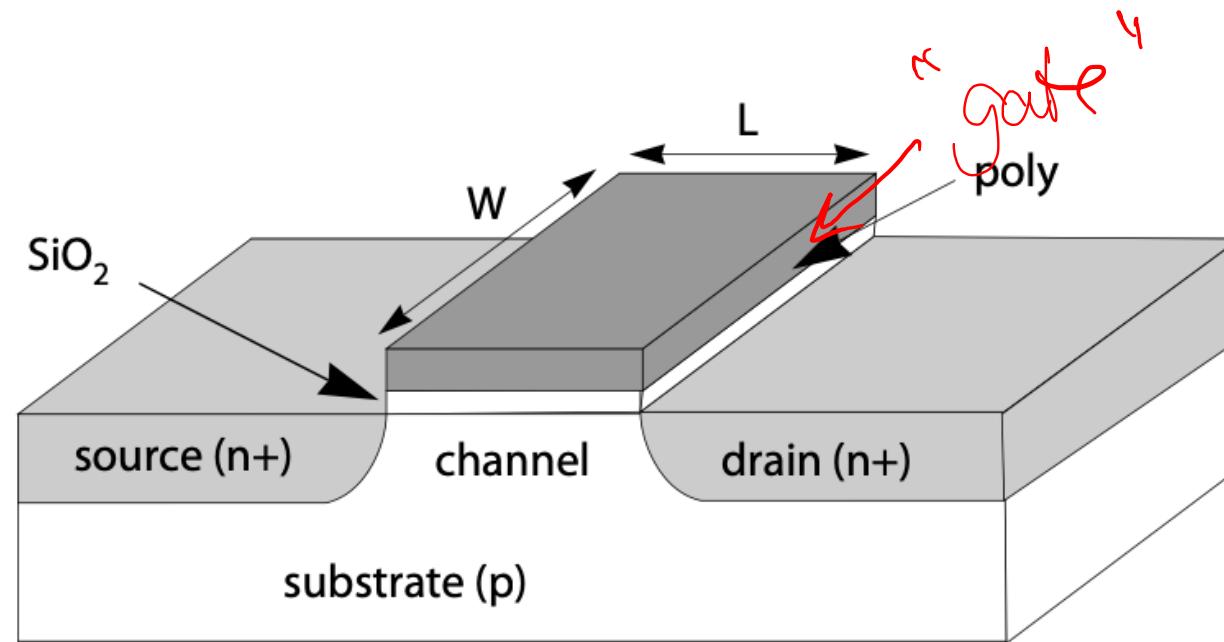


Devices

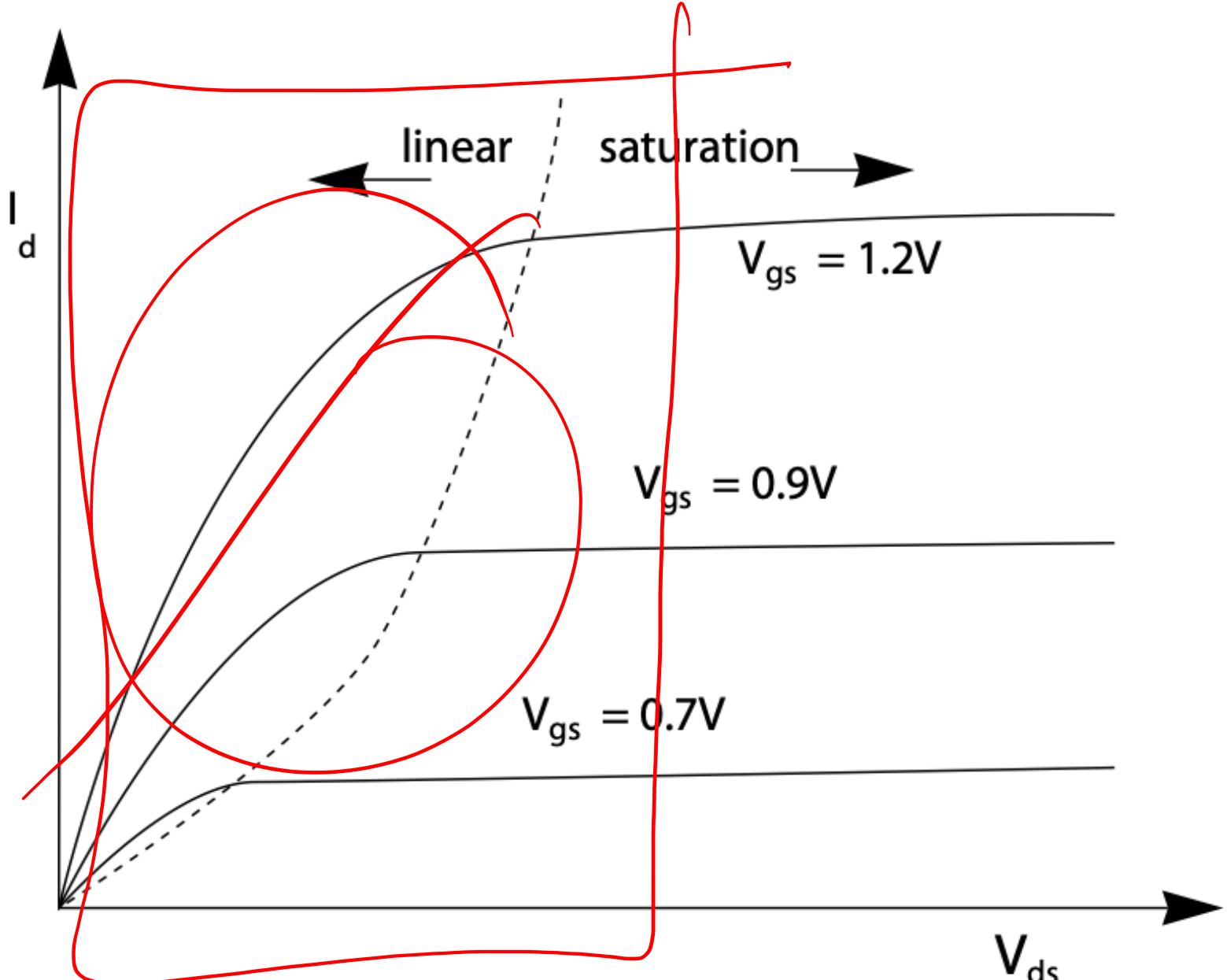
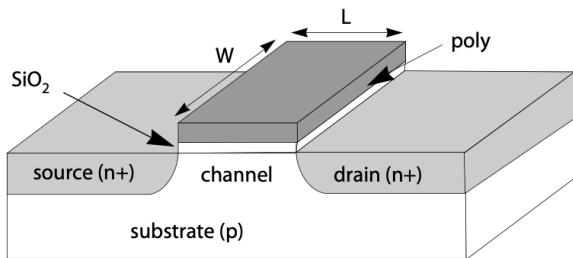
Integrated Circuits are ~2 things. Transistors and Wires.



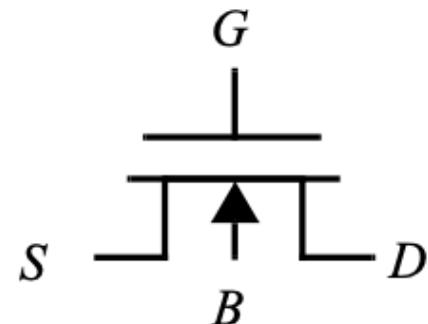
Transistors



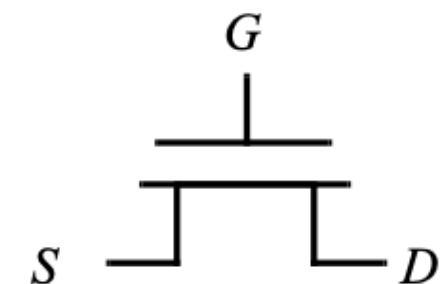
Transistors



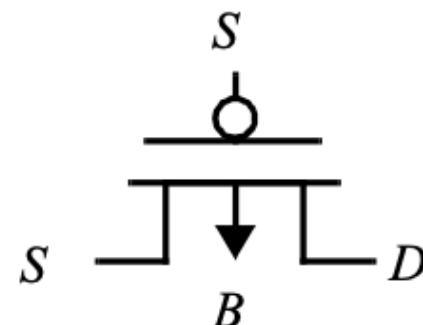
2 main types of transistors: NMOS and PMOS



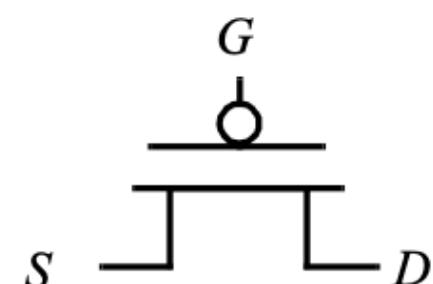
(a) NMOS transistor
as 4-terminal device



(b) NMOS transistor
as 3-terminal device



(c) PMOS transistor
as 4-terminal device



(d) PMOS transistor
as 3-terminal device

NMOS vs. PMOS

NMOS vs. PMOS

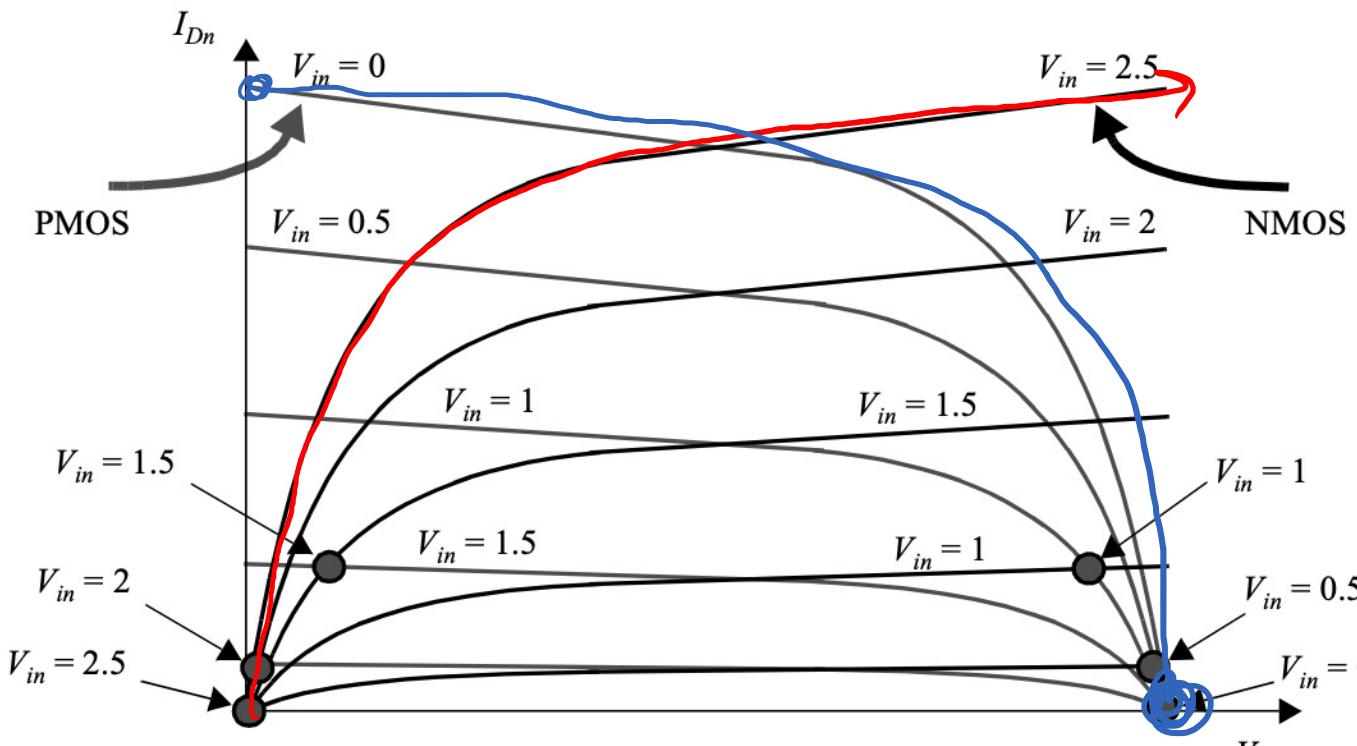
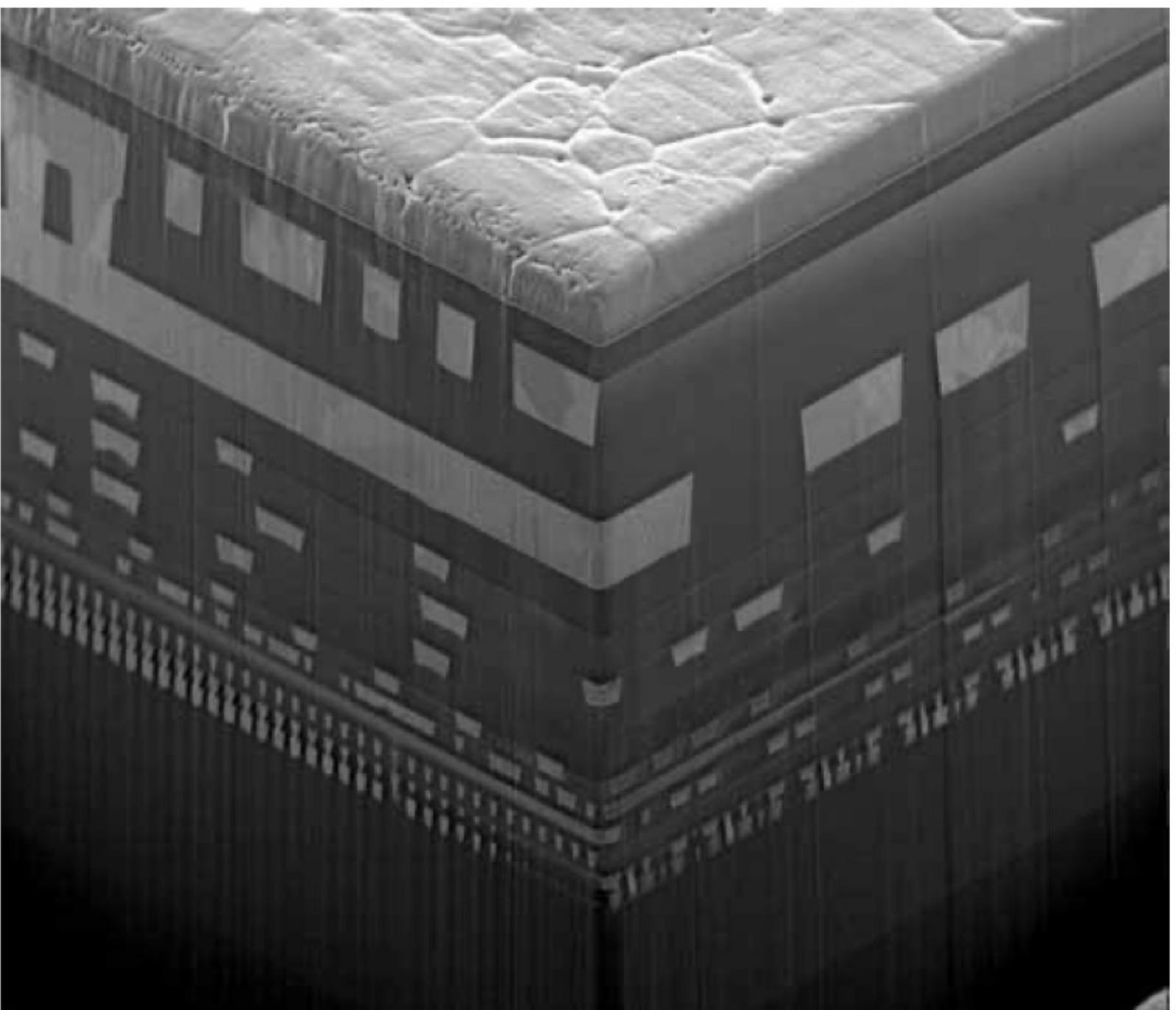
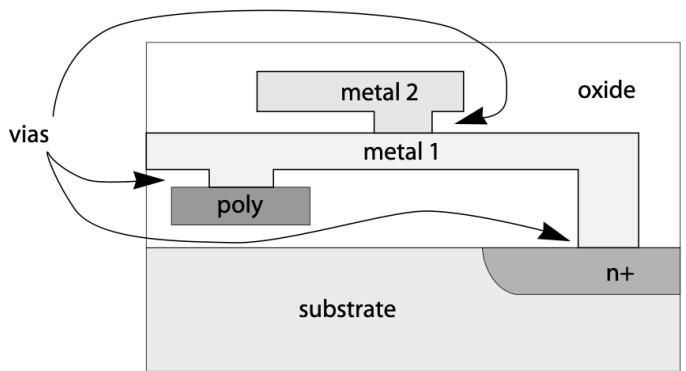
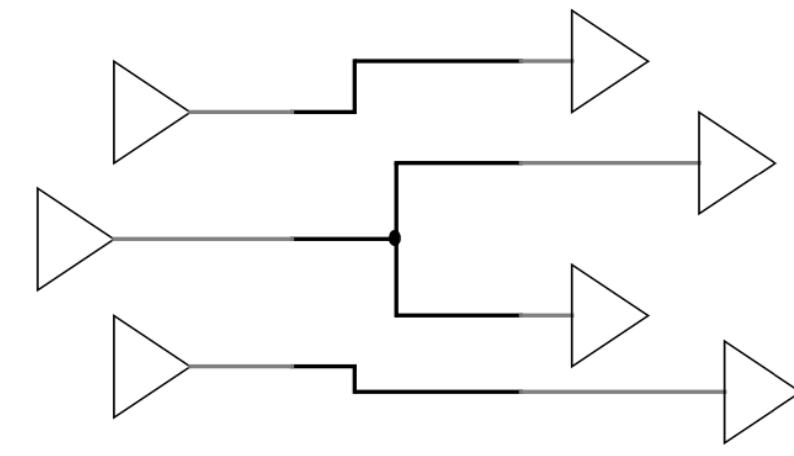


Figure 5.4 Load curves for NMOS and PMOS transistors of the static CMOS inverter ($V_{DD} = 2.5$ V). The dots represent the dc operation points for various input voltages.

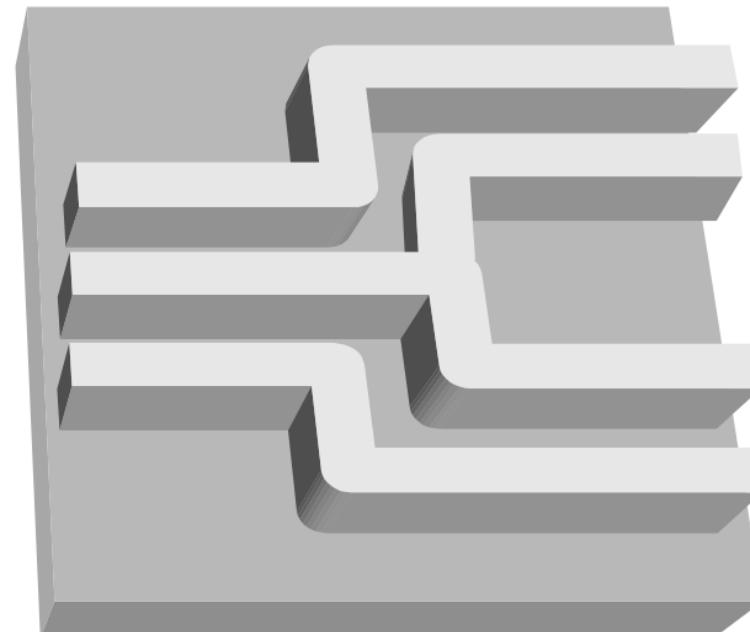
Wires



Wires

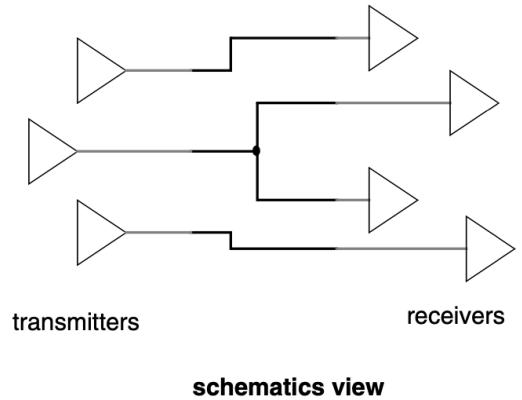
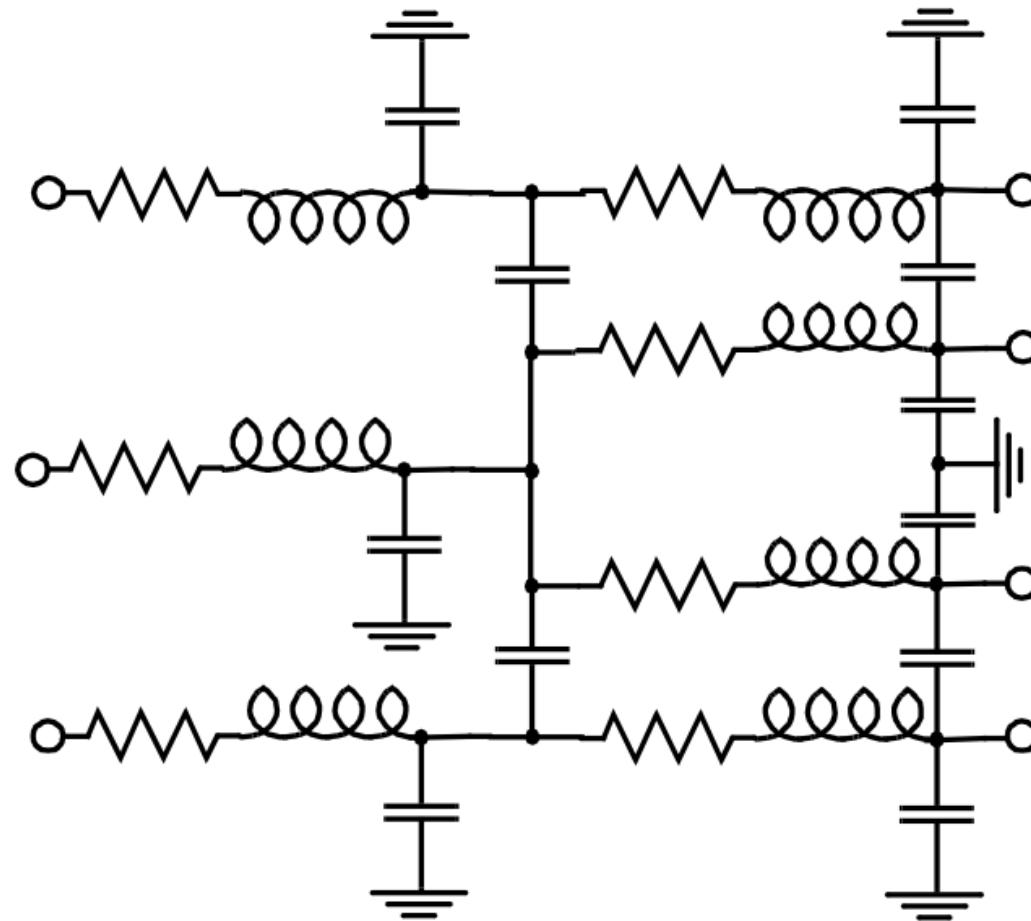


schematics view

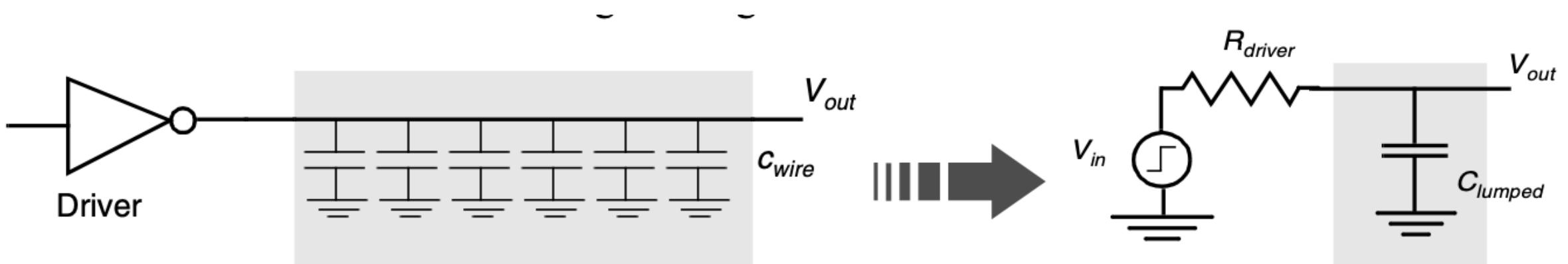


physical view

Wires



Wires



Wires

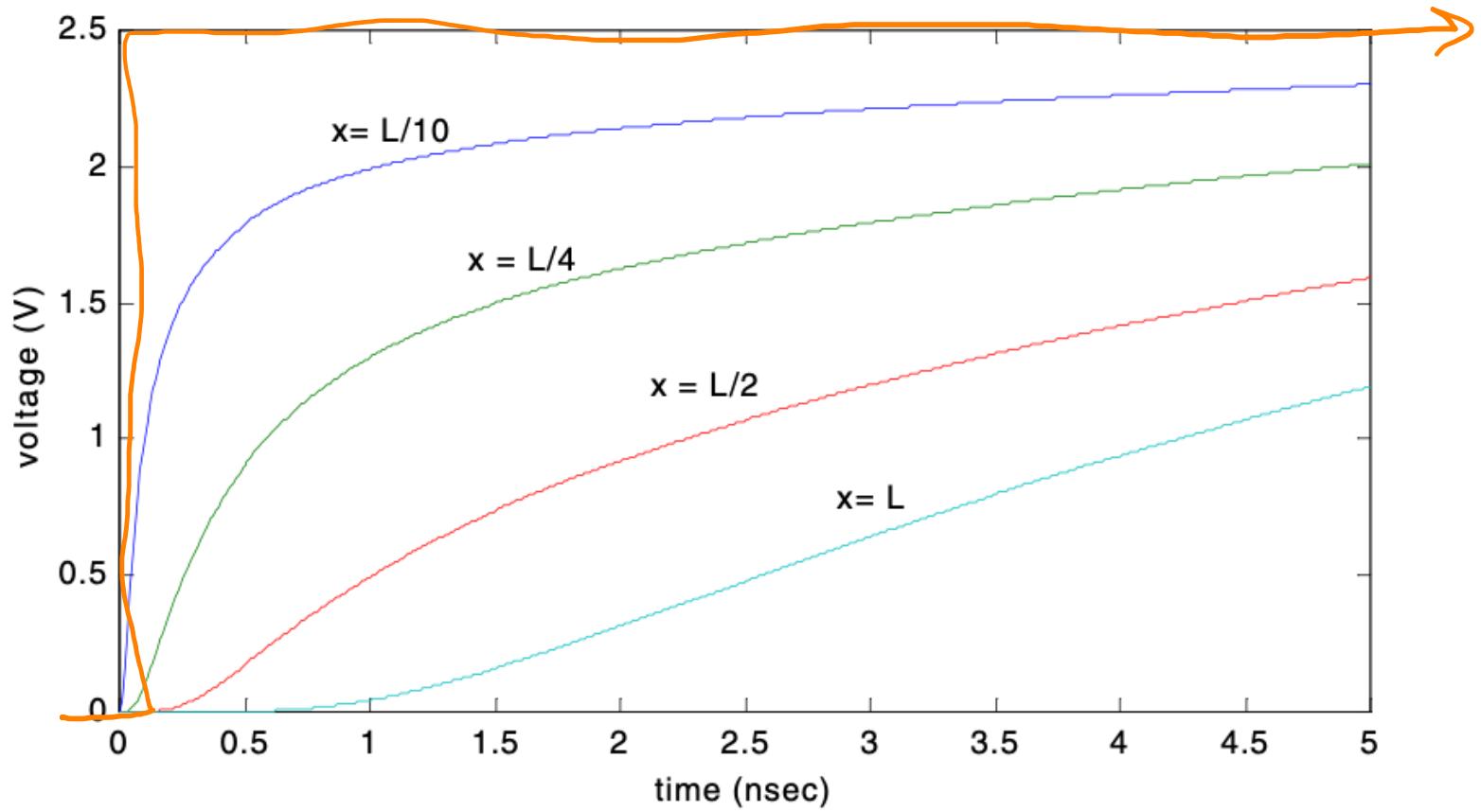


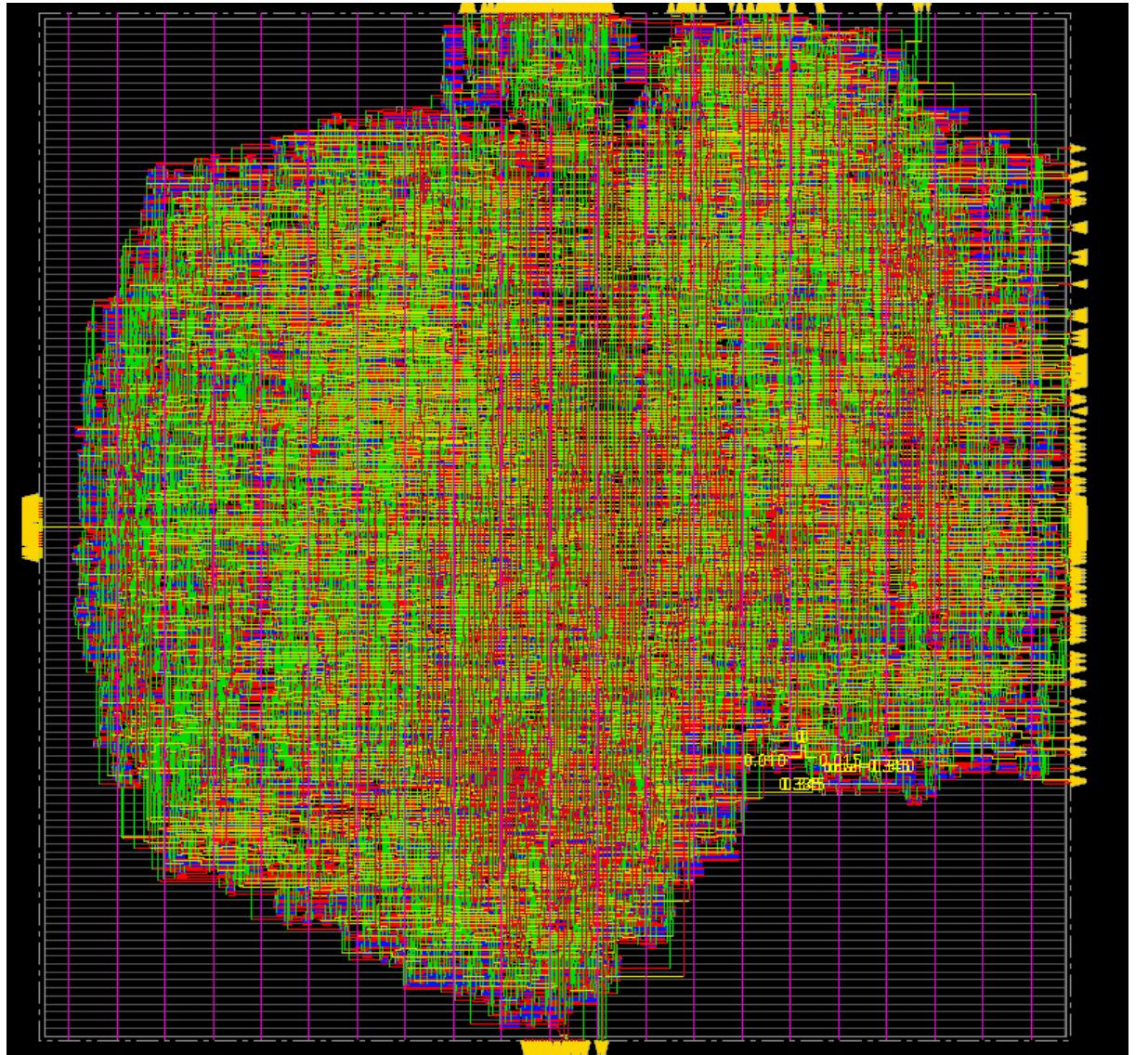
Figure 4.15 shows the response of a wire to a step input, plotting the waveforms at different points in the wire as a function of time. Observe how the step waveform “dif-fuses” from the start to the end of the wire, and the waveform rapidly degrades, resulting in a considerable delay for long wires. Driving these rc lines and minimizing the delay and signal degradation is one of the trickiest problems in modern digital integrated circuit design.

Devices Review

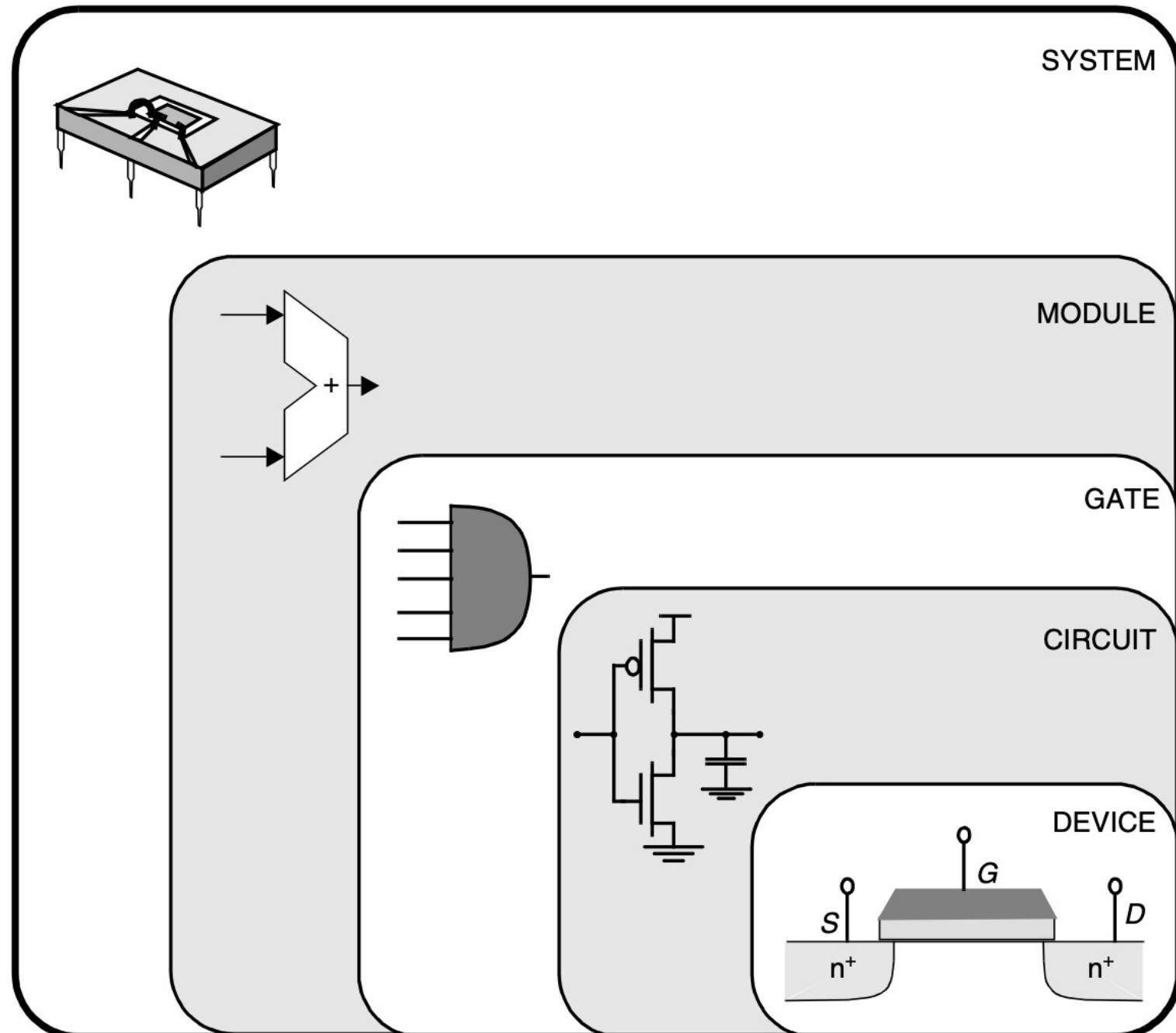
- Transistors
 - Voltage on gate causes conduction between source + drain. Aka “Magic”
 - Only consider fully-off or fully-on (saturated)
 - Two types: NMOS and PMOS
 - PMOS: 0V=on
 - NMOS: 0V =off
- Wires
 - Resistor + Capacitor
 - Longer wires = slower signals

Project 1

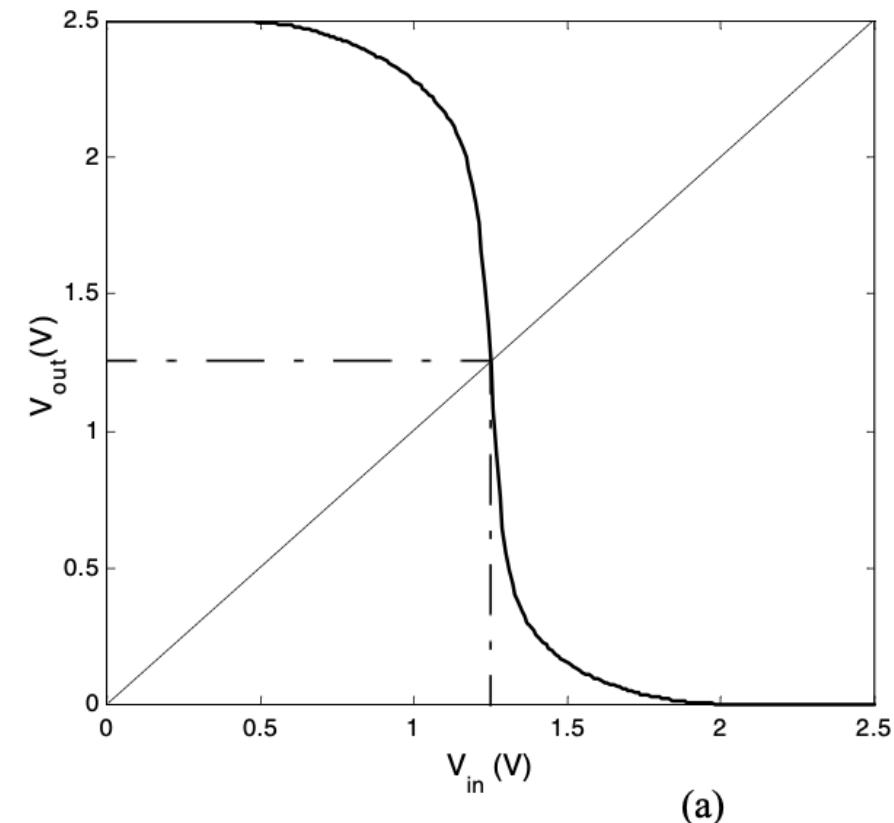
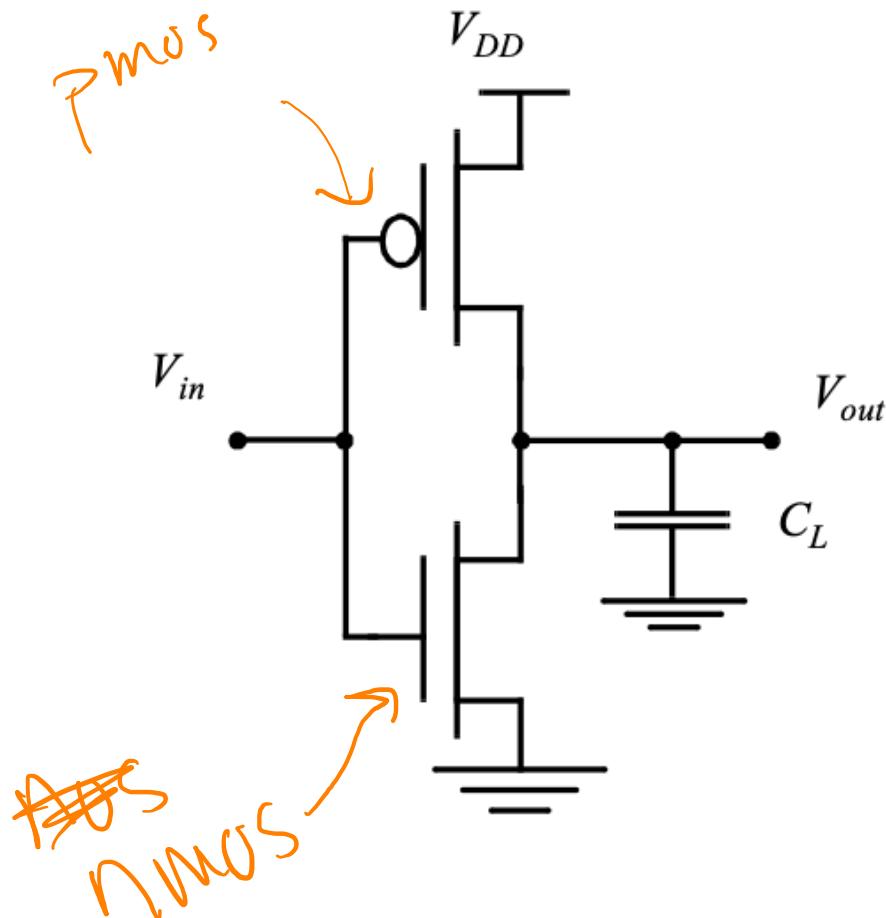
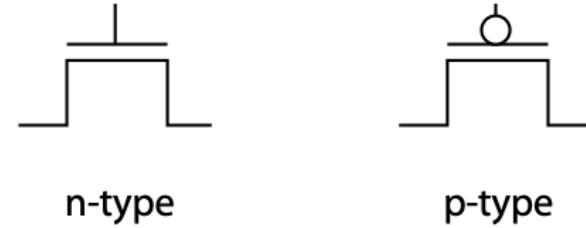
- Pnr



Combinational Circuits

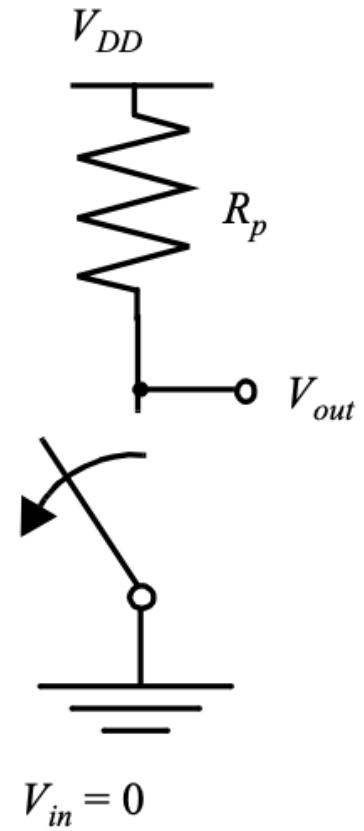
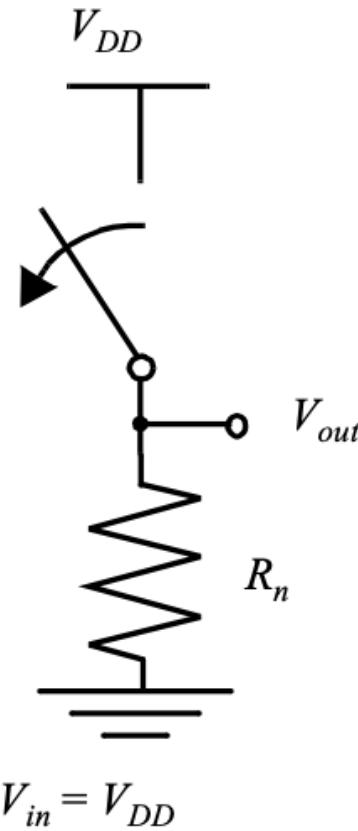
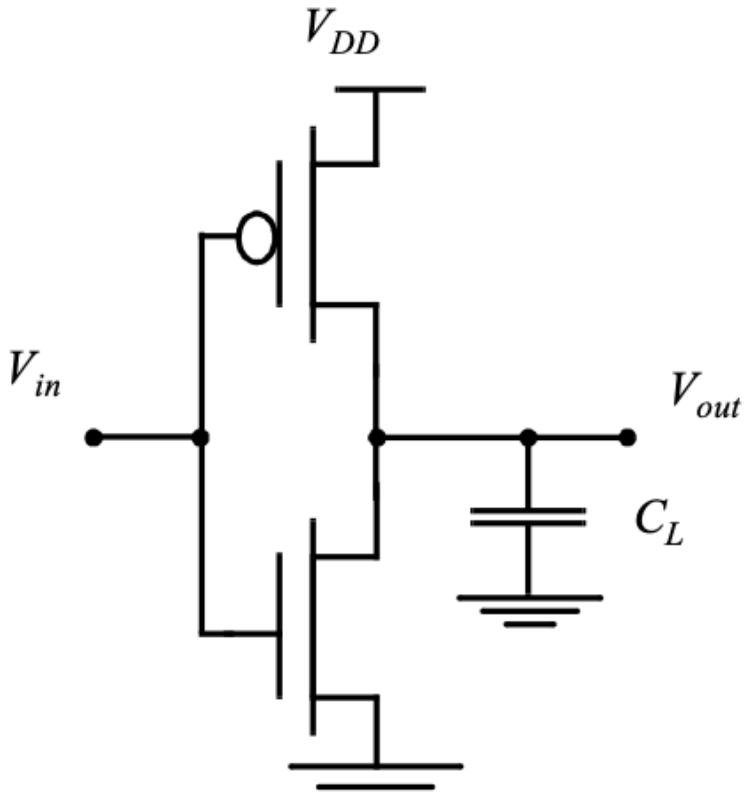
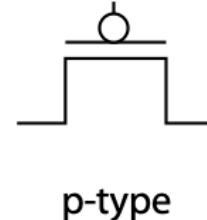
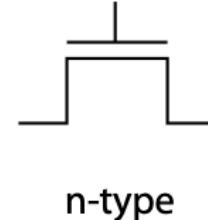


The CMOS Inverter



The CMOS Inverter

PMOS: 0V=on
NMOS: 0V =off



The CMOS Inverter

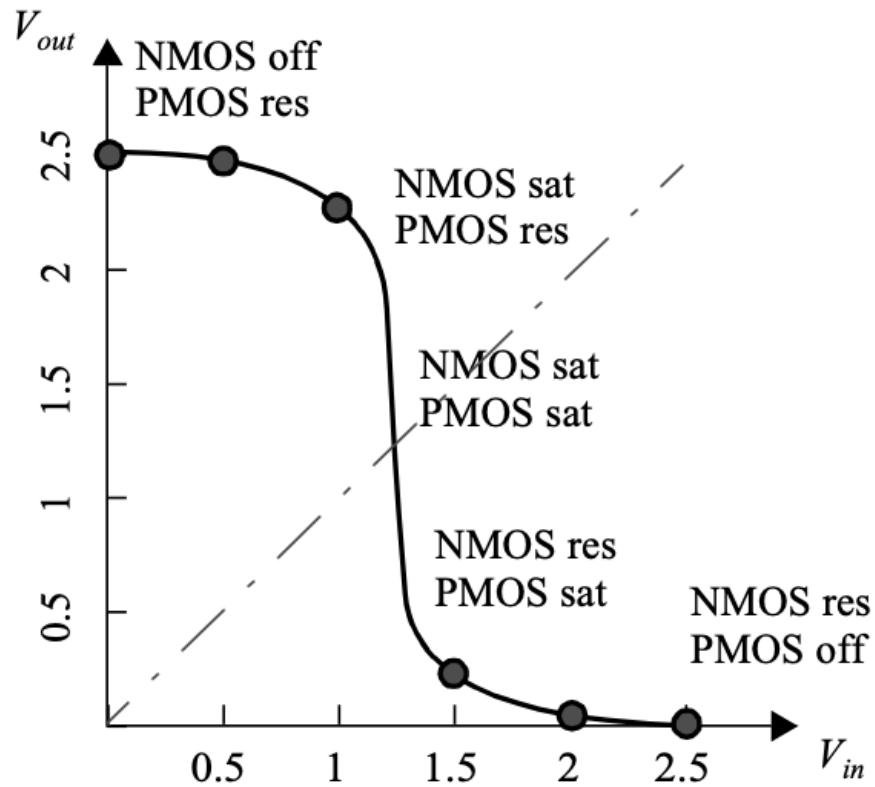
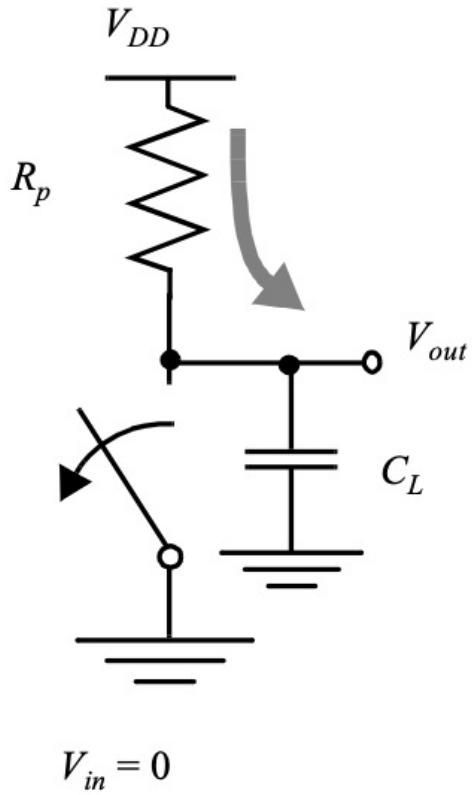
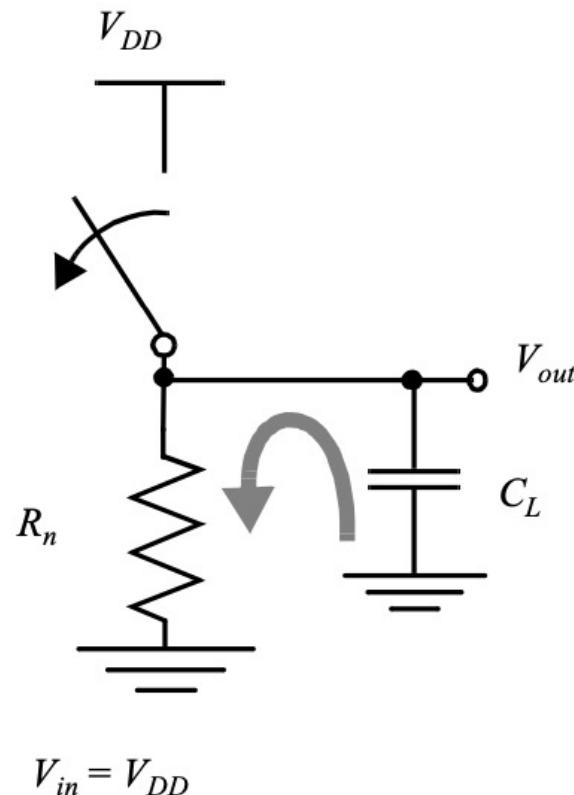


Figure 5.5 VTC of static CMOS inverter, derived from Figure 5.4 ($V_{DD} = 2.5$ V). For each operation region, the modes of the transistors are annotated — off, res(istive), or sat(urated).

The CMOS Inverter



(a) Low-to-high

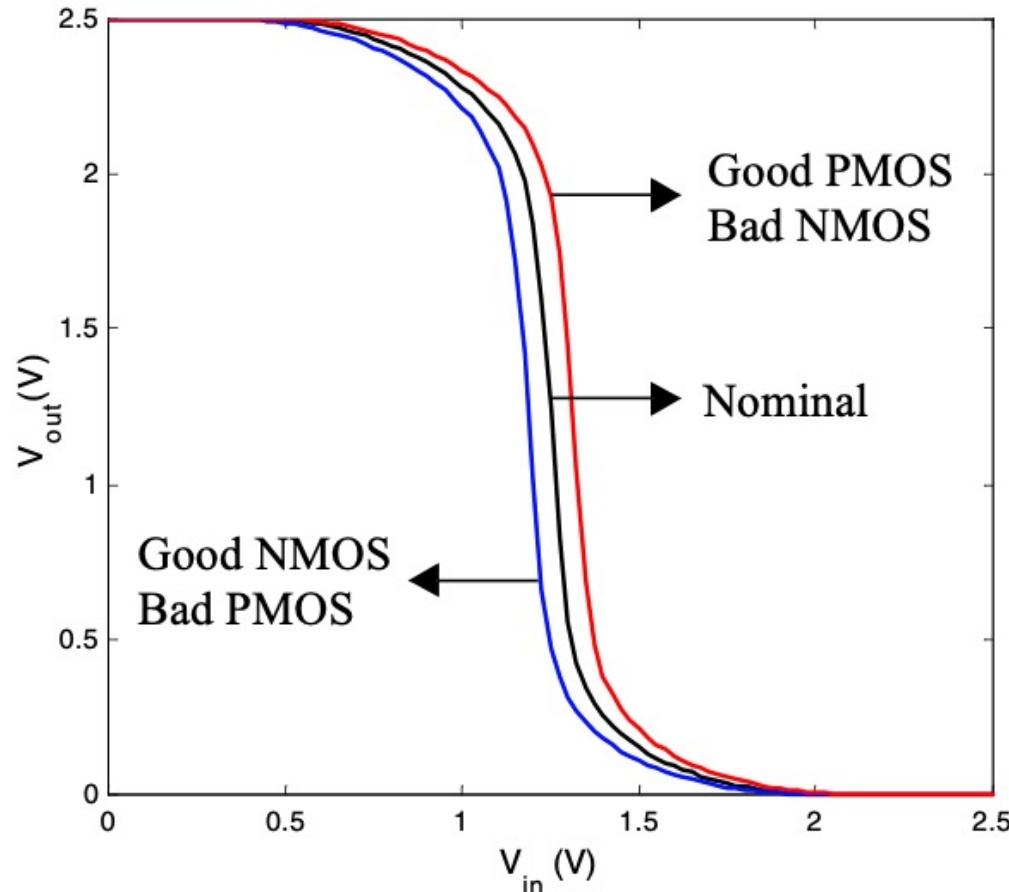


(b) High-to-low

Figure 5.6 Switch model of dynamic behavior of static CMOS inverter.

Process Variation causes all transistors to be slightly different.

Process Variation causes some transistors to be slightly “faster”, some “slower”.

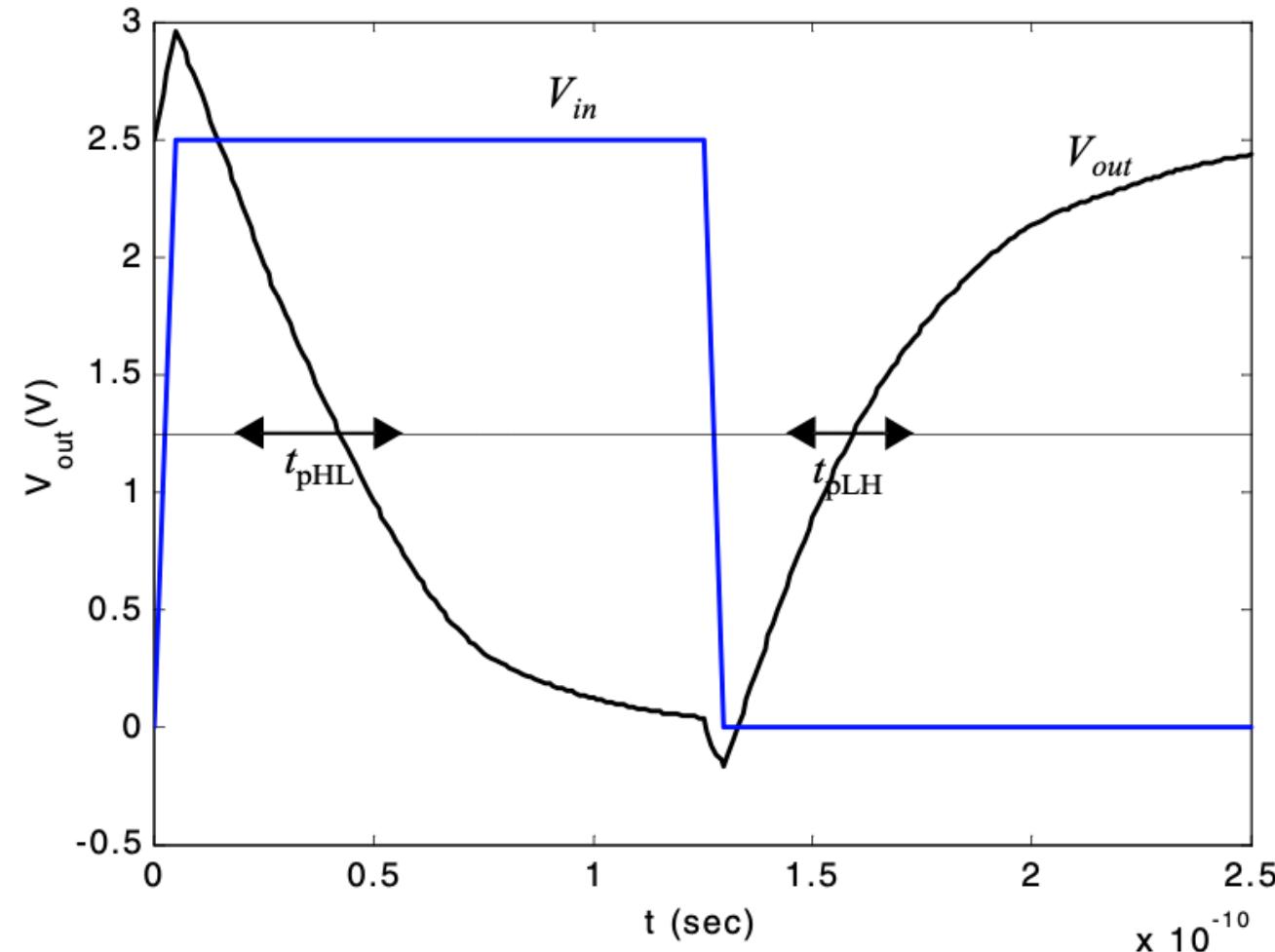


V doesn't go to 0, Leakage?

Figure 5.11 Impact of device variations on static CMOS inverter VTC. The “good” device has a smaller oxide thickness (- 3nm), a smaller length (-25 nm), a higher width (+30 nm), and a smaller threshold (-60 mV). The opposite is true for the “bad” transistor.

Intrinsic Delay measures how long the output takes to reflect changes in input

Intrinsic Delay measures how long the output takes to reflect changes in input



PMOS is usually slower than NMOS, so we end up making the PMOS bigger to better balance them delays.

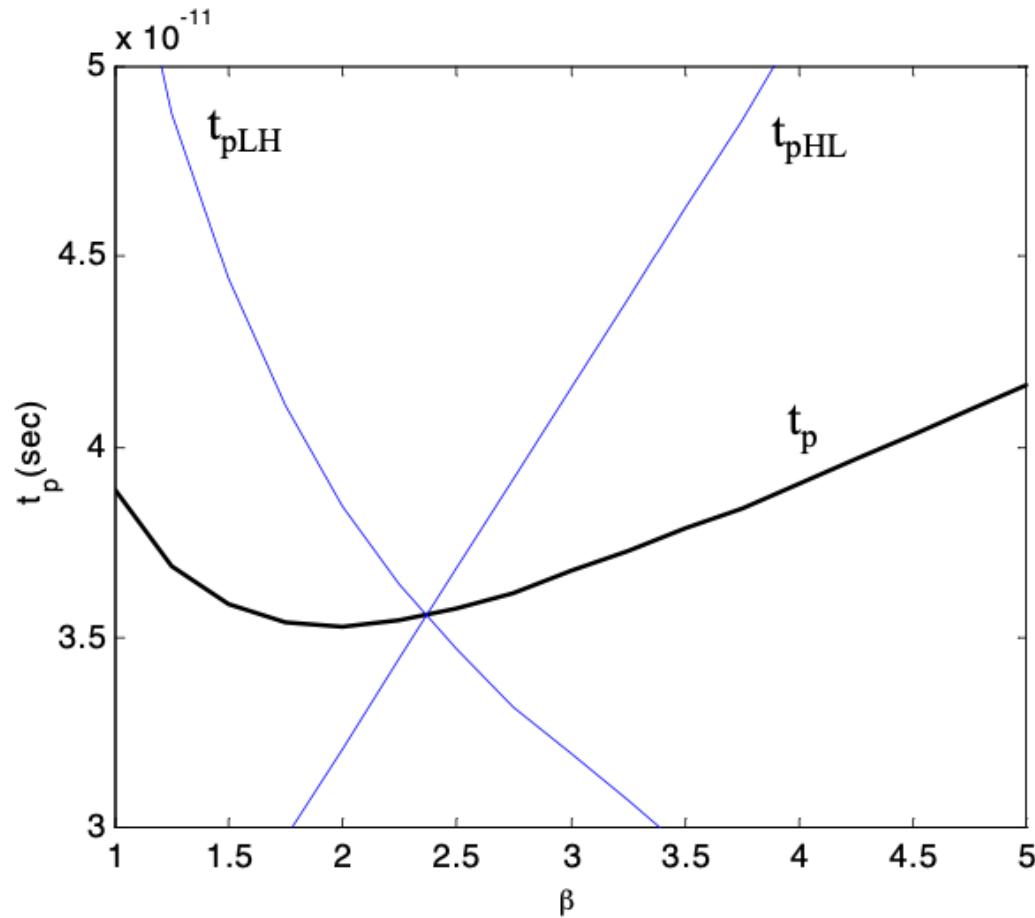


Figure 5.18 Propagation delay of CMOS inverter as a function of the PMOS/NMOS transistor ratio β .

Making bigger transistors decreases delay, to a point

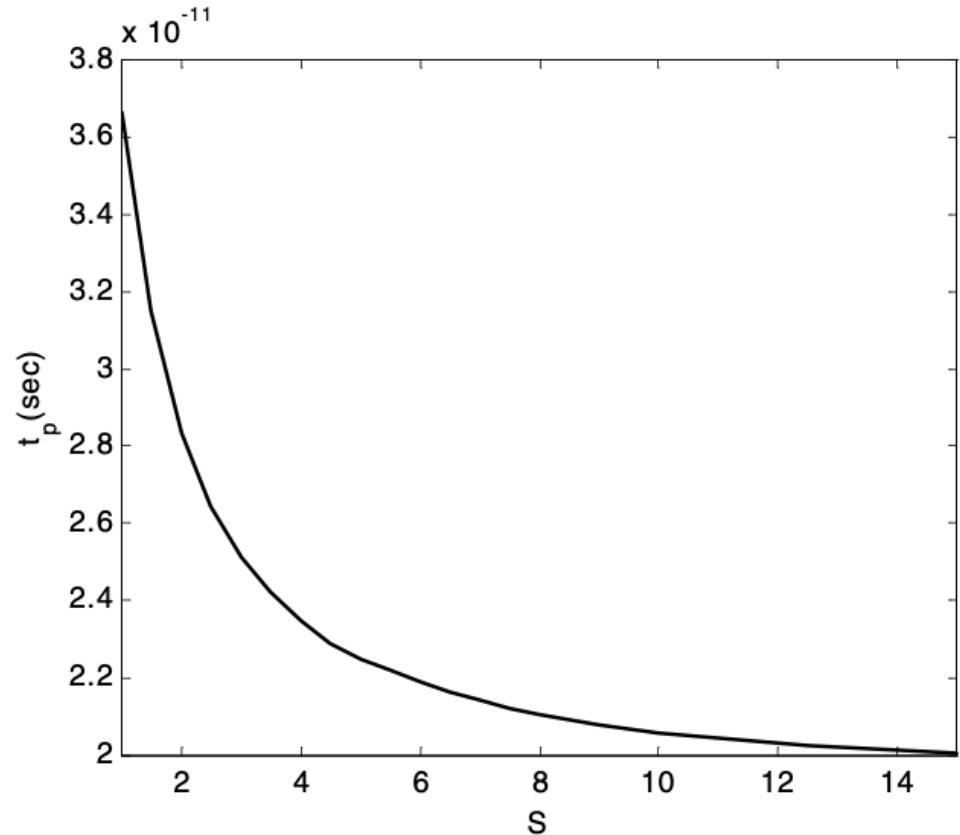
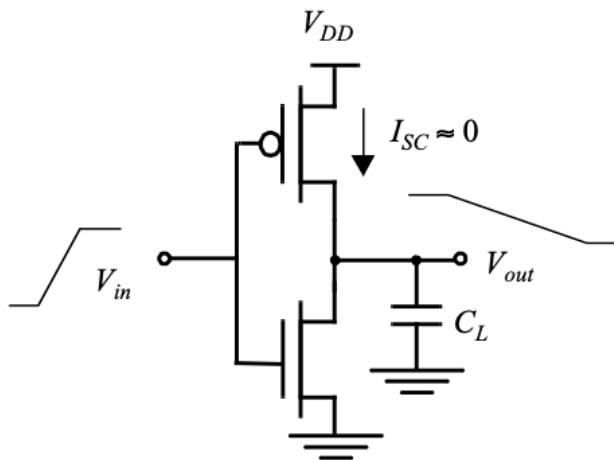
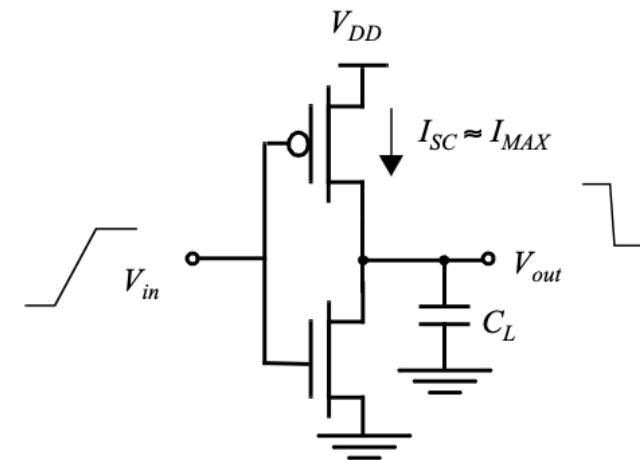


Figure 5.19 Increasing inverter performance by sizing the NMOS and PMOS transistor with an identical factor S for a fixed fanout (inverter of Figure 5.15).

Capacitive load impacts delay and power.

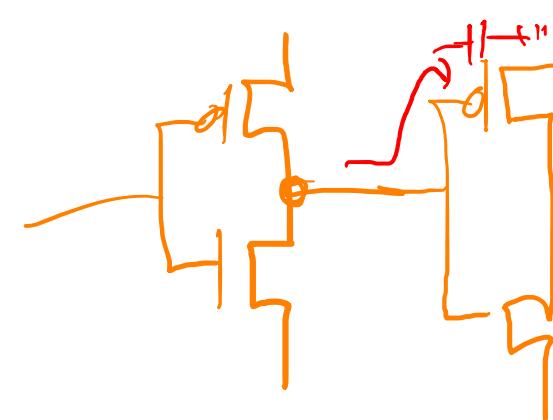
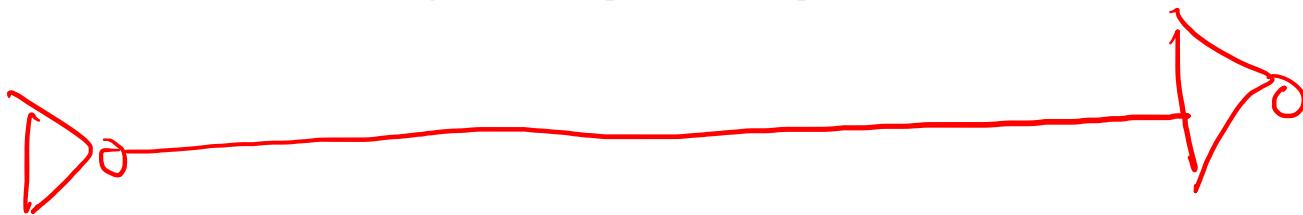


(a) Large capacitive load



(b) Small capacitive load

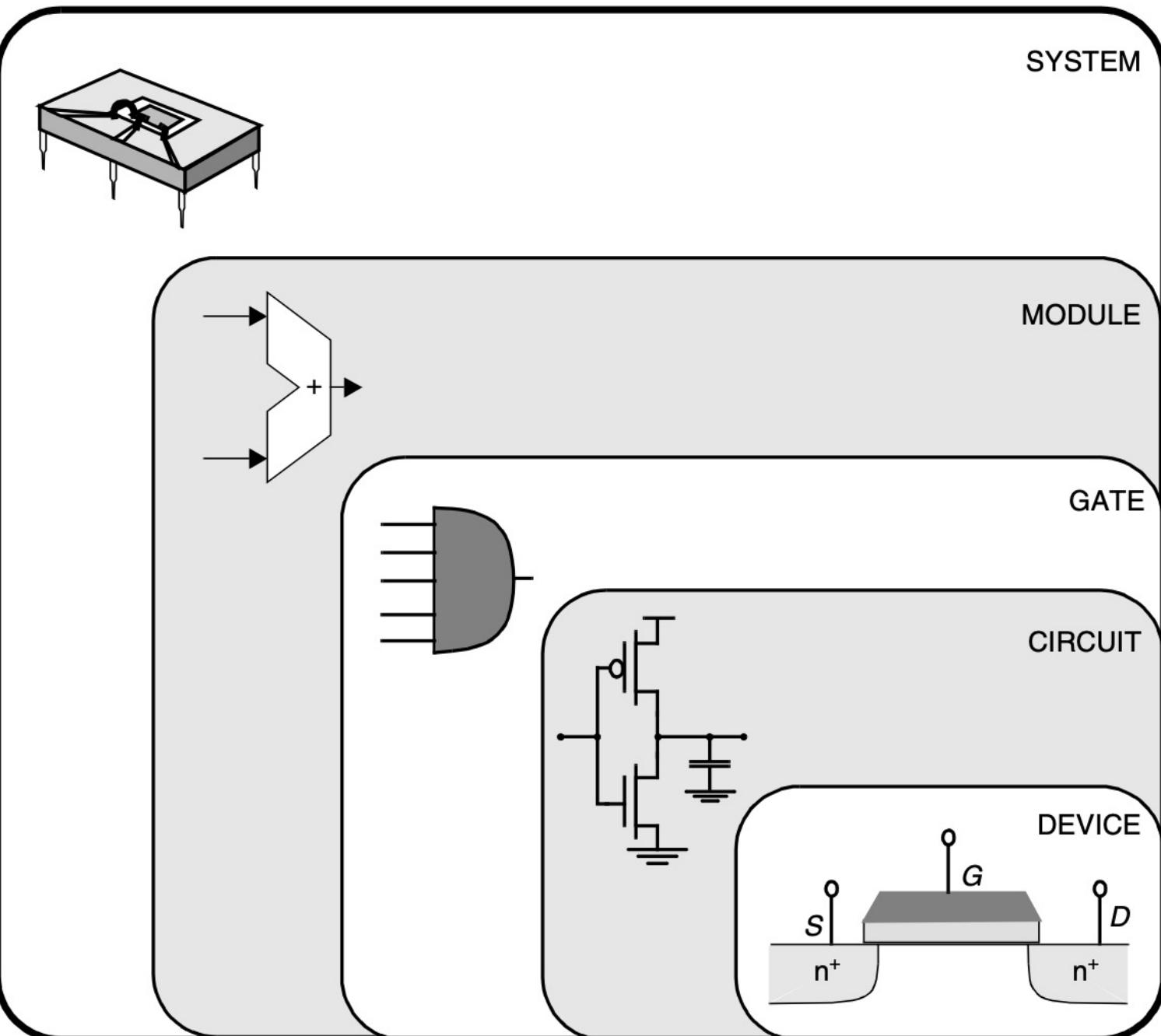
Figure 5.31 Impact of load capacitance on short-circuit current.



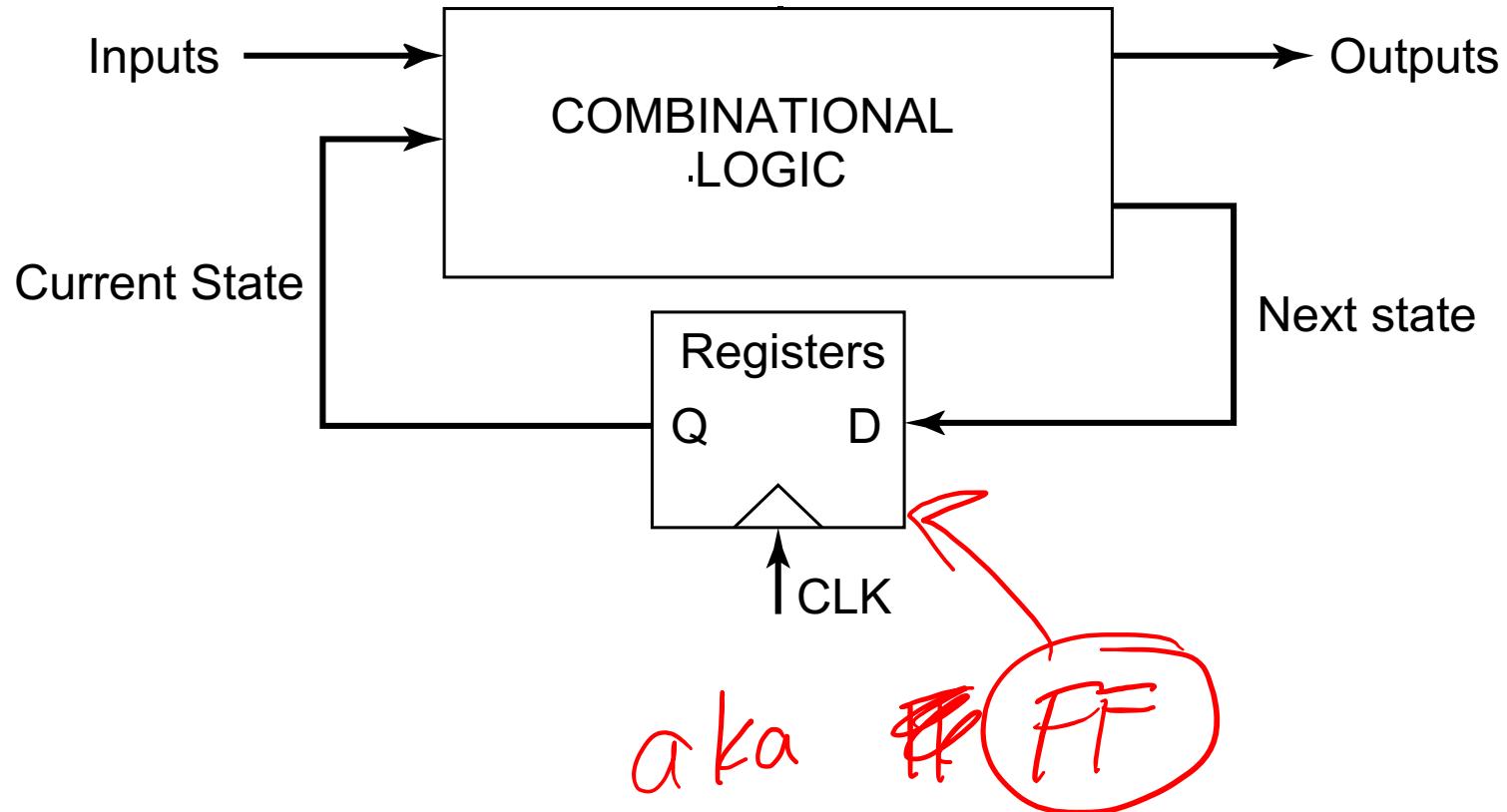
Combinational Circuits Review

- Inverter: 1 NMOS + 1 PMOS
- Process Variation:
 - Some faster, some slower transistors
- Intrinsic Delay:
 - Fundamental delay in all transitions
 - Bigger transistors reduce delays, to a point.
- Other Delays
 - output takes times to reflect input changes
 - Bigger capacitive loads increase delays

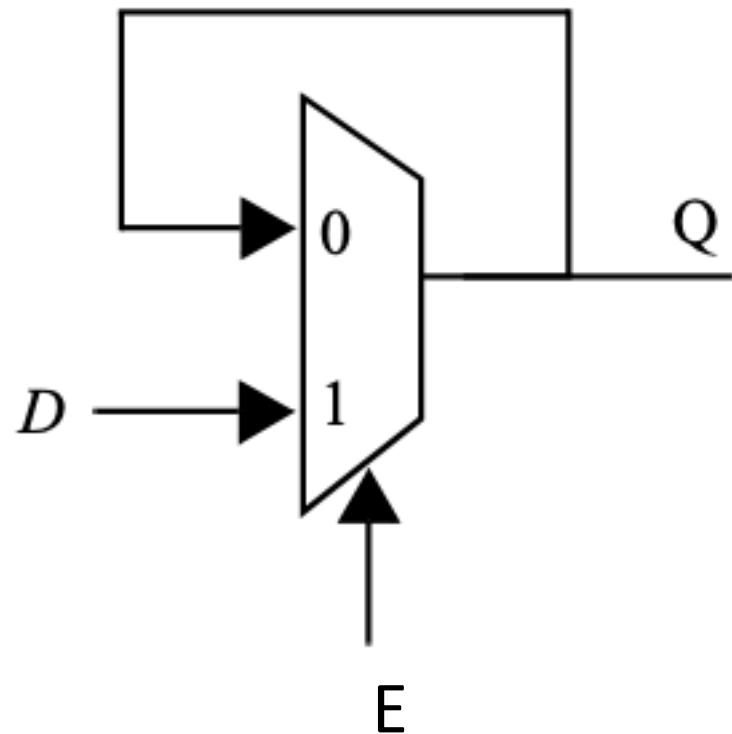
Sequential Circuits



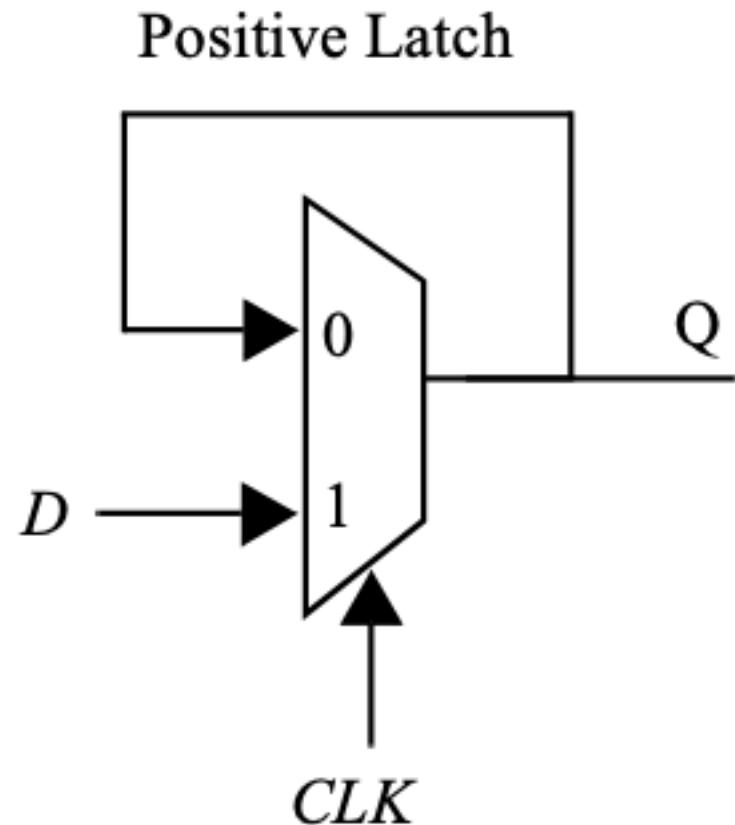
Sequential Logic Circuits



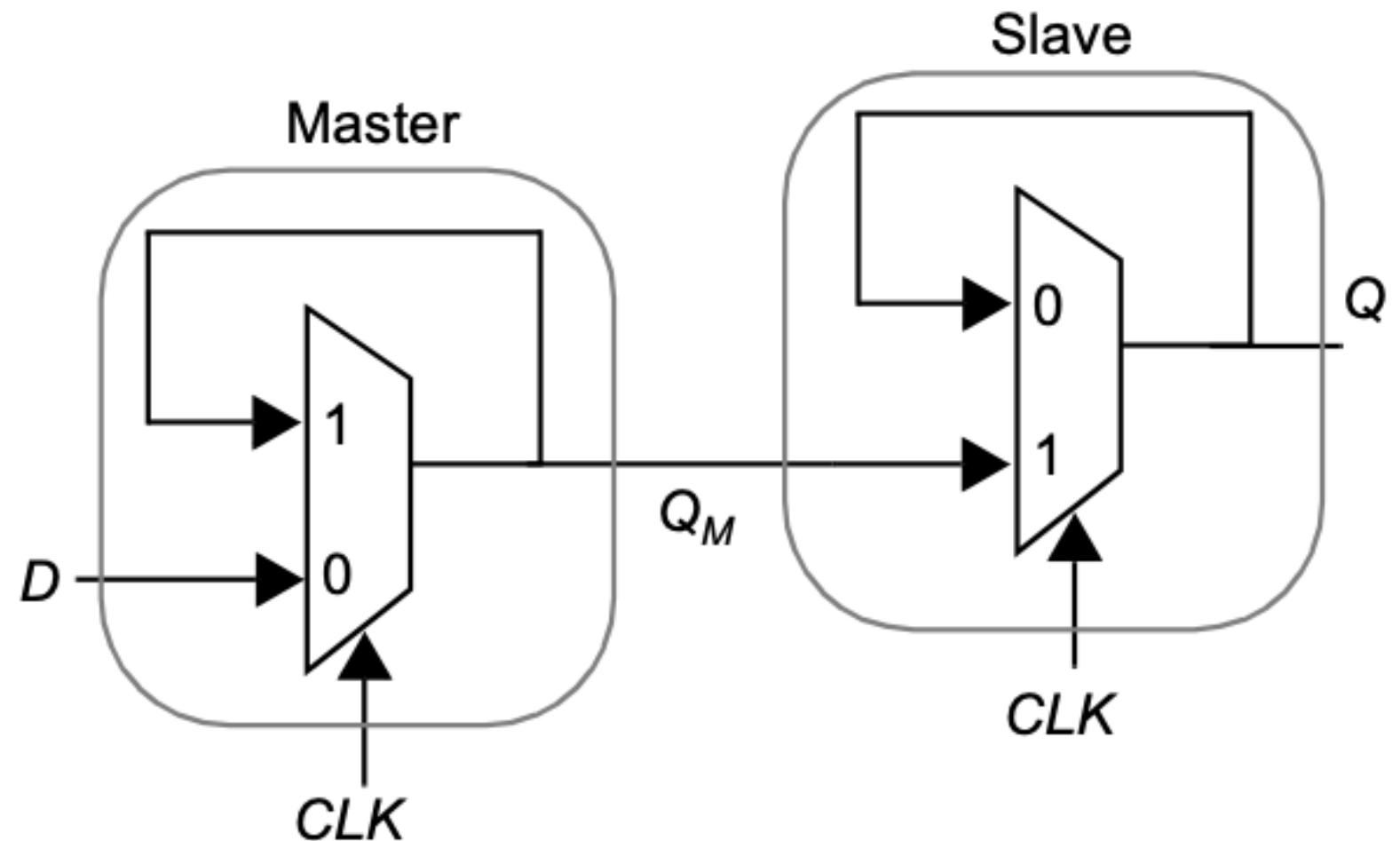
What is this circuit?



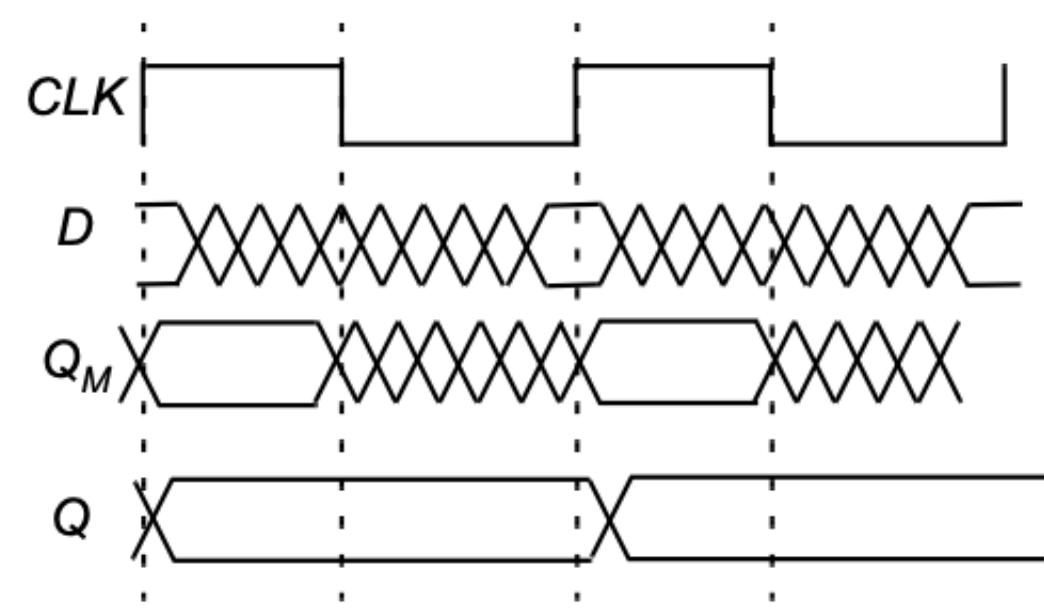
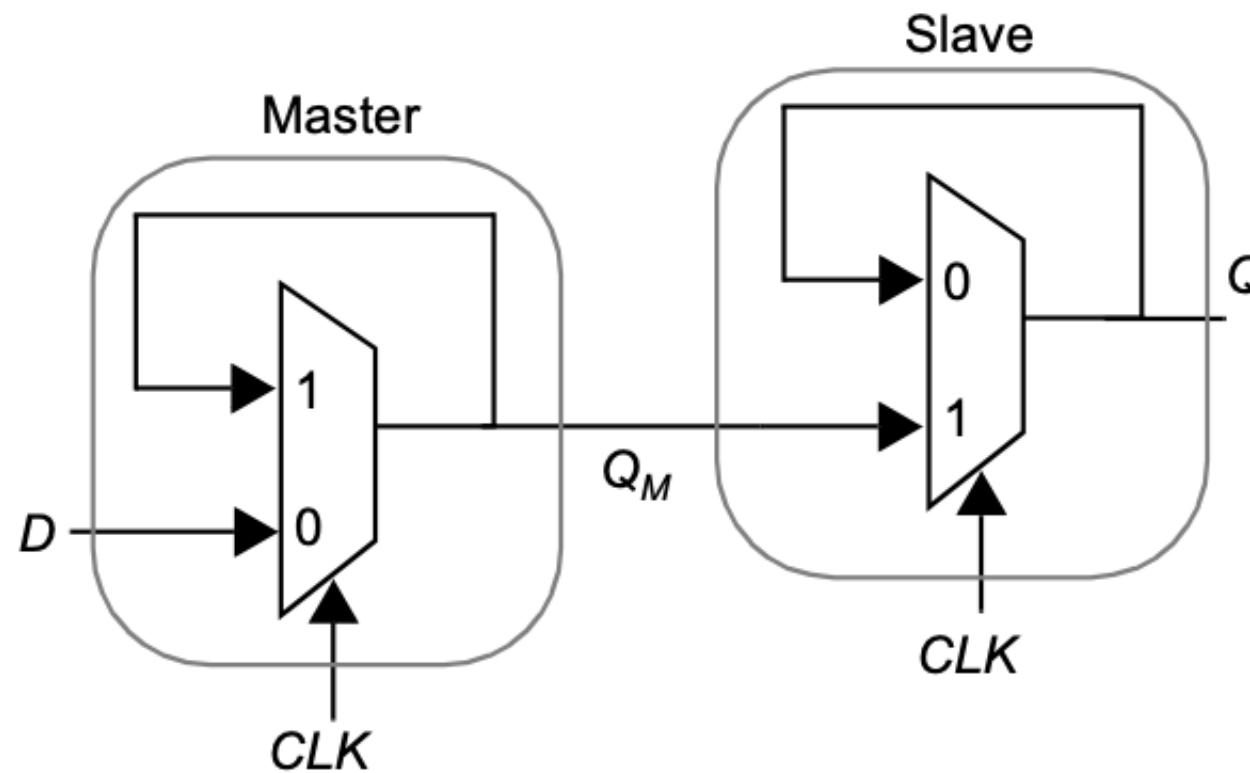
What is this circuit? Latch



What is this circuit?



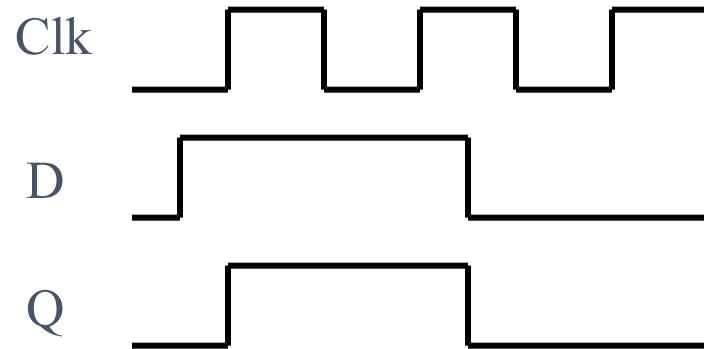
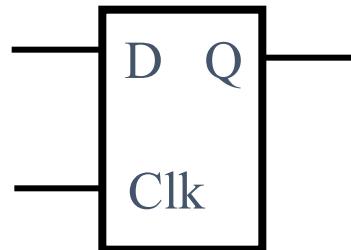
D Flip-Flop (Register)



Latch versus D Flip-Flop/Register

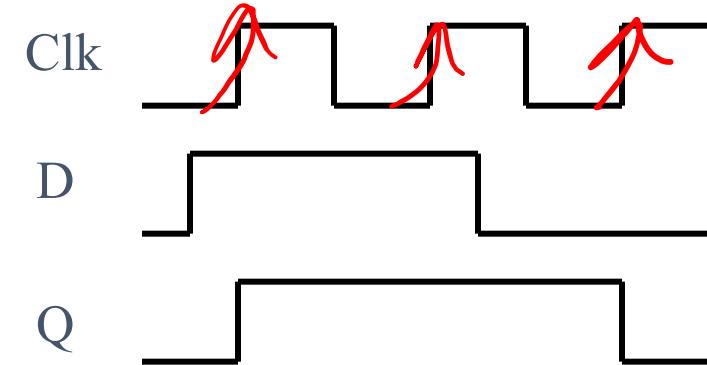
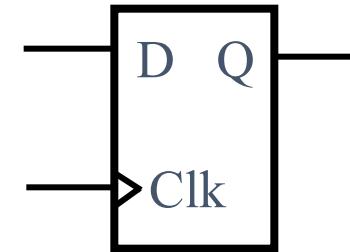
- ❑ Latch

stores data when
clock is ~~low~~ *high*

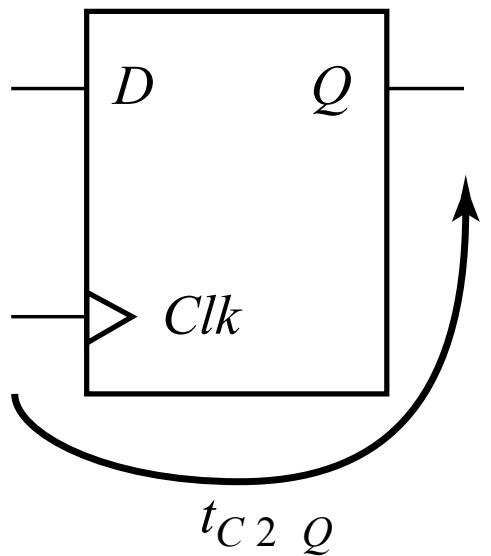


- ❑ Register

stores data when
clock rises

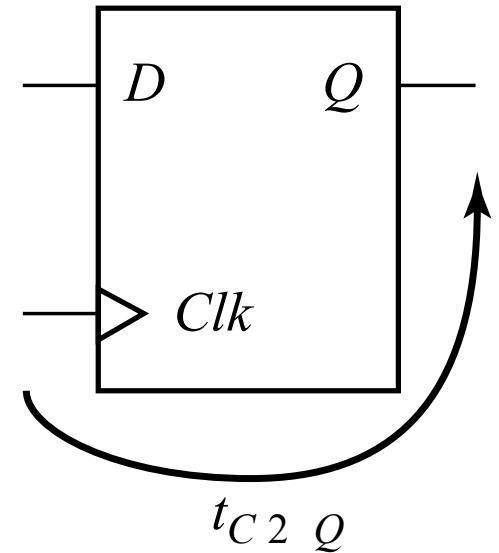
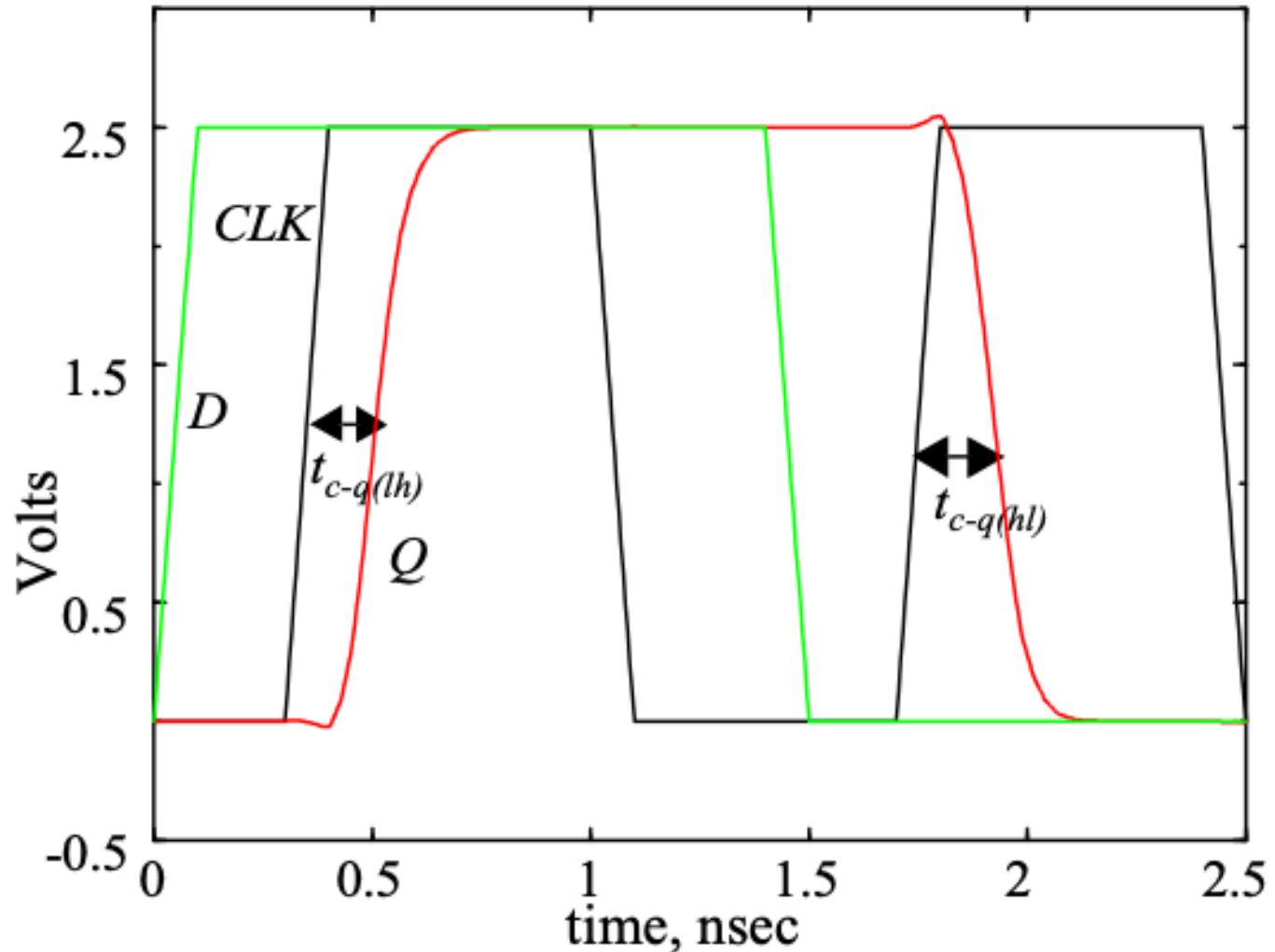


Clk-to-Q Intrinsic Delay

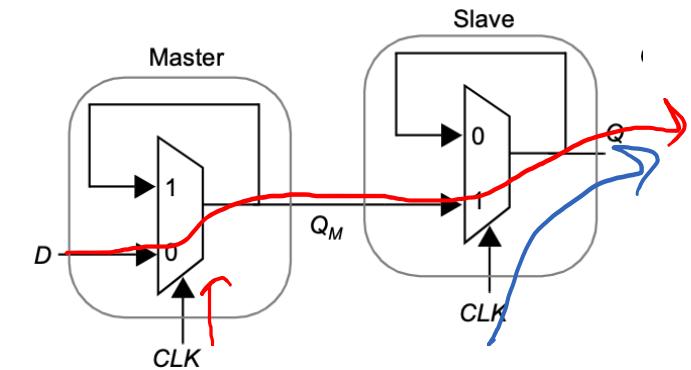


Register

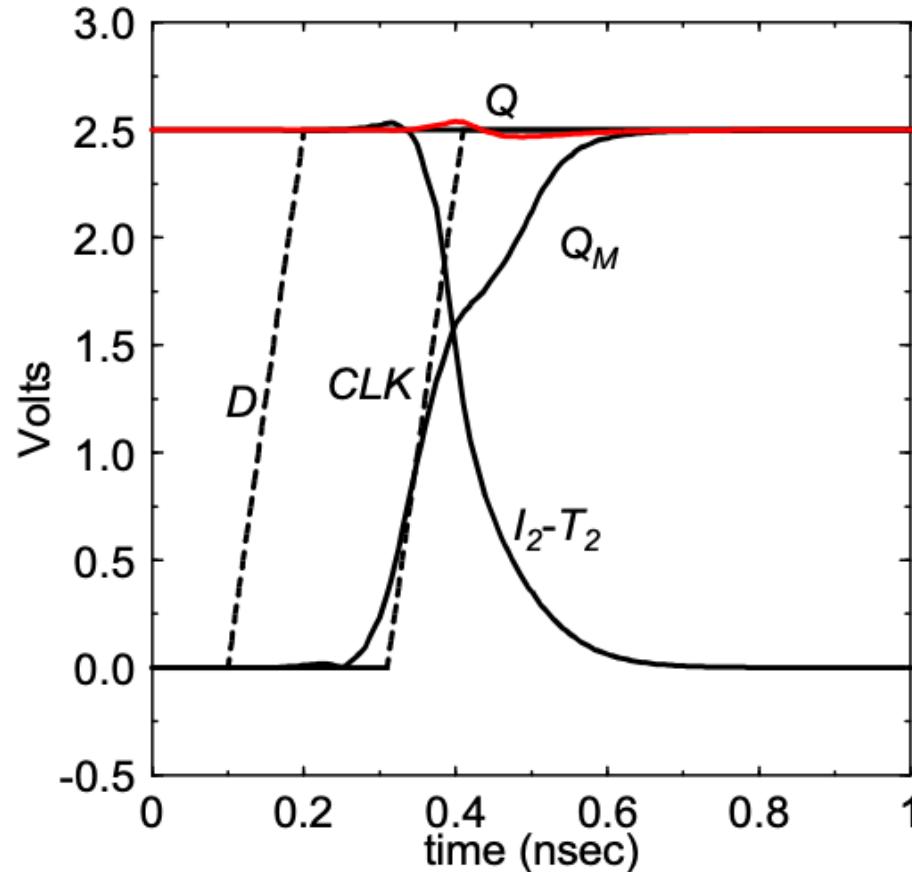
Clk-Q Intrinsic Delay



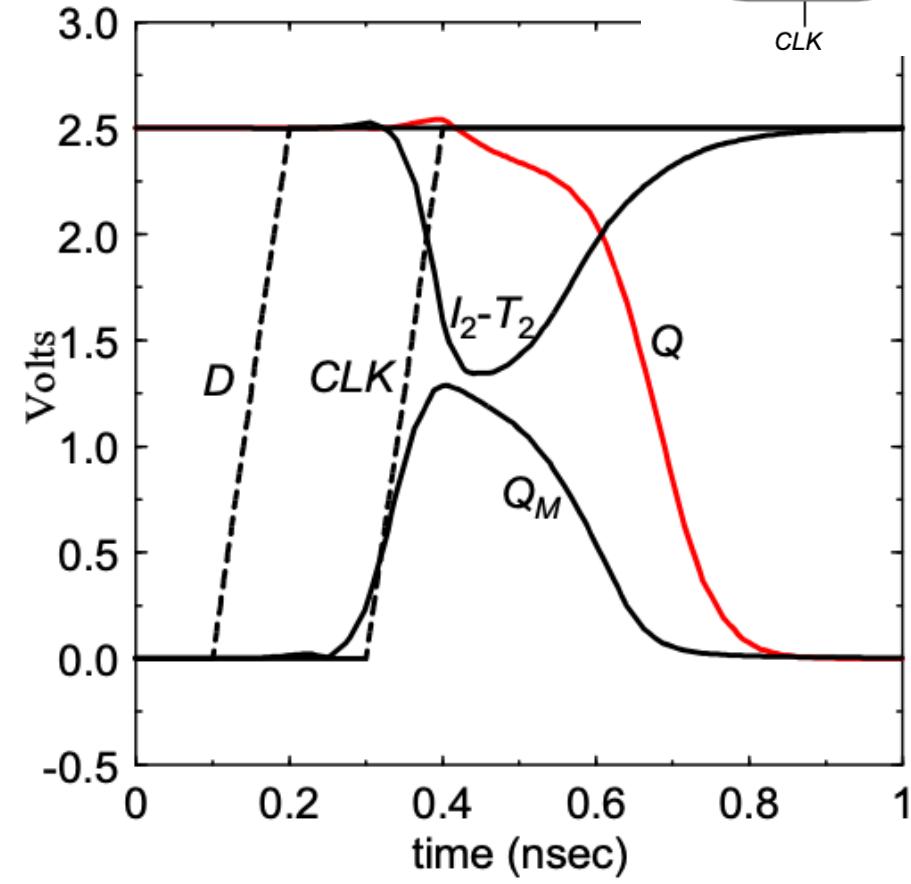
D-to-Clk Delay



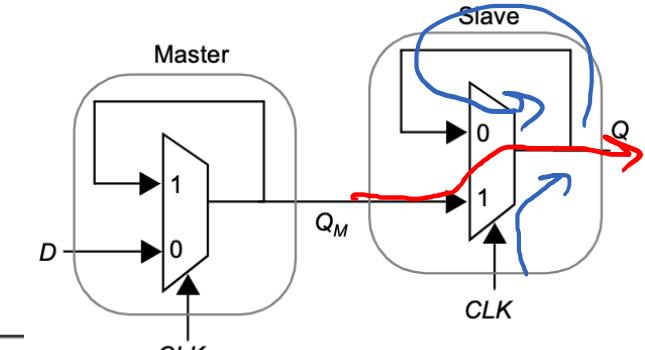
D-to-Clk Delay



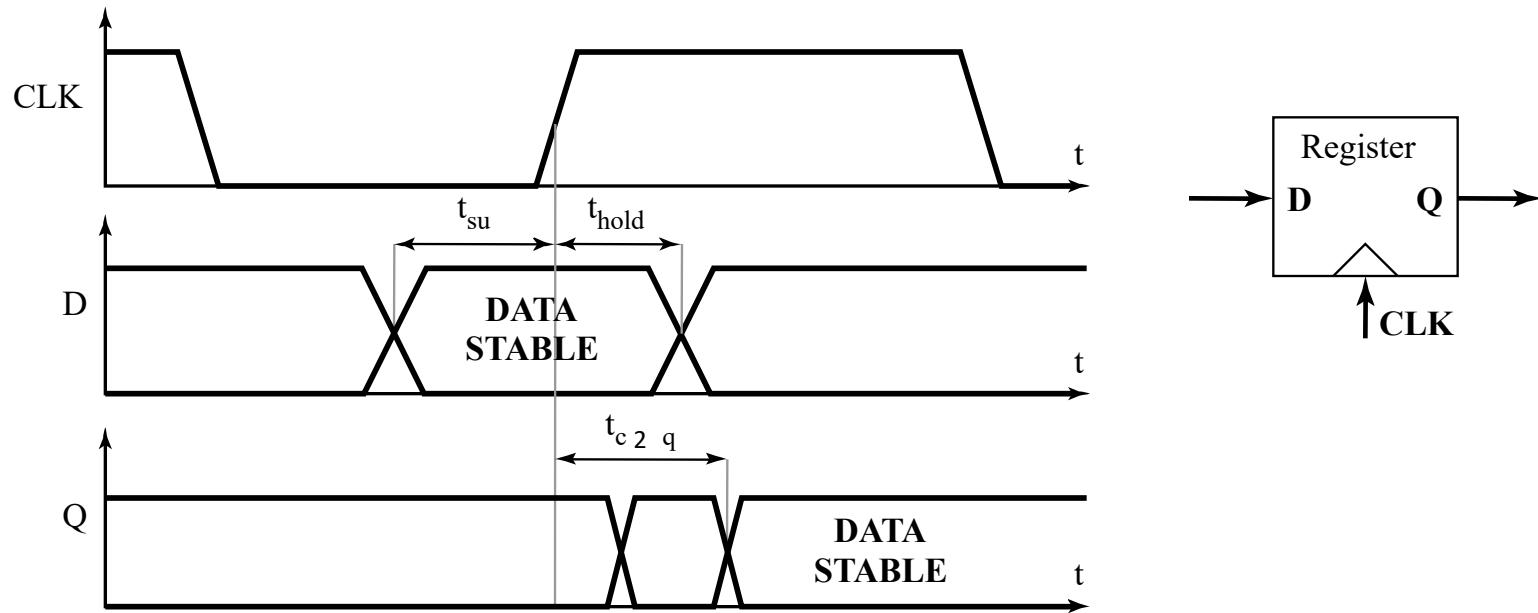
(a) $T_{\text{setup}} = 0.21 \text{ nsec}$



(b) $T_{\text{setup}} = 0.20 \text{ nsec}$



Timing Definitions



Glitch

move and

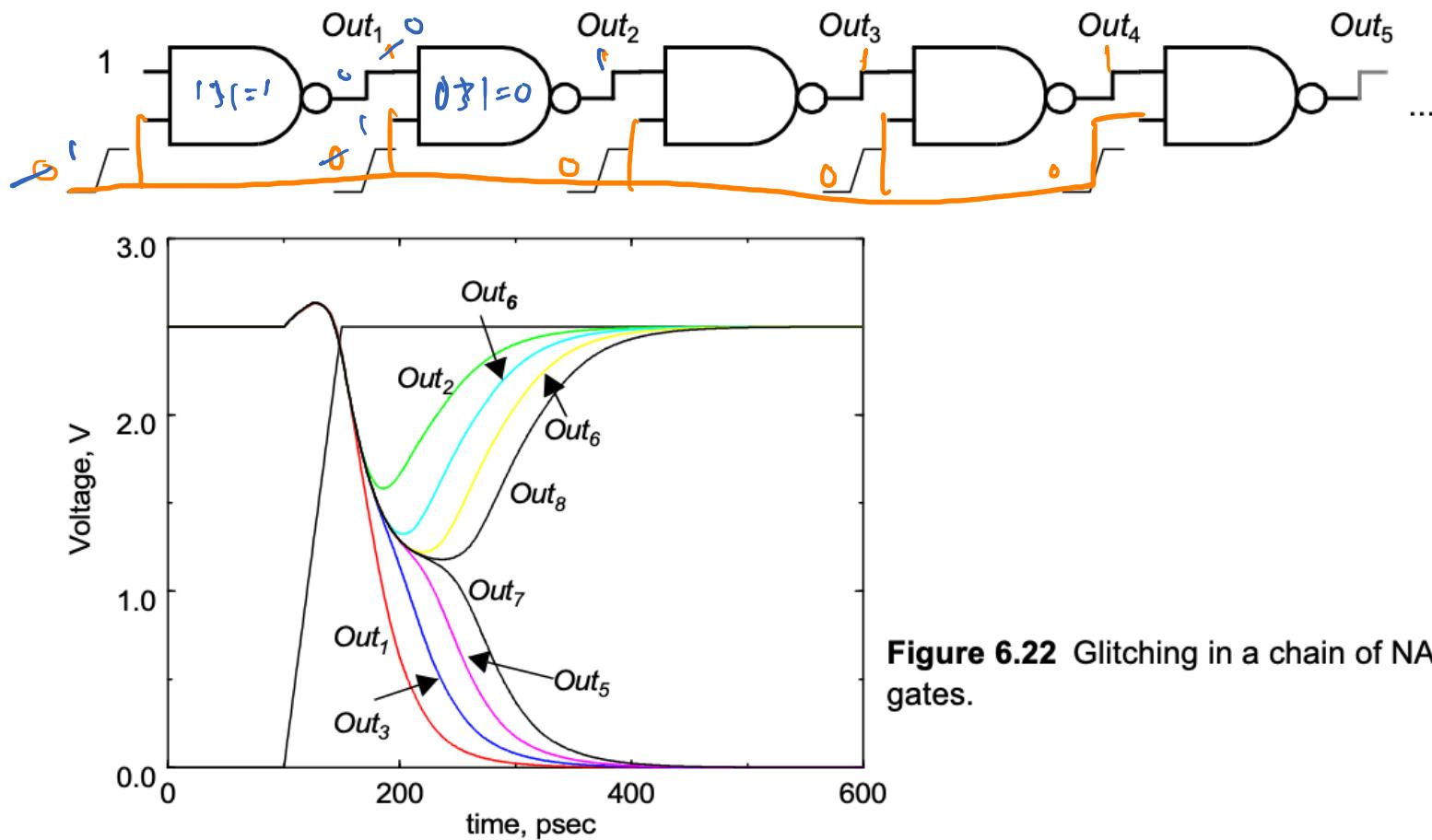
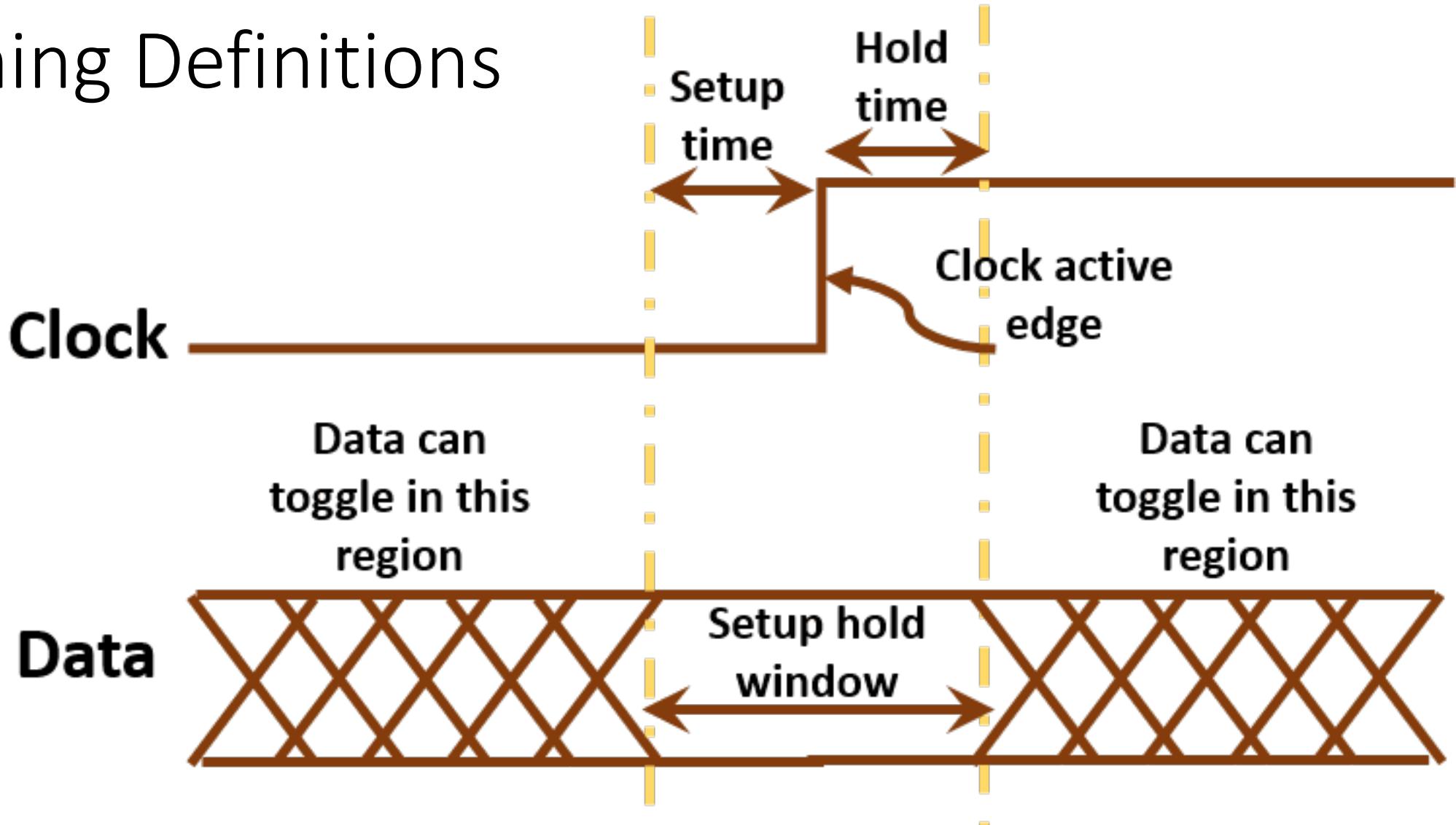


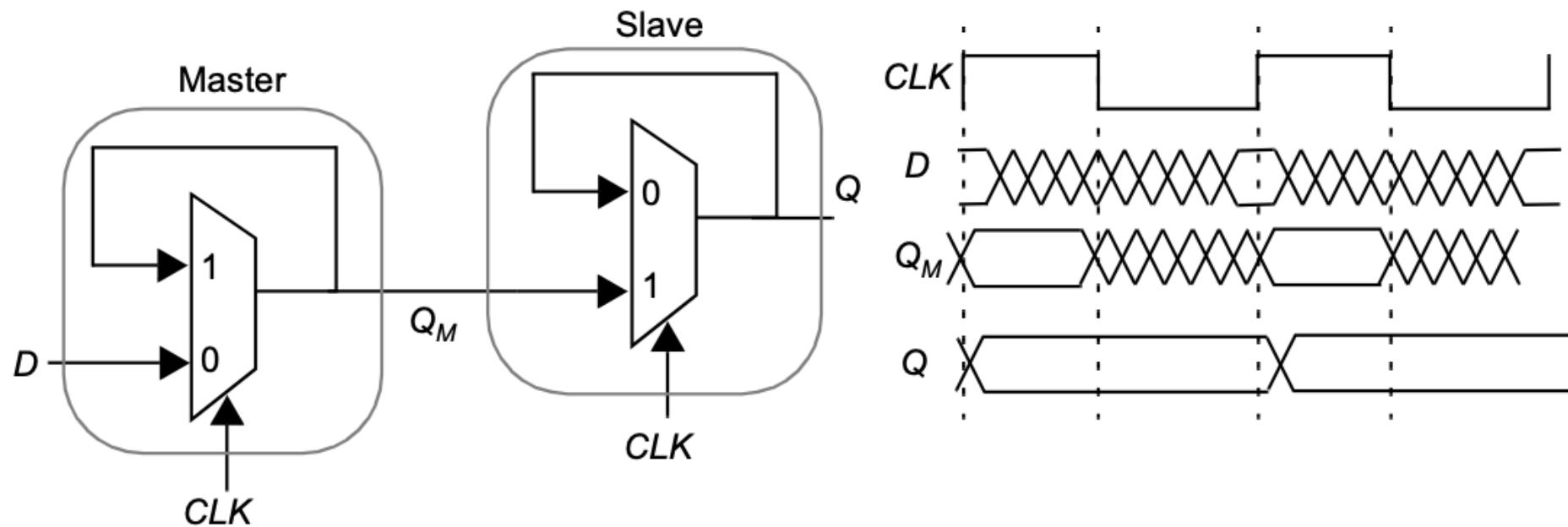
Figure 6.22 Glitching in a chain of NAND gates.

Timing Definitions



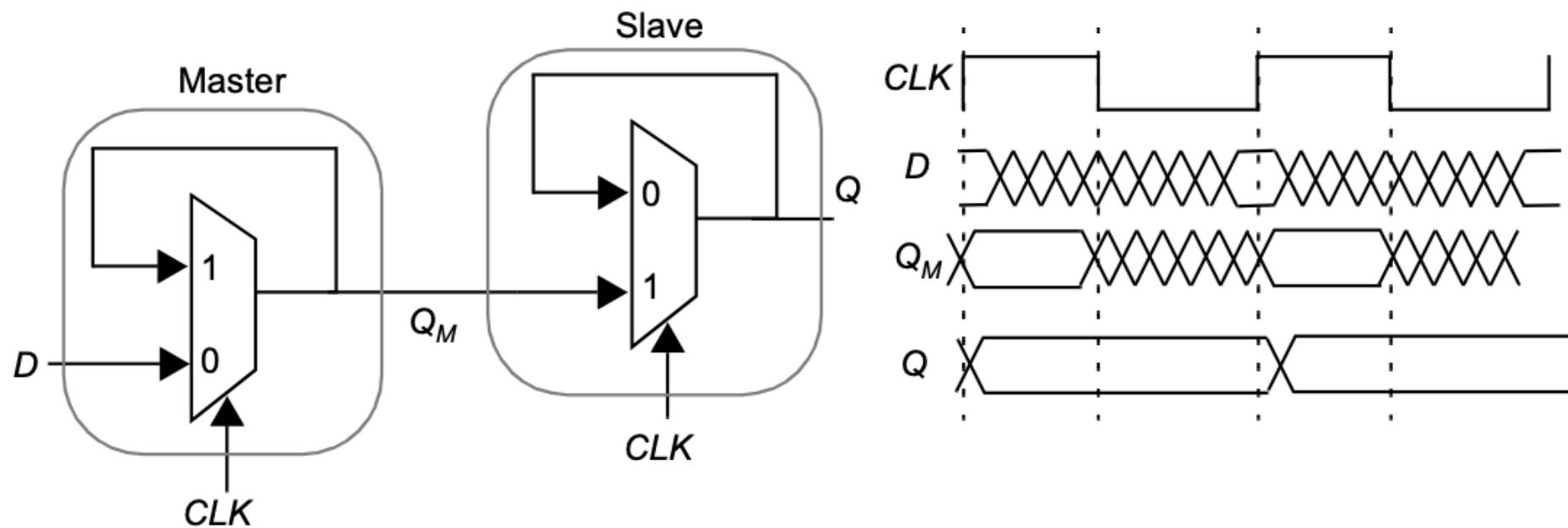
Setup Time

- The set-up time is the time before the rising edge of the clock that the input data D must become valid. Another way to ask the question is how long before the rising edge does the D input have to be stable such that QM samples the value reliably.

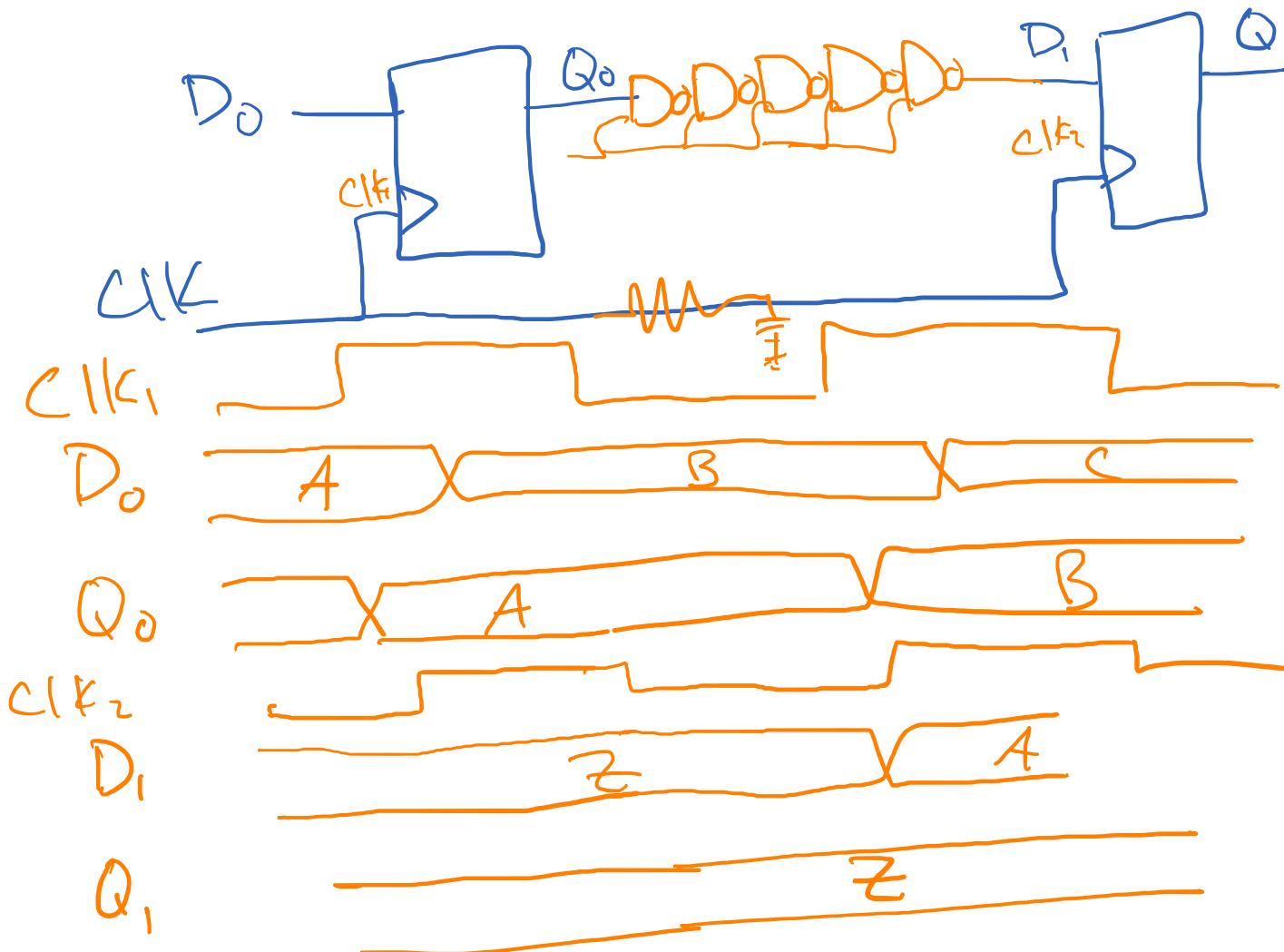


Hold Time

- The hold time represents the time that the input must be held stable after the rising edge of the clock.

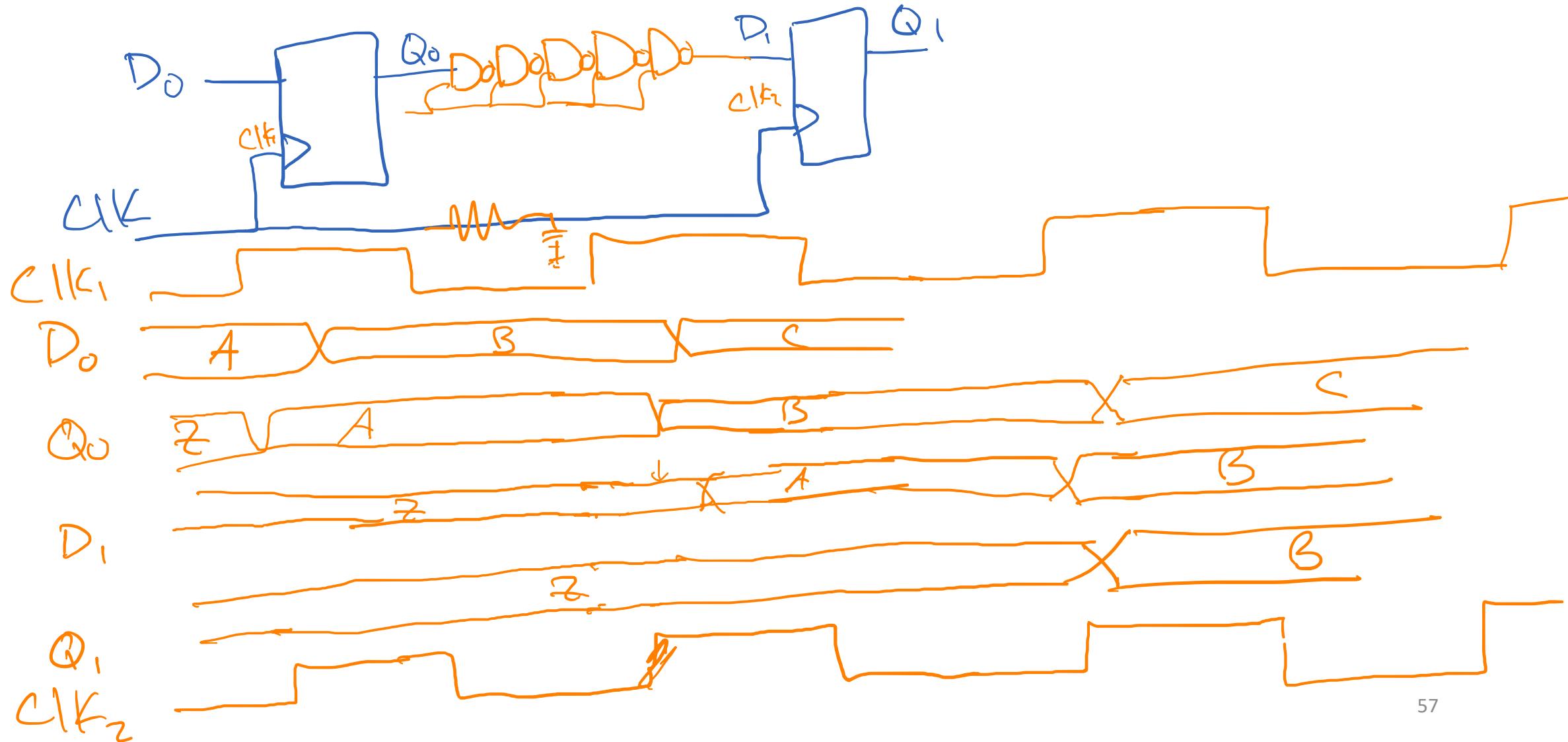


Setup Time

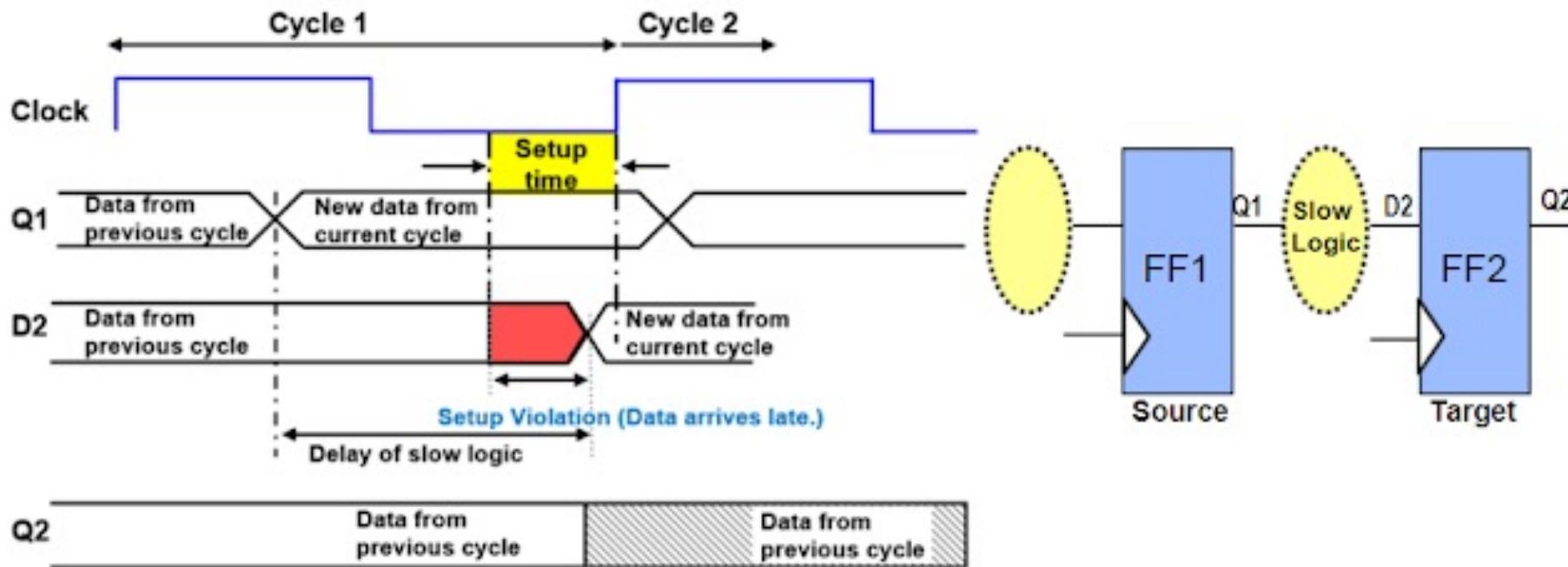


- Hold Time

Setup Time

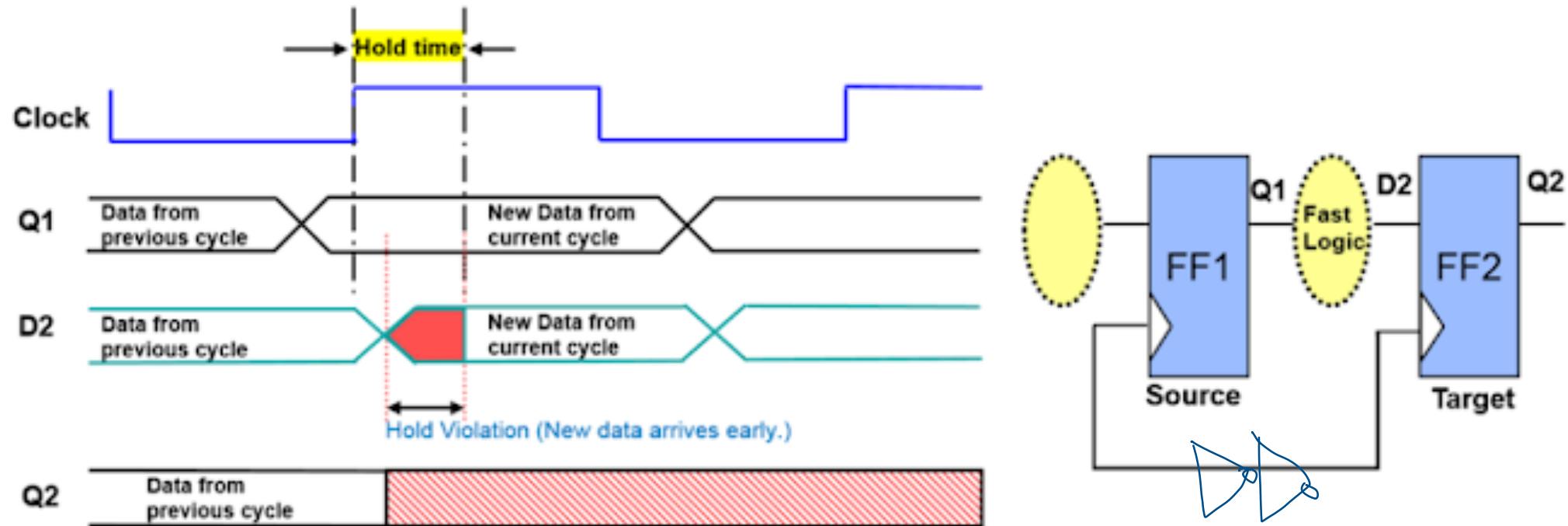


Setup Time



Hold Time

Hold Time

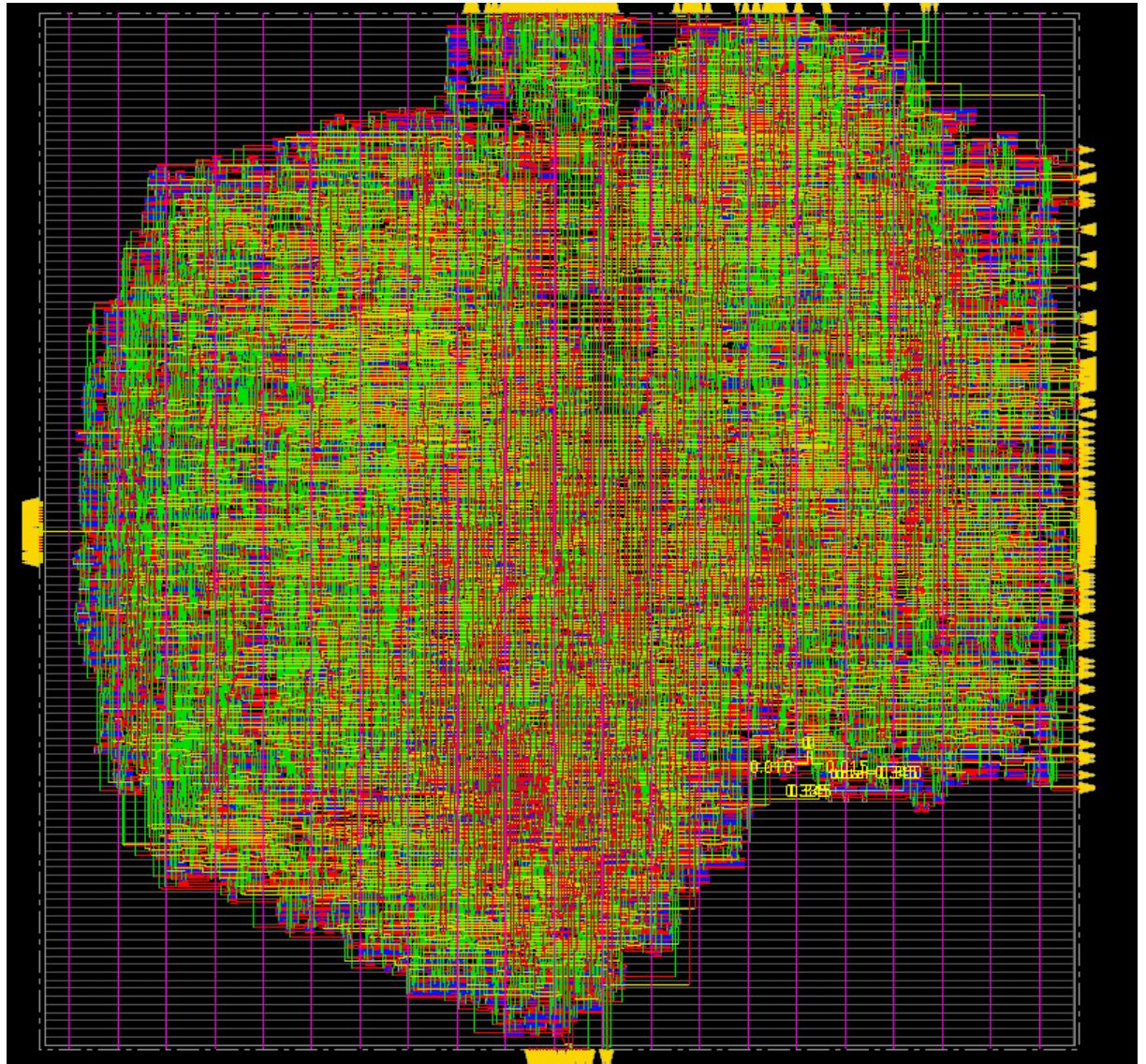


WARNING: HOLD TIMES ARE A BIG DEAL!!!

- You can always fix setup times with a slower clock.
- Hold times are unfixable....
- You do not want a hold-time violation in your design!

Project 1

- Timing Report



Project 1 – make synth

- What is synthesis?

a process where an abstract description of a digital circuit (often at the register transfer level or RTL) is automatically translated into a gate-level implementation, optimized for specific design constraints

a.k.a “compiling”

Project 1 – make pnr

- What is pnr?
- Place and Route
- Aka P&R, Automatic Place and Route (APR)

is where electronic components and their interconnections are automatically arranged and routed on a chip or printed circuit board (PCB)

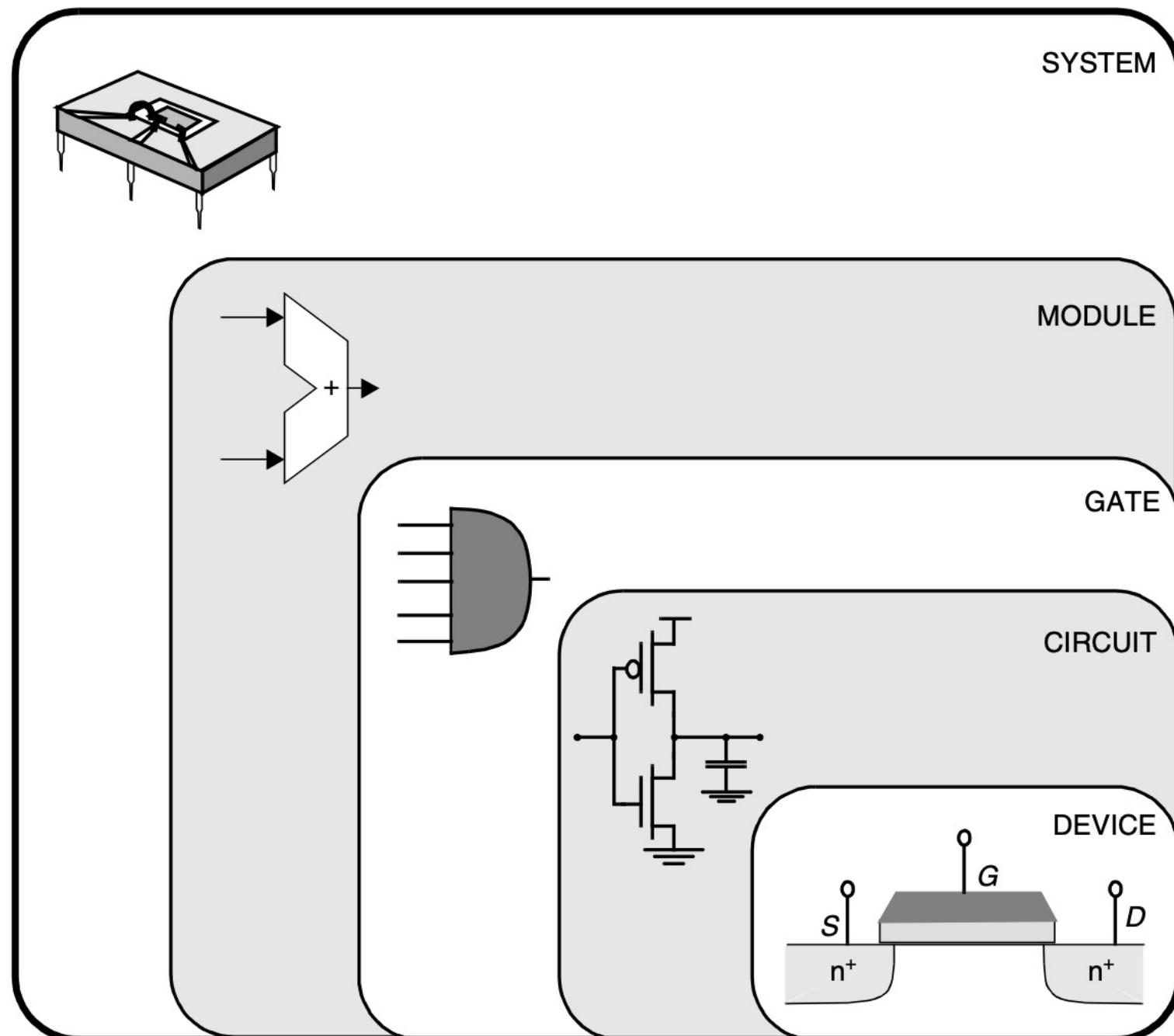
Report Timing

- Setup: report_timing -early
- Hold: report_timing -late

- picoriv

~ add v1P docs 250W Hz target
- add docs on reports
- unity docs docs on

Next Time: Gates

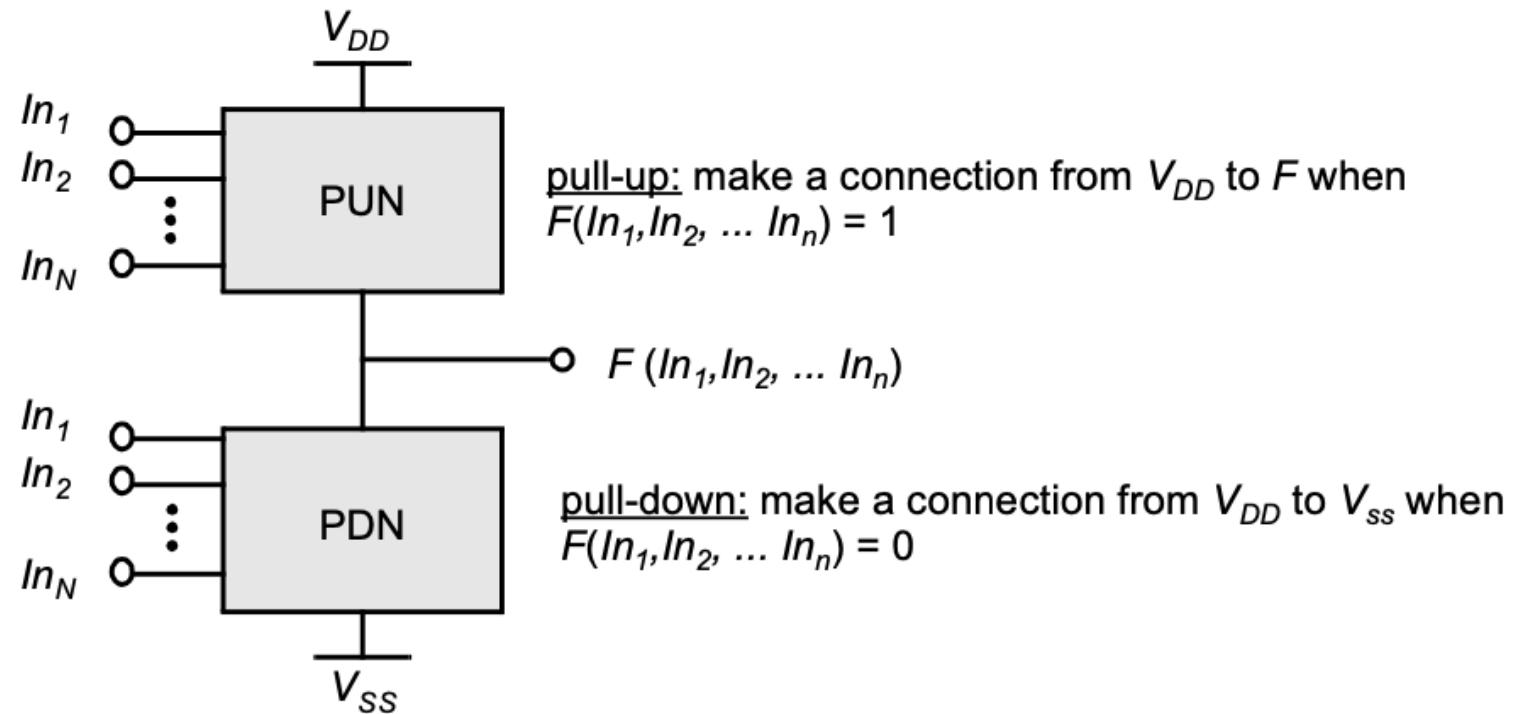


List of interesting stuff

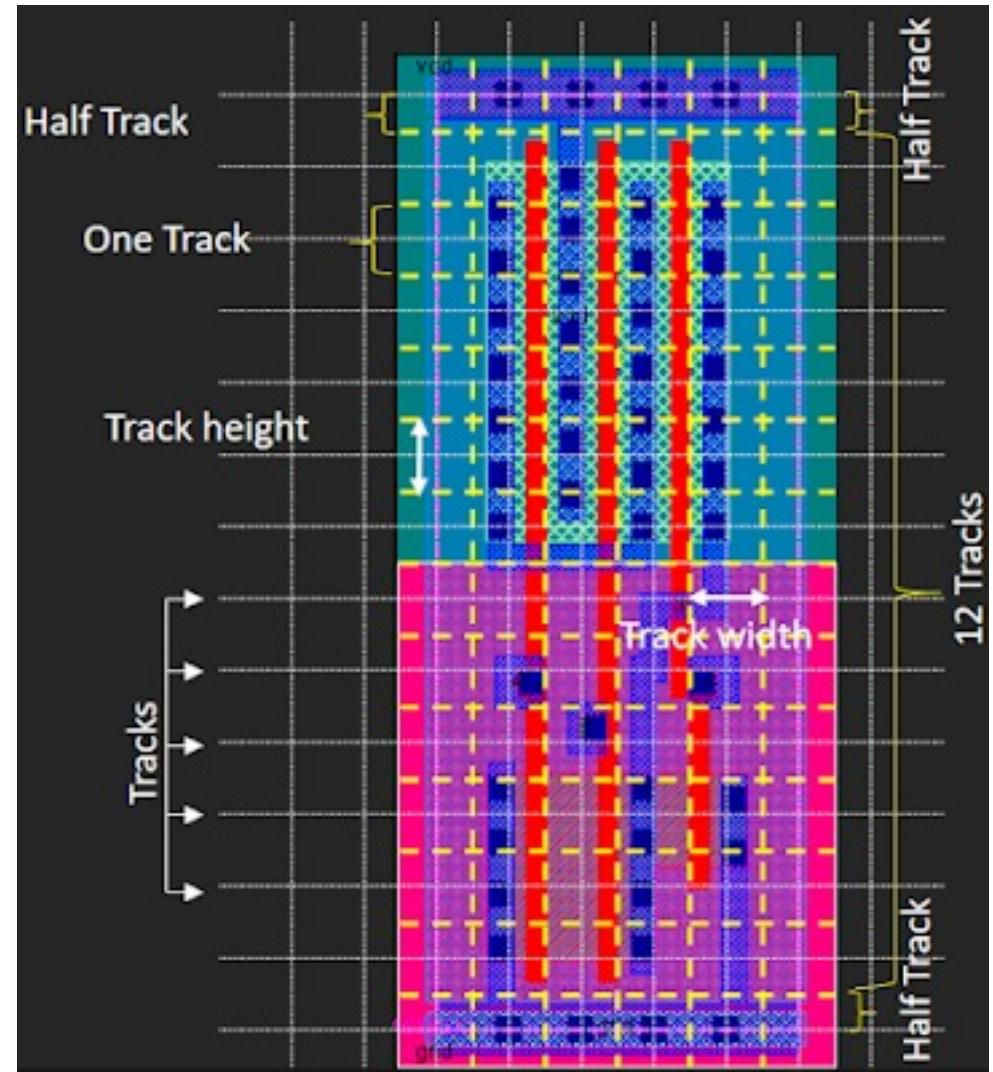
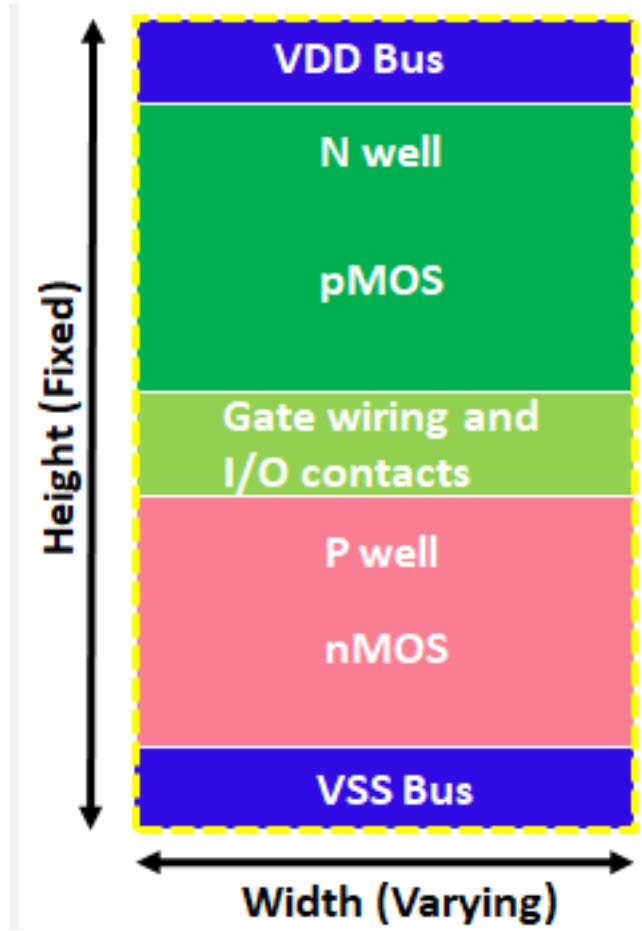
- PDK
- StdCell Library
- IO Cell Library
- Others

Standard Cells

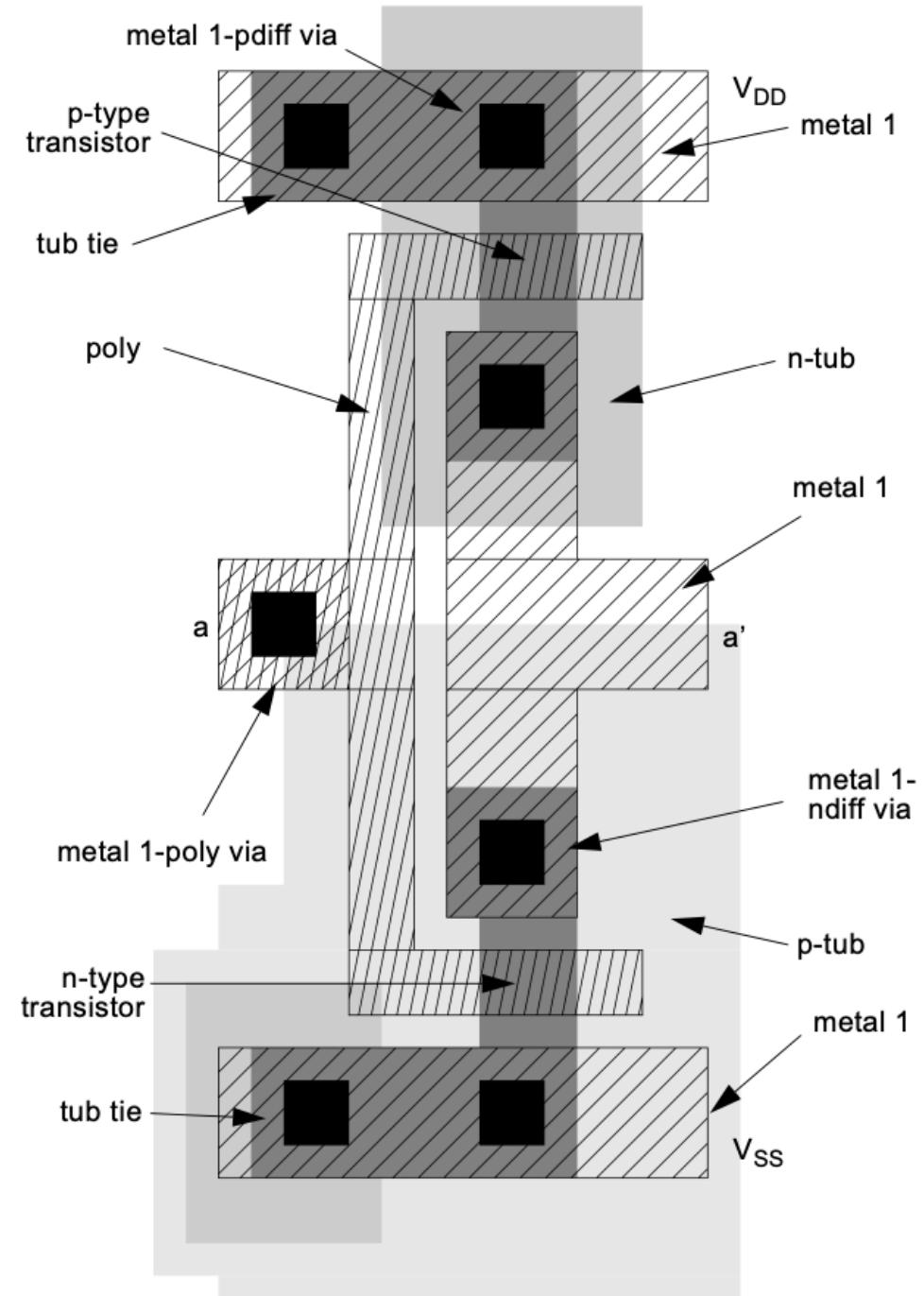
Standardized Logic Gates

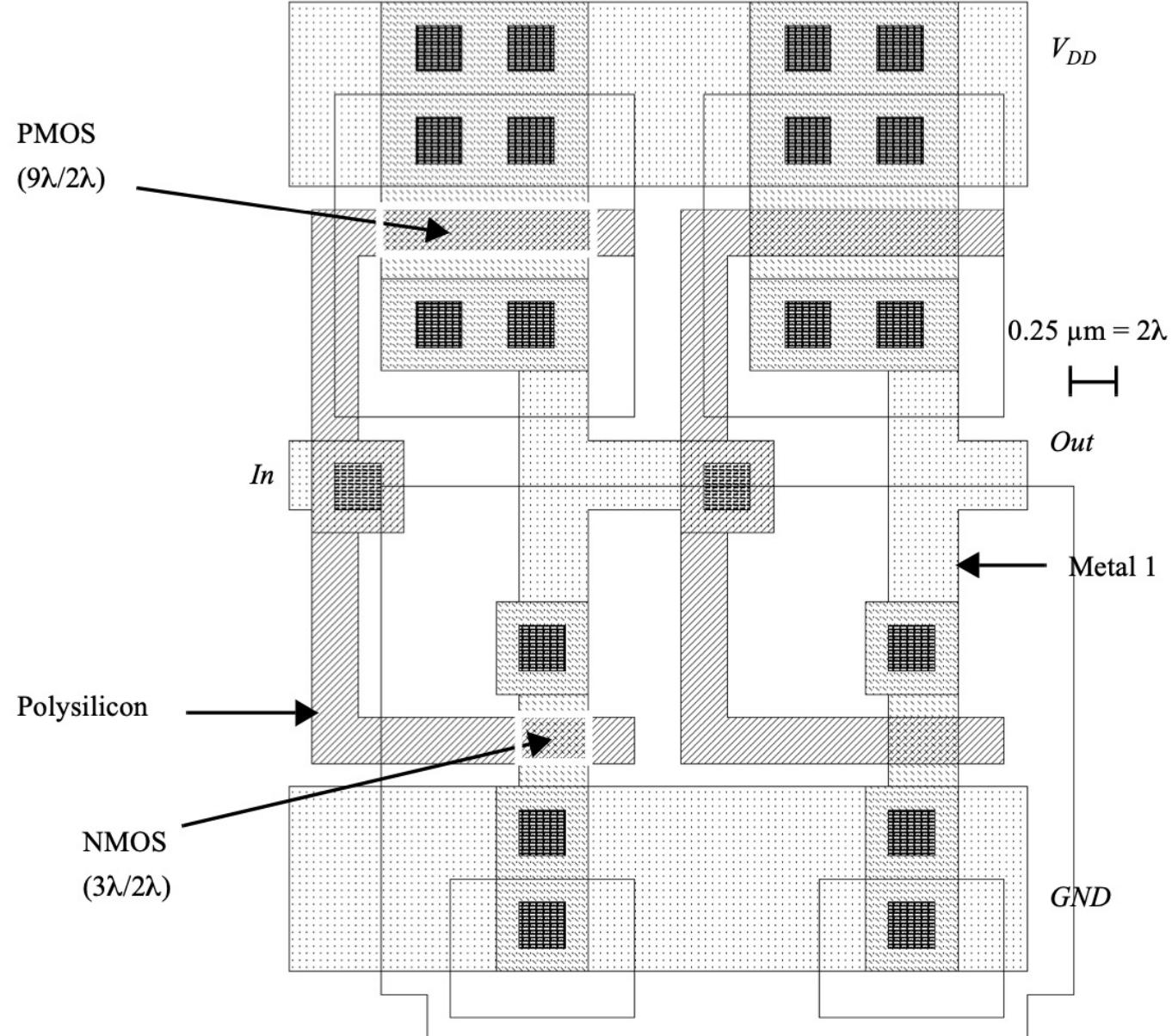


Standard Cells



Inverter Layout



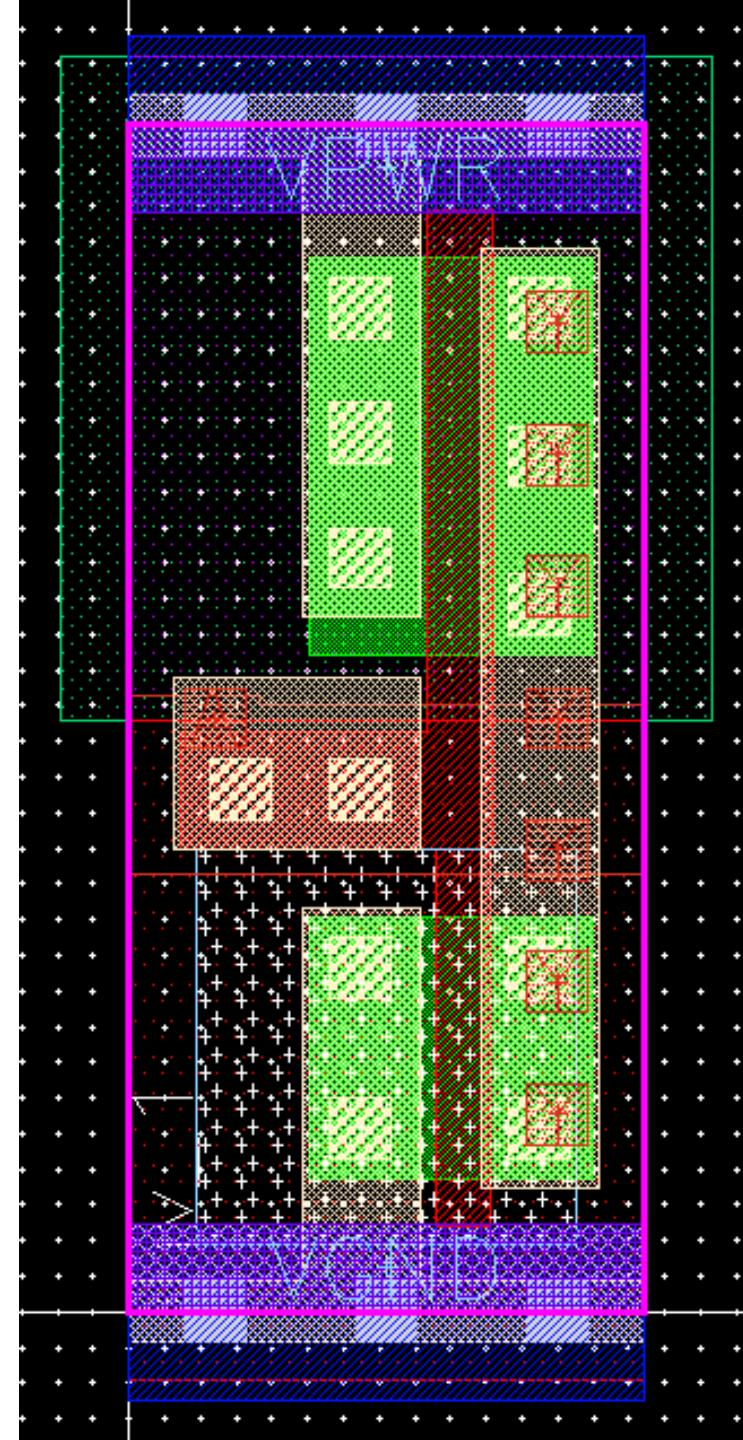


[Digital Integrated
Circuits: A Design
Perspective]

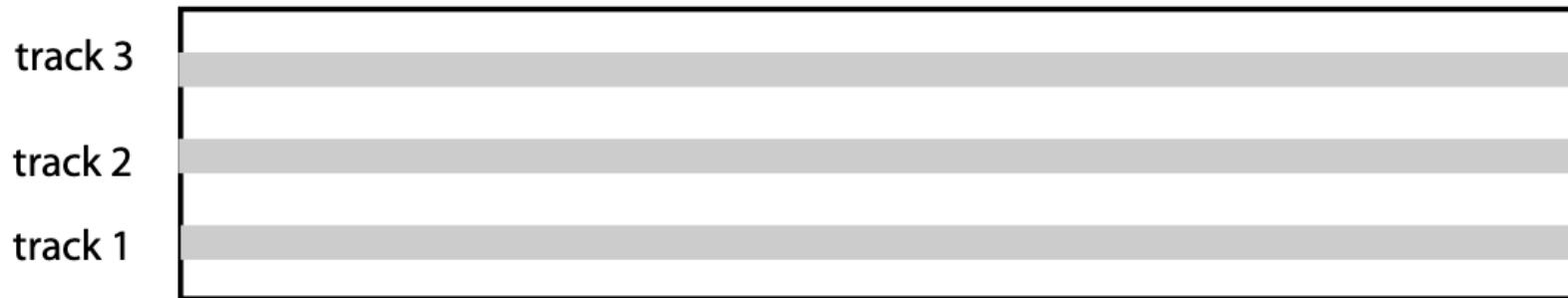
Figure 5.15 Layout of two chained, minimum-size inverters using SCMSOS Design Rules (see also Color-plate 6).

Our INV_X1

[demo time]



Routing Tracks



NAND/NOR/INV

NAND

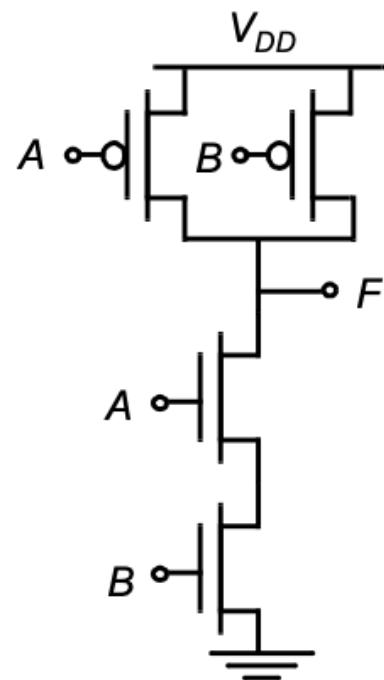
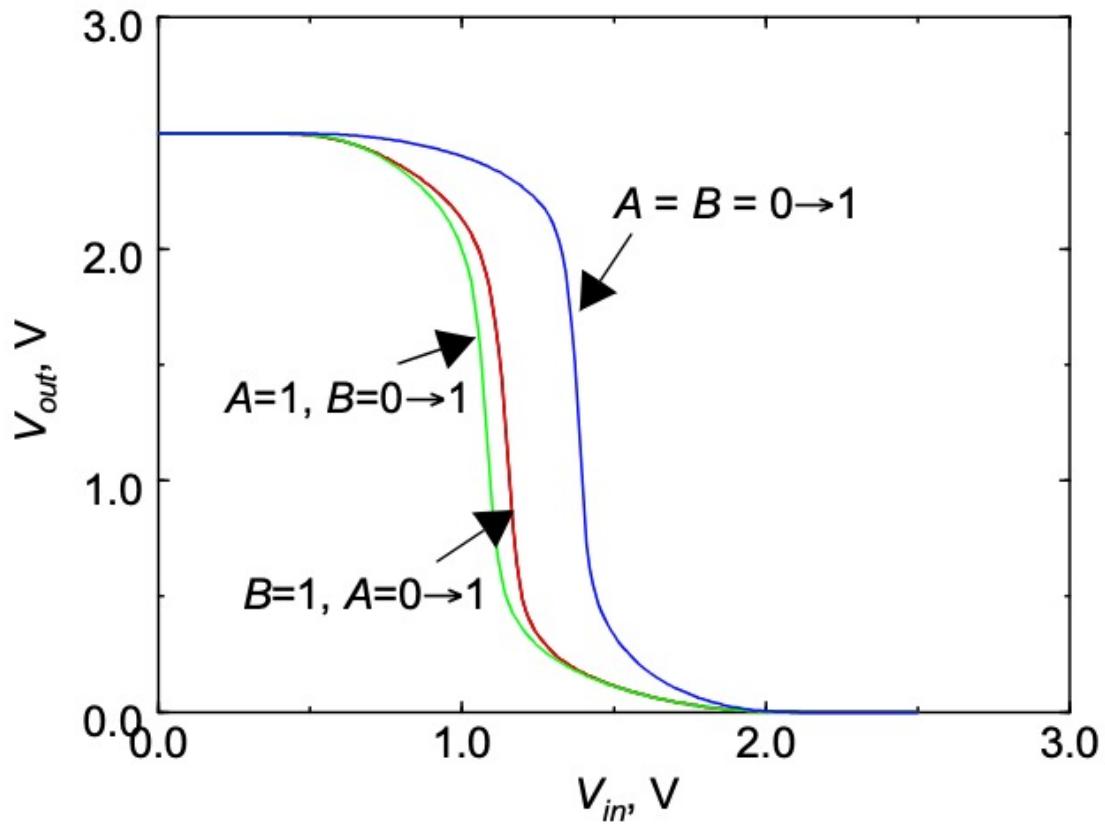
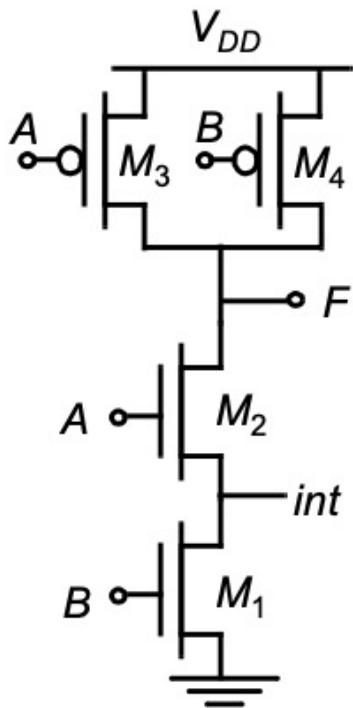


Table 6.1 Truth Table for 2 input NAND

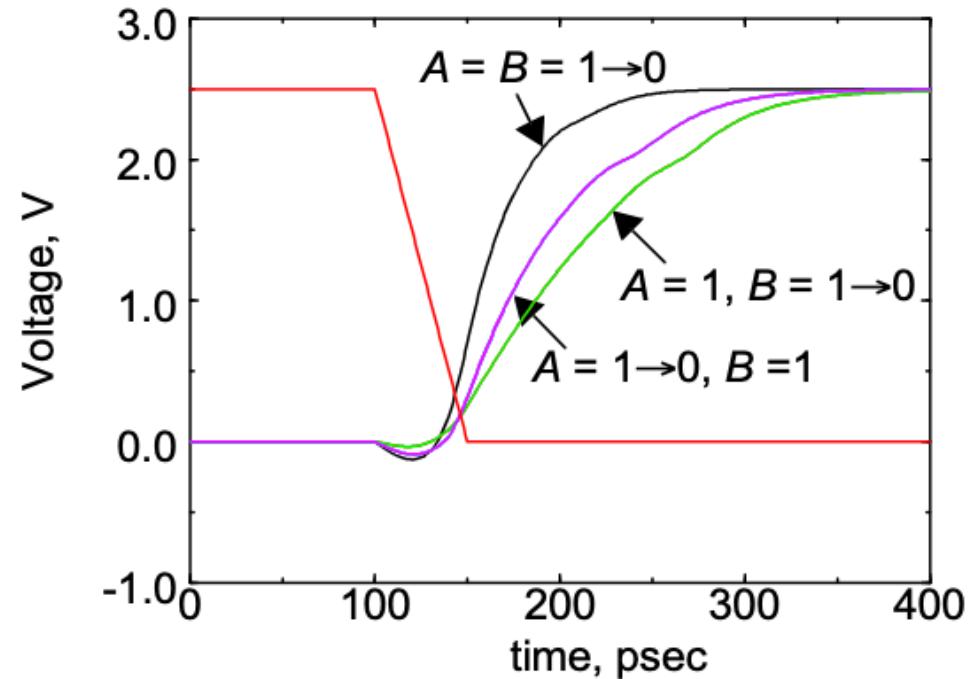
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

Figure 6.5 Two-input NAND gate in complementary static CMOS style.

Output delays are dependent on inputs



Output delays are dependent on inputs



Input Data Pattern	Delay (psec)
$A = B = 0 \rightarrow 1$	69
$A = 1, B = 0 \rightarrow 1$	62
$A = 0 \rightarrow 1, B = 1$	50
$A = B = 1 \rightarrow 0$	35
$A = 1, B = 1 \rightarrow 0$	76
$A = 1 \rightarrow 0, B = 1$	57

Figure 6.9 Example showing the delay dependence on input patterns.

Output delays are also dependent on Fan-Out, or the number of dependent gates connected to driver output

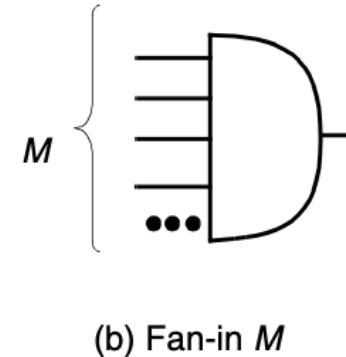
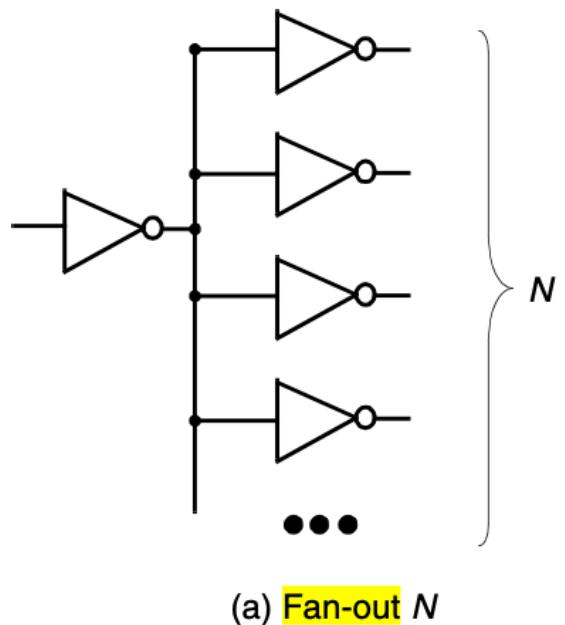


Figure 1.16 Definition of fan-out and fan-in of a digital gate.

Output delays are also-also dependent on wire delay.

