EE Department, UET, Lahore
Faisalabad Campus

Reg. No. 2017-EE-387

EE312 Power Electronics

Comprehensive Exam (24 Aug. 2020, Session 2017)

Time Allowed: 180 Minutes
Total Marks: 70

- Start solution of every new question on a new page.
- All the related parts of a question must be solved together.
- Time division suggestion – Q1- Q5 are like mid-term exam – solve in 60-70 mins

Q.1 (Marks: 2 + 4, CLO1)

Consider a three phase full-wave converter as shown in the figure. It is operated from a three phase Y-connected supply with

$V_{LL\text{-}rms} = 400V$, 50Hz $\quad R_{Load} = 10\Omega$

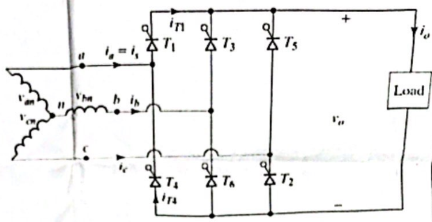
The converter is operated with a firing angle $\alpha = 30°$. Analyze this system to calculate:

a. The average i.e. dc value of load voltage.

b. The rectification efficiency of the converter. For your ease, the equation for evaluating the rms output voltage, is being provided:

$$V_{rms} = \sqrt{3}\, V_m \left(\frac{1}{2} + \frac{3\sqrt{3}}{4\pi}\cos 2\alpha\right)^{1/2}$$

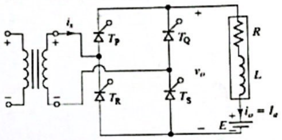
Vm is peak value of line-neutral supply voltage.



Q.2 (Marks: 4)

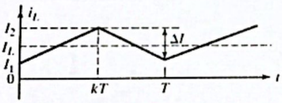
For the analysis of a single phase, controlled rectifier as shown in the figure, sketch waveform one complete cycle of output voltage v_o for a firing angle α of 90°, when the circuit is in steady state. Assume a highly inductive load and a DC voltage source on the load side as shown.

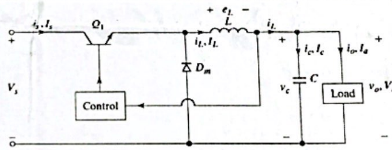
Furthermore, on the v_o waveform, clearly mention which pair of thyristors is conducting at what time – Thyristor names are given in the figure, use these names.



Q.3 (Marks: 5, CLO2)

A DC/DC Buck converter is shown in the figure, Analyze this circuit and sketch its equivalent



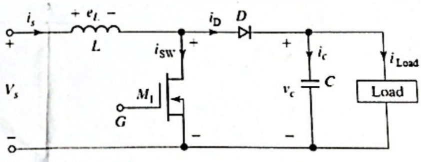


circuits in on-state and off-state (i.e. mode 1 and mode 2) for the continuous conduction mode (CCM). Lastly, sketch one complete cycle of the inductor voltage e_L. Use the same polarity for e_L as shown in the figure. For your ease, the inductor current waveform is being given.

Q.4 (Marks: 10)

Analyze the Boost DC/DC converter shown in the figure and sketch waveforms of one complete cycle for the following variables. Use the same direction for current as shown in the figure, and assume the converter to operate in steady state in continuous conduction mode. Also assume capacitor voltage to be smooth, ripple free.

(a) i_S (b) i_D
(c) i_C (d) i_{Load}
(e) i_{SW}

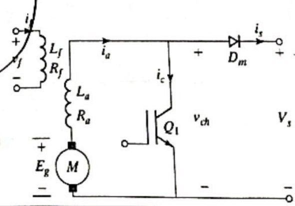


Q.5 (Marks: 5)

A DC/DC converter is operating a DC motor in regenerative mode. The DC supply voltage is 500V, duty cycle k is 50% and the average armature current Ia is fixed at 250A.
Analyze this system and calculate

a. Average chopper Voltage V_{ch}

b. The regenerated power P_g



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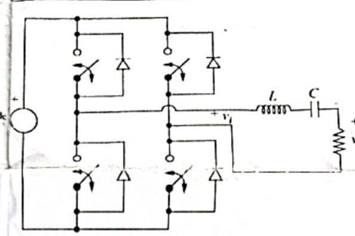
Q.6 Design the LC filter for a single phase full bridge series resonant inverter as shown the figure. The load is 10 Ω – resistive and it requires a 1000-Hz, 100-Vrms sinusoidal voltage. The THD of the load voltage must be no more than 5 percent (include third harmonic only, ignore other harmonics). An adjustable dc source is available. Subsequent to designing your system, analyze its performance by evaluating the power delivered to the load at the fundamental frequency, and at the third harmonic frequency.
Relevant equations are being provided for your ease.

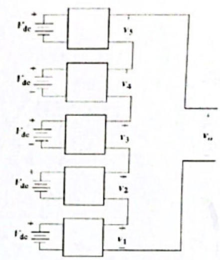
$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC}$$

$$\frac{V_o}{V_i} = \frac{1}{\sqrt{1 + Q^2((\omega/\omega_0) - (\omega_0/\omega))^2}}$$



15 — CLO3

Q.7 A five source multi-level inverter is shown in the figure. Sketch its output voltage. Also sketch waveforms for individual voltages $v1 - v5$ while showing the concept of pattern swapping. Furthermore, write down simultaneous equations for delay angles that will eliminate harmonics 5, 7 and 11 from the output voltage v_o.



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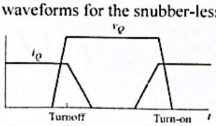
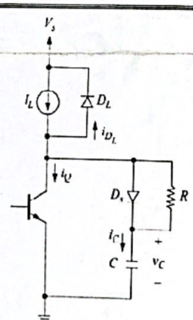
Q.8

a. A power MOSFET is connected in a circuit where it is dissipating 6.5W. A heat sink is connected with it. The ambient temperature is 30°C. The thermal resistances are given as follows. Calculate the junction temperature of this MOSFET and justify that the heat sink is functioning properly. R_{JC} = 2.5°C/W R_{CS} = 2°C/W R_{SA} = 10°C/W. T_J-max = 150°C. — 3

b. A turn-off snubber circuit for a BJT is shown in the figure. An increase in the value of snubber capacitance lowers the power loss across the switch – justify this by sketching waveforms of transistor voltage v_Q, transistor current i_Q and the corresponding power loss p_Q for three different values of C i.e. small, medium and large. For your convenience, v_Q, and i_Q waveforms for the snubber-less circuit are being shown as under. — 6





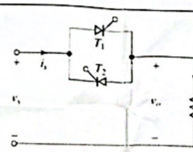
CLO4

Q.9 Two options for AC/AC voltage control are shown. You have to answer the following questions.

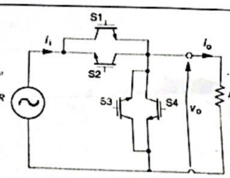
i. Which circuit is better in terms of ease-of-filtration for the harmonic content?

ii. Which circuit will have lower switching power loss?

Justify/Support each of your answers with detailed and valid arguments. (No marks without proper arguments)



Phase Controlled AC/AC Conv.



PWM AC/AC Conv.

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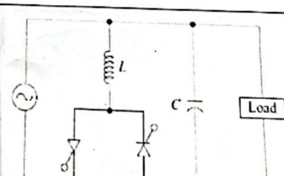
Q10 Justify that the provided circuit can be used as a Static Var Compensator for loads of varying reactive power demand. (Assume that the load is always of lagging current).
Only provide supporting arguments, any waveforms or equations are not necessary.



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