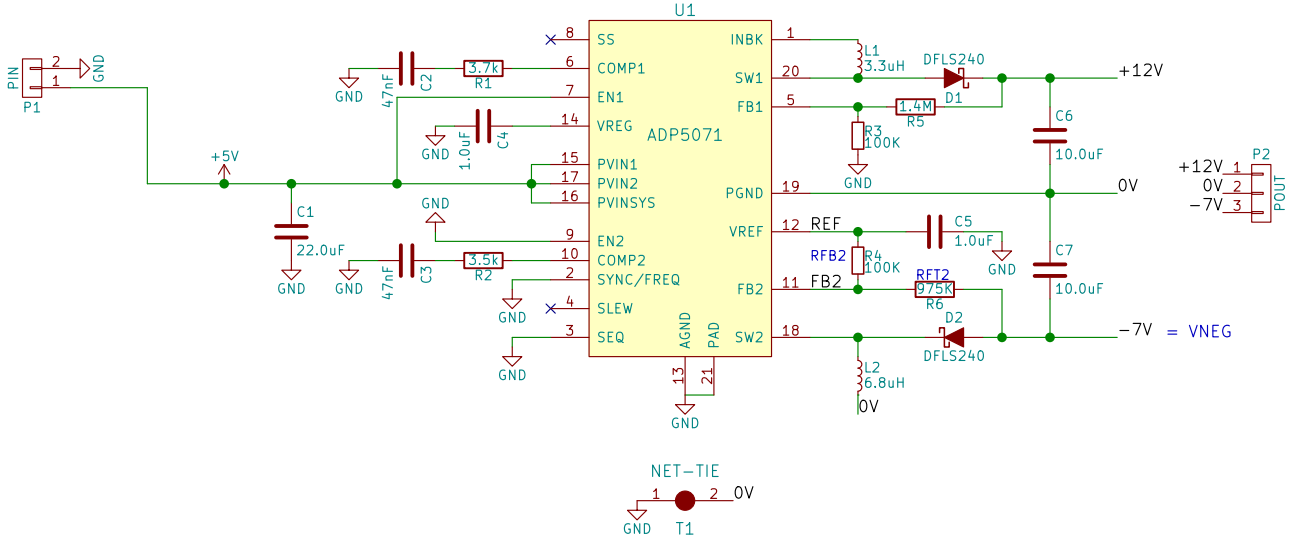
TODO:
* **BUY**
  - **R6 = 975K (1%)**
  - **C2, C3 = 47 nF**
  - **L2 = 6.8 uH (XAL4030)**
* **CHECK DESIGN IN ADISIM (ESP R1 and R2)**
* **CONSIDER POST LDO REGULATORS FOR MIN RIPPLE**
* **LAYOUT IS TOO SPACY**

SYNC/FREQ = GND : 1.2 MHz
SYNC/FREQ = VREG : 2.4 MHz

tSS = 4 ms if open
tSS = 38.4e-3 - 1.28e-7 x RSS(Ohm), where 50 kOhm ≤ RSS ≤ 268 kOhm.

VPOS = VFB1 x (1 + RFT1/RFB1)
= 0.8 x (1 + 1.4M/0.1M) [V] = 0.8 x 15 [V] = 12 [V]



INDUCTORS: XAL4030 line
Value (uH) : 3.3/ 4.7/ 6.8/ 8.2/ 10/ 15
DCR (mOhm) : 26.0/40.1/67.4/60.8/84.0/109
SRF (MHz) : 43/ 36/ 29/ 27/ 24/ 20
ISat (A) : 5.5/4.5/3.6/4.0/3.0/2.8
Irms (A) : 6.6/5.1/3.9/3.4/3.1/2.8

DIODE:
Peak Repetitive Reverse Voltage: 40 [V]
Working Peak Reverse Voltage: 40 [V]
DC Blocking Voltage: 40 [V]
RMS Reverse Voltage: 28 [V]
Average Forward Current: 2.0 [A]
Non-repetitive peak forward surge current (8.32ms): 50 [A]
Forward voltage: 0.45 [V] @ 2.0 [A]
Leakage current: 0.1-10 [mA]
Capacitance: 90 [pF]

DUTY2 = (|VNEG|+VDIODE2)/(VIN+|VNEG|+VDIODE2),
where VDIODE2 is the forward voltage drop over Schottky diode
I_L2 = I_OUT2 / (1 - DUTY2)
t_ON2 = DUTY2 / f_SW
/\I_L2 = VIN x t_ON2 / L2

Ripple current max of 30% of maximum dc:
L2 = VIN x t_ON2 x (1 - DUTY2) / (0.30 x I_OUT2)

Ensure: Peak inductor current [max input curr + 1/2 ind ripple curr] is below the rated saturation current of the inductor.

Ensure: Max rated RMS current > max DC input current to regulator

Ensure: L2 > L_min2 = Vin x (0.13/(1-DUTY2) - 0.16) [uH]

VNEG = VFB2 - RFT2 / RFB2 x (VREF - VFB2) [VREF=1.6, VREF-VFB2=0.8]
= 0.8 - 975/100 x 0.8 [V] = -7.0 [V]

DUTY2 = (7+0.45)/(5+7+0.45) = 60%

I_L2 = 0.5 / (1-0.6) = 1.25 [A]

t_ON2 = 0.6 / 1.2MHz = 0.5 us

/\I_L2 = 5.0 x 0.5e-6 / 6.6e-6 = 378 [uA]

L2 = 5.0 x 0.5e-6 x (1-0.60) / (0.30 x 0.5) = 6.66 [uH]

L2_min = 5.0 x (0.13/(1-0.6) - 0.16) = 0.825 [uH]

Engstad Design Studio

Sheet: /		
File: PowerRail.sch		
Title: ADP5071 PowerRail		
Size: A4	Date: 2015-09-17	**Rev: 0.2**
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