Floor Planner and Top Level Router

Phase 2

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Components

1) Floor Planner

2) Pin Assignment

3) Router

Abstract Steps

1) Macros are placed on the die to optimize their placement

2) Place the pins of the soft macros based on the interconnect to avoid congestion

3) Route the required nets

Inputs

- DEF for the hard macros
- LEF for the soft macros
- Technology LEF
- Verilog gatelevel netlist

Floor Planner

- DEF Files parsing
- DEF File components section output
- Margins
- Optimization by Connection trials
- More Legalization
- Testing

Router Progress

- Technology LEF parsing
- Supports having n metal layers with direction that is extracted from TECH LEF during runtime
- Supports metal layers of different pitches hat are extracted from TECH LEF during runtime
- Supports multi-pin nets (was done last phase on 3 metal layers with known directions)
- Generates nets segment in the DEF

Pin Assignment

- Implemented this phase
- An important step between floorplanning and routing
- Connects pins of hard macros and then soft macros
- Input: gate level netlist and output of the floor planning and Tech Lef
- Output: x,y,z coordinates of each pin

What’s missing

- Parse gatelevel netlist to get interconnect information and I/Os
- Connect the floorplanner with the router (macros act as obstacles in all metal layers)
- Enhance format of nets section in DEF (e.g. place asterisk in place of repeated coordinates)
- Complete the DEF output
- Connecting data from the technology LEF to the floor-planner
- Output the I/Os in the grid