Floor Planner and Top Level Router

Phase 2

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Components

1) Floor Planner

2) Pin Assignment

3) Router

Inputs

- DEF for the hard macros
- LEF for the soft macros
- Technology LEF
- Verilog gatelevel netlist

Floor Planner

- DEF Files parsing
- DEF File components section output
- Margins
- Optimization by Connection trials
- More Legalization
- Testing

Router Progress

- Technology LEF parsing
- Supports having n metal layers with direction that is extracted from TECH LEF during runtime
- Supports metal layers of different pitches hat are extracted from TECH LEF during runtime
- Supports multi-pin nets (was done last phase on 3 metal layers with known directions)
- Generates nets segment in the DEF

Pin Assignment

- Implemented this phase
- An important step between floorplanning and routing
- Connects pins of hard macros and then soft macros
- Input: gate level netlist and output of the floor planning and Tech Lef
- Output: x,y,z coordinates of each pin