```
1   `timescale 1ns / 1ps
2   /*************************************************************************
3    * File Name: vga_sync.v
4    * Project: VGA Sync
5    * Designer: Marc Cabote
6    * Email: marcdominic011@gmail.com
7    * Rev. Date: 11 October, 2017
8    *
9    * Purpose: This module will generate the hysnc signal. Hsync
10   *          specifies the time required to scan a row. This module also
11   *          generates the vsync signal which takes care of the time
12   *          required to scan the entire screen. This will take into account
13   *          a screen with 640 x 480 resolution with has a 25Mhz refresh rate.
14   *
15   * Notes:   -  This module has an asynchronous reset input.
16   *          -  vide_on enables objects to be displayed
17   *************************************************************************/
18  module vga_sync(input            clk, rst,
19                  //output [9:0] pixel_x, pixel_y,
20                  output         hsync, vsync, video_on);
21
22     /*********************************
23     *Counter to generate 25Mhz clock
24     *********************************/
25     reg [1:0] count;
26     wire tick;
27
28     assign tick = (count == 2'b11);
29
30     always @ (posedge clk, posedge rst)
31        if (rst)  count <= 2'b0; else
32        if (tick) count <= 2'b0; else
33                  count <= count + 2'b1;
34
35
36     /*********************************
37     *Horizontal count 0-799
38     *********************************/
39     reg [9:0] hcount;
40     wire endh;
41
42     //assign pixel_x = hcount ;
43     assign endh = (hcount == 799);
44
45     always @ (posedge clk, posedge rst)
46        if (rst) hcount <= 10'b0; else
47        if (tick)
48           if (endh) hcount <= 10'b0; else
49                     hcount <= hcount +10'b1;
50
51     assign hsync = ~(hcount >= 656 & hcount <= 751);
52
53     /*********************************
54     *Vertical count 0-524
55     *********************************/
56     reg [9:0] vcount;
57     wire endv;
```

```
58
59      //assign pixel_y = vcount;
60      assign endv = (vcount == 524);
61
62      always @ (posedge clk, posedge rst)
63         if (rst) vcount <= 10'b0; else
64         if (tick)
65            if(endh)
66               if(endv) vcount <= 10'b0; else
67                        vcount <= vcount + 10'b1;
68
69      assign vsync = ~(vcount >= 490 & vcount <= 491);
70
71      //display would be on when vsync and hsync are "inside" the
72      //vga monitor
73      assign video_on = ((vsync) & (hsync));
74
75   endmodule
76
```