```
1   `timescale 1ns / 1ps
2   /*************************************************************************
3    * File Name: displayController.v
4    * Project: Counter using AISO
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7    * Rev. Date: 20 September, 2017
8    *
9    * Purpose: The asynchronous in syncrhonous out (AISO) is designed to
10   *          produce a synchronized reset from an asynchronous reset.
11   *          The reset output from the aiso is then fed to all the rest
12   *          of the modules for this project. The reset is produced at every
13   *          rising edge of the clock. This module forces two flops to zero
14   *          at a press of the reset button, which tells us the input from 1
15   *          turns to zero at the output producing a synchronous reset.
16   *
17   * Notes:   -  This module has an asynchronous reset input.
18   *
19   *************************************************************************/
20  module aiso(input  clk, rst,
21              output rst_out);
22
23     //local registers
24     reg qMeta, qOk;
25
26     always @(posedge clk, posedge rst)
27        if(rst) begin
28             qMeta <= 1'b0;//reset metastable and stable output
29             qOk <= 1'b0;
30        end
31
32        else begin
33             qMeta <= 1'b1;//metastable gets 1 from button press
34             qOk <= qMeta; //stable gets metastable
35        end
36
37     assign rst_out = ~qOk; //invert the output to produce synchronous out
38
39  endmodule
40
```