```
1   `timescale 1ns / 1ns
2   /*************************************************************************
3    * File Name: vga_sync_tb.v
4    * Project: VGA Sync
5    * Designer: Marc Cabote
6    * Email: marcdominic011@gmail.com
7    * Rev. Date: 11 October, 2017
8    *
9    * Purpose: The purpose of this module is to test if the vga_sync
10   *          will behave the way it is expected to behave. From this
11   *          test we will see that the waveform for vsync will be less
12   *          frequent thatn hsync as expected. This test is used
13   *          for verification specific to the vga_sync module.
14   *
15   *
16   *
17   * Notes:
18   *
19   *
20   *************************************************************************/
21
22  module vga_sync_tb;
23
24     // Inputs
25     reg clk;
26     reg rst;
27
28     // Outputs
29     //wire [9:0] pixel_x;
30     //wire [9:0] pixel_y;
31     wire hsync;
32     wire vsync;
33     wire video_on;
34
35     // Instantiate the Unit Under Test (UUT)
36     vga_sync uut (
37        .clk(clk),
38        .rst(rst),
39        //.pixel_x(pixel_x),
40        //.pixel_y(pixel_y),
41        .hsync(hsync),
42        .vsync(vsync),
43        .video_on(video_on)
44     );
45
46     // initialize clock to always so it will
47     // oscillate the clock source model every 1 clock unit
48     always #1 clk =~clk;
49
50     initial begin
51        //reset high to test reset
52        //notice that clock is set to 0
53        //as reset is asynchronous
54        clk = 0;
55        rst = 1;
56
57        // Wait 1 clock unit for global reset to finish
```

```
58          #1;
59          rst = 0;
60
61
62          // Add stimulus here
63
64      end
65
66
67  endmodule
68
69
```