CECS 360 Project 5 – Simple Timing Presentation

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Introduction

This project is a continuation of the Animated VGA project. From there, we will use timing analysis to consider system timing for our design. The clock edge will then be referenced in order for us to identify the synchronous elements in the design. The delays must be managed in order for us to know if our design would meet the timing constraints before we program it to our boards.

Horizontal Synchronization

The switching characteristics of the hysnc will help me with my timing analysis. The hsync signal will be obtained from a 0-799 counter and a decoding circuit. The counts will then be used to mark the end of the horizontal display indicated by endh. The hsync signal is also specified to be low active from count 656 to 751 and high active from 0 to 639.

Static Timing Analysis

Static timing analysis allows us to generate post-place and route static timing. It gives us a report of the analysis if our design meets the timing constraints. Depending on the input and output timing offsets, max frequency where design works may vary. For example if I put input and output offsets at 3 ns, the maximum frequency where design works is at around 240-250 MHz. However, if no offsets where given, the design runs maximum frequency at approximately 324 MHz—this is based on the negative and positive value; if I increase the frequency it will give me negative results. The thing with static timing analysis, you will have to assume the value for the offset which then changes the maximum frequency the design could run.

Dynamic Timing Analysis

Dynamic timing analysis is a little more thorough than static. When you run your post-route waveform it generates a log file for you where you can see the timing for all elements in your

design. You will also have to look at the waveform to see if your design is functioning properly. Like what I said where in static I ignored the offset for the fact that max frequency changes depending on the offset you set it to. It was also mentioned in class that the max frequency for static and dynamic analysis will be different.

One way to do this without looking at the waveform is make a self-checking test bench which verifies the rgb values. Increasing the clock will then give you errors at some frequency. However, I used the waveform to verify if my design is meeting the timing constraints. If the switching of the hysnc overlaps with the clock then the clock is no longer ideal. By doing this I was able to determine that the max frequency is around 370 MHz.

Conclusion

The static timing analysis was easier to understand than the dynamic analysis. Static timing analysis will also tell you if you are meeting the timing constraints before it even creates the report for you. With the dynamic timing analysis, you have to understand how your waveform works and compare delays based on your clock in order to get the maximum frequency. The two approaches for timing analysis is pretty straightforward but the dynamic timing analysis just needs a little bit of work to understand—it becomes easier the more I simulate the waveforms.