```
1   `timescale 1ns / 1ps
2
3   ////////////////////////////////////////////////////////////////////////////////
4   // Company:
5   // Engineer:
6   //
7   // Create Date:   21:17:36 02/04/2018
8   // Design Name:   tramelblaze_top
9   // Module Name:   F:/Spring2018/CECS460/project1/project1_460/tramelblaze_tb.v
10  // Project Name:  project1_460
11  // Target Device:
12  // Tool versions:
13  // Description:
14  //
15  // Verilog Test Fixture created by ISE for module: tramelblaze_top
16  //
17  // Dependencies:
18  //
19  // Revision:
20  // Revision 0.01 - File Created
21  // Additional Comments:
22  //
23  ////////////////////////////////////////////////////////////////////////////////
24
25  module tramelblaze_tb;
26
27     // Inputs
28     reg CLK;
29     reg RESET;
30     reg [15:0] IN_PORT;
31     reg INTERRUPT;
32
33     // Outputs
34     wire [15:0] OUT_PORT;
35     wire [15:0] PORT_ID;
36     wire READ_STROBE;
37     wire WRITE_STROBE;
38     wire INTERRUPT_ACK;
39
40     // Instantiate the Unit Under Test (UUT)
41     tramelblaze_top uut (
42        .CLK(CLK),
43        .RESET(RESET),
44        .IN_PORT(IN_PORT),
45        .INTERRUPT(INTERRUPT),
46
47        .OUT_PORT(OUT_PORT),
48        .PORT_ID(PORT_ID),
49        .READ_STROBE(READ_STROBE),
50        .WRITE_STROBE(WRITE_STROBE),
51        .INTERRUPT_ACK(INTERRUPT_ACK)
52     );
53
54  // setup clock
55  always #5 CLK = ~CLK;
56
57  //initialize the clock and assert reset
```

```
58
59    initial
60       begin
61       CLK = 0;
62       IN_PORT = 0;
63       INTERRUPT = 0;
64       RESET = 1;
65
66       #100
67       RESET = 0;
68       repeat(10)
69          begin
70
71          #1000
72          @(posedge CLK)
73          INTERRUPT = 1;
74          @(posedge INTERRUPT_ACK)
75          INTERRUPT = 0;
76          end
77       end
78
79    endmodule
80
81
```