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## This file is a general .ucf for the Nexys4 DDR Rev C board
## To use it in a project:
## - uncomment the lines corresponding to used pins
## - rename the used signals according to the project

## Clock signal
NET "clk"   LOC = "E3"  | IOSTANDARD = "LVCMOS33";             #Bank = 35, Pin name =
#IO_L12P_T1_MRCC_35,              Sch name = clk100mhz
NET "clk" TNM_NET = sys_clk_pin;
TIMESPEC TS_sys_clk_pin = PERIOD sys_clk_pin 100 MHz HIGH 50%;


## Switches
#NET "sw<1>"          LOC=J15 | IOSTANDARD=LVCMOS33; #IO_L24N_T3_RS0_15
NET "ohel"          LOC=L16 | IOSTANDARD=LVCMOS33; #IO_L3N_T0_DQS_EMCCLK_14
NET "pen"          LOC=M13 | IOSTANDARD=LVCMOS33; #IO_L6N_T0_D08_VREF_14
NET "eight"          LOC=R15 | IOSTANDARD=LVCMOS33; #IO_L13N_T2_MRCC_14
NET "baud[0]"          LOC=R17 | IOSTANDARD=LVCMOS33; #IO_L12N_T1_MRCC_14
NET "baud[1]"          LOC=T18 | IOSTANDARD=LVCMOS33; #IO_L7N_T1_D10_14
NET "baud[2]"          LOC=U18 | IOSTANDARD=LVCMOS33; #IO_L17N_T2_A13_D29_14
NET "baud[3]"          LOC=R13 | IOSTANDARD=LVCMOS33; #IO_L5N_T0_D07_14
#NET "sw<8>"          LOC=T8 | IOSTANDARD=LVCMOS18; #IO_L24N_T3_34
#NET "sw<9>"          LOC=U8 | IOSTANDARD=LVCMOS18; #IO_25_34
#NET "sw<10>"         LOC=R16 | IOSTANDARD=LVCMOS33; #IO_L15P_T2_DQS_RDWR_B_14
#NET "sw<11>"         LOC=T13 | IOSTANDARD=LVCMOS33; #IO_L23P_T3_A03_D19_14
#NET "sw<12>"         LOC=H6 | IOSTANDARD=LVCMOS33; #IO_L24P_T3_35
#NET "sw<13>"         LOC=U12 | IOSTANDARD=LVCMOS33; #IO_L20P_T3_A08_D24_14
#NET "sw<14>"         LOC=U11 | IOSTANDARD=LVCMOS33; #IO_L19N_T3_A09_D25_VREF_14
#NET "sw<15>"         LOC=V10 | IOSTANDARD=LVCMOS33; #IO_L21P_T3_DQS_14


## Buttons
#NET "cpu_resetn"     LOC=C12 | IOSTANDARD=LVCMOS33; #IO_L3P_T0_DQS_AD1P_15

NET "rst"           LOC=N17 | IOSTANDARD=LVCMOS33; #IO_L9P_T1_DQS_14
#NET "btnd"           LOC=P18 | IOSTANDARD=LVCMOS33; #IO_L9N_T1_DQS_D13_14
#NET "btnl"           LOC=P17 | IOSTANDARD=LVCMOS33; #IO_L12P_T1_MRCC_14
#NET "btnr"           LOC=M17 | IOSTANDARD=LVCMOS33; #IO_L10N_T1_D15_14
#NET "btnu"           LOC=M18 | IOSTANDARD=LVCMOS33; #IO_L4N_T0_D05_14


## LEDs
NET "leds<0>"         LOC=H17 | IOSTANDARD=LVCMOS33; #IO_L18P_T2_A24_15
NET "leds<1>"         LOC=K15 | IOSTANDARD=LVCMOS33; #IO_L24P_T3_RS1_15
NET "leds<2>"         LOC=J13 | IOSTANDARD=LVCMOS33; #IO_L17N_T2_A25_15
NET "leds<3>"         LOC=N14 | IOSTANDARD=LVCMOS33; #IO_L8P_T1_D11_14
NET "leds<4>"         LOC=R18 | IOSTANDARD=LVCMOS33; #IO_L7P_T1_D09_14
NET "leds<5>"         LOC=V17 | IOSTANDARD=LVCMOS33; #IO_L18N_T2_A11_D27_14
NET "leds<6>"         LOC=U17 | IOSTANDARD=LVCMOS33; #IO_L17P_T2_A14_D30_14
NET "leds<7>"         LOC=U16 | IOSTANDARD=LVCMOS33; #IO_L18P_T2_A12_D28_14
NET "leds<8>"         LOC=V16 | IOSTANDARD=LVCMOS33; #IO_L16N_T2_A15_D31_14
NET "leds<9>"         LOC=T15 | IOSTANDARD=LVCMOS33; #IO_L14N_T2_SRCC_14
NET "leds<10>"        LOC=U14 | IOSTANDARD=LVCMOS33; #IO_L22P_T3_A05_D21_14
NET "leds<11>"        LOC=T16 | IOSTANDARD=LVCMOS33; #IO_L15N_T2_DQS_DOUT_CSO_B_14
NET "leds<12>"        LOC=V15 | IOSTANDARD=LVCMOS33; #IO_L16P_T2_CSI_B_14
NET "leds<13>"        LOC=V14 | IOSTANDARD=LVCMOS33; #IO_L22N_T3_A04_D20_14
NET "leds<14>"        LOC=V12 | IOSTANDARD=LVCMOS33; #IO_L20N_T3_A07_D23_14
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57  NET "leds<15>"          LOC=V11 | IOSTANDARD=LVCMOS33; #IO_L21N_T3_DQS_A06_D22_14
58
59
60  ##LEDs_RGB
61  #NET "led16_b"          LOC=R12 | IOSTANDARD=LVCMOS33; #IO_L5P_T0_D06_14
62  #NET "led16_g"          LOC=M16 | IOSTANDARD=LVCMOS33; #IO_L10P_T1_D14_14
63  #NET "led16_r"          LOC=N15 | IOSTANDARD=LVCMOS33; #IO_L11P_T1_SRCC_14
64  #NET "led17_b"          LOC=G14 | IOSTANDARD=LVCMOS33; #IO_L15N_T2_DQS_ADV_B_15
65  #NET "led17_g"          LOC=R11 | IOSTANDARD=LVCMOS33; #IO_0_14
66  #NET "led17_r"          LOC=N16 | IOSTANDARD=LVCMOS33; #IO_L11N_T1_SRCC_14
67
68
69  ## 7 segment display
70  #NET "ca"               LOC=T10 | IOSTANDARD=LVCMOS33; #IO_L24N_T3_A00_D16_14
71  #NET "cb"               LOC=R10 | IOSTANDARD=LVCMOS33; #IO_25_14
72  #NET "cc"               LOC=K16 | IOSTANDARD=LVCMOS33; #IO_25_15
73  #NET "cd"               LOC=K13 | IOSTANDARD=LVCMOS33; #IO_L17P_T2_A26_15
74  #NET "ce"               LOC=P15 | IOSTANDARD=LVCMOS33; #IO_L13P_T2_MRCC_14
75  #NET "cf"               LOC=T11 | IOSTANDARD=LVCMOS33; #IO_L19P_T3_A10_D26_14
76  #NET "cg"               LOC=L18 | IOSTANDARD=LVCMOS33; #IO_L4P_T0_D04_14
77  #NET "dp"               LOC=H15 | IOSTANDARD=LVCMOS33; #IO_L19N_T3_A21_VREF_15
78
79  #NET "an<0>"            LOC=J17 | IOSTANDARD=LVCMOS33; #IO_L23P_T3_FOE_B_15
80  #NET "an<1>"            LOC=J18 | IOSTANDARD=LVCMOS33; #IO_L23N_T3_FWE_B_15
81  #NET "an<2>"            LOC=T9 | IOSTANDARD=LVCMOS33; #IO_L24P_T3_A01_D17_14
82  #NET "an<3>"            LOC=J14 | IOSTANDARD=LVCMOS33; #IO_L19P_T3_A22_15
83  #NET "an<4>"            LOC=P14 | IOSTANDARD=LVCMOS33; #IO_L8N_T1_D12_14
84  #NET "an<5>"            LOC=T14 | IOSTANDARD=LVCMOS33; #IO_L14P_T2_SRCC_14
85  #NET "an<6>"            LOC=K2 | IOSTANDARD=LVCMOS33; #IO_L23P_T3_35
86  #NET "an<7>"            LOC=U13 | IOSTANDARD=LVCMOS33; #IO_L23N_T3_A02_D18_14
87
88
89  ## Pmod Header JA
90  #NET "ja<1>"            LOC=C17 | IOSTANDARD=LVCMOS33; #IO_L20N_T3_A19_15
91  #NET "ja<2>"            LOC=D18 | IOSTANDARD=LVCMOS33; #IO_L21N_T3_DQS_A18_15
92  #NET "ja<3>"            LOC=E18 | IOSTANDARD=LVCMOS33; #IO_L21P_T3_DQS_15
93  #NET "ja<4>"            LOC=G17 | IOSTANDARD=LVCMOS33; #IO_L18N_T2_A23_15
94  #NET "ja<7>"            LOC=D17 | IOSTANDARD=LVCMOS33; #IO_L16N_T2_A27_15
95  #NET "ja<8>"            LOC=E17 | IOSTANDARD=LVCMOS33; #IO_L16P_T2_A28_15
96  #NET "ja<9>"            LOC=F18 | IOSTANDARD=LVCMOS33; #IO_L22N_T3_A16_15
97  #NET "ja<10>"           LOC=G18 | IOSTANDARD=LVCMOS33; #IO_L22P_T3_A17_15
98
99  ## Pmod Header JB
100 #NET "jb<1>"            LOC=D14 | IOSTANDARD=LVCMOS33; #IO_L1P_T0_AD0P_15
101 #NET "jb<2>"            LOC=F16 | IOSTANDARD=LVCMOS33; #IO_L14N_T2_SRCC_15
102 #NET "jb<3>"            LOC=G16 | IOSTANDARD=LVCMOS33; #IO_L13N_T2_MRCC_15
103 #NET "jb<4>"            LOC=H14 | IOSTANDARD=LVCMOS33; #IO_L15P_T2_DQS_15
104 #NET "jb<7>"            LOC=E16 | IOSTANDARD=LVCMOS33; #IO_L11N_T1_SRCC_15
105 #NET "jb<8>"            LOC=F13 | IOSTANDARD=LVCMOS33; #IO_L5P_T0_AD9P_15
106 #NET "jb<9>"            LOC=G13 | IOSTANDARD=LVCMOS33; #IO_0_15
107 #NET "jb<10>"           LOC=H16 | IOSTANDARD=LVCMOS33; #IO_L13P_T2_MRCC_15
108
109 ## Pmod Header JC
110 #NET "jc<1>"            LOC=K1 | IOSTANDARD=LVCMOS33; #IO_L23N_T3_35
111 #NET "jc<2>"            LOC=F6 | IOSTANDARD=LVCMOS33; #IO_L19N_T3_VREF_35
112 #NET "jc<3>"            LOC=J2 | IOSTANDARD=LVCMOS33; #IO_L22N_T3_35
113 #NET "jc<4>"            LOC=G6 | IOSTANDARD=LVCMOS33; #IO_L19P_T3_35
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114   #NET "jc<7>"          LOC=E7 | IOSTANDARD=LVCMOS33; #IO_L6P_T0_35
115   #NET "jc<8>"          LOC=J3 | IOSTANDARD=LVCMOS33; #IO_L22P_T3_35
116   #NET "jc<9>"          LOC=J4 | IOSTANDARD=LVCMOS33; #IO_L21P_T3_DQS_35
117   #NET "jc<10>"         LOC=E6 | IOSTANDARD=LVCMOS33; #IO_L5P_T0_AD13P_35
118
119   ## Pmod Header JD
120   #NET "jd<1>"          LOC=H4 | IOSTANDARD=LVCMOS33; #IO_L21N_T3_DQS_35
121   #NET "jd<2>"          LOC=H1 | IOSTANDARD=LVCMOS33; #IO_L17P_T2_35
122   #NET "jd<3>"          LOC=G1 | IOSTANDARD=LVCMOS33; #IO_L17N_T2_35
123   #NET "jd<4>"          LOC=G3 | IOSTANDARD=LVCMOS33; #IO_L20N_T3_35
124   #NET "jd<7>"          LOC=H2 | IOSTANDARD=LVCMOS33; #IO_L15P_T2_DQS_35
125   #NET "jd<8>"          LOC=G4 | IOSTANDARD=LVCMOS33; #IO_L20P_T3_35
126   #NET "jd<9>"          LOC=G2 | IOSTANDARD=LVCMOS33; #IO_L15N_T2_DQS_35
127   #NET "jd<10>"         LOC=F3 | IOSTANDARD=LVCMOS33; #IO_L13N_T2_MRCC_35
128
129   ##Pmod Header JXADC
130   #NET "xa_n<1>"        LOC=A14 | IOSTANDARD=LVDS; #IO_L9N_T1_DQS_AD3N_15
131   #NET "xa_p<1>"        LOC=A13 | IOSTANDARD=LVDS; #IO_L9P_T1_DQS_AD3P_15
132   #NET "xa_n<2>"        LOC=A16 | IOSTANDARD=LVDS; #IO_L8N_T1_AD10N_15
133   #NET "xa_p<2>"        LOC=A15 | IOSTANDARD=LVDS; #IO_L8P_T1_AD10P_15
134   #NET "xa_n<3>"        LOC=B17 | IOSTANDARD=LVDS; #IO_L7N_T1_AD2N_15
135   #NET "xa_p<3>"        LOC=B16 | IOSTANDARD=LVDS; #IO_L7P_T1_AD2P_15
136   #NET "xa_n<4>"        LOC=A18 | IOSTANDARD=LVDS; #IO_L10N_T1_AD11N_15
137   #NET "xa_p<4>"        LOC=B18 | IOSTANDARD=LVDS; #IO_L10P_T1_AD11P_15
138
139
140   ##VGA Connector
141   #NET "vga_r<0>"       LOC=A3 | IOSTANDARD=LVCMOS33; #IO_L8N_T1_AD14N_35
142   #NET "vga_r<1>"       LOC=B4 | IOSTANDARD=LVCMOS33; #IO_L7N_T1_AD6N_35
143   #NET "vga_r<2>"       LOC=C5 | IOSTANDARD=LVCMOS33; #IO_L1N_T0_AD4N_35
144   #NET "vga_r<3>"       LOC=A4 | IOSTANDARD=LVCMOS33; #IO_L8P_T1_AD14P_35
145
146   #NET "vga_g<0>"       LOC=C6 | IOSTANDARD=LVCMOS33; #IO_L1P_T0_AD4P_35
147   #NET "vga_g<1>"       LOC=A5 | IOSTANDARD=LVCMOS33; #IO_L3N_T0_DQS_AD5N_35
148   #NET "vga_g<2>"       LOC=B6 | IOSTANDARD=LVCMOS33; #IO_L2N_T0_AD12N_35
149   #NET "vga_g<3>"       LOC=A6 | IOSTANDARD=LVCMOS33; #IO_L3P_T0_DQS_AD5P_35
150
151   #NET "vga_b<0>"       LOC=B7 | IOSTANDARD=LVCMOS33; #IO_L2P_T0_AD12P_35
152   #NET "vga_b<1>"       LOC=C7 | IOSTANDARD=LVCMOS33; #IO_L4N_T0_35
153   #NET "vga_b<2>"       LOC=D7 | IOSTANDARD=LVCMOS33; #IO_L6N_T0_VREF_35
154   #NET "vga_b<3>"       LOC=D8 | IOSTANDARD=LVCMOS33; #IO_L4P_T0_35
155
156   #NET "vga_hs"         LOC=B11 | IOSTANDARD=LVCMOS33; #IO_L4P_T0_15
157   #NET "vga_vs"         LOC=B12 | IOSTANDARD=LVCMOS33; #IO_L3N_T0_DQS_AD1N_15
158
159
160   ##Micro SD Connector
161   #NET "sd_sck"         LOC=B1 | IOSTANDARD=LVCMOS33; #IO_L9P_T1_DQS_AD7P_35
162   #NET "sd_reset"       LOC=E2 | IOSTANDARD=LVCMOS33; #IO_L14P_T2_SRCC_35
163   #NET "sd_cd"          LOC=A1 | IOSTANDARD=LVCMOS33; #IO_L9N_T1_DQS_AD7N_35
164   #NET "sd_cmd"         LOC=C1 | IOSTANDARD=LVCMOS33; #IO_L16N_T2_35
165   #NET "sd_dat<0>"      LOC=C2 | IOSTANDARD=LVCMOS33; #IO_L16P_T2_35
166   #NET "sd_dat<1>"      LOC=E1 | IOSTANDARD=LVCMOS33; #IO_L18N_T2_35
167   #NET "sd_dat<2>"      LOC=F1 | IOSTANDARD=LVCMOS33; #IO_L18P_T2_35
168   #NET "sd_dat<3>"      LOC=D2 | IOSTANDARD=LVCMOS33; #IO_L14N_T2_SRCC_35
169
170
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171  ##PWM Audio Amplifier
172  #NET "aud_pwm"          LOC=A11 | IOSTANDARD=LVCMOS33; #IO_L4N_T0_15
173  #NET "aud_sd"           LOC=D12 | IOSTANDARD=LVCMOS33; #IO_L6P_T0_15
174
175
176  ##Accelerometer
177  #NET "acl_miso"         LOC=E15 | IOSTANDARD=LVCMOS33; #IO_L11P_T1_SRCC_15
178  #NET "acl_mosi"         LOC=F14 | IOSTANDARD=LVCMOS33; #IO_L5N_T0_AD9N_15
179  #NET "acl_sclk"         LOC=F15 | IOSTANDARD=LVCMOS33; #IO_L14P_T2_SRCC_15
180  #NET "acl_csn"          LOC=D15 | IOSTANDARD=LVCMOS33; #IO_L12P_T1_MRCC_15
181  #NET "acl_int<1>"       LOC=B13 | IOSTANDARD=LVCMOS33; #IO_L2P_T0_AD8P_15
182  #NET "acl_int<2>"       LOC=C16 | IOSTANDARD=LVCMOS33; #IO_L20P_T3_A20_15
183
184
185  ##Temperature Sensor
186  #NET "tmp_ct"           LOC=B14 | IOSTANDARD=LVCMOS33; #IO_L2N_T0_AD8N_15
187  #NET "tmp_int"          LOC=D13 | IOSTANDARD=LVCMOS33; #IO_L6N_T0_VREF_15
188  #NET "tmp_scl"          LOC=C14 | IOSTANDARD=LVCMOS33; #IO_L1N_T0_AD0N_15
189  #NET "tmp_sda"          LOC=C15 | IOSTANDARD=LVCMOS33; #IO_L12N_T1_MRCC_15
190
191
192  ##USB-RS232 Interface
193  #NET "uart_cts"         LOC=D3 | IOSTANDARD=LVCMOS33; #IO_L12N_T1_MRCC_35
194  #NET "uart_rts"         LOC=E5 | IOSTANDARD=LVCMOS33; #IO_L5N_T0_AD13N_35
195  NET "Tx"    LOC=D4 | IOSTANDARD=LVCMOS33; #IO_L11N_T1_SRCC_35
196  NET "Rx"     LOC=C4 | IOSTANDARD=LVCMOS33; #IO_L7P_T1_AD6P_35
197
198
199  ##Omnidirectional Microphone
200  #NET "m_clk"            LOC=J5 | IOSTANDARD=LVCMOS33; #IO_25_35
201  #NET "m_data"           LOC=H5 | IOSTANDARD=LVCMOS33; #IO_L24N_T3_35
202  #NET "m_lrsel"          LOC=F5 | IOSTANDARD=LVCMOS33; #IO_0_35
203
204
205  ##USB HID (PS/2)
206  #NET "ps2_clk"          LOC=F4 | IOSTANDARD=LVCMOS33; #IO_L13P_T2_MRCC_35
207  #NET "ps2_data"         LOC=B2 | IOSTANDARD=LVCMOS33; #IO_L10N_T1_AD15N_35
208
209
210  ##Quad SPI Flash
211  #NET "qspi_csn"         LOC=L13 | IOSTANDARD=LVCMOS33; #IO_L6P_T0_FCS_B_14
212  #NET "qspi_dq<0>"       LOC=K17 | IOSTANDARD=LVCMOS33; #IO_L1P_T0_D00_MOSI_14
213  #NET "qspi_dq<1>"       LOC=K18 | IOSTANDARD=LVCMOS33; #IO_L1N_T0_D01_DIN_14
214  #NET "qspi_dq<2>"       LOC=L14 | IOSTANDARD=LVCMOS33; #IO_L2P_T0_D02_14
215  #NET "qspi_dq<3>"       LOC=M14 | IOSTANDARD=LVCMOS33; #IO_L2N_T0_D03_14
216
217
218  ##SMSC Ethernet PHY
219  #NET "eth_rxd<0>"       LOC=C11 | IOSTANDARD=LVCMOS33; #IO_L13P_T2_MRCC_16
220  #NET "eth_rxd<1>"       LOC=D10 | IOSTANDARD=LVCMOS33; #IO_L19N_T3_VREF_16
221  #NET "eth_txd<0>"       LOC=A10 | IOSTANDARD=LVCMOS33; #IO_L14P_T2_SRCC_16
222  #NET "eth_txd<1>"       LOC=A8 | IOSTANDARD=LVCMOS33; #IO_L12N_T1_MRCC_16
223  #NET "eth_crsdv"        LOC=D9 | IOSTANDARD=LVCMOS33; #IO_L6N_T0_VREF_16
224  #NET "eth_intn"         LOC=B8 | IOSTANDARD=LVCMOS33; #IO_L12P_T1_MRCC_16
225  #NET "eth_mdc"          LOC=C9 | IOSTANDARD=LVCMOS33; #IO_L11P_T1_SRCC_16
226  #NET "eth_mdio"         LOC=A9 | IOSTANDARD=LVCMOS33; #IO_L14N_T2_SRCC_16
227  #NET "eth_refclk"       LOC=D5 | IOSTANDARD=LVCMOS33; #IO_L11P_T1_SRCC_35
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228   #NET "eth_rstn"        LOC=B3 | IOSTANDARD=LVCMOS33; #IO_L10P_T1_AD15P_35
229   #NET "eth_txen"        LOC=B9 | IOSTANDARD=LVCMOS33; #IO_L11N_T1_SRCC_16
230   #NET "eth_rxerr"       LOC=C10 | IOSTANDARD=LVCMOS33; #IO_L13N_T2_MRCC_16
231
```