```verilog
1     `timescale 1ns / 1ps
2     /**************************************************************************
3      * File Name: baud_decoder.v
4      * Project: UART
5      * Designer: Marc Dominic Cabote
6      * Email: marcdominic011@gmail.com
7      * Rev. Date: 5 May, 2018
8      *
9      * Purpose:Determines the rate of data communication
10     *
11     * Notes:   -  This module has a synchronous reset input.
12     *
13     **************************************************************************/
14    module baud_decoder(input [3:0] baud,
15                        output reg[18:0] k );
16
17
18        always @(*) begin
19            case (baud)
20                4'b0000: k = 333333; //300
21                4'b0001: k = 83333;  //1200
22                4'b0010: k = 41667;  //2400
23                4'b0011: k = 20833;  //4800
24                4'b0100: k = 10417;  //9600
25                4'b0101: k = 5208;   //19200
26                4'b0110: k = 2604;   //38400
27                4'b0111: k = 1736;   //57600
28                4'b1000: k = 868;    //115200
29                4'b1001: k = 434;    //230400
30                4'b1010: k = 217;    //460800
31                4'b1011: k = 109;    //921600
32                default: k = 333333; //300
33            endcase
34        end
35
36    endmodule
37
```