```
1   `timescale 1ns / 1ps
2   /**********************************************************************
3    * File Name: UART_TSI.v
4    * Project: UART_TSI
5    * Designer: Marc Dominic Cabote
6    * Email: marcdominic011@gmail.com
7    * Rev. Date: 14 May, 2018
8    *
9    * Abstract - Top level design of our UART with the TSI block
10   *
11   * Notes:   -  This module has an asynchronous reset input.
12   *
13   **********************************************************************/
14  module UART_TSI(  input clk, rst, Rx, eight, pen, ohel,
15                    input [3:0] baud,
16                    output [15:0] reads, writes,
17                    output [15:0] leds,
18                    output Tx
19                 );
20
21     //=====================================================================
22     // wires to connect UART with the TSI
23     //=====================================================================
24        wire clk_buf, rst_buf, Rx_buf, eight_buf, pen_buf, ohel_buf;
25        wire [3:0] baud_buf;
26        wire [15:0] leds_buf;
27        wire Tx_buf;
28
29
30     //=====================================================================
31     // UART
32     //=====================================================================
33        UART  UART(.clk(clk_buf),
34                   .rst(rst_buf),
35                   .Rx(Rx_buf),
36                   .eight(eight_buf),
37                   .pen(pen_buf),
38                   .ohel(ohel_buf),
39                   .baud(baud_buf),
40                   .reads(reads),
41                   .writes(writes),
42                   .leds(leds_buf),
43                   .Tx(Tx_buf)
44                  );
45
46     //=====================================================================
47     // TSI
48     //=====================================================================
49        TSI      buffer(.clk_i(clk),
50                        .rst_i(rst),
51                        .Rx_i(Rx),
52                        .eight_i(eight),
53                        .pen_i(pen),
54                        .ohel_i(ohel),
55                        .baud_i(baud),
56                        .leds_i(leds_buf),
57                        .Tx_i(Tx_buf),
```

```
58                          .clk_o(clk_buf),
59                          .rst_o(rst_buf),
60                          .Rx_o(Rx_buf),
61                          .eight_o(eight_buf),
62                          .pen_o(pen_buf),
63                          .ohel_o(ohel_buf),
64                          .baud_o(baud_buf),
65                          .leds_o(leds),
66                          .Tx_o(Tx)
67                         );
68
69  endmodule
70
```