```
1   //*************************************************************//
2   //  This document contains information proprietary to the      //
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5   //                                                             //
6   //  Class: CECS 460                                            //
7   //  Project name: TRAMBLAZE PROCESSOR                          //
8   //  File name: tramelblaze_top.v                               //
9   //  Release: 1.0 Release Date 17Feb2016                        //
10  //                                                             //
11  //  Created by John Tramel on 20Feburary2016                   //
12  //  Copyright  2016 John Tramel. All rights reserved.          //
13  //  Copyright  2017 John Tramel. All rights reserved.          //
14  //                                                             //
15  //  Abstract: Top level for TRAMBLAZE processor                //
16  //  Edit history: 2016JAN25 - created                          //
17  //  20FEB - top created for processor and memory               //
18  //          tramelblaze_top                                    //
19  //               - tramelblaze                                 //
20  //               - tramelblaze_mem                             //
21  //                                                             //
22  //  02march2017 release 3.0                                    //
23  //
24  //  In submitting this file for class work at CSULB            //
25  //  I am confirming that this is my work and the work          //
26  //  of no one else.                                            //
27  //                                                             //
28  //  In the event other code sources are utilized I will        //
29  //  document which portion of code and who is the author       //
30  //                                                             //
31  // In submitting this code I acknowledge that plagiarism       //
32  // in student project work is subject to dismissal from the class //
33  //*************************************************************//
34
35  `timescale 1ns/1ns
36
37  module tramelblaze_top (CLK, RESET, IN_PORT, INTERRUPT,
38                          OUT_PORT, PORT_ID, READ_STROBE, WRITE_STROBE, INTERRUPT_ACK);
39
40  input         CLK;
41  input         RESET;
42  input  [15:0] IN_PORT;
43  input         INTERRUPT;
44
45  output [15:0] OUT_PORT;
46  output [15:0] PORT_ID;
47  output        READ_STROBE;
48  output        WRITE_STROBE;
49  output        INTERRUPT_ACK;
50
51  wire   [15:0] INSTRUCTION;
52  wire   [11:0] ADDRESS;
53
54  tramelblaze tramelblaze
55        (
56        .CLK(CLK),
57        .RESET(RESET),
```

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58          .IN_PORT(IN_PORT),
59          .INTERRUPT(INTERRUPT),
60
61          .OUT_PORT(OUT_PORT),
62          .PORT_ID(PORT_ID),
63          .READ_STROBE(READ_STROBE),
64          .WRITE_STROBE(WRITE_STROBE),
65          .INTERRUPT_ACK(INTERRUPT_ACK),
66
67          .ADDRESS(ADDRESS),
68          .INSTRUCTION(INSTRUCTION)
69          );
70
71    tb_rom your_instance_name
72          (
73          .clka(CLK), // input clka
74          .addra(ADDRESS), // input [11 : 0] addra
75          .douta(INSTRUCTION) // output [15 : 0] douta
76          );
77
78    endmodule
79
```