```
1   `timescale 1ns / 1ps
2   /**********************************************************************
3    * File Name: mux_8to1.v
4    * Project: Counter using AISO
5    * Designer: Marc Cabote
6    * Email: marcdominic011@gmail.com
7    * Rev. Date: 20 September 2017
8    *
9    * Purpose: The 8-to-1 Multiplexer module is a combinational logic circuit designed
10   *          to "select" one of eight input data line and transmit one output data
11   *          line. One of the eight input data lines is selected using a 3-bit
12   *          "control". The selected line is transmitted to the output line.
13   *
14   * Notes:   - Only one input data line can be selected at a time.
15   **********************************************************************/
16  module mux_8to1(input      [2:0] select,
17                  input      [3:0] d7, d6, d5, d4, d3, d2, d1, d0,
18                  output reg [3:0] Y
19                  );
20
21     // Execute block if sel or D changes
22     always @( select, d7, d6, d5, d4, d3, d2, d1, d0 ) begin
23           case( select )
24              3'b000:  Y = d7;     // If select is 000, then Y gets d7
25              3'b001:  Y = d6;     // If select is 001, then Y gets d6
26              3'b010:  Y = d5;     // If select is 010, then Y gets d5
27              3'b011:  Y = d4;     // If select is 011, then Y gets d4
28              3'b100:  Y = d3;     // If select is 100, then Y gets d3
29              3'b101:  Y = d2;     // If select is 101, then Y gets d2
30              3'b110:  Y = d1;     // If select is 110, then Y gets d1
31              3'b111:  Y = d0;     // If select is 111, then Y gets d0
32              default: Y = 4'b0;   // Default Case
33           endcase
34     end
35
36  endmodule
37
```