```
1   `timescale 1ns / 1ps
2   /**********************************************************************
3    * File Name: srflop.v
4    * Project: Counter using TramelBlaze
5    * Designer: Marc Cabote
6    * Email: marcdominic011@gmail.com
7    * Rev. Date: 8 February, 2018
8    *
9    * Purpose: An SR Flop is an arrangement of logic gates that maintains a
10   *          stable output even after the inputs are turned off.  This simple
11   *          flip flop circuit has a set input (S) and a reset input (R).
12   *
13   * Notes:   -  This module has a synchronous reset input.
14   *
15   **********************************************************************/
16  module srflop(input clk, rst, s, r,
17                output reg srOut);
18
19
20     always @(posedge clk, posedge rst)
21        if(rst) srOut <= 1'b0; else
22        if(s)   srOut <= 1'b1; else
23        if(r)   srOut <= 1'b0;
24        else    srOut <= srOut;//not really needed
25
26
27  endmodule
28
```