```
1
     `timescale 1ns / 1ps
     /************************
 2
     * File Name: displayController.v
 3
 4
      * Project: Counter using TramelBlaze
     * Designer: Marc Cabote
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 6
 7
      * Rev. Date: 20 September, 2017
 8
      * Purpose: The Display Controller module is a top-level sequential logic circuit
9
                designed to display a 4-bit hexidecimal input on the Nexys4 DDR seven-
10
                segment display. This module consists of an LED Clock module used to
11
12
                reduce the incoming clock frequency of the Nexys4 DDR board clock, an LED
1.3
                Controller module used to cycle between turning on one of eight anodes
14
                of the seven-segment display, an 8-to-1 Multiplexer module used to select
15
                which data to display on each anode of the seven-segment display, and a
                Hex-to-7-Segment module used to convert the 4-bit hexidecimal input to a
16
17
                7-bit segment output.
18
19
      * Notes:
              - This module has a synchronous reset input coming from the AISO.
     ************************
2.0
21
    module displayController(input
                                    clk, rst,
22
                             input
                                    [3:0] seg7, seg6, seg5, seg4, seg3, seg2, seg1, seg0,
23
                             output a7, a6, a5, a4, a3, a2, a1, a0,
2.4
                                     a, b, c, d, e, f, g
25
                             );
26
2.7
                           // Connects led clk to led controller
       wire
                  clk out;
28
       wire [2:0] seg sel; // Connects led controller to mux 8to1
                           // Connects mux_8to1 to hex to 7seg
29
       wire [3:0] Y;
30
31
       wire tick;
32
       reg[16:0] count;
33
34
35
       // Module instantiations for creating the Display Controller
36
                           m0 (rst, clk, clk out);
       //led clk
37
38
       39
       // counter to generate 1KHz clock
40
       assign tick = (count == 99999); //tick will then be fed to led controller clock
41
42
         //assign tick = clk;
43
       always @ (posedge clk, posedge rst)
          if (rst) count <= 17'b0; else</pre>
44
45
          if (tick) count <= 17'b0; else //check if tick is 1</pre>
                    count <= count + 17'b1; //increment count</pre>
46
47
48
49
       // Module instantiations for creating the Display Controller
50
       //led clk
                           m0 (reset, clk, clk out);
51
                        m1 (tick, rst, a7, a6, a5, a4, a3, a2, a1, a0, seg sel);
52
       led controller
53
                        m2 (seg sel, seg7, seg6, seg5, seg4, seg3, seg2, seg1, seg0, Y);
       mux 8to1
54
       hex to 7seg
                       m3 (Y, a, b, c, d, e, f, g);
5.5
56
     endmodule
57
```