

```
1  `timescale 1ns / 1ps
2  /*****
3   * File Name: reg16.v
4   * Project: Counter using TramelBlaze
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7   * Rev. Date: 8 February, 2018
8   *
9   * Purpose: This 16-Bit Register module is a sequential logic circuit designed
10  *           to load and store a 16-bit binary value. When the load input is active,
11  *           the stored 16-bit data is transmitted to one of two output busses. When
12  *           the load input is inactive, then the 16-bit data remains in the register.
13  *           The selected output bus is determined by two enable inputs; there is one
14  *           enable input for each output bus. When the enable input for one output bus
15  *           is active, the data is transmitted to the corresponding output bus. If
16  *           this module shares the same output bus with other registers, then the outputs
17  *           of those registers enter a high-impedence state which isolates them from the
18  *           same output bus. This prevents the register from transmitting more than one
19  *           output to the output bus at a time.
20  *
21  * Notes:   - This module has an asynchronous reset input.
22  *           - This module has a tri-state output.
23  *****/
24  module reg16(input clk, rst, ld,
25               input [15:0] d,
26               output reg [15:0] q);
27
28      always @(posedge clk, posedge rst)
29          if (rst)
30              q <= 16'b0; else
31              if (ld)
32                  q <= d; //if load is high
33              else
34                  q <= q; //default
35
36
37
38  endmodule
39
```