```
1   `timescale 1ns / 1ps
2   /**********************************************************************
3    * File Name: ped.v
4    * Project: Counter using AISO
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7    * Rev. Date: 20 September, 2017
8    *
9    * Purpose: The positive edge detect(PED) creates and sends out a pulse to
10   *          the counter. The pulse fed to the counter adjusts the output
11   *          value depending on the up-high down-low switch. The signal is
12   *          coming from the output of the debounce to determine if it will
13   *          send a pulse. The pulse is driven by two flops with one output
14   *          being high (AND)ed with the other output being low; hence the
15   *          inverter on the (AND) gate.
16   *
17   * Notes:   -  This module has an synchronous reset input coming from the AISO.
18   *          -  Signal is coming from the debounce module:
19   *             if signal is 1 q1 gets 1 and q2 gets 0 producing the pulse
20   **********************************************************************/
21  module ped(input   clk, rst, signal,
22             output  pulse);
23
24     //local registers
25     reg q1, q2; //q1-level; q2-delayReg
26
27     always @(posedge clk, posedge rst)
28        if(rst) begin
29             q1 <= 1'b0;//q1 and q2 gets reset
30             q2 <= 1'b0;
31        end
32
33        else begin
34             q1 <= signal; //q1 gets signal
35             q2 <= q1;     //q2 gets q1
36        end
37
38     assign pulse = q1 & ~q2;//AND gate for a Positive Edge Detect Output
39
40
41
42  endmodule
43
```