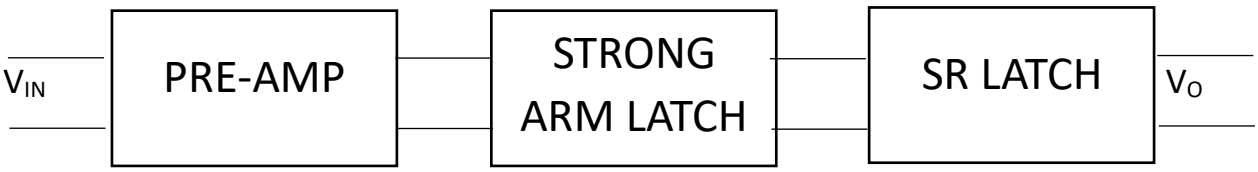
COMPARATOR

- **Eniyan E (230121020)**
- **Swayam Naik (230121060)**

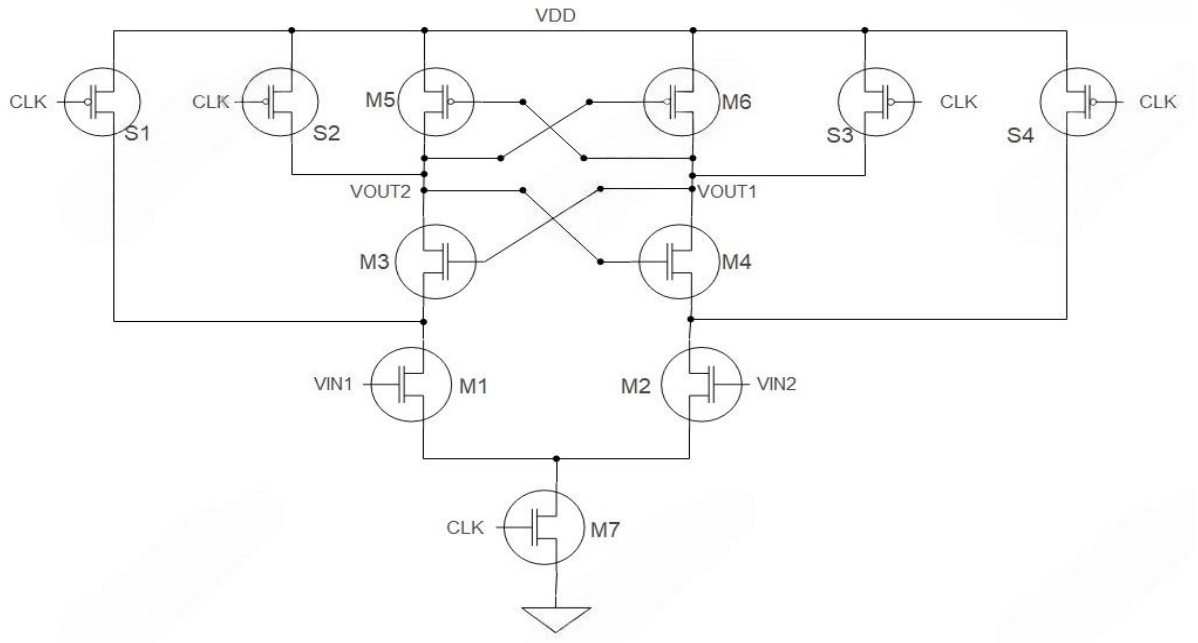
Designed on 180nm CMOS Process

Operates on clock frequency of 100MHz

BLOCK DIAGRAM:



STRONG ARM LATCH:



The Strong Latch works based on the regenerative action and produces rail to rail output.

It offers low dynamic offset.

It consumes zero static power.

The input referred offset of the circuit is majorly due to the differential pair. The offset due to the mismatch of the other transistors are divided by the gain of the differential pair which reduces the contribution (M3, M4, M5, M6).

Design of M7:

* Taking the overdrive of the Diff pair as 0.3V

$V_{DS7} = V_{S(diff\ pair)} = V_{in_1} - V_{GS_1}$

$V_{GS1} = V_T + \Delta V = 0.5V + 0.3V = 0.8V$

The common mode voltage is Taken to be $0.9V = V_{in_1}$

$V_{DS7} = 0.9V - 0.8V = 0.1V$

$V_{GS7} = 1.8V$ (when the clk is High)

The transistor will be in Triode region ($V_{DS} < V_{GS} - V_T$)

So, $I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (2(V_{GS} - V_T)^2 V_{DS} - V_{DS}^2)$

Taking the width as 4 μm

$I_D = \frac{300}{2} \times \frac{4}{0.18} (2 \times (1.3)^2 \times 0.1 - 0.01)$

$I_D \approx 0.83 \mu m$

$\boxed{W_7 = 4\mu m \ ; \ L_7 = 0.18\mu m}$

Design of Differential pair:

$Gain = \frac{2\, g_{m1,2}\, V_{Th\,3,4}}{I_{tail}}$ [Taking a gain of 15]

$15 = \frac{2 \times g_{m1,2} \times 0.5}{0.8}$

$g_{m1,2} = 12mS$

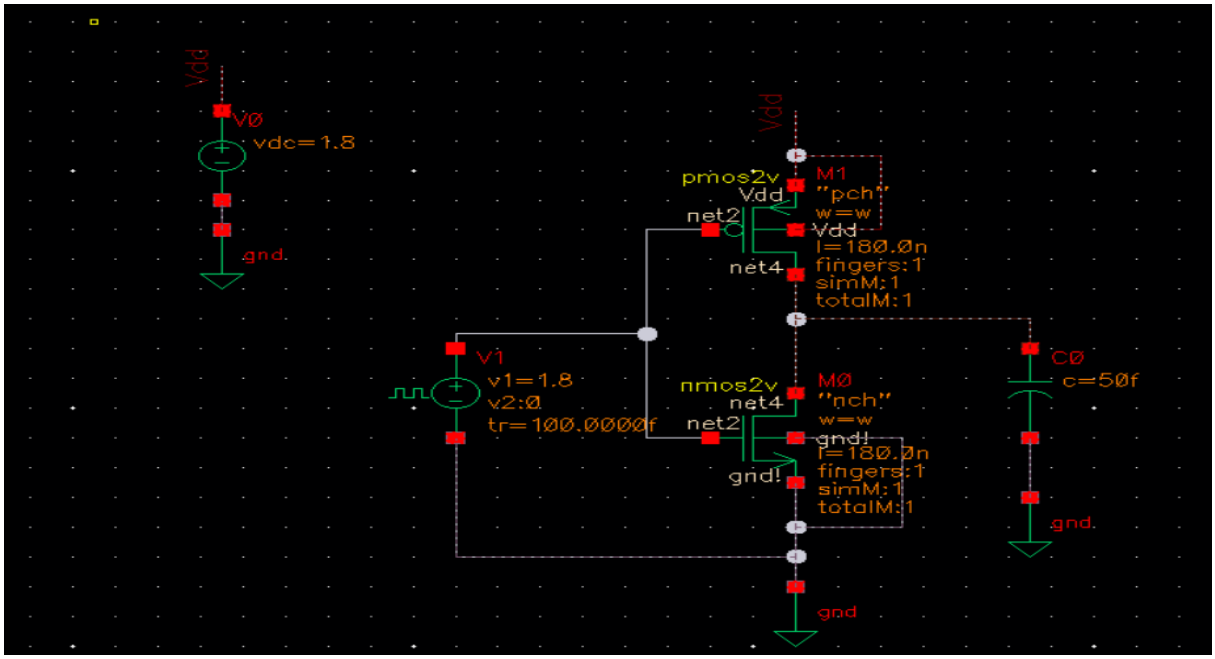
$\mu_n C_{ox} \left(\frac{W}{L}\right)_{1,2} \Delta V = 12 \times 10^{-3} \Rightarrow 300 \times \left(\frac{W}{L}\right)_{1,2} \times 0.3 = 12 \times 10^{-3}$

$\left(\frac{W}{L}\right)_{1,2} = \frac{400}{3}$

$\boxed{W = 24\mu m \ ; \ L = 0.18\mu m}$

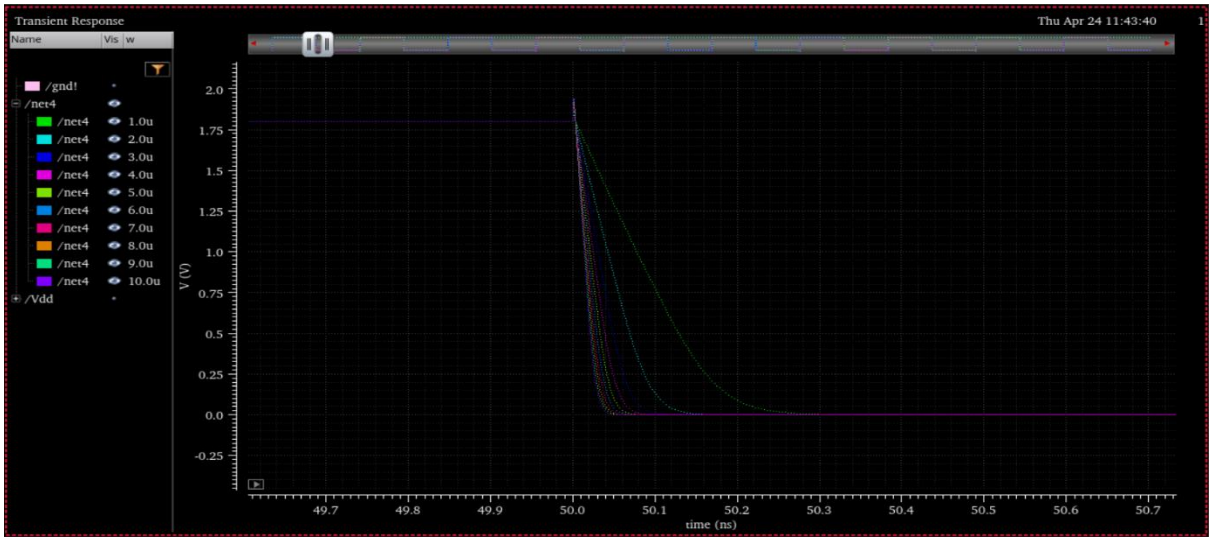
Design of Remaining Transistors:

To meet the speed specifications, we simulated an inverted with both the transistors having a length of 180nm (to reduce parasitics improve the speed of the circuit) and ran a parametric analysis by varying the width of both the transistors and checked the Rise time & Fall time of the Output. The input to the inverter is square wave with a frequency of 100MHz. The inverter is loaded by a 50fF capacitor.

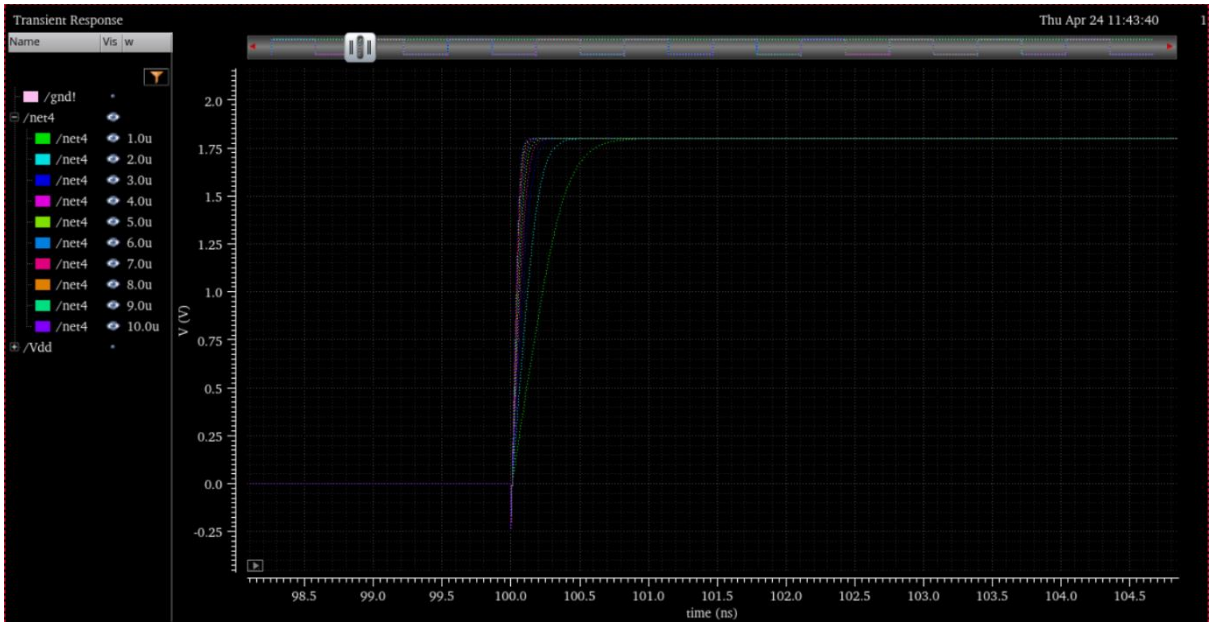


The width is chosen as 7um

The Average fall time was around 20ps



The average rise time was around 47ps

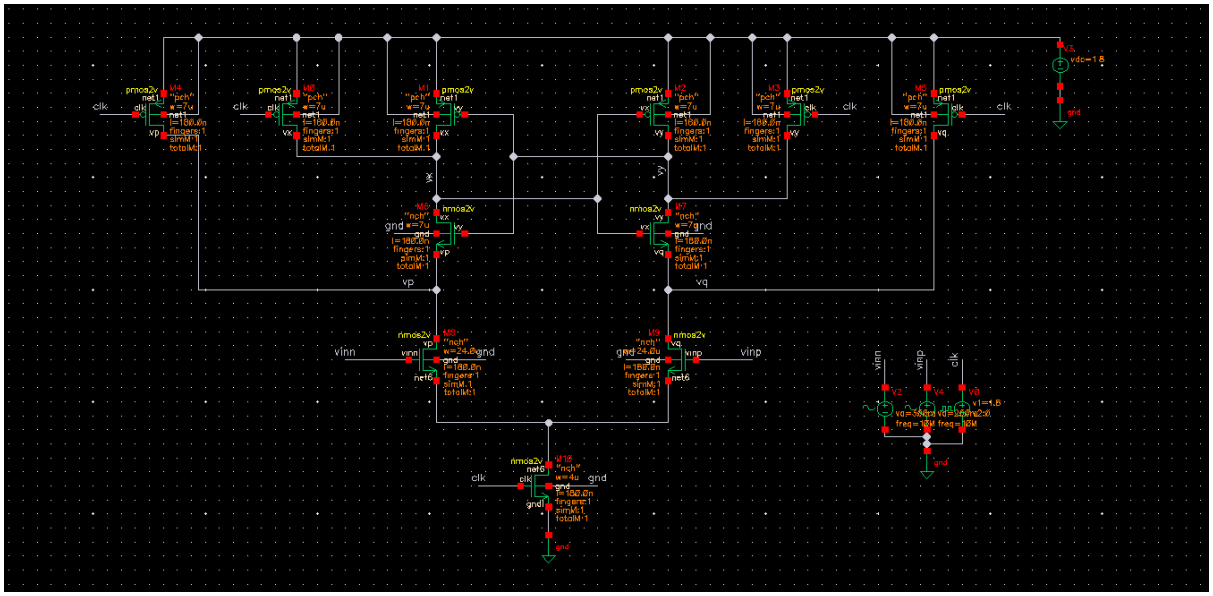


The Switches S1, S2, S3, S4 should pull their drain to VDD within 5ns to complete the resetting of the nodes to x, y, p, q to reduce the dynamic offset and make the comparator ready for the next comparison.

The change in the threshold value is given by the relation

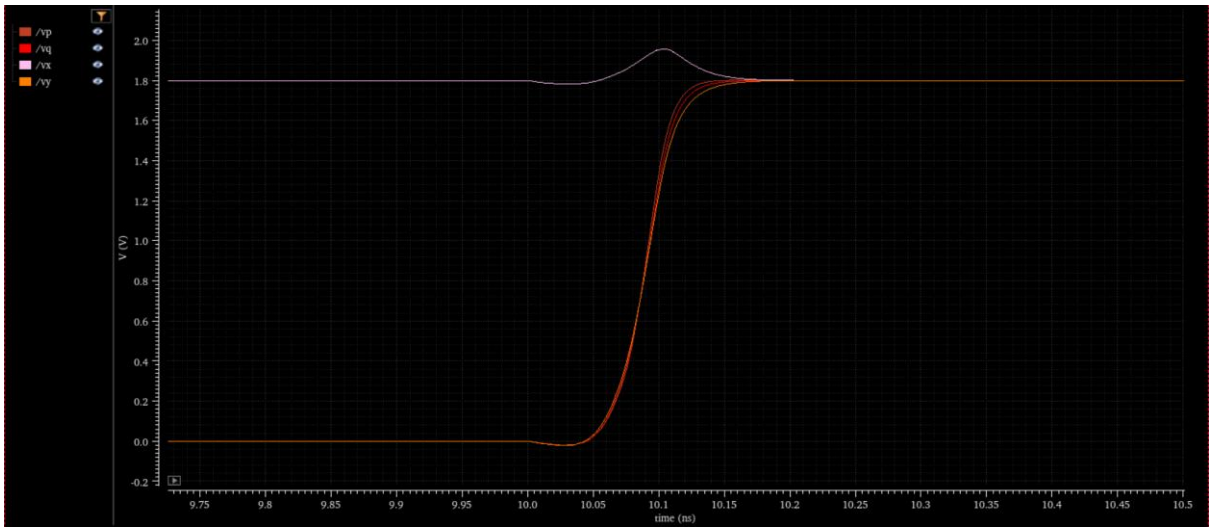
$$\Delta V_{TH1,2} = \frac{A_{VTH}}{\sqrt{(WL)_{1,2}}},$$

So, this is considered while choosing the value of the width of the cross coupled pairs.

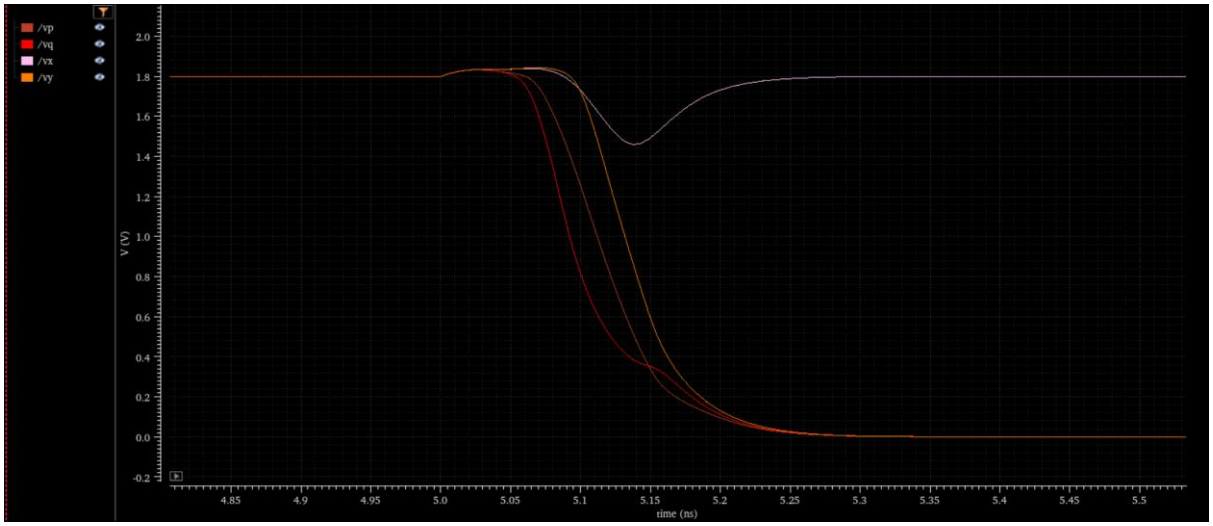


Simulation Results:

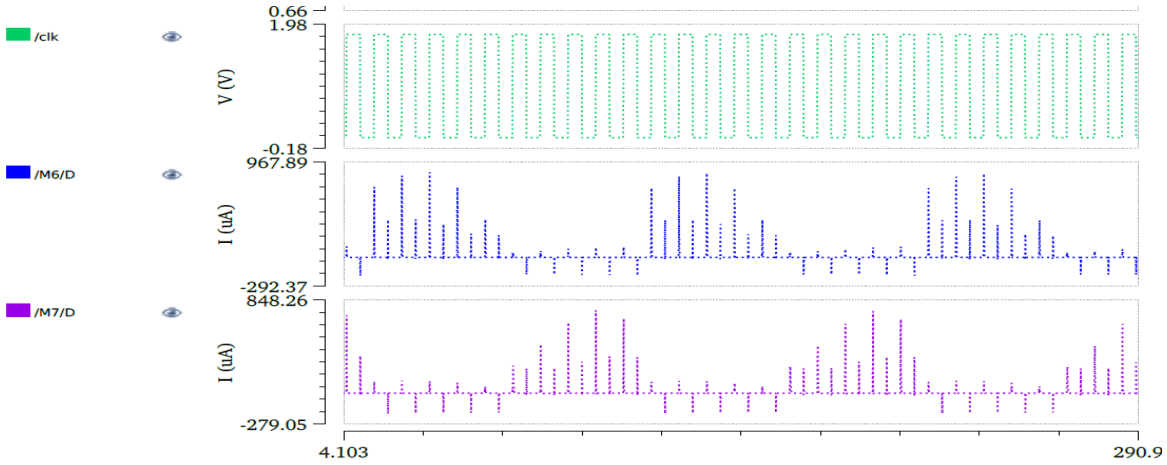
During the resetting phase (when the clock is low after a comparison)



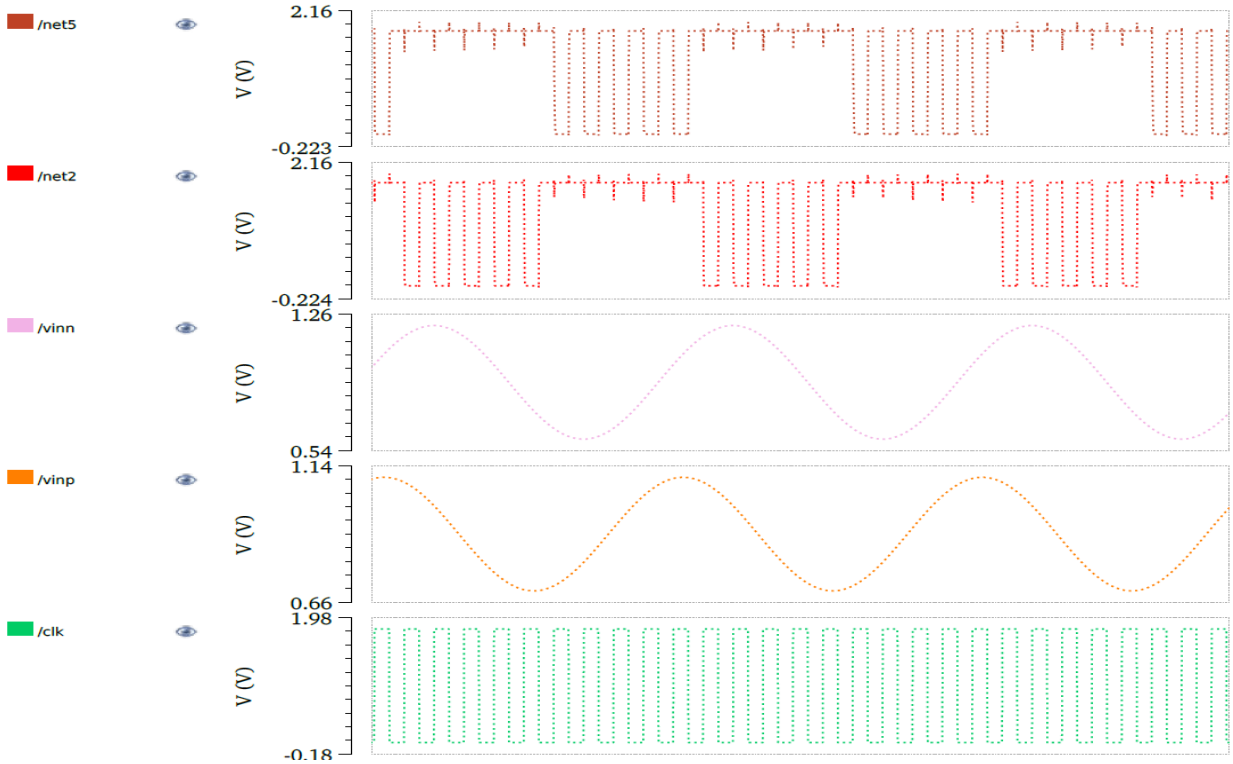
The Comparing action



This plot shows that current through the circuit only for a very short duration after the



rising edge.

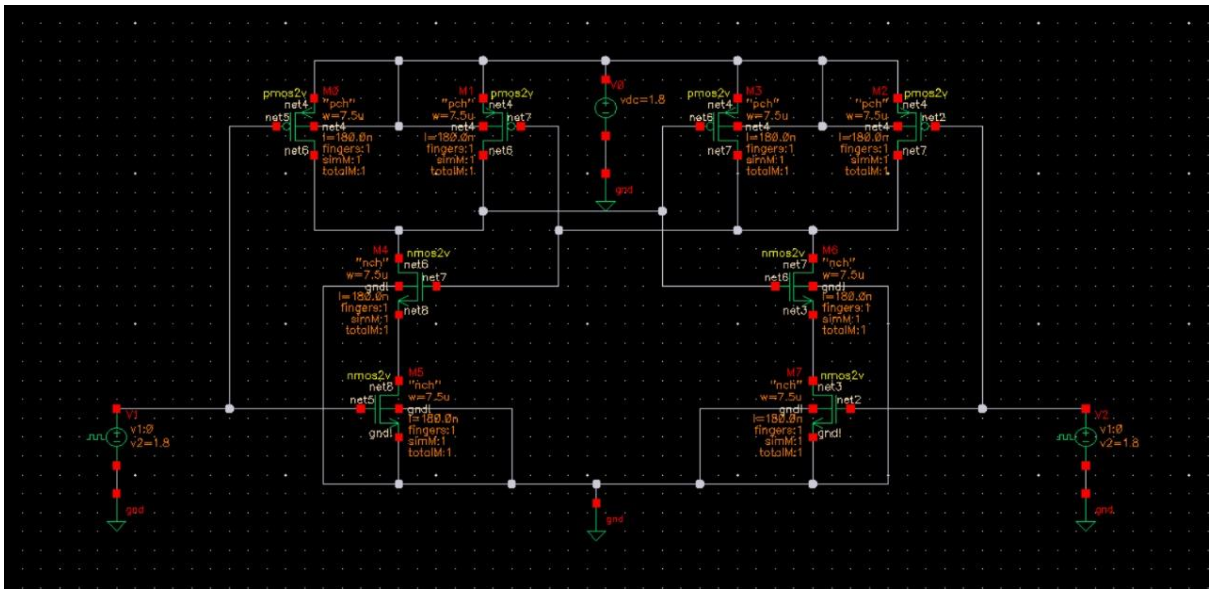


SR latch:

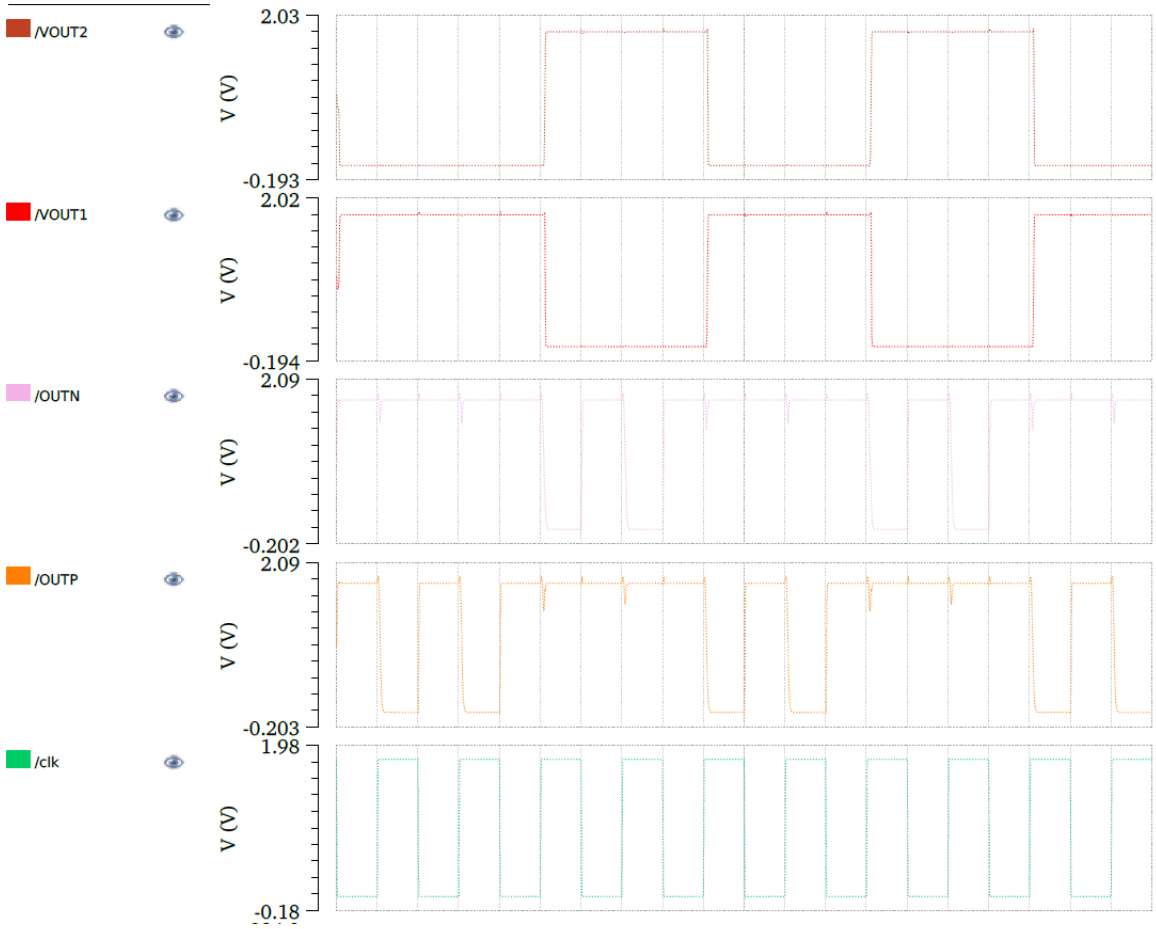
This is a NAND gate based SR latch.

The SR Latch cascaded with the Strong-Arm Latch to store the output (after the comparison) because when the clock goes low both the output reaches VDD and the Latch the stores the output of the previous comparison till the next pulse and it goes the memory state.

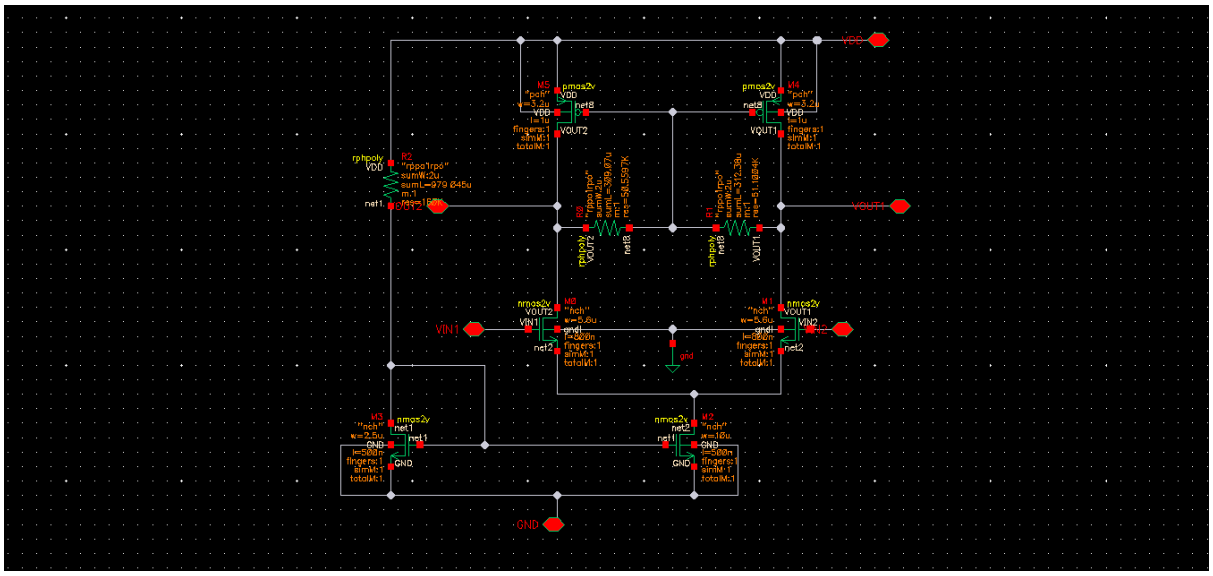
The length of all the transistors is set to 180nm and the width is set to 7.5µm. This value is obtained from the simulation of the inverter.



Simulation with the Strong-Arm Latch:

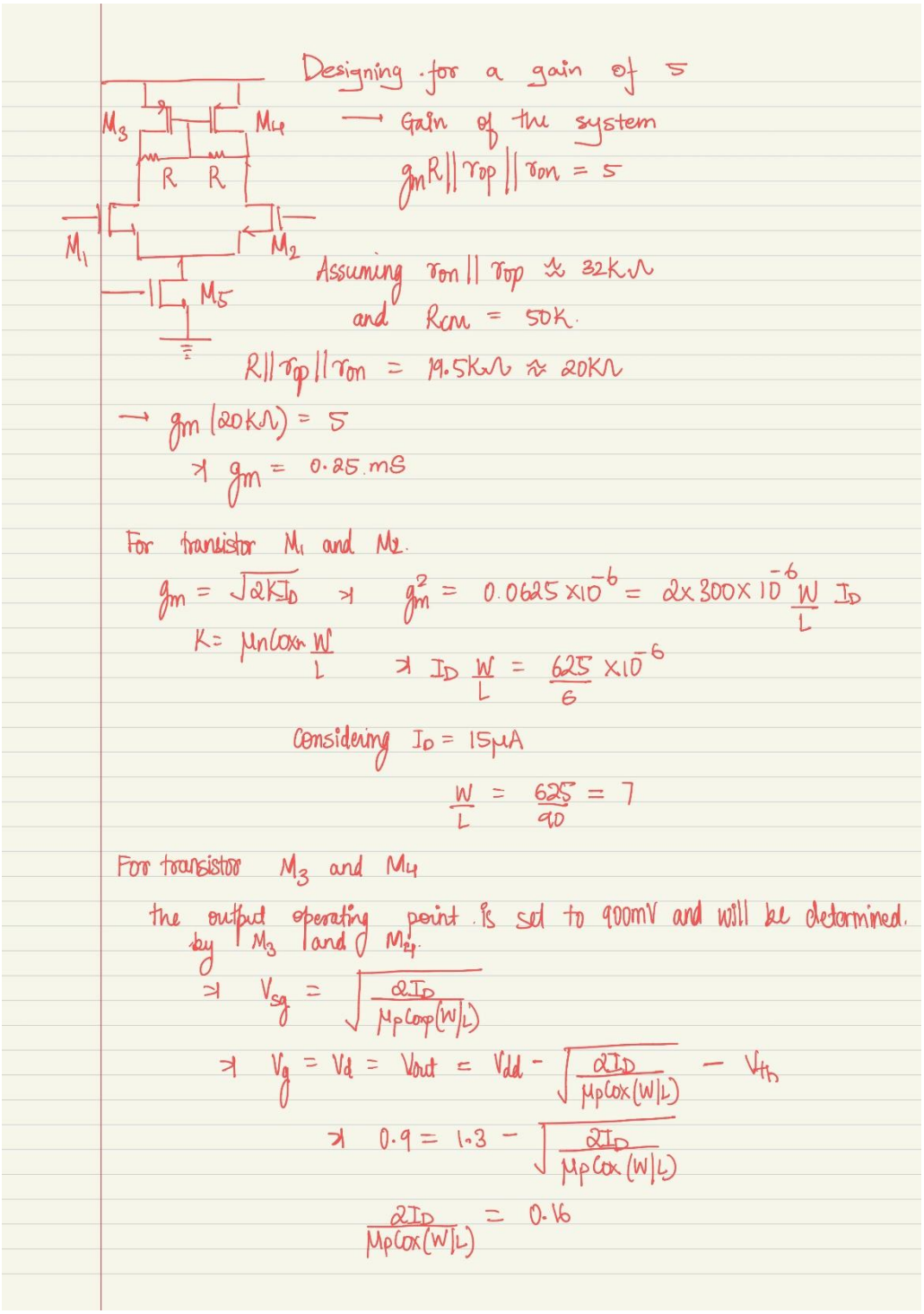


PRE AMPLIFER:



One of the main issues with the Strong Arm Latch is its offset. To minimise this offset we use a Pre-Amp. Now we can model the offset of the SA-Latch as an input signal which divides the original value by the gain of the Preamp. Here we have used a Common Mode Feedback Amplifier so that we can set all the DC voltages to a set value.

Design Procedure:



$$\frac{2 \times 15}{\frac{150}{10} \times W/L} = 0.16$$

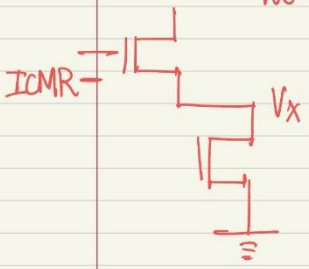
$$W/L = \frac{2}{1.6} = 1.25 \approx 1.5$$

The overdrive voltage of M_1 and M_2

$$15 \times 10^{-6} = \frac{1}{2} \times 300 \times 10^{-6} \times 7 \times (\Delta V)^2$$

$$\Delta V = \sqrt{1/70} = 0.12\ V$$

For M_5 we need M_1 and M_2 in Saturation.



Consider ICMR − as 0.7.

therefore $V_x = ICMR - - \Delta V$

$$\Rightarrow V_x = 0.7 - 0.12$$

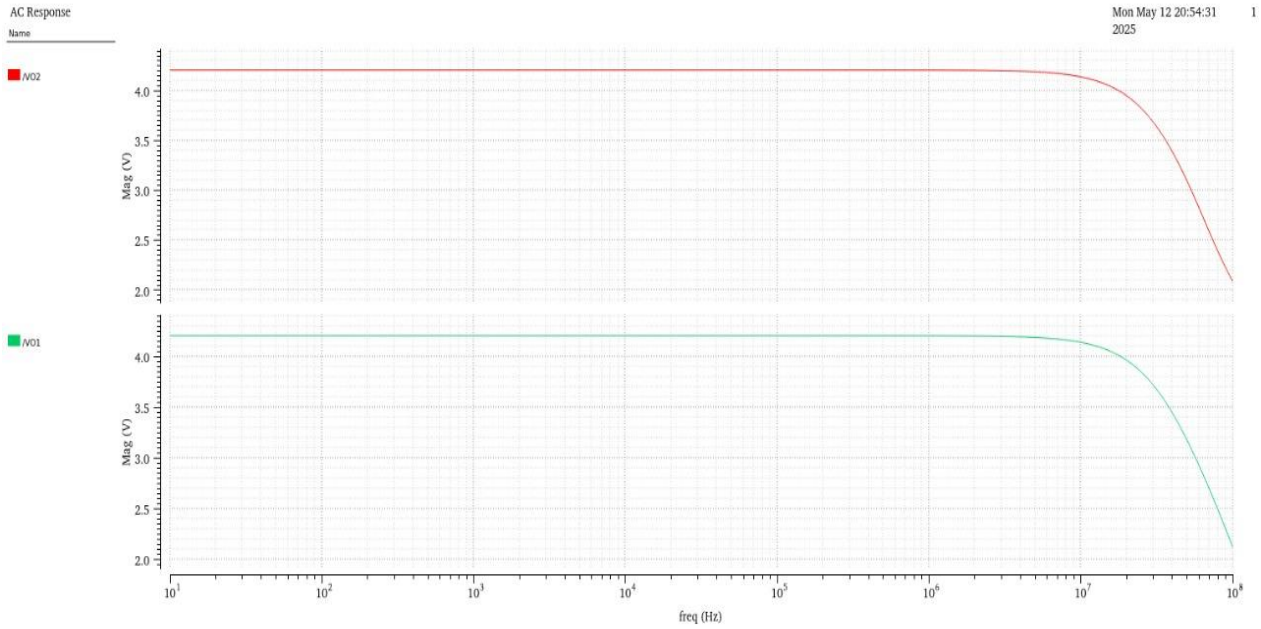
$$= 0.58 \approx 0.6V$$

$$\Rightarrow I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (\Delta V)^2$$

$$30 \times 10^{-6} = \frac{1}{2} \times 300 \times 10^{-6} \times \frac{W}{L} (0.6 - 0.5)^2$$

$$\frac{W}{L} = \frac{100}{5} = 20$$

AC analysis:

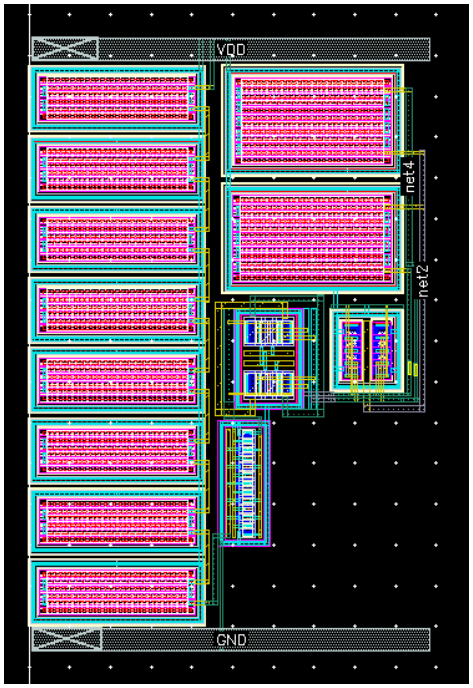


The Gain is around 4.2(Magnitude).

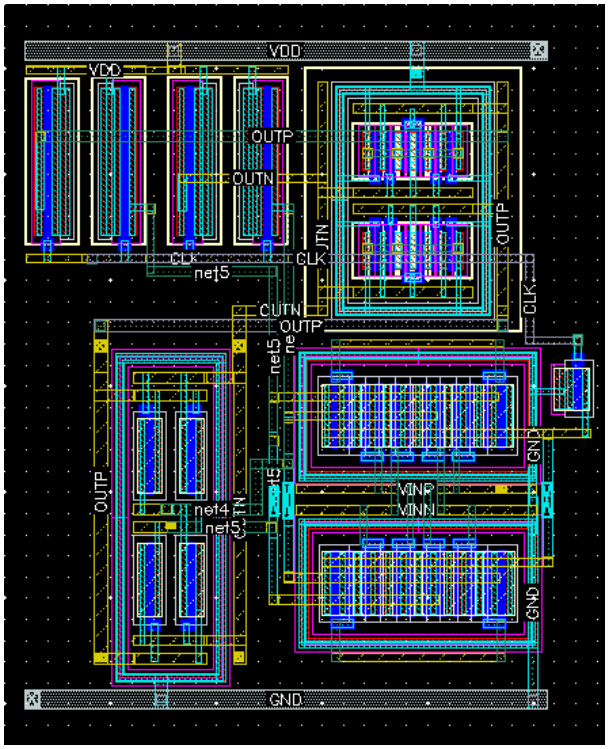
Layouts:

Common Centroid matching technique is used to match the transistors in all the layouts.

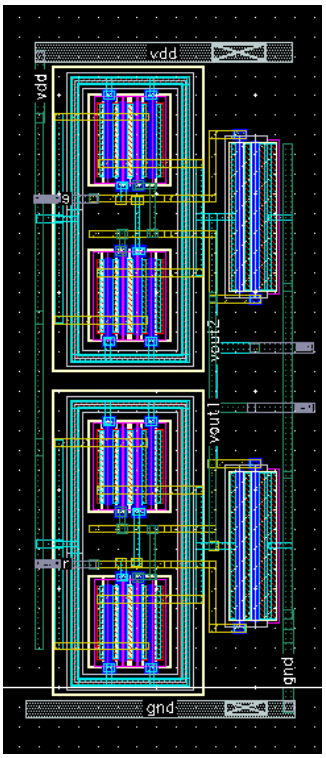
Pre Amplifier:



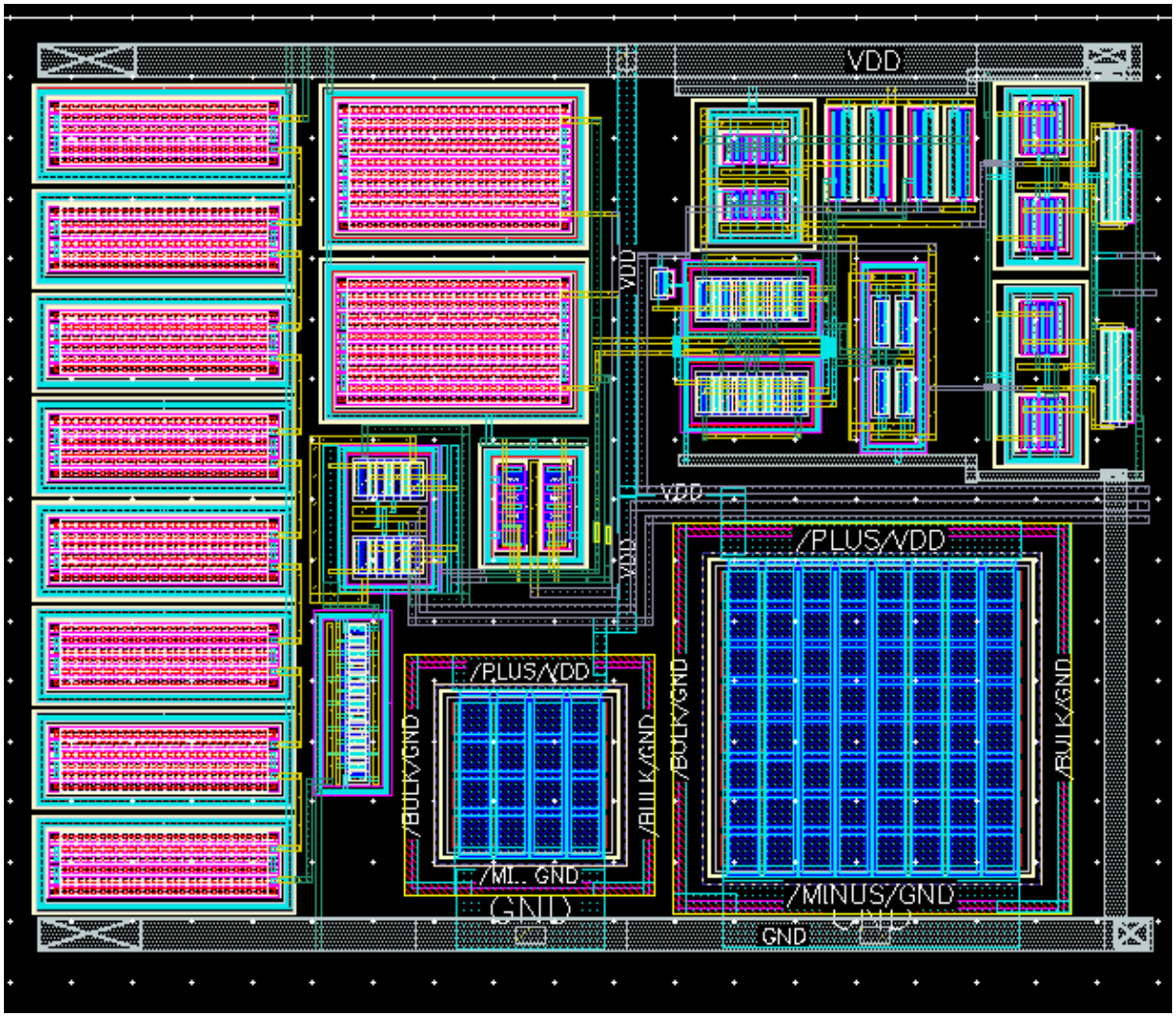
Strong Arm Latch:



SR Latch:



OVERALL:


VDD
VDD
VDD
VDD
/PLUS/VDD
/PLUS/VDD
/BULK/GND
/BULK/GND
/BULK/GND
/BULK/GND
/ML_GND
GND
/MINUS/GND
GND