इलेक्ट्रॉनिकी एवं
सूचना प्रौद्योगिकी मंत्रालय
MINISTRY OF
ELECTRONICS AND
INFORMATION TECHNOLOGY
सत्यमेव जयते

Digital India
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ANALOG and DIGITAL HACKATHONS
Under C2S Programme

Team FETManiacs

IIT GUWAHATI

Bandgap Current Reference (BGCR)

The objective of this design is to develop a bandgap current reference circuit that maintains a stable output current across a wide temperature range, from -40°C to 125°C, with low power consumption and excellent load regulation.

Specifications

Output Current : 100 μA +- 5% across the temperature range of -40°C to 125°C.
Technology : 90nm CMOS process
Power Supply : 1.8V to 3.3V
Power Consumption: Less than 50 μW for the entire current reference circuit.
Temperature Coefficient : Less than 50 ppm/°C for the output current.
Load Regulation : Output current should remain stable within 2% when the load voltage varies from 0 to 1V.

Design Considerations:

- Use a bandgap voltage reference to set the bias current.
- Design a current mirror to generate the output current.
- Consider process variations, transistor matching, and temperature stability in the 90nm process.

Device Characterization

NMOS (n18_t)	PMOS (p18_t)
$\mu_n C_{ox} = 428.7\ \mu A/V^2$	$\mu_p C_{ox} = 192.2\ \mu A/V^2$
$V_{tn} = 0.329\ V$	$V_{tp} = 0.24$

NMOS

File View Results Window Help

ISOURCE | MOS | VSRC | NET

Filter results... | Advanced sorting... | (Showing 1 of 1) | Show Advanced Filters

	gd	cgg	cgs	css	gds	gm	gmbs	ib	id	ids	ig	is	region	ueff	vbs	vds	vdsat	vgs	vth
1	52f	1.74919f	1.21836f	1.47672f	3.65127u	0.110281m	14.9828u	-11.6a	10u	10u	0	-10u	1	52.5941m	0	0.479267	0.148602	0.479267	0.329414

PMOS

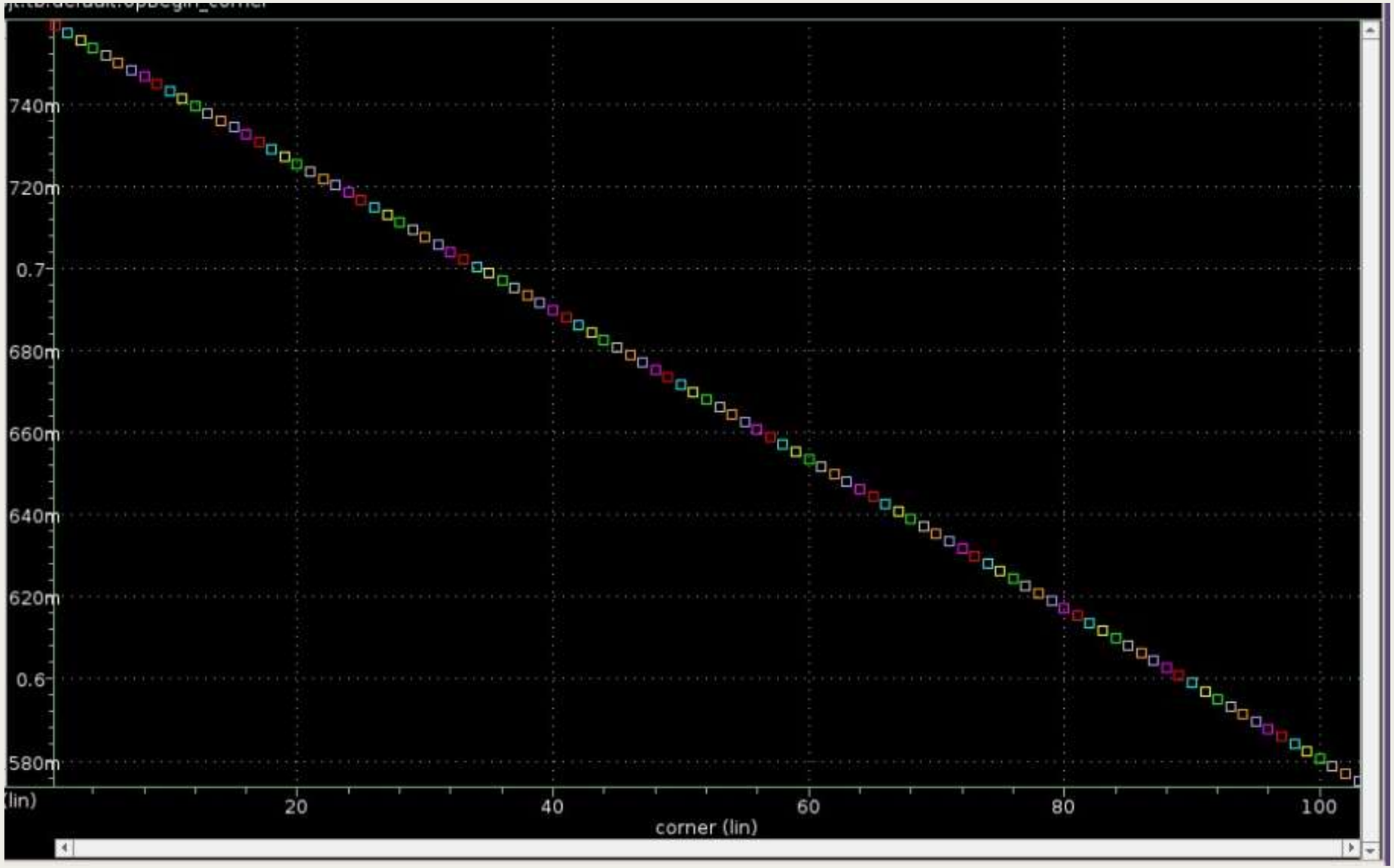
File View Results Window Help

ISOURCE | MOS | VSRC | NET

Filter results... | Advanced sorting... | (Showing 1 of 1) | Show Advanced Filters

	gd	cgg	cgs	css	gds	gm	gmbs	ib	id	ids	ig	is	region	ueff	vbs	vds	vdsat	vgs	vth
1	44f	1.79922f	1.28005f	1.56056f	2.82371u	66.1103u	11.1886u	-88.261f	-10u	-10u	0	10u	1	19.4719m	-0.229616	-0.547493	-0.242633	-0.547493	-0.293117

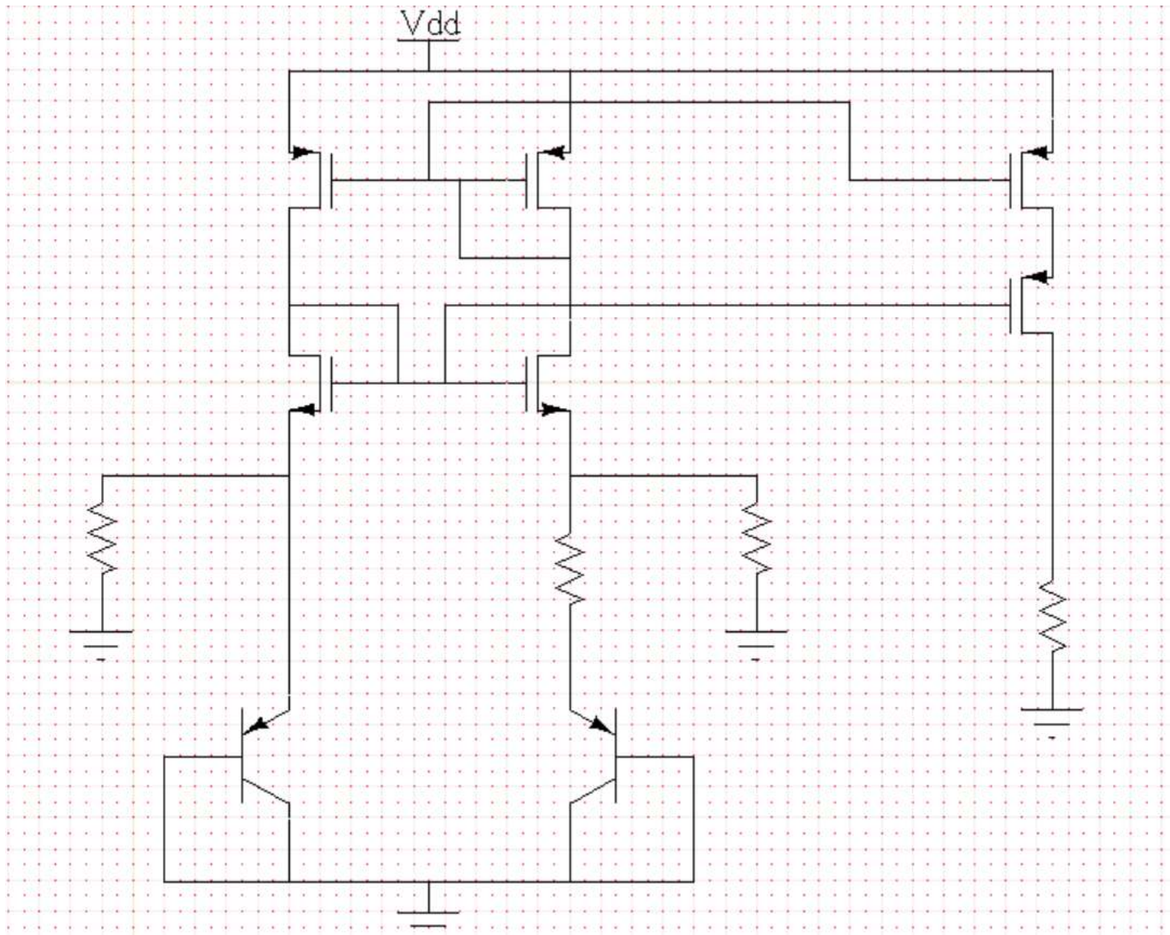
Temperature coefficient of V_{be} of VPNP $= 1.8\ mV/K$



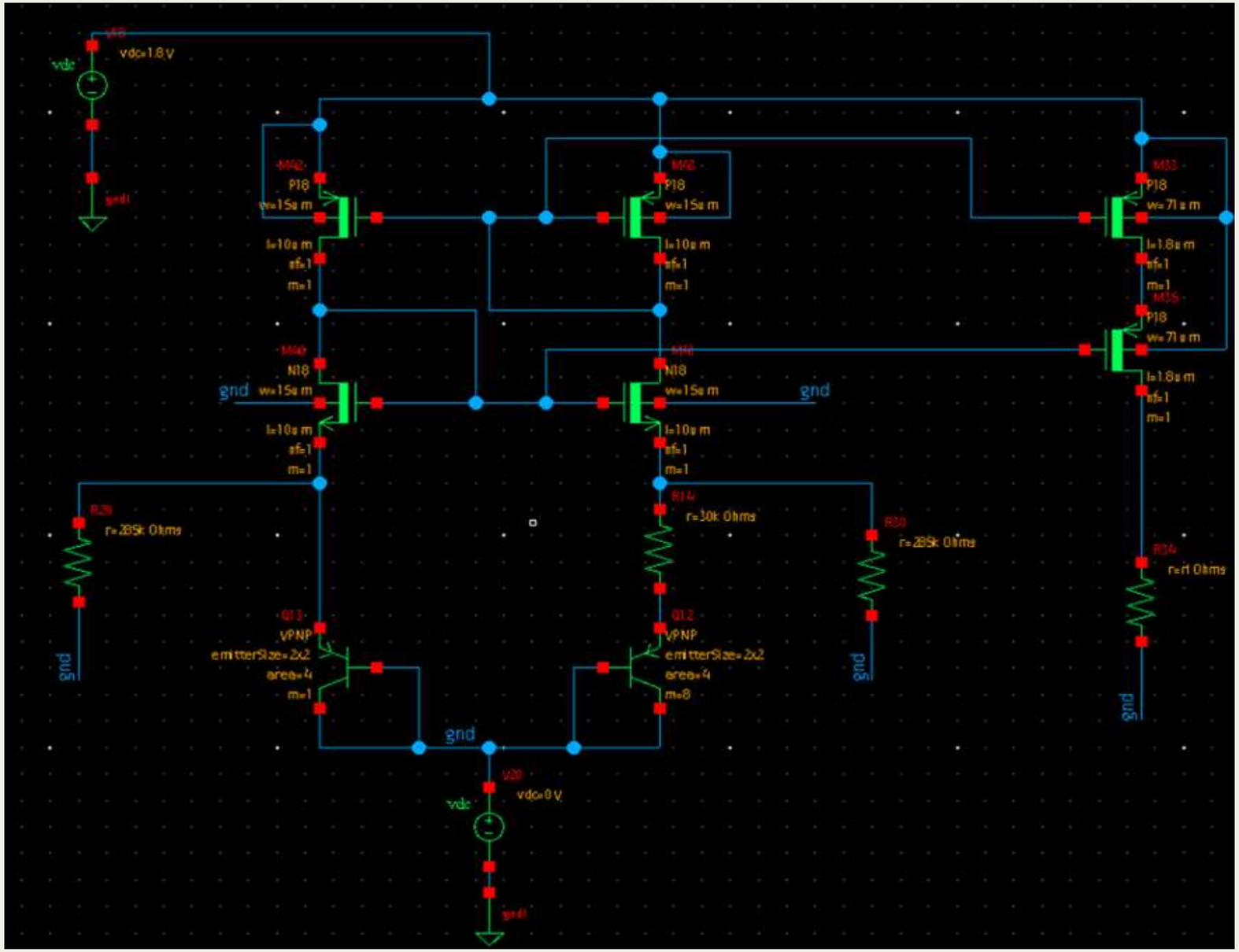
Design

The design employs a Bandgap Voltage Reference that is converted into a current reference by adding appropriate resistors to add a CTAT current to a PTAT current and mirroring the temperature independent current using a cascode current mirror to improve load regulation.

Design Schematic



Design Schematic



Design Flow

The first choice we made was for $n = 8$, so that we could use a 3×3 cube to match the PNP transistors in the layout.

Next, we chose the value of resistor R_1. We assumed a nominal current value of $2\,\mu\text{A}$, so

$$V_1 - V_n = V_T \ln(n),$$

and we calculated

$$R_1 = \frac{26\,\text{mV} \cdot \ln(8)}{2\,\mu\text{A}} = 30\,\text{k}\Omega.$$

For R_2, we needed the current to have a zero temperature coefficient (TC). Let $\frac{R_2}{R_1} = k$.

The current is given by:

$$i = \frac{V_{BE}}{R_2} + \frac{V_T \ln(n)}{R_1}.$$

For i to have a zero temperature coefficient:

$$\mathrm{TC}(V_{BE}) = \frac{R_2}{R_1} \cdot \frac{V_T \ln(n)}{300}.$$

Thus,

$$k = \frac{\mathrm{TC}(V_{BE}) \cdot 300}{V_T \ln(n)}.$$

Here, we get $k = 10$, so:

$$R_2 = k \cdot R_1 = 10 \cdot 30\,\mathrm{k\Omega} = 300\,\mathrm{k\Omega}.$$

For $\left(\frac{W}{L}\right)$, we assumed an overdrive voltage of 125 mV.
The current is given by:

$$I = i_{\text{PTAT}} + i_{\text{CTAT}} = 2\,\mu\text{A} + \frac{V_{be1}}{R_2} = 2\,\mu\text{A} + \frac{0.42}{300} \approx 3.5\,\mu\text{A}.$$

Using the relationship:

$$3.5 = \frac{350}{2}\left(\frac{W}{L}\right)(0.125)^2,$$

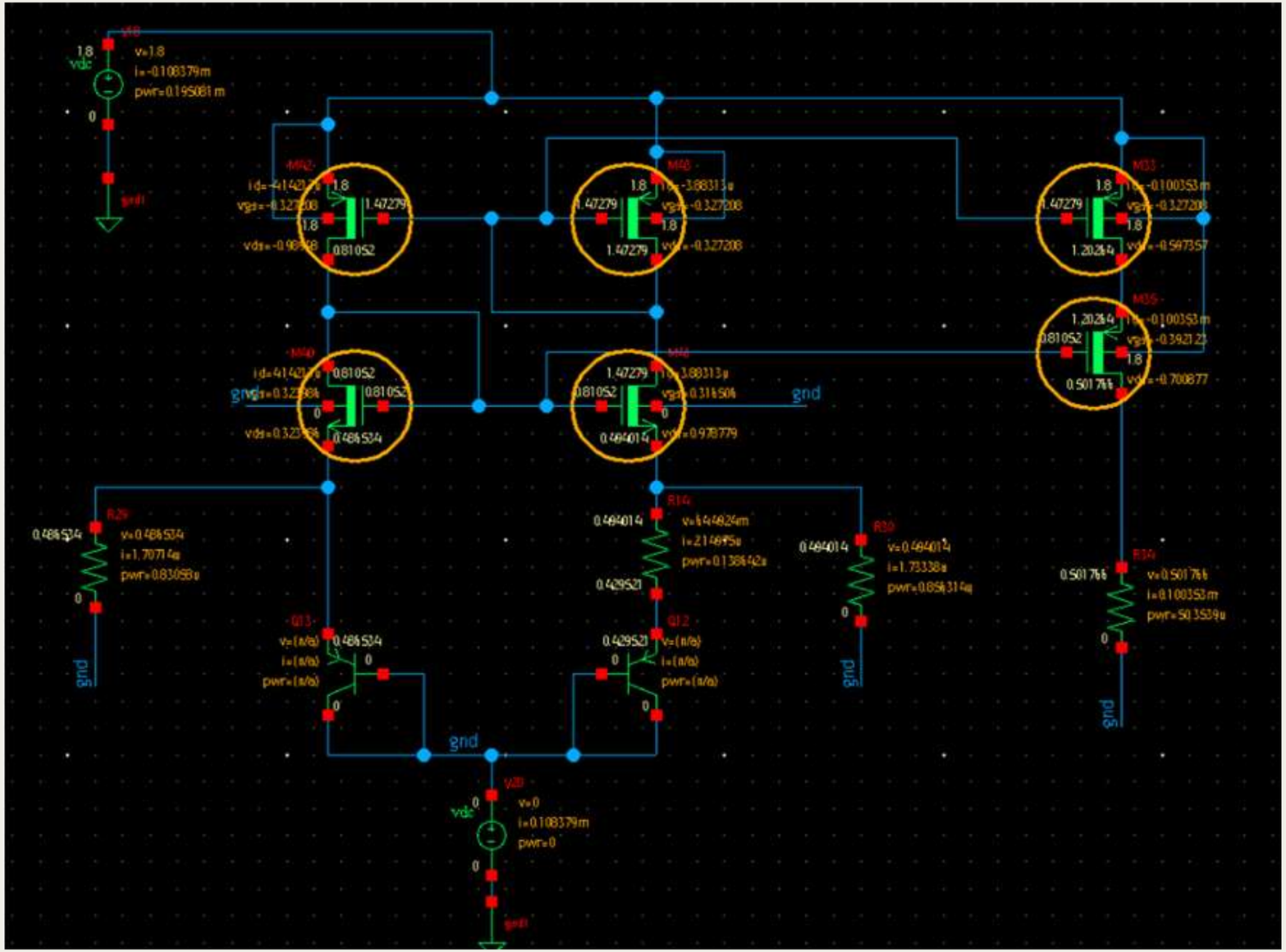
we find:

$$\left(\frac{W}{L}\right) = 1.5.$$

Here, $\left(\frac{W}{L}\right)_p = \left(\frac{W}{L}\right)_n = 1.5$ (for β-multiplier).
We choose $L = 10\,\mu\text{m}$ (for better r_0 and improved mirroring).
Now, for mirroring 4 mA to 100 mA:

$$\left(\frac{W}{L}\right)_{\text{output}} \approx 25 \times 1.5 = 37.5.$$

DC Operating Point



Performance and Achieved Specifications

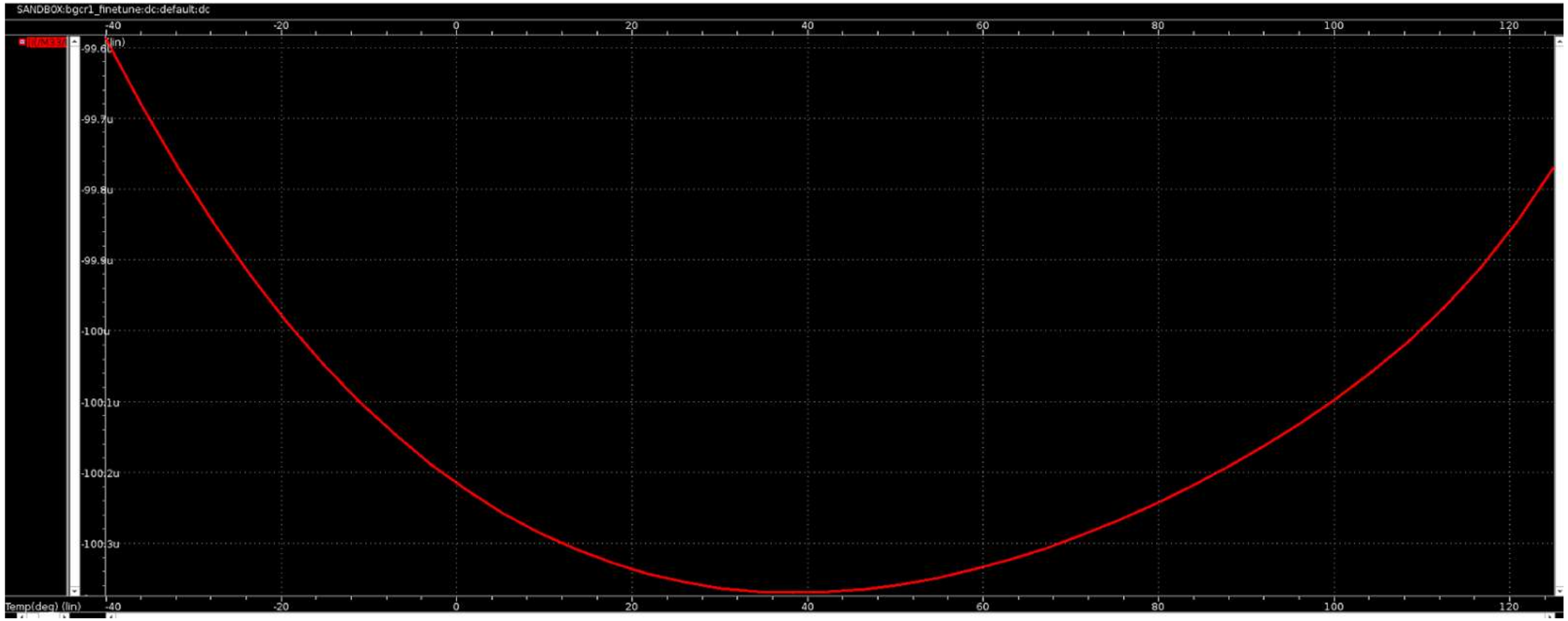
Temperature Performance : The variation of current with temperature was measured, showing that the output current ranges from 99.6 μA to 100.4 μA over the temperature range of -40°C to 125°C.

This corresponds to a temperature coefficient of less than 50 ppm/°C, as required. A curvature compensated Vref design is used.

Technology used : 90nm CMOS
Power supply used : 1.8V

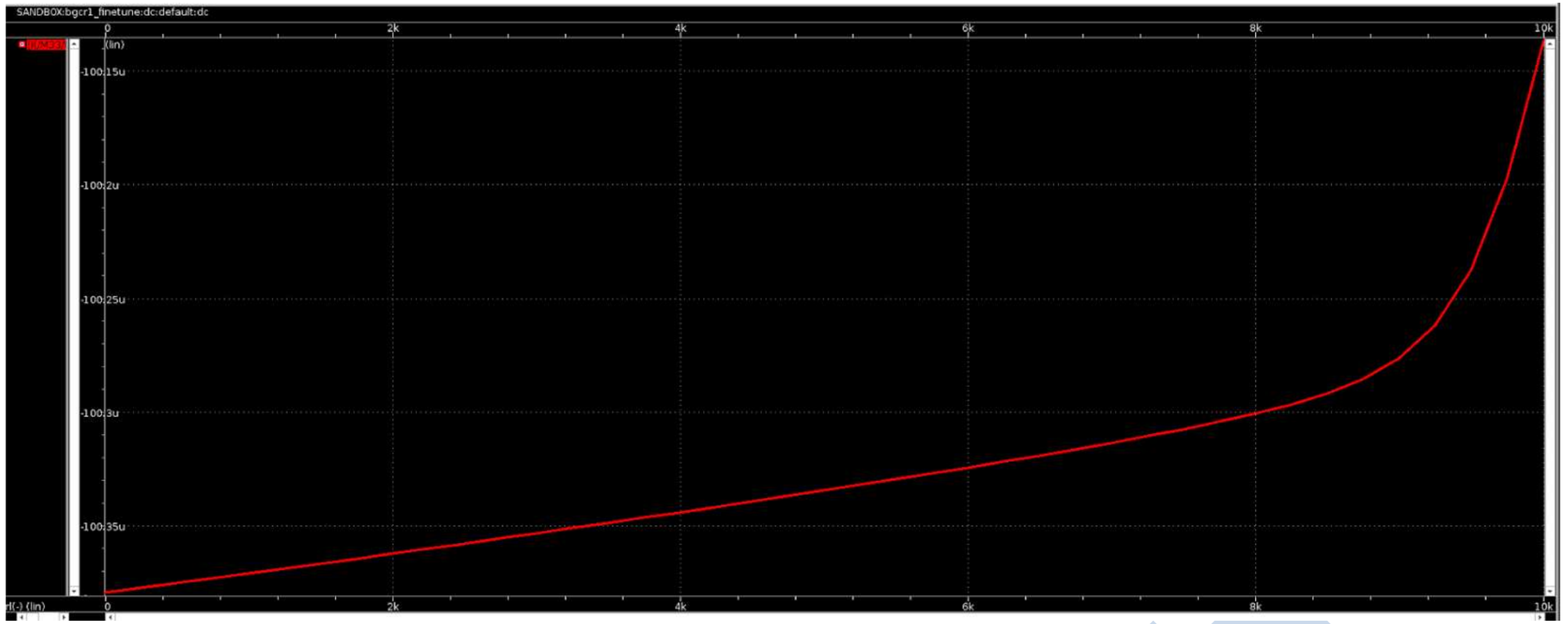
Power Consumption : ~20 μW (less than 50 μW)

Output current sweep with temperature



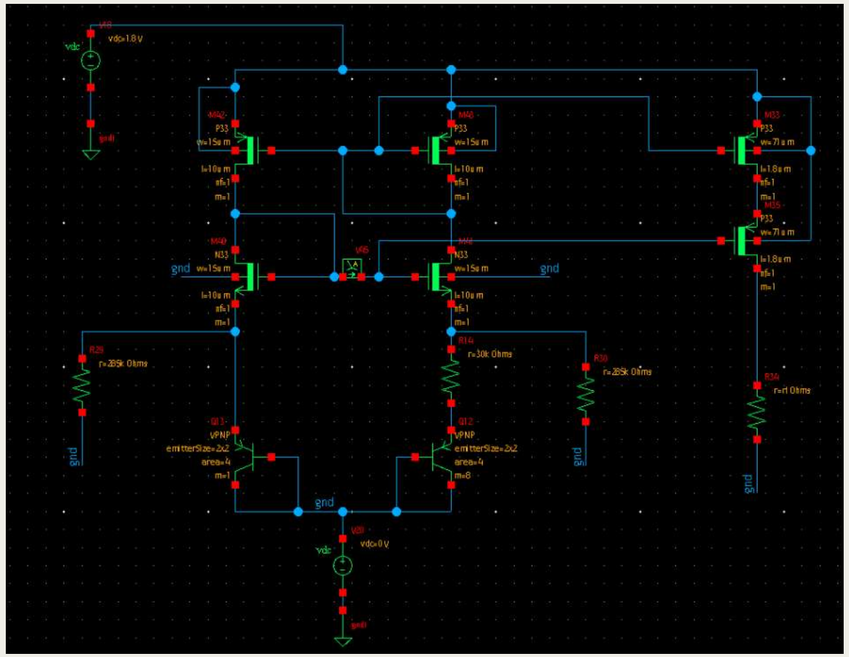
Output current sweep with temperature

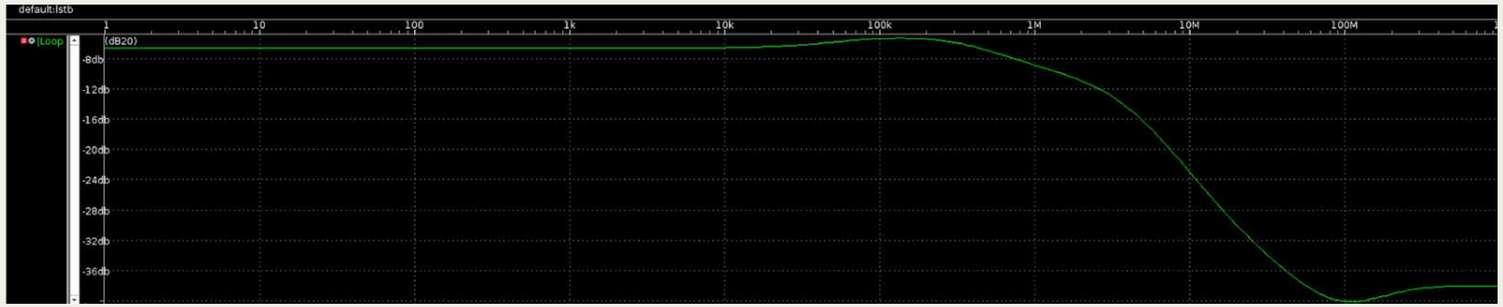
Variation from 100.4 μA to 100.15 μA (0.25 % variation < 2% allowed variation)



Stability Verification

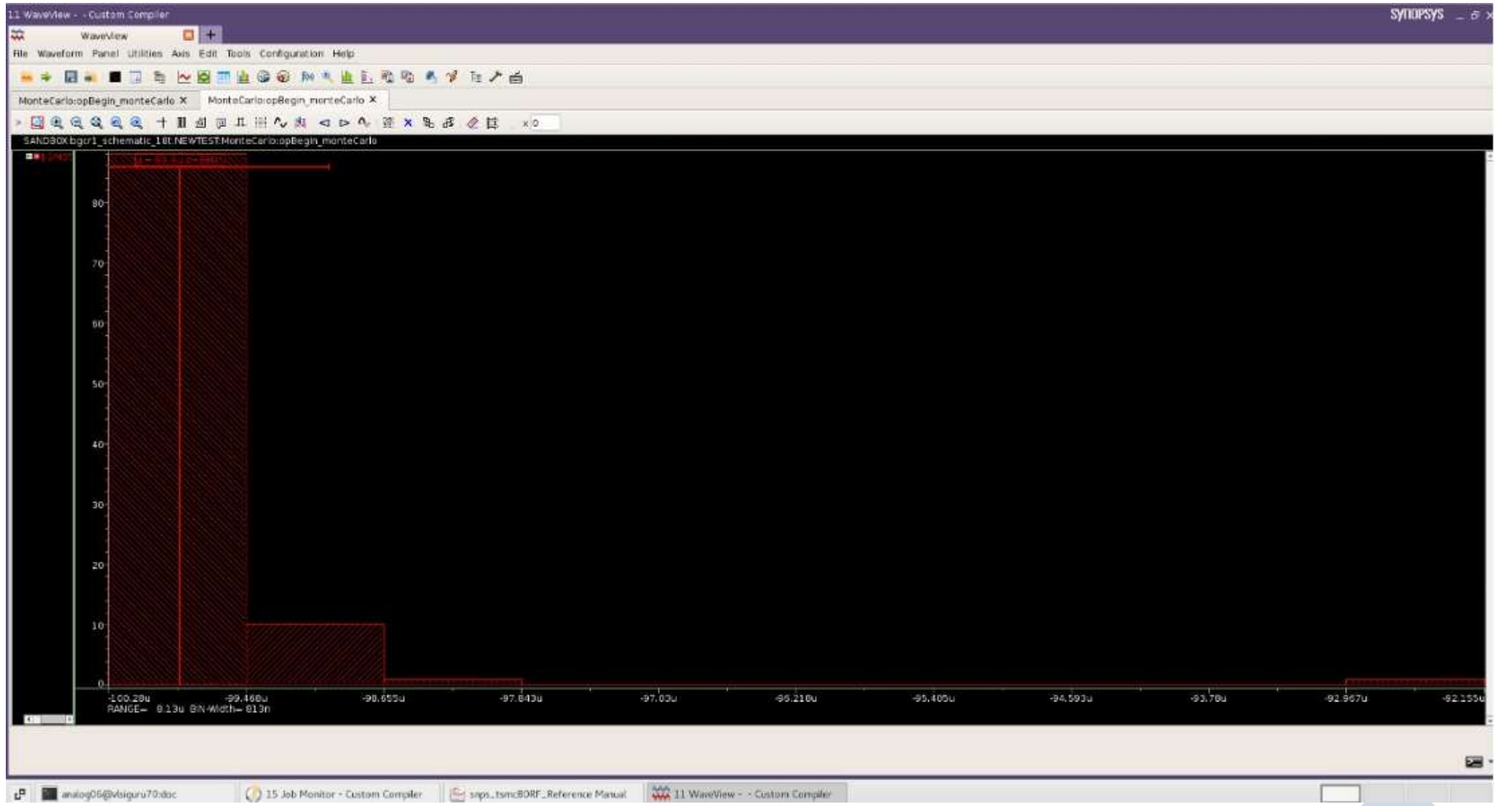
A stb analysis was run using irpb method available in primewave, and the loop gain's magnitude was found to be <1 for all frequencies, ensuring stable operation.



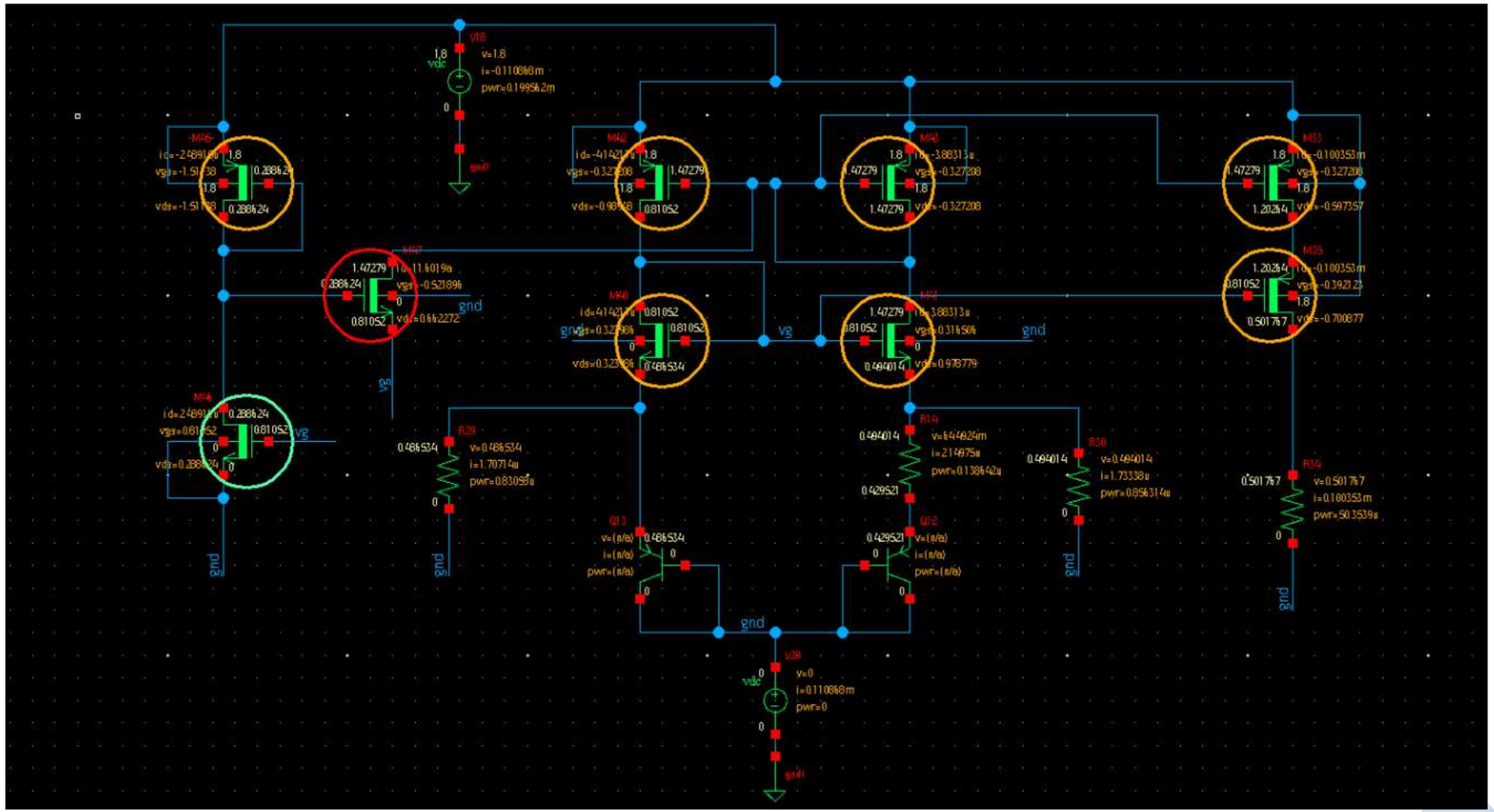


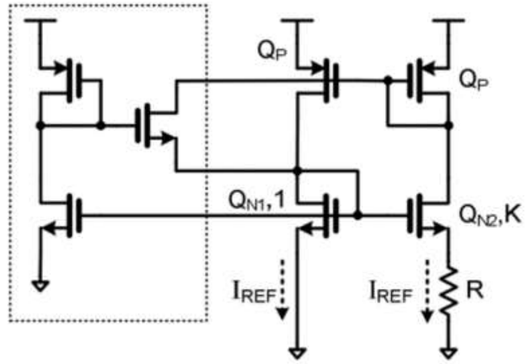
Monte Carlo Simulation

At 25 degrees, we got variance of 880 nA and mean of 99.9 μA



Startup Circuit



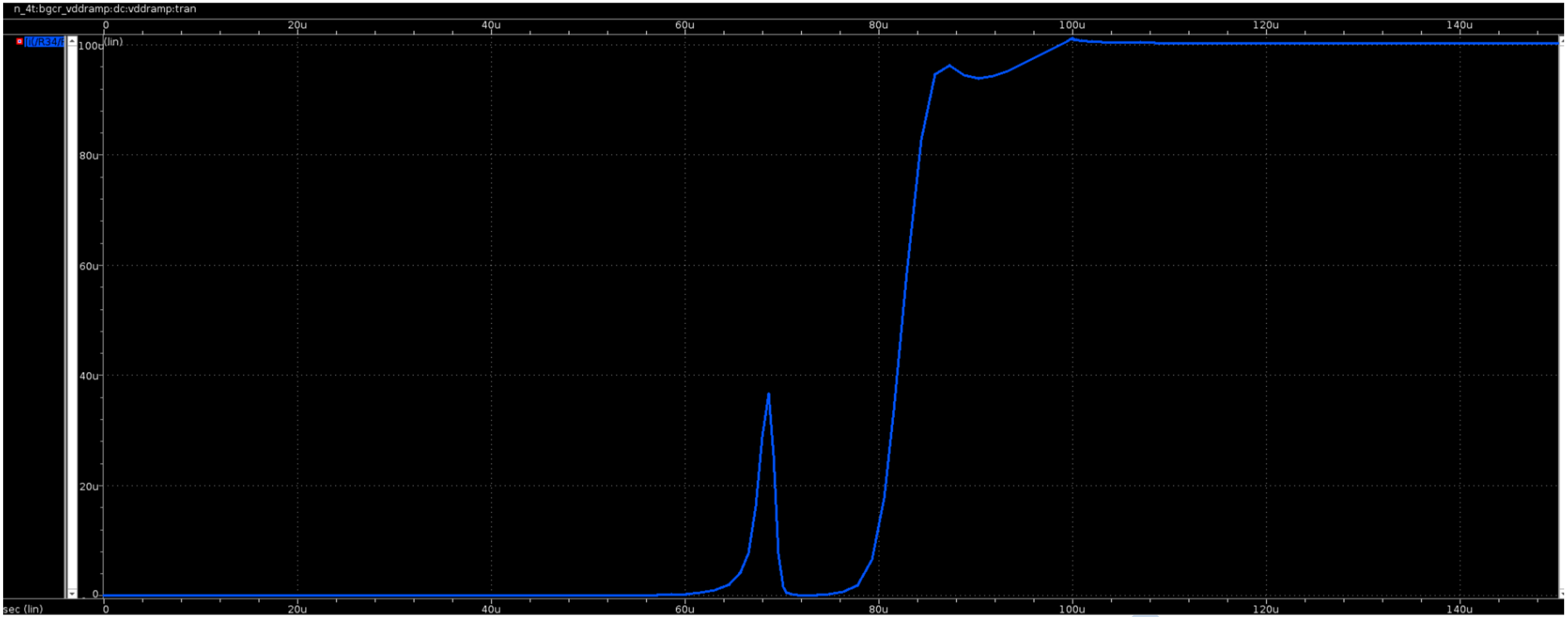


For the startup circuit, we size all transistors to low values of $\left(\frac{W}{L}\right)$, for different reasons, the diode connected PMOS is sized low, so that when the BGCR circuit is on, the overdrive of PMOS is high so that the NMOS connected to the BGCR circuit turns off properly due to low gate voltage.

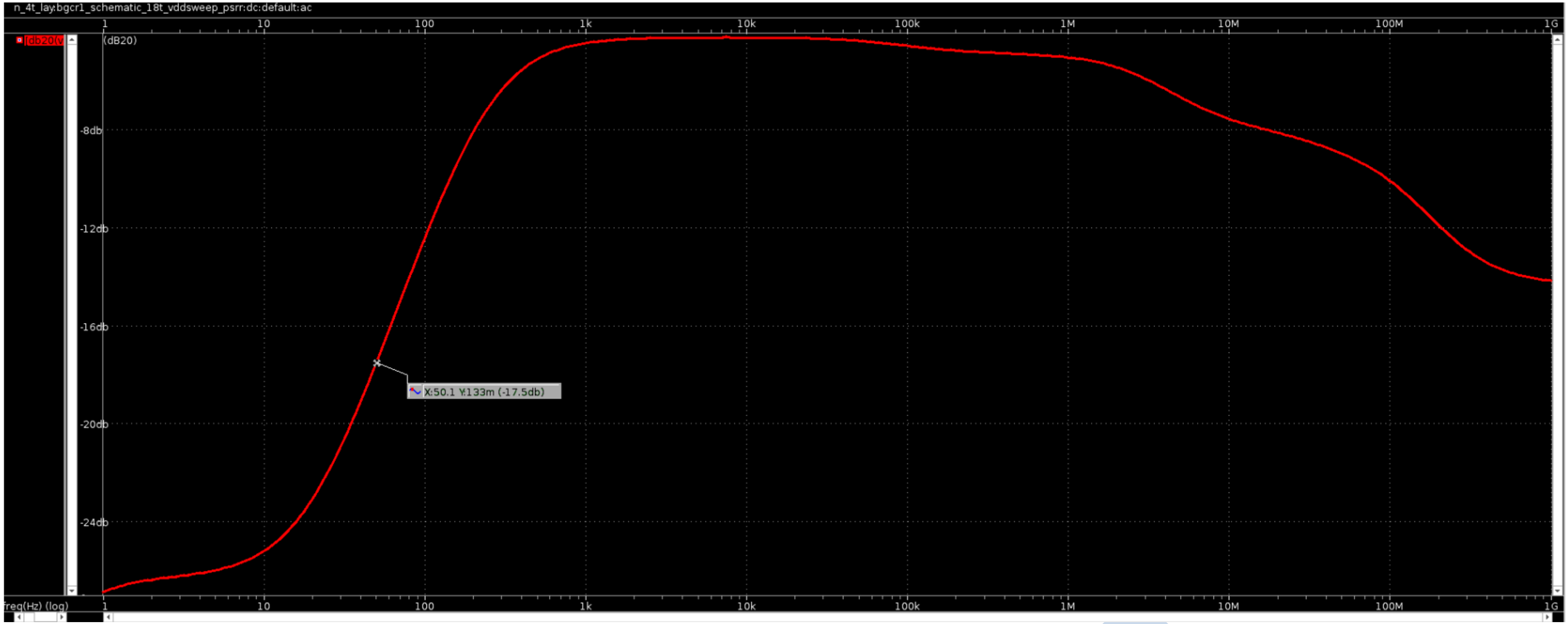
The NMOS below the diode connected PMOS is sized lower to minimize static power consumption of the startup circuit, since the V_{gs} of that NMOS is fixed by the bias point of the BGCR circuit.

The NMOS connected to the BGCR is sized lower so that it does not load the BGCR circuit (does not draw current from it) when it is on and working properly at the given temperature range.

Startup Transients on a Vdd ramp of $1.8V/50\mu s$

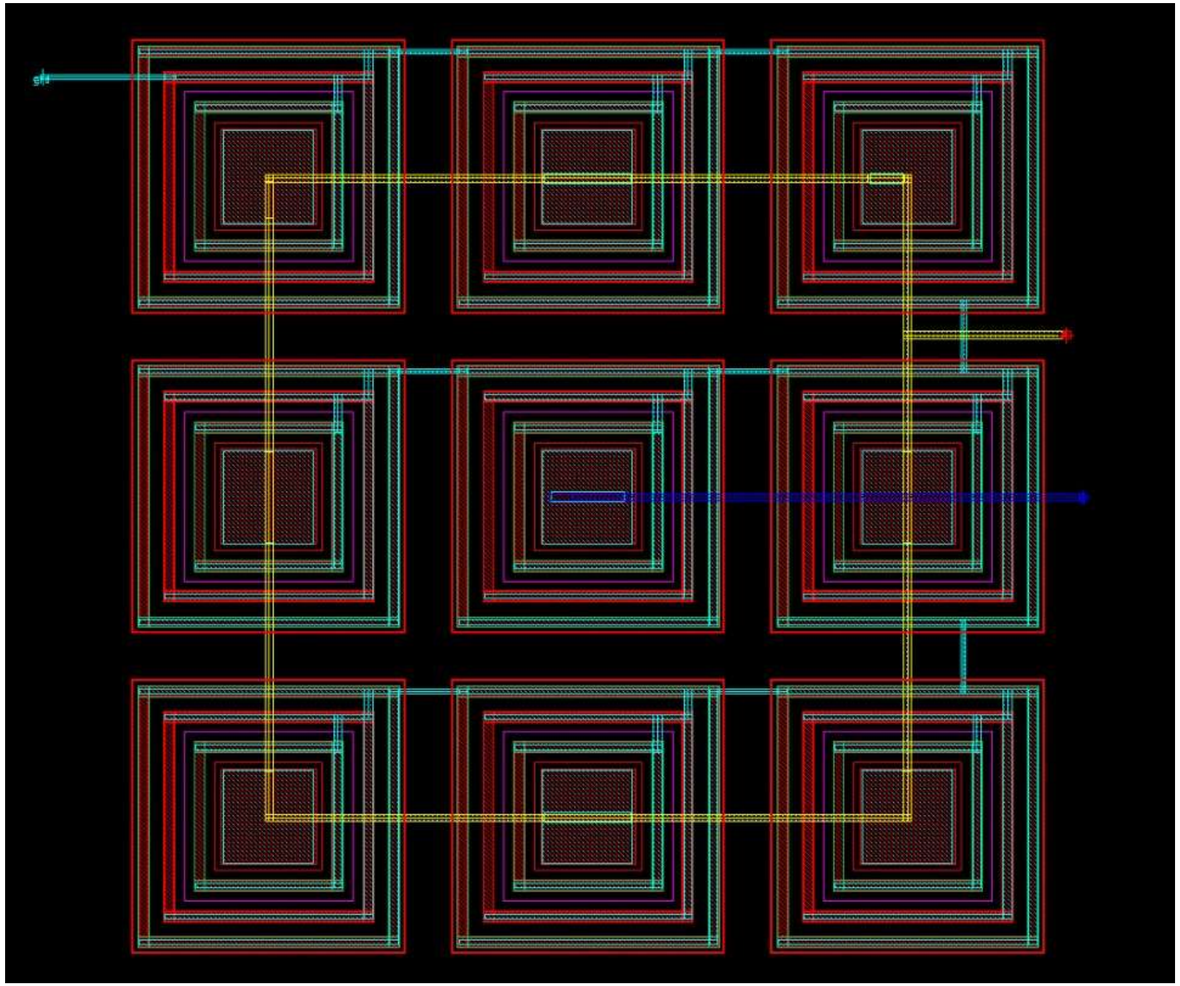


PSRR (17.5 dB to reject 50 Hz supply noise)

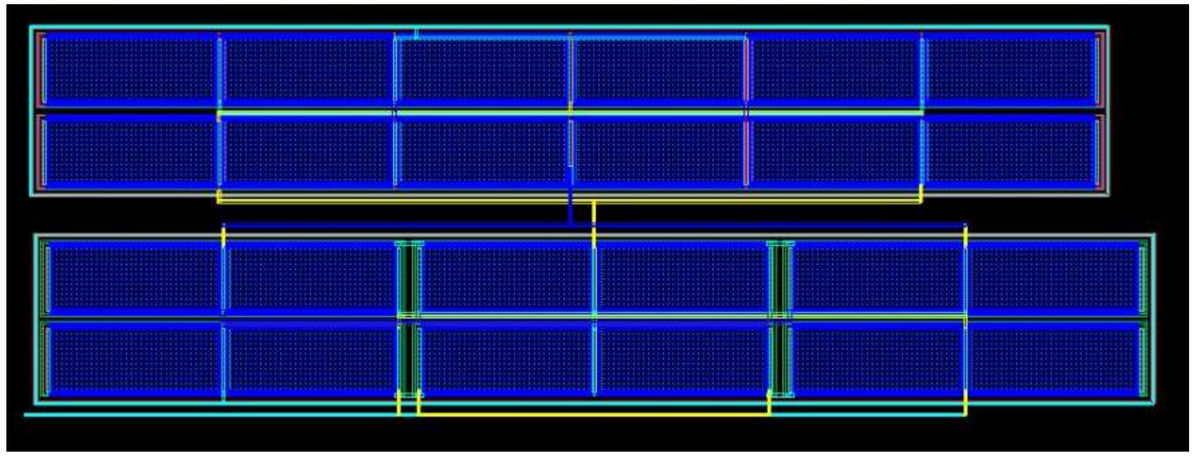


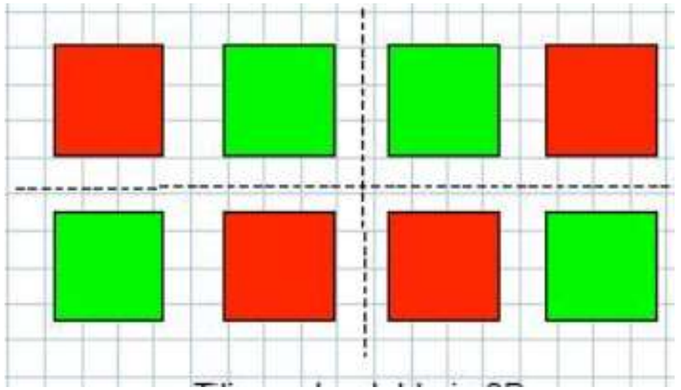
LAYOUT

The VPNP 1:8 Layout

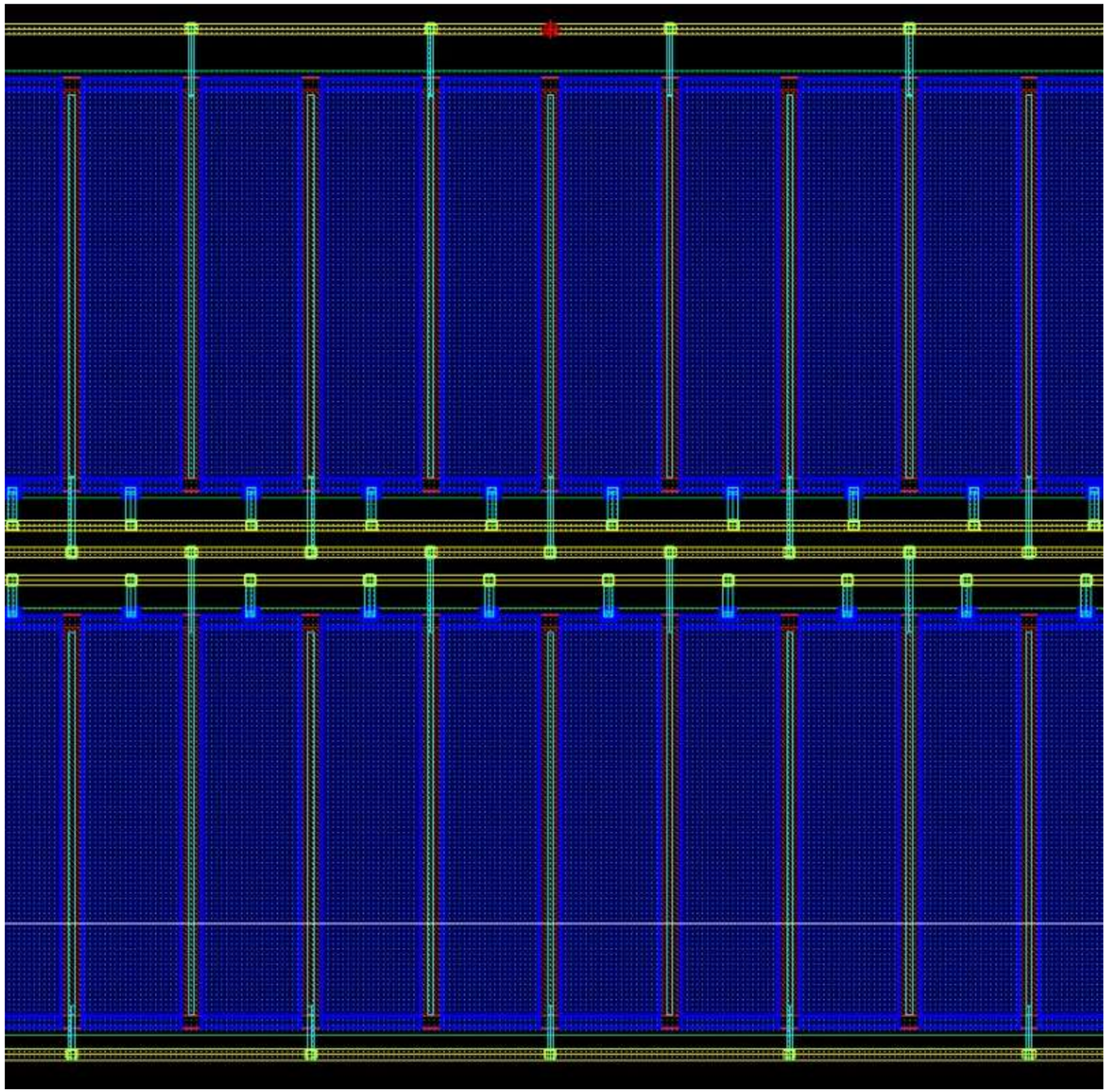


Beta Multiplier

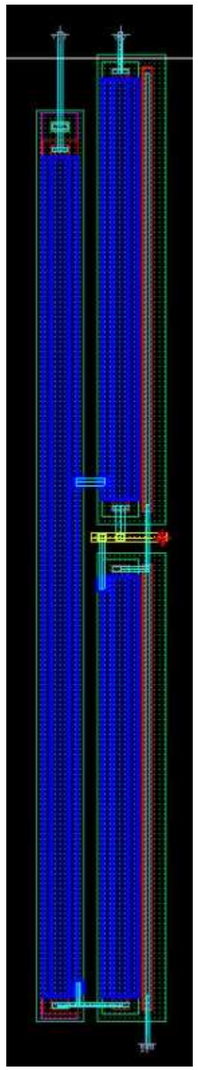




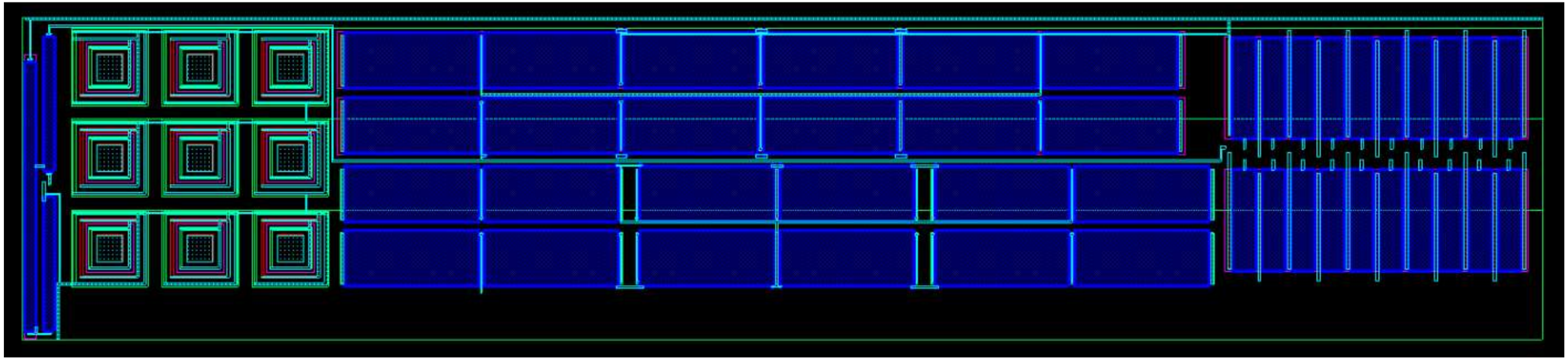
PMOS current mirror (Output Mirror)



Startup



Combined Layout and its PEX (StarRC view)



Smartwatches: The Ideal Use Case for BGCR

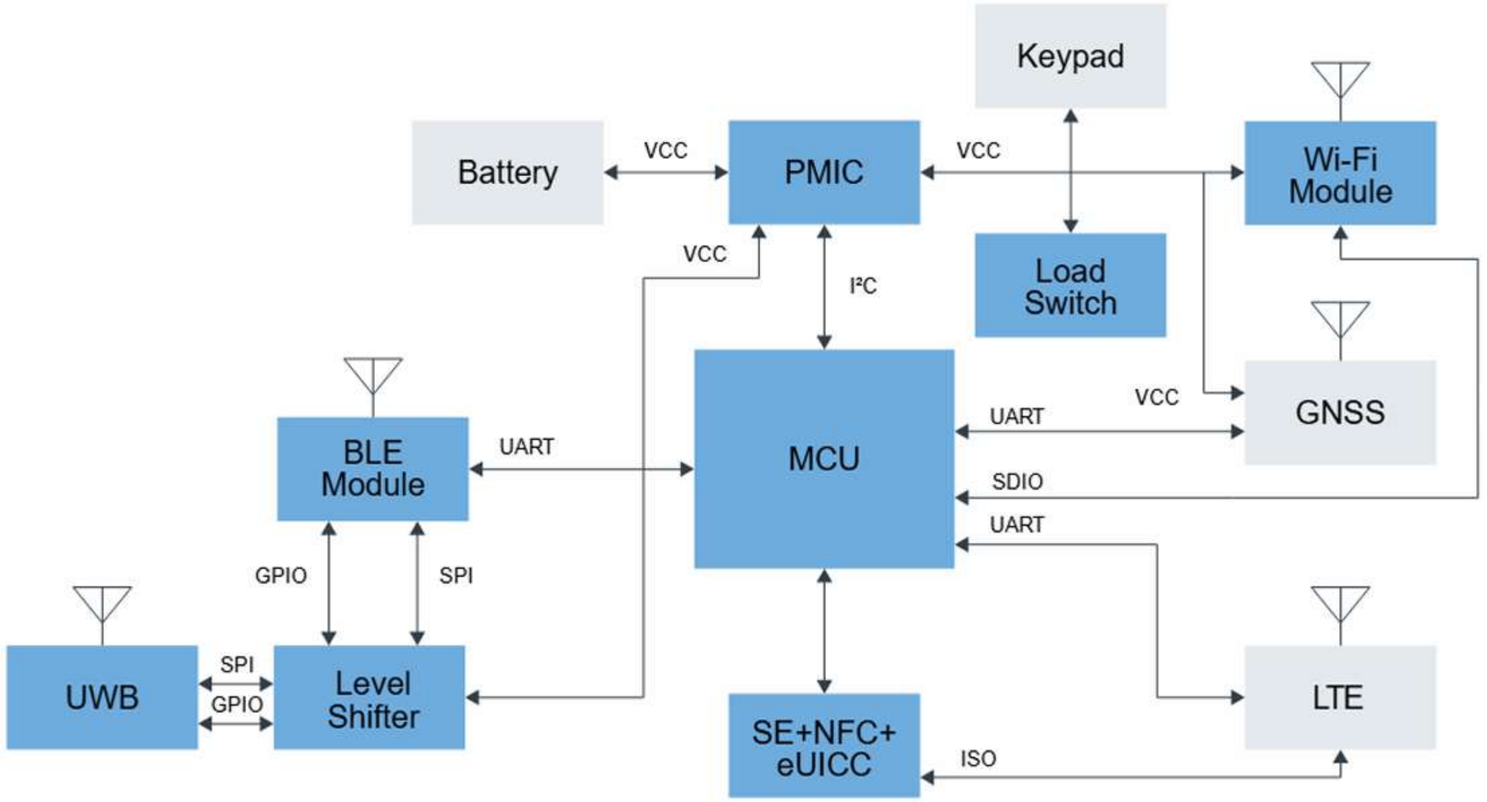
- **Reliable Biasing** : Delivers stable current for sensors, RF transceivers, analog front ends, ADCs, and filters, enabling accurate sensing and seamless BLE communication.
- **Wide Temperature Resilience** : Operates flawlessly across -40°C to 125°C, ensuring reliable performance in diverse environments, from extreme outdoor conditions to everyday use.
- **Excellent Load Regulation** : Maintains ±0.2% output stability to support varying loads, such as displays, sensors, and communication modules.

- **Low Power Consumption** : Consumes only 20 μW, optimizing battery life for extended use in power-constrained devices like smartwatches.

- **RF Stability** : Ensures frequency Stability of RF oscillators, enabling consistent and reliable BLE connectivity.

- **LDO Integration** : Acts as a dependable bias source for LDO regulators, powering multiple smartwatch subsystems efficiently.

Power Management IC (PMIC) uses the current reference to bias the MCU and Wi-fi Module



THANK YOU

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