

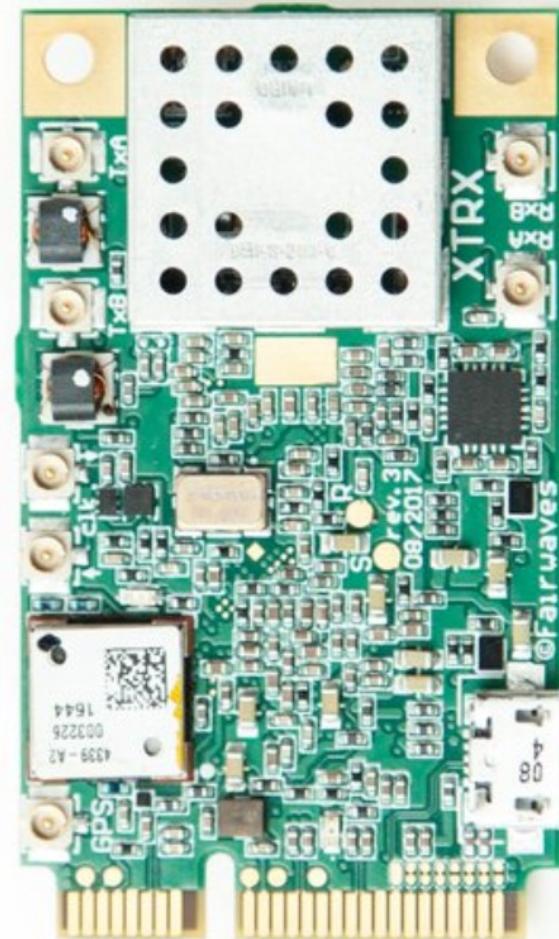
OsmoDevCon2018

XTRX update

Sergey Kostanbaev / Fairwaves

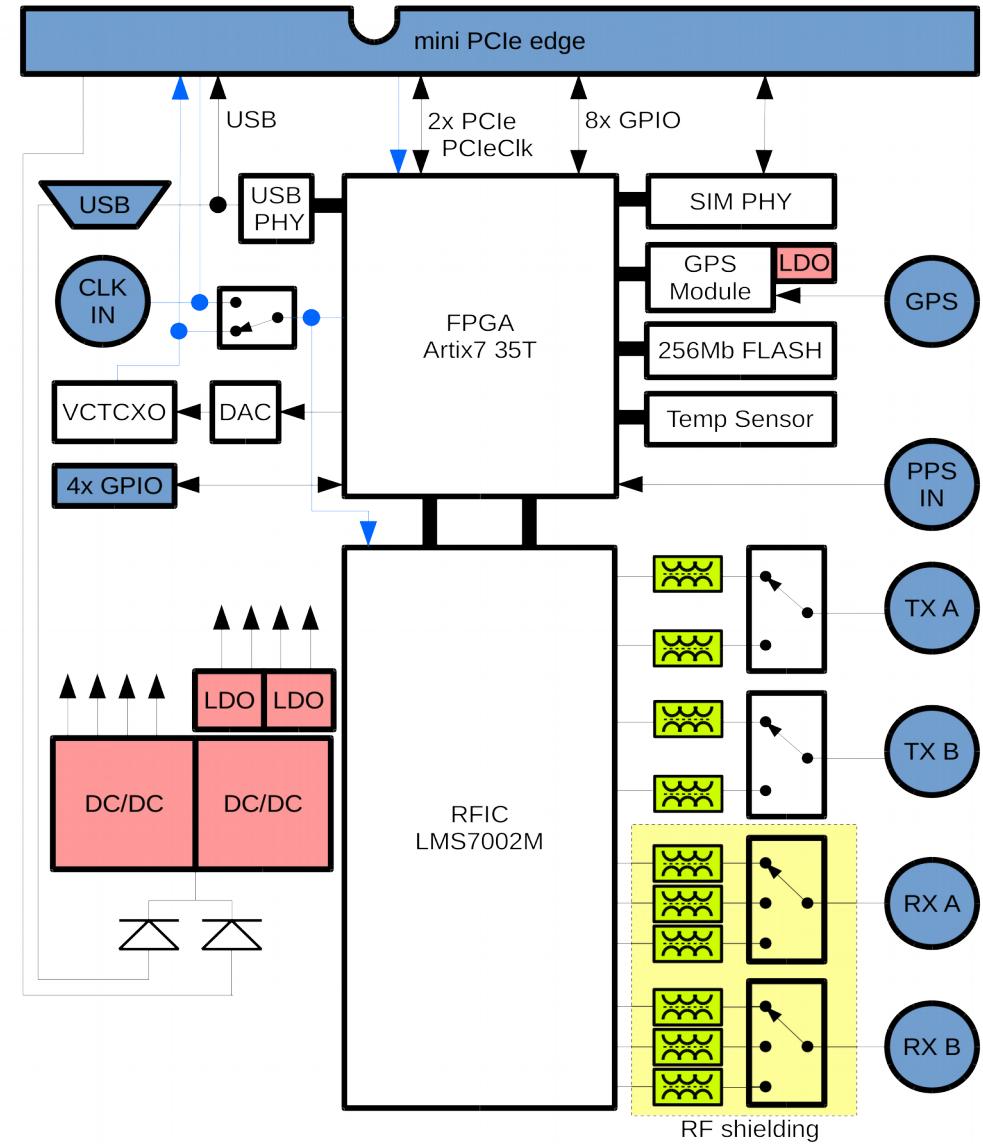
# What's the XTRX?

- miniPCIe SDR (30x50)
- x2 PCIe 2.0 (10Gbit/s)
- LMS7002M RFIC (MIMO)
- GPSDO onboard
- Ext. clock synchronization
- GPIO



# Main features

- GPSDO built-in
- SIM interface
- USB2 PHY
- 12 GPIO (opt. 5 diff)
- Efficient power system
- RF matching and switches for all LMS7 bands
- High samplerate (100+ MSPS)



# A little bit of history. Second-system effect?

- Jan 2016 – First block diagram of miniPCIe SDR board
- Mar 2016 – First schematics of XTRX
- Jul 2016 – First samples mfg
- Dec 2016 – PCIe DMA Tx/Rx working, GNURadio
- Jan 2017 – rev.2 (never manufactured)
- Apr 2017 – rev.3 design, USB3 to PCIe development
- Sep 2017 – rev.3 samples mfg
- Dec 2017 – CrowdSupply campaign
- Mar 2018 – Finalization of rev.4 and USB adapter
- Apr 2018 – Mfg of samples (final HW rev)

# High sample rate issues

- Dreamed of 160MSPS initially
- 100MSPS means 200Mhz DDR on LMS7002M LML bus
- LML is CMOS bus, hard for high rate (DDR RAM SSTL)
- Turned out only (stable performance)
  - 90MSPS MIMO
  - 120MSPS SISO
- With dynamic Vio control+active cooling+lucky chips+phase calibration (RX)
  - 115MSPS MIMO
  - 150MSPS SISO

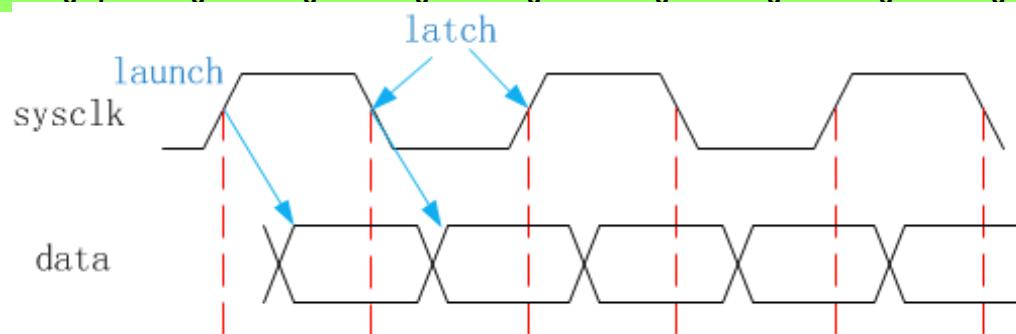
# VIO vs MIMO Samplerate

5MSPS	1.00 to 3.30		
15MSPS	1.26 to 3.30		
30MSPS	1.30 to 3.30		
40MSPS	1.40 to 3.30		
70MSPS	1.56 to 3.30		
80MSPS	1.60 to 3.30		
90MSPS	1.64 to 3.30	1.70-2.94 at 95C	stops at 105C
95MSPS	1.68 to 3.30	1.70-2.22 at 95C	stops at 100C
100MSPS	1.68 to 3.30		stops at 60C
110MSPS	1.74 to 1.82 (phase cal)		stops at ~50C
115MSPS	1.74 to 1.76 (phase cal)		stops at ~43C

# DDR Phase calibration on LFSR

140MSPS SISO @3.3V (each phase tap ~67ps)

000: 0000	-1 errs= 0 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
001: 0000	-1 errs= 0 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
002: 0000	-1 errs= 0 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
003: 0000	768924 errs= 228 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 228 ]
004: 0000	1700 errs= 177698 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 179917 ]
005: 0000	36 errs=1294092 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1450764 ]
006: 0000	36 errs=1865480 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2203192 ]
007: 0002	36 errs=2292422 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2687418 ]
008: 249e	32 errs=3386633 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 2428 ] 0 4163527 215 ]
009: 8218	32 errs=3714601 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 41525 991312 ] 0 4190070 858508 ]
010: aa6c	32 errs=3988465 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 508315 3298334 ] 0 4199236 203593 ]
011: a91e	32 errs=3947611 [ 673233 079226 502577 162263 390118 183209 062014 248087 181125 088745 221597 207594 ]
012: 28c7	32 errs=2870843 [ 101082 11 149368 1711 153678 3356 0 25565 0 2462487 0 0 ]
013: 8959	32 errs=2447551 [ 695702 0 40353 71 58358 239 0 2679 0 2174975 0 0 ]
014: 9664	32 errs=1636329 [ 17614 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1667591 ] 0 0 ]
015: 0100	32 errs=1320352 [ 656 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1359786 ] 0 0 ]
016: 0000	32 errs= 335904 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 336327 ] 0 0 ]
017: 0000	184 errs= 49735 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 49737 ] 0 0 ]
018: 0000	184 errs= 3715 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 3715 ] 0 0 ]
019: 0000	22544 errs= 146 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 146 ] 0 0 ]
020: 0000	-1 errs= 0 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
021: 0000	-1 errs= 0 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
022: 0000	-1 errs= 0 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
023: 0000	-1 errs= 0 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]
024: 0000	-1 errs= 0 [ 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ]



# High sample rate issues (part 2)

- Very few software is ready for 100MPS+ rate
- fosphor on my laptop allows only 65 MSPS.  
Needs more optimization
- Efficient 12bit → 16bit host translation is hard

# Bus speed calculations

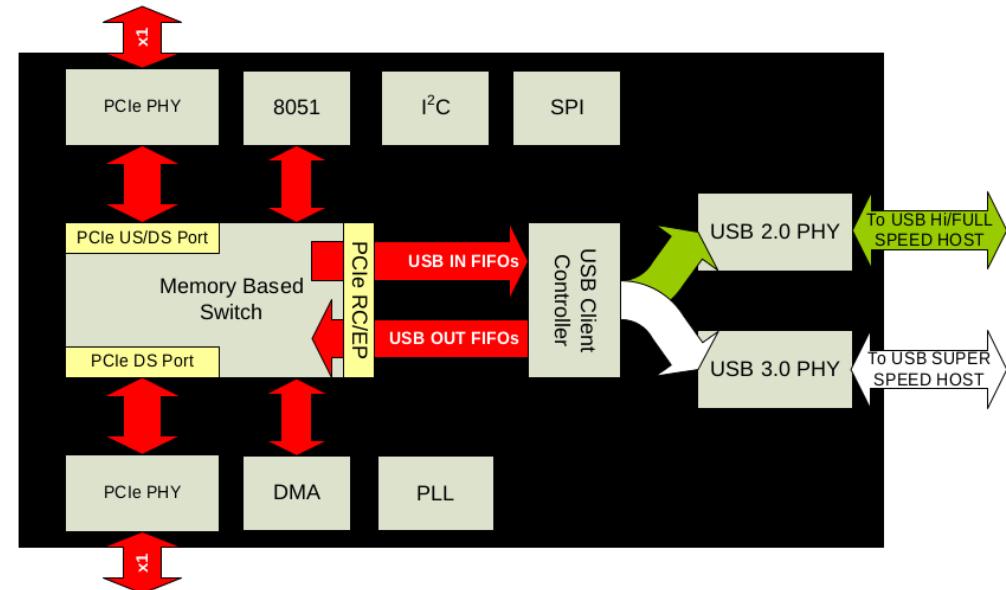
- x2 PCIe 2.0 – 10Gbit/s
  - 4b5 coding → 8Gbit/s
  - 128b payload → 0.87 efficiency → 6.96Gbit/s
  - DMA control traffic → 0.98 efficiency → 6.82Gbit/s
  - 6.82Gbit/s → 106MSPS@16bits MIMO (theoretical maximum)
  - **6.70Gbit/s achieved over TB3 adapter** (98.2% efficiency!!)
- USB3.0 – 5Gbit/s
  - 4b5 coding → 4Gbit/s
  - 1024b max payload → 0.99+ efficiency
  - 3.1Gbit/s stream achieved via USB3380

# Power optimization

- MiniPCIe card specification  $\leq$  2.5W total
- REV.1 (3 DC/DC; 2 LDO):
  - 1.8V VIO fixed → Limited sample rate
  - 3.3V to 1.8VA for LMS7 LDO
  - Almost **0.9W** was lost in single LDO
  - Supply 3.0V-3.6V
- REV.3 (8 DC/DC; 5 LDO):
  - All DC/DC are programmable 1.0-3.3V
  - 2.05V → 1.8VA, 1.4V → 1.25VA, 1.65V → 1.4VA for LMS7
  - Supply 3.0V-5.5V
  - The only configuration which goes above 2.5W is MIMO TX+RX+RxTSP+TxTSP at 100MSPS  
Simpler modes are below 2.5W

# USB3 to PCIe converter

- In Jan 2016 I thought it's almost impossible
- But found USB3380 chip
- No direct conversion → support library
- Turned out it's very useful
  - Unbricking (after a failed FPGA programming)
  - Full hot plug (no more rebooting!)
  - Laptops without miniPCIe and TB3
  - 100+MSPS SISO!



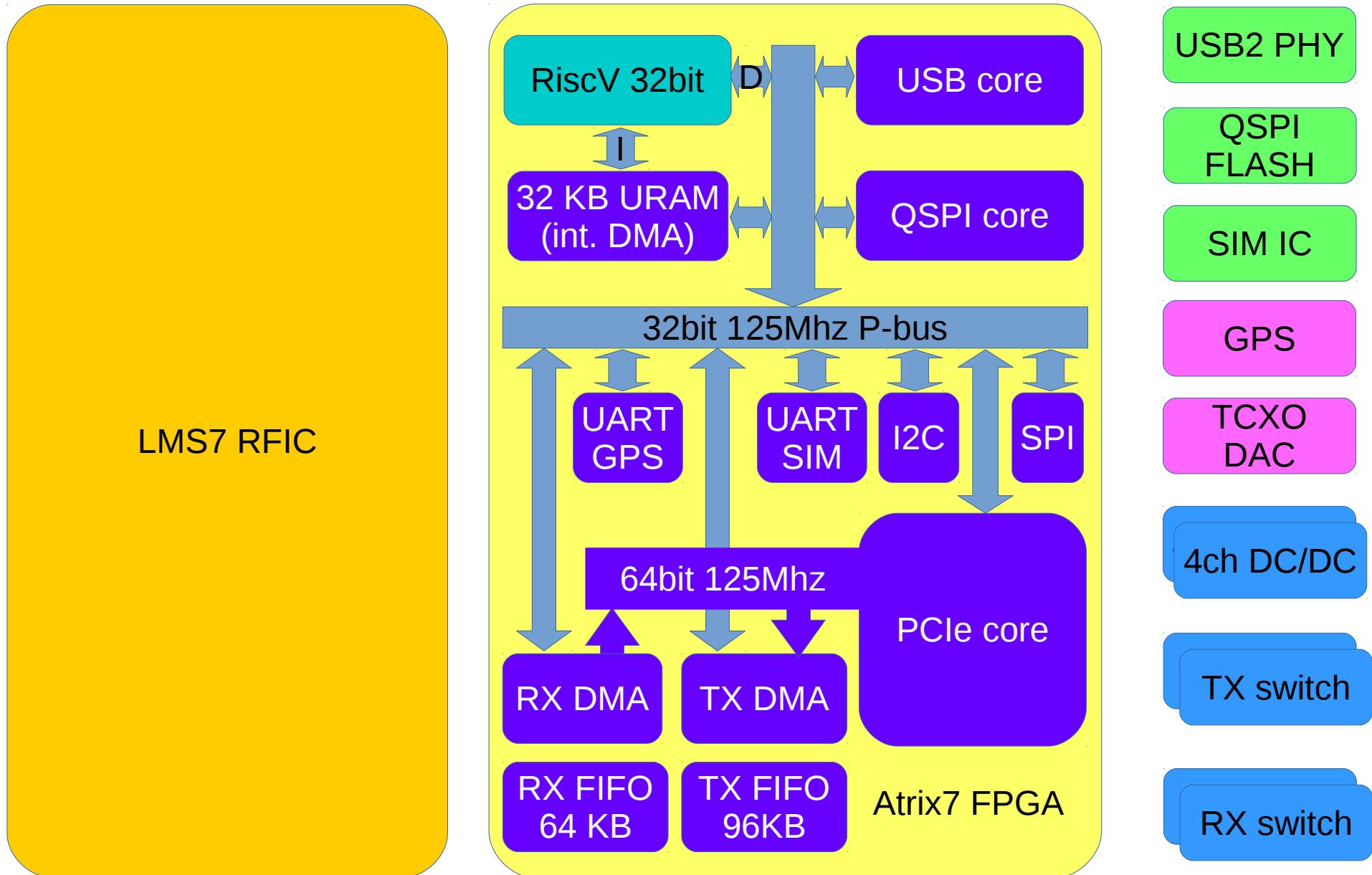
# USB3 Challenges

- GPIO used for JTAG emulation (xc3progs)
  - libusb bit banging => ~40 min
  - libusb bit banging (opt) => ~27 min
  - 8051 bit banging => 3.5 min
  - 8051 bit banging (opt) => 70 sec
- PCIe ↔ USB
  - 4x GPEP, 4KB FIFO max
  - Host PIO operations are serialized, ideally need a special 8051 fw

# USB3 Performance

- Single EP operation
  - TX 160MB/s RX 128MB/s
- Multi EP (GPEP0/GPEP1/GPEP0/GPEP1/...)
  - TX 310MB/s RX 340MB/s
  - But hard to recover from overruns/underruns
- Hard to add CDC interface for GPS/SIM
  - Need 3 EPs for CDC ACM device
- High sample rate is very jittery over libusb (>250MB/s)
  - Will kernel driver help?

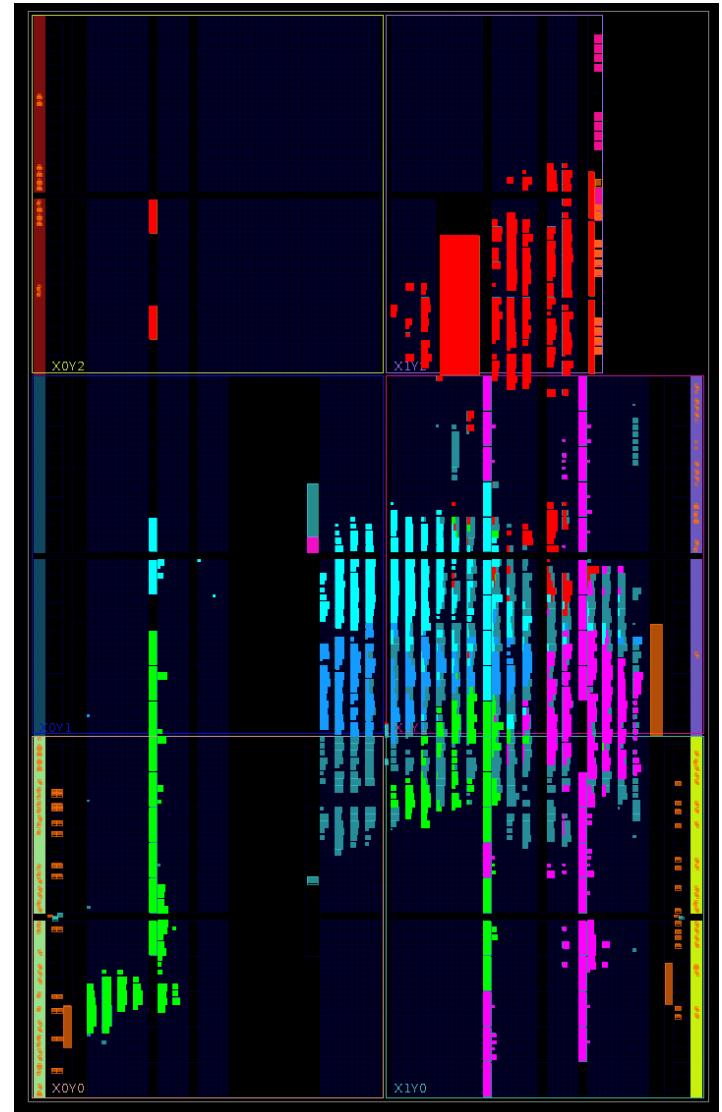
# FPGA high level diagram



# FPGA utilization (35T)

- 100% BRAM but
  - 16 RX FIFO + 24 TX FIFO
  - 2 PCIe core + 8 URAM
- 0 DSP bloks (yet)
- Can also fit in 15T  
(by reducing FIFO sizes)

Resource	Utilization	Available	Utilization %
LUT	4895	20800	23.53
LUTRAM	329	9600	3.43
FF	4309	41600	10.36
BRAM	50	50	100.00
IO	84	106	79.25
GT	2	2	100.00
BUFG	11	32	34.38
MMCM	1	5	20.00
PCIe	1	1	100.00



# Native USB2 support status

- Not all miniPCIe have PCIe lanes
- 100+ MSPS is not always needed
- RPI3, etc.
- ULPI to EP FIFO core is ready
- Enumeration is done in RiscV softcore
- No support in host libraries yet
- Hope to have a support right after board shipping

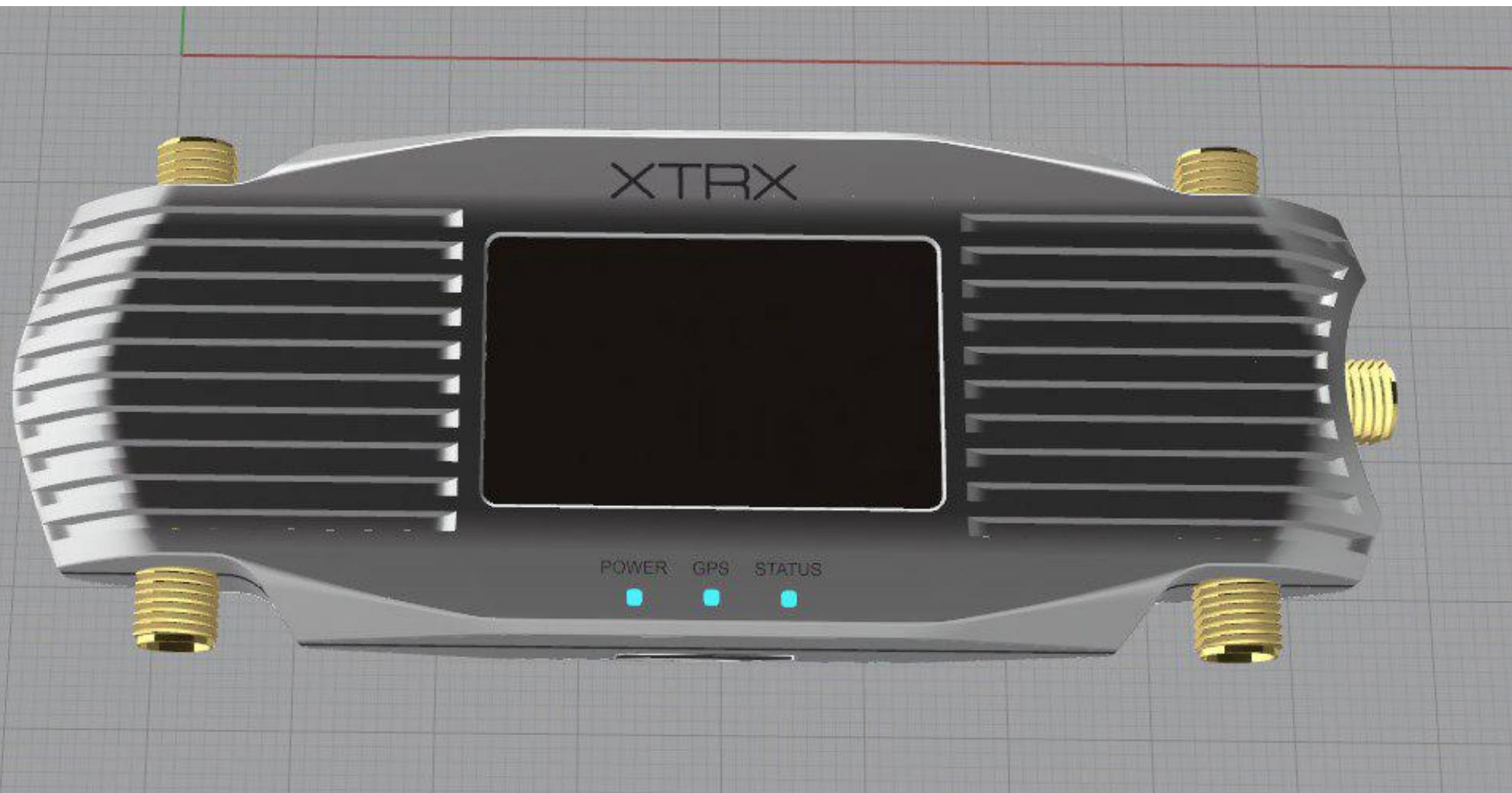
# Software status

- All host libraries and kernel driver are on GitHub
- Support for 3<sup>rd</sup> parties:
  - SoapySDR plugin (not all feature supported)
  - gr-osmosdr (native – timed tags support)
  - omso-trx (native interface – get rid of tons of dependencies)
  - SRS LTE (WIP)
  - Amarisoft LTE
  - SDRangel
- FPGA code will be published before shipping
- Multi-XTRX synchronized operation support is in progress
- Right now we're focused on user experience

# CrowdSource

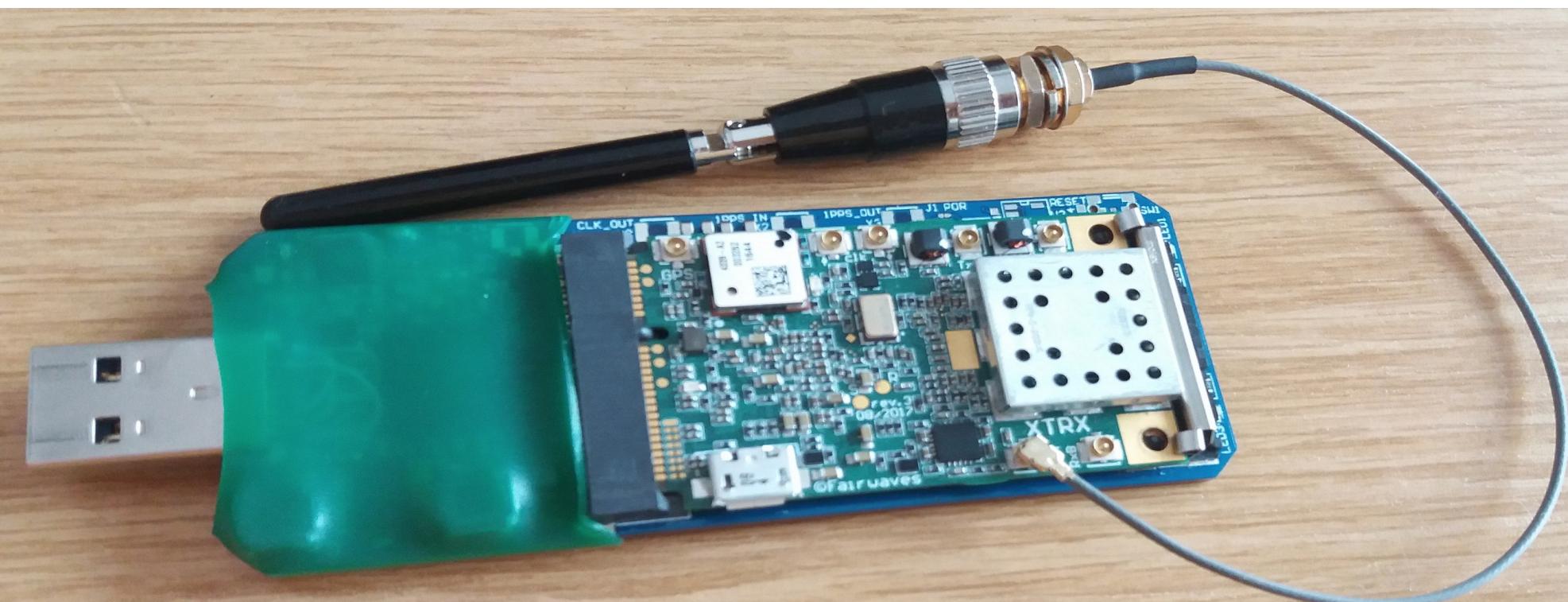
- More HW options → quantity will be spread → higher cost → higher price :(
- That's why
  - Just one hardware option for XTRX
  - Just one option for USB3 adapter with case
  - Just one option for PCIe to miniPCIe adapter
  - Just one MaMIMO package Octopack with 8 XTRX

# Original USB3 Adapter Idea



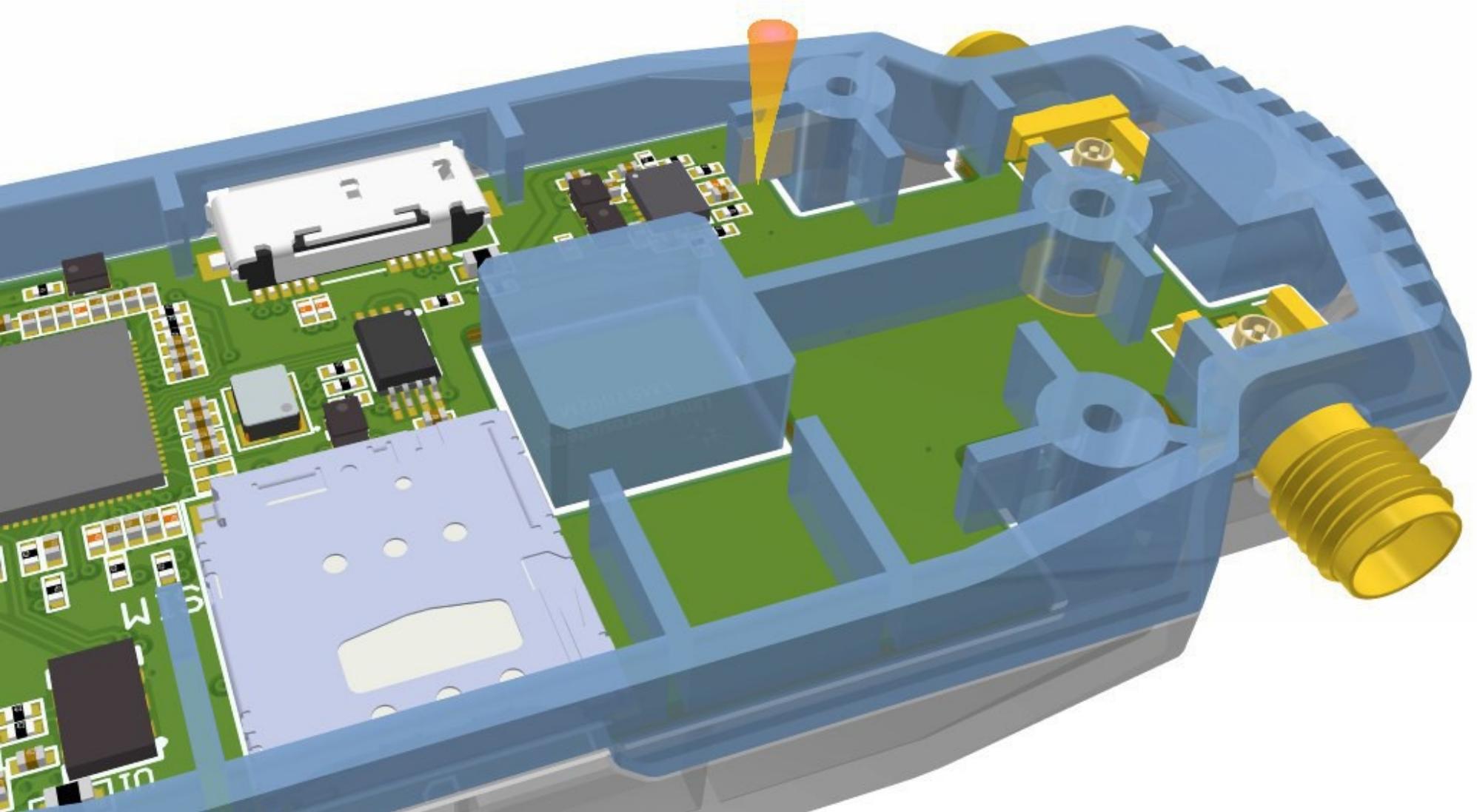
# USB3 adapter history

- Took a lot of time just to design case
- PCB v1.0 → v1.1 → v1.2
- 6 layers in the end  
(to remove high speed lanes from top and bottom planes)





# USB3 thermal optimization

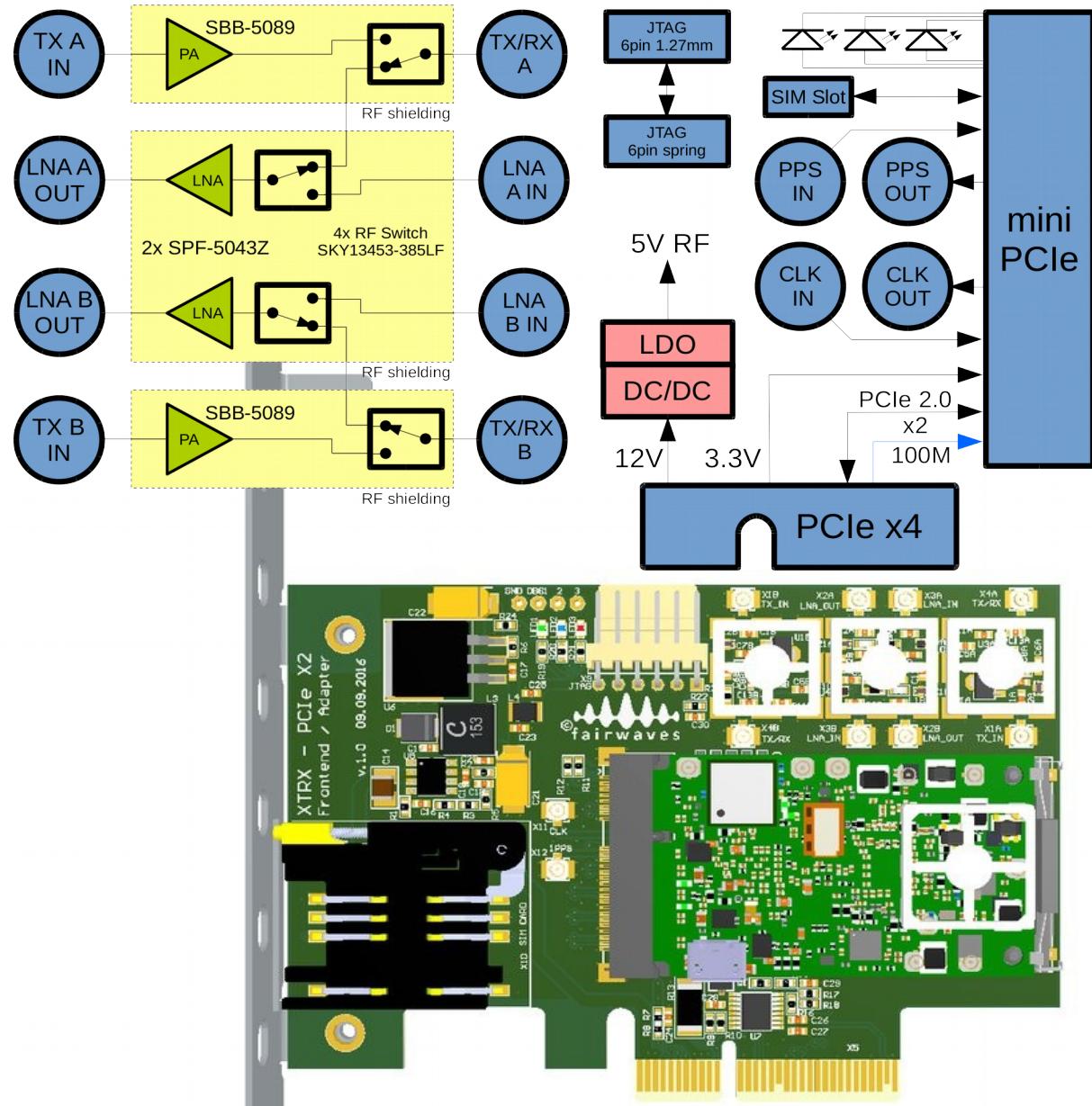






# PCIe to miniPCIe adapter

- x2 PCIe
  - TDD switch
  - LNA
  - PreAMP
  - JTAG breakout
  - GPIO breakout
  - SIM card holder



# PreDriver A Gain (TX\_IN -> TX/RX)

Step 20.000000 MHz

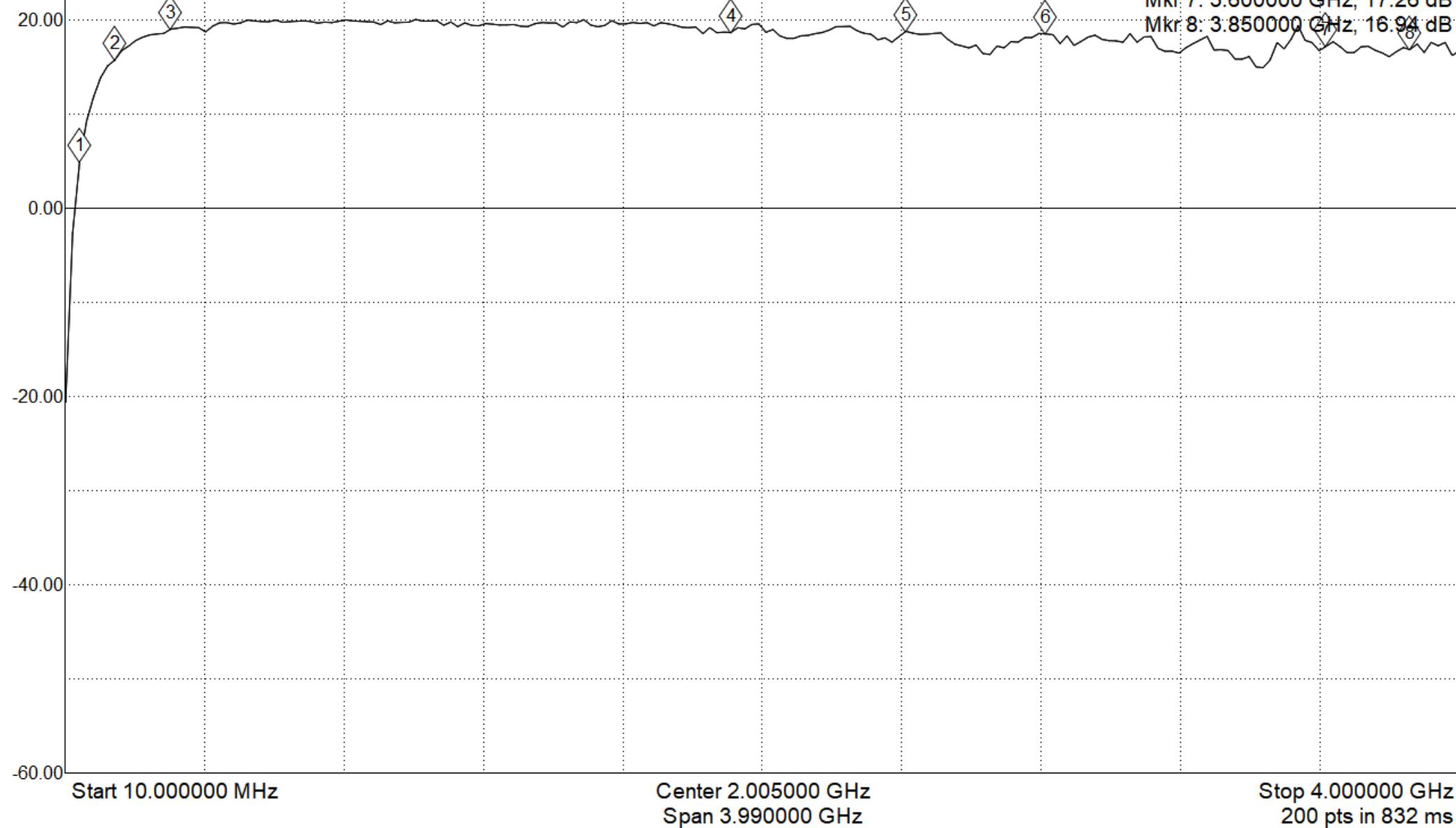
Atten --

VBW --

Ref 40.00 dB

Div 10.0

Mkr 1: 40.000000 MHz, 4.98 dB  
Mkr 2: 150.000000 MHz, 15.78 dB  
Mkr 3: 300.000000 MHz, 19.08 dB  
Mkr 4: 1.900000 GHz, 18.73 dB  
Mkr 5: 2.400000 GHz, 18.86 dB  
Mkr 6: 2.800000 GHz, 18.59 dB  
Mkr 7: 3.600000 GHz, 17.26 dB  
Mkr 8: 3.850000 GHz, 16.94 dB



# LNA A Gain (LNA\_IN -> LNA\_OUT)

Step 20.000000 MHz

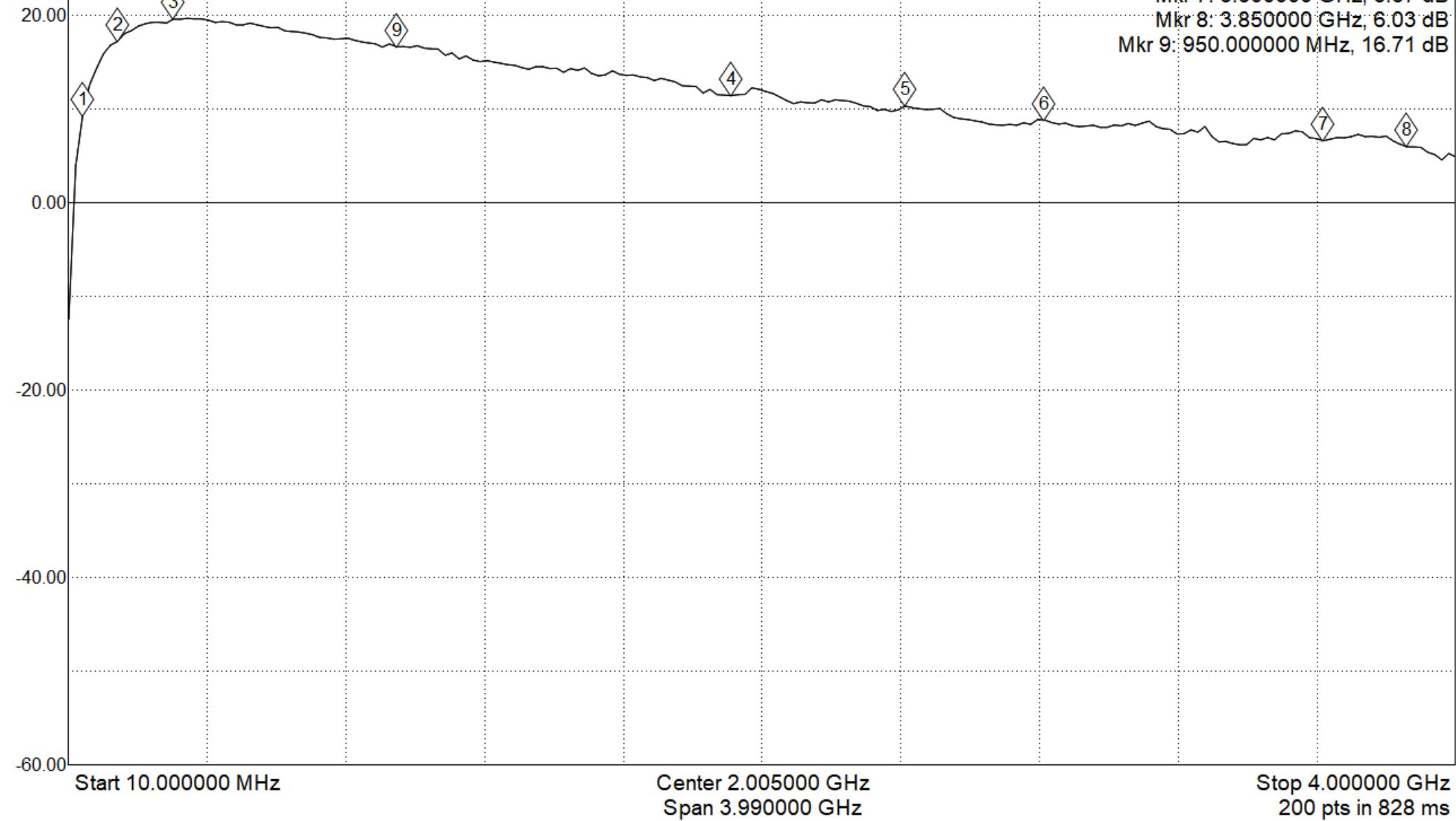
Atten --

VBW --

Ref 40.00 dB

Div 10.0

Mkr 1: 40.000000 MHz, 9.39 dB  
Mkr 2: 150.000000 MHz, 17.28 dB  
Mkr 3: 300.000000 MHz, 19.65 dB  
Mkr 4: 1.900000 GHz, 11.49 dB  
Mkr 5: 2.400000 GHz, 10.38 dB  
Mkr 6: 2.800000 GHz, 8.90 dB  
Mkr 7: 3.600000 GHz, 6.67 dB  
Mkr 8: 3.850000 GHz, 6.03 dB  
Mkr 9: 950.000000 MHz, 16.71 dB



# Overall CrowdSupply status

- HW design is finished and final prototypes are being manufactured
- Turned out some components are more expensive than expected
  - e.g. USB3 adapter mold cost is 3x the expected
  - We have to increase price
- Initial delivery date 31 May is unrealistic :(
  - Delivery date for TCXO is 26 July
  - Plus manufacturing, testing, shipping
  - End of August is what we're targeting

# XTRX future

- Single XTRX CS version will be split:
  - PRO: Bigger FPGA, 0.1ppm TCXO, industrial
  - Light: Smaller FPGA, ~1ppm TCXO, commercial
- XTRX is a framework for more products
- Maybe an M.2 version  
(but which form factor and which keying?)
- Maybe an XTRX with a PA

EOF