Basic Buck Converter — Step-Down DC–DC Conversion

This paper is part of the Power Electronics Learning Portfolio, a self-study documentation series.

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Abstract

This study examines the basic operation of a buck converter and the influence of circuit parameters on voltage regulation and transient response. Using PSIM simulation, output behavior under different duty ratios was analyzed to confirm the relationship between duty cycle and output voltage. The results highlight how inductance, capacitance, and startup conditions affect overshoot and ripple, providing fundamental design guidelines for stable DC–DC converter operation.

Introduction

In this experiment, a DC–DC buck converter was simulated to confirm its basic voltage step-down operation and to examine how circuit design influences overall converter behavior.
The study focuses on two main aspects:
(1) How the output voltage and inductor current respond to changes in the duty cycle (D = 0.3, 0.5, 0.7) under open-loop PWM control, and
(2) How circuit parameters such as inductance (L) and capacitance (C) affect voltage regulation, ripple, and transient response during startup.

The converter was modeled with a 50 V DC input and a resistive load, and the simulations were carried out using PSIM to observe waveform differences.
Through these comparisons, the study aims to clarify the relationship between design parameters and converter performance, providing foundational knowledge for future closed-loop control implementation and hardware design.

Basic Principle

Operating Modes

When the switch is ON:
The input voltage is applied to the inductor, and energy is stored in its magnetic field.

$$V_L = V_{in} - V_{out}$$

When the switch is OFF:
The inductor releases stored energy through the diode into the load, maintaining continuous current flow.

$$V_L = -V_{out}$$

The average output voltage is given by:

$$V_{out} = D * V_{in}$$

where D is the duty cycle.

Example: For $V_{in} = 50V$ and $D = 0.5, V_{out} \approx 25V$.

Circuit Parameters

PARAMETER	SYMBOL	VALUE	DESCRIPTION
INPUT VOLTAGE	(Vin)	50 V	Supply voltage
LOAD RESISTANCE	(R)	5Ω	Represents load
INDUCTOR	(L)	1 mH	Controls current ripple
CAPACITOR	(C)	100 µF	Smooths voltage ripple
SWITCHING FREQUENCY	(fs)	5 kHz	Determines ripple and loss
DUTY CYCLE	(D)	0.3 0.5 0.7	Target ratio

The parameters were selected to keep output voltage ripple below 10 % while ensuring stable operation and visible waveform characteristics.

Simulation Results

The PSIM simulation circuit is shown in Figure 1 The output voltage and inductor current are shown in **Error! Reference source not found.** and Figure 3

- The average output voltage stabilized around 25 V.
- When the duty cycle was changed to 0.3, 0.5, and 0.7, the output voltage increased proportionally with D.
- During startup with L = 1 mH and C = 100 µF, an overshoot appeared before reaching steady state.
- When L was increased to 5 mH and C reduced to 30–50 µF, the voltage rose smoothly without overshoot.
- These results confirmed the expected voltage–duty relationship and showed clear differences in waveform behavior depending on circuit parameters.

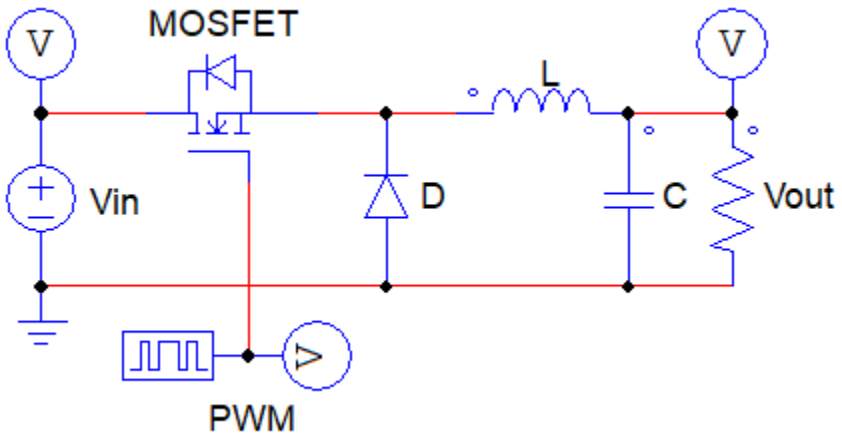

Figure 1

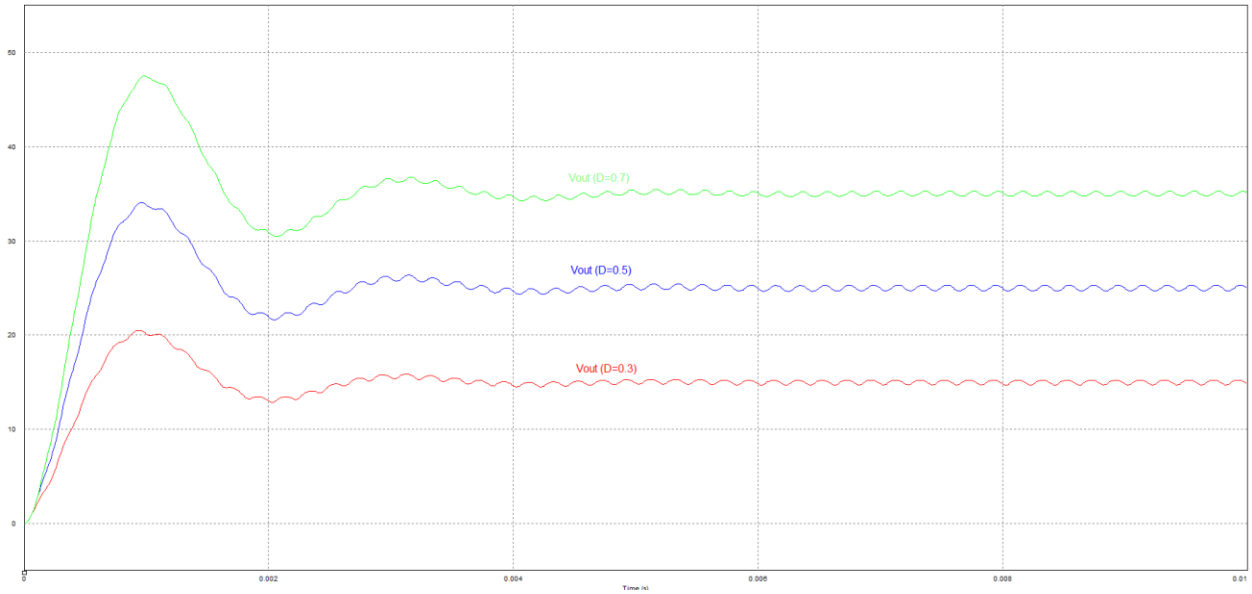

Figure 2 Comparison of output voltage waveforms at duty cycles D = 0.3, 0.5, and 0.7.

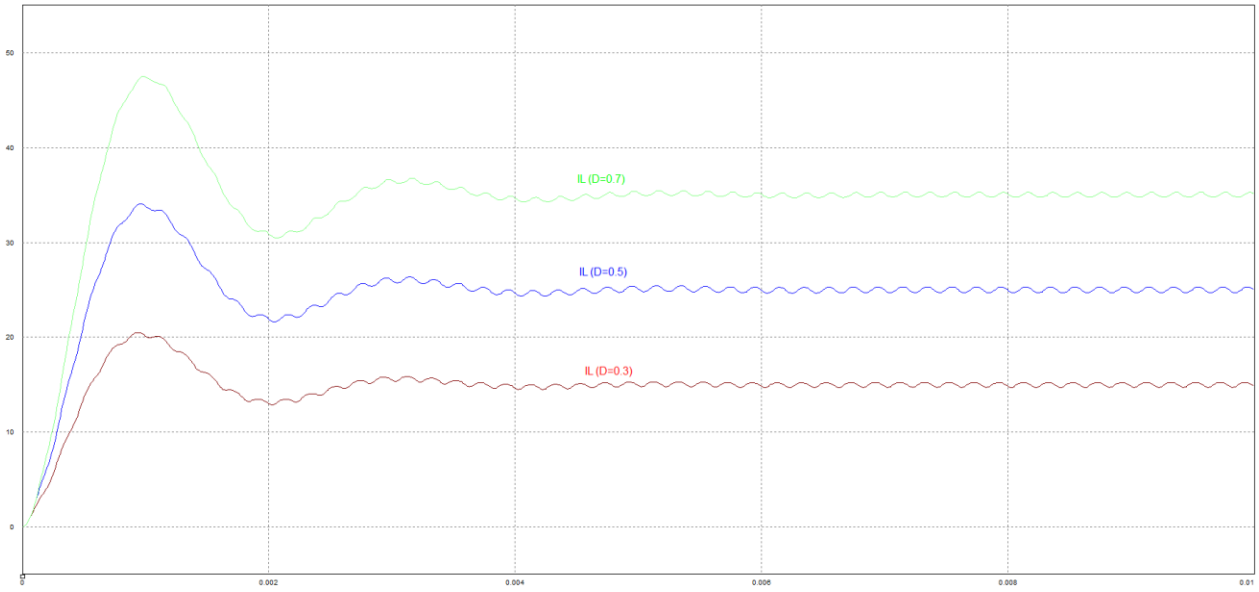

Figure 3 Comparison of inductor's current waveforms at duty cycles D = 0.3, 0.5, and 0.7.

Discussion

The simulation confirmed that as the duty cycle increased from 0.3 to 0.7, the output voltage rose proportionally. All three waveforms were captured in one window for comparison. The 0.3 duty case showed a stable and low output voltage, while the 0.5 and 0.7 cases produced higher voltages with gradually larger ripple.

During startup, the 1 mH and 100 µF setup caused a clear overshoot before settling to the steady value. When the inductance was changed to 5 mH and the capacitance reduced to 50 µF, the overshoot disappeared and the voltage rose smoothly as shown in Figure 4.

Overall, the difference between each condition showed that both the duty ratio and component values directly affected the waveform shape and transition behavior. The results were consistent and easy to observe in PSIM.

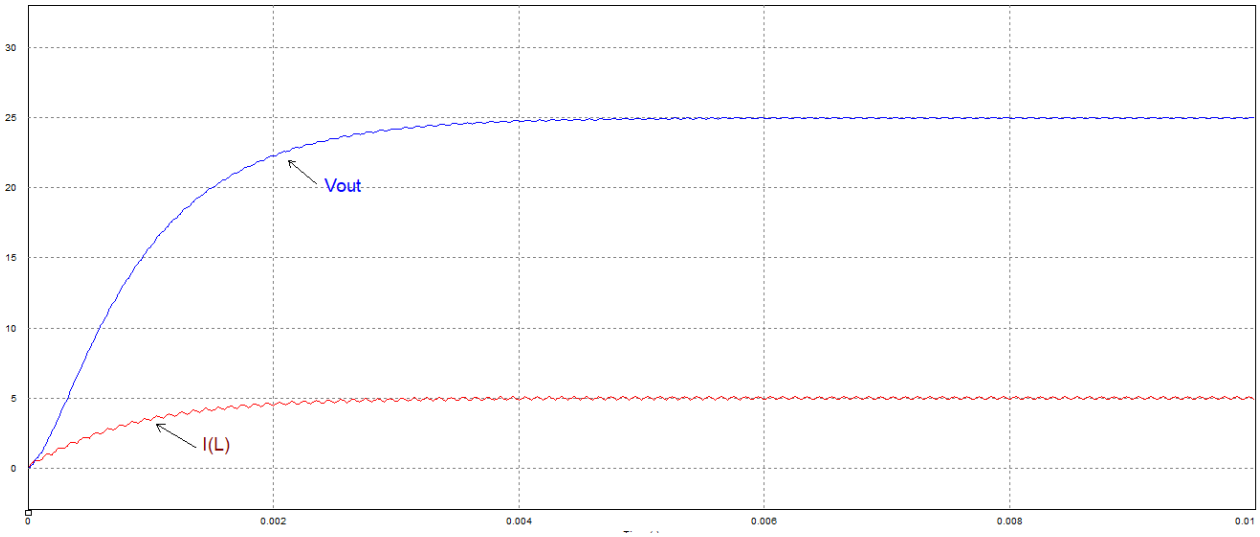

Figure 4

Conclusion

The PSIM simulation successfully confirmed the basic operation of the buck converter. The output voltage changed according to the duty cycle, and the difference between D = 0.3, 0.5, and 0.7 was clearly shown. Startup tests showed that changing inductance and capacitance also changed the voltage rise pattern. With smaller inductance and larger capacitance, overshoot occurred, while larger inductance and smaller capacitance produced a smoother startup.
These results clearly showed how converter output responds under different operating conditions.