# 数字系统设计作业报告

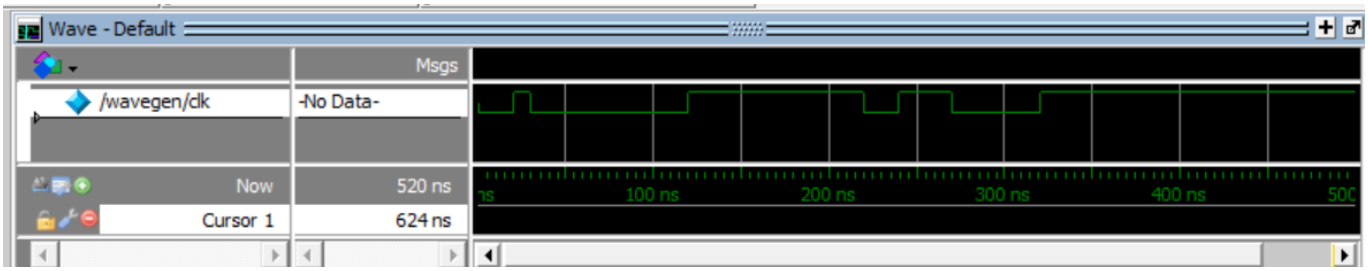

- 学号：518021910628
- 姓名：吴小茜


## EXP2-1

### 设计/测试模块

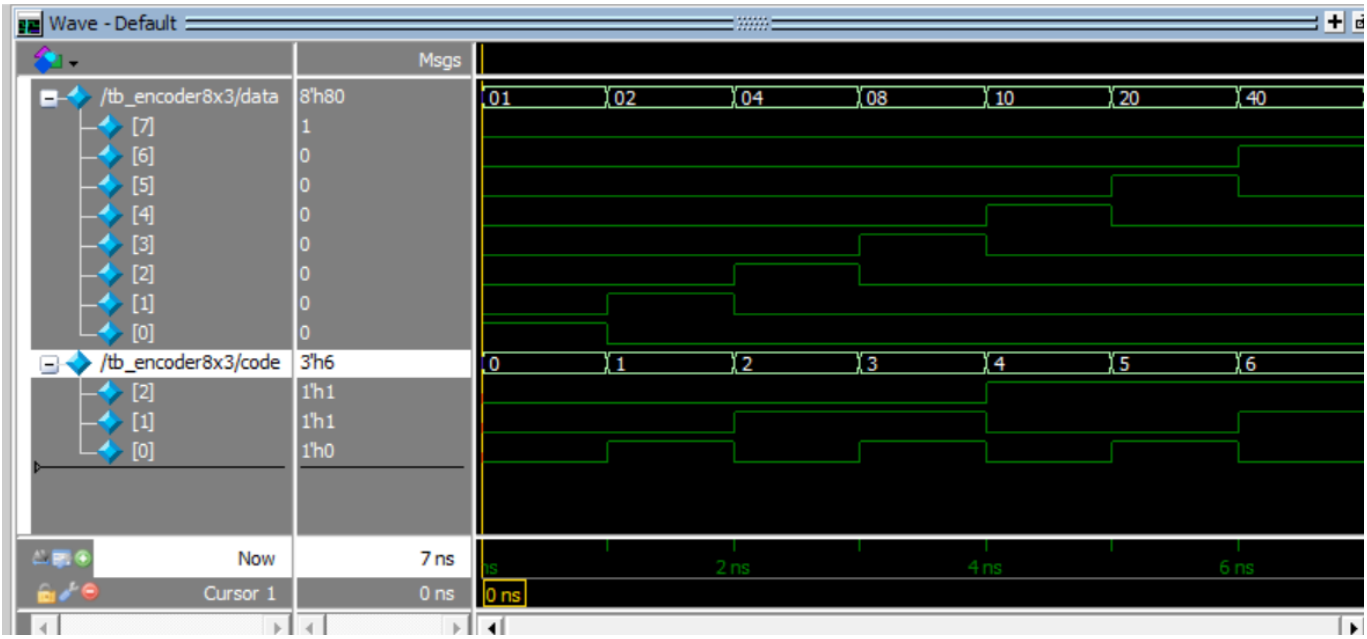
```
// File: wavegen.v

`timescale 10 ns / 1 ns

module wavegen;

    reg clk;

    initial begin
        clk = 1'b0;
        #2 clk = 1'b1;
        #1 clk = 1'b0;
        #9 clk = 1'b1;
        #10 clk = 1'b0;
        #2 clk = 1'b1;
        #3 clk = 1'b0;
        #5 clk = 1'b1;
    #20 $stop;
    end

endmodule
```

### 仿真结果




## EXP2-2

### 仿真结果




```
# At time     0, data=00000001, code=0
# At time     1, data=00000010, code=1
# At time     2, data=00000100, code=2
# At time     3, data=00001000, code=3
# At time     4, data=00010000, code=4
# At time     5, data=00100000, code=5
# At time     6, data=01000000, code=6
# At time     7, data=10000000, code=7

VSIM 50>
```