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Output for Project 3: Pipeline Datapath Simulator

///////////////////

// Clock Cycle 1 //

///////////////////

Before we copy the write side of pipeline registers to the read side

--------------------------------------------------------------------

IF/ID WRITE (written to by the IF stage):

     Inst = 0xA1020000  [sw  $2, 0($8)]

IF/ID READ (read by the ID stage):

     Inst = 0x00000000

ID/EX WRITE (written to by the ID stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 0

         ALUOp    = 0b0

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ReadReg1Value  = 0x00000000

     ReadReg2Value  = 0x00000000

     SE Offset     = 0x00000000

     WriteReg\_20\_16 = 0

     WriteReg\_15\_11 = 0

     Function       = 0x00

ID/EX READ (read by the EX stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 0

         ALUOp    = 0b0

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ReadReg1Value  = 0x00000000

     ReadReg2Value  = 0x00000000

     SE Offset     = 0x00000000

     WriteReg\_20\_16 = 0

     WriteReg\_15\_11 = 0

     Function       = 0x00

EX/MEM WRITE (written to by the EX stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     SBValue     = 0x00000000

     WriteRegNum = 0

EX/MEM READ (read by the MEM stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     SBValue     = 0x00000000

     WriteRegNum = 0

MEM/WB WRITE (written to by the MEM stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     LBDataValue = 0x00000000

     WriteRegNum = 0

MEM/WB READ (read by the WB stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     LBDataValue = 0x00000000

     WriteRegNum = 0

Registers:

----------

$0: 0x0

$1: 0x101

$2: 0x102

$3: 0x103

$4: 0x104

$5: 0x105

$6: 0x106

$7: 0x107

$8: 0x108

$9: 0x109

$10: 0x10A

$11: 0x10B

$12: 0x10C

$13: 0x10D

$14: 0x10E

$15: 0x10F

$16: 0x110

$17: 0x111

$18: 0x112

$19: 0x113

$20: 0x114

$21: 0x115

$22: 0x116

$23: 0x117

$24: 0x118

$25: 0x119

$26: 0x11A

$27: 0x11B

$28: 0x11C

$29: 0x11D

$30: 0x11E

$31: 0x11F

///////////////////

// Clock Cycle 2 //

///////////////////

Before we copy the write side of pipeline registers to the read side

--------------------------------------------------------------------

IF/ID WRITE (written to by the IF stage):

     Inst = 0x810AFFFC  [lw  $10, -4($8)]

IF/ID READ (read by the ID stage):

     Inst = 0xA1020000

ID/EX WRITE (written to by the ID stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 1

         ALUOp    = 0b0

         MemRead  = 0

         MemWrite = 1

         MemToReg = 0

         RegWrite = 0

     ReadReg1Value  = 0x00000108

     ReadReg2Value  = 0x00000102

     SE Offset     = 0x00000000

     WriteReg\_20\_16 = 2

     WriteReg\_15\_11 = 0

     Function       = 0x00

ID/EX READ (read by the EX stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 0

         ALUOp    = 0b0

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ReadReg1Value  = 0x00000000

     ReadReg2Value  = 0x00000000

     SE Offset     = 0x00000000

     WriteReg\_20\_16 = 0

     WriteReg\_15\_11 = 0

     Function       = 0x00

EX/MEM WRITE (written to by the EX stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     SBValue     = 0x00000000

     WriteRegNum = 0

EX/MEM READ (read by the MEM stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     SBValue     = 0x00000000

     WriteRegNum = 0

MEM/WB WRITE (written to by the MEM stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     LBDataValue = 0x00000000

     WriteRegNum = 0

MEM/WB READ (read by the WB stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     LBDataValue = 0x00000000

     WriteRegNum = 0

Registers:

----------

$0: 0x0

$1: 0x101

$2: 0x102

$3: 0x103

$4: 0x104

$5: 0x105

$6: 0x106

$7: 0x107

$8: 0x108

$9: 0x109

$10: 0x10A

$11: 0x10B

$12: 0x10C

$13: 0x10D

$14: 0x10E

$15: 0x10F

$16: 0x110

$17: 0x111

$18: 0x112

$19: 0x113

$20: 0x114

$21: 0x115

$22: 0x116

$23: 0x117

$24: 0x118

$25: 0x119

$26: 0x11A

$27: 0x11B

$28: 0x11C

$29: 0x11D

$30: 0x11E

$31: 0x11F

///////////////////

// Clock Cycle 3 //

///////////////////

Before we copy the write side of pipeline registers to the read side

--------------------------------------------------------------------

IF/ID WRITE (written to by the IF stage):

     Inst = 0x00831820  [add $3, $4, $3]

IF/ID READ (read by the ID stage):

     Inst = 0x810AFFFC

ID/EX WRITE (written to by the ID stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 1

         ALUOp    = 0b0

         MemRead  = 1

         MemWrite = 0

         MemToReg = 1

         RegWrite = 1

     ReadReg1Value  = 0x00000108

     ReadReg2Value  = 0x0000010A

     SE Offset     = 0xFFFFFFFC

     WriteReg\_20\_16 = 10

     WriteReg\_15\_11 = 31

     Function       = 0x3C

ID/EX READ (read by the EX stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 1

         ALUOp    = 0b0

         MemRead  = 0

         MemWrite = 1

         MemToReg = 0

         RegWrite = 0

     ReadReg1Value  = 0x00000108

     ReadReg2Value  = 0x00000102

     SE Offset     = 0x00000000

     WriteReg\_20\_16 = 2

     WriteReg\_15\_11 = 0

     Function       = 0x00

EX/MEM WRITE (written to by the EX stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 1

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000108

     SBValue     = 0x00000102

     WriteRegNum = 2

EX/MEM READ (read by the MEM stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     SBValue     = 0x00000000

     WriteRegNum = 0

MEM/WB WRITE (written to by the MEM stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     LBDataValue = 0x00000000

     WriteRegNum = 0

MEM/WB READ (read by the WB stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     LBDataValue = 0x00000000

     WriteRegNum = 0

Registers:

----------

$0: 0x0

$1: 0x101

$2: 0x102

$3: 0x103

$4: 0x104

$5: 0x105

$6: 0x106

$7: 0x107

$8: 0x108

$9: 0x109

$10: 0x10A

$11: 0x10B

$12: 0x10C

$13: 0x10D

$14: 0x10E

$15: 0x10F

$16: 0x110

$17: 0x111

$18: 0x112

$19: 0x113

$20: 0x114

$21: 0x115

$22: 0x116

$23: 0x117

$24: 0x118

$25: 0x119

$26: 0x11A

$27: 0x11B

$28: 0x11C

$29: 0x11D

$30: 0x11E

$31: 0x11F

///////////////////

// Clock Cycle 4 //

///////////////////

Before we copy the write side of pipeline registers to the read side

--------------------------------------------------------------------

IF/ID WRITE (written to by the IF stage):

     Inst = 0x01263820  [add $7, $9, $6]

IF/ID READ (read by the ID stage):

     Inst = 0x00831820

ID/EX WRITE (written to by the ID stage):

     Control Signals:

         RegDst   = 1

         ALUSrc   = 0

         ALUOp    = 0b10

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ReadReg1Value  = 0x00000104

     ReadReg2Value  = 0x00000103

     SE Offset     = 0x00001820

     WriteReg\_20\_16 = 3

     WriteReg\_15\_11 = 3

     Function       = 0x20

ID/EX READ (read by the EX stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 1

         ALUOp    = 0b0

         MemRead  = 1

         MemWrite = 0

         MemToReg = 1

         RegWrite = 1

     ReadReg1Value  = 0x00000108

     ReadReg2Value  = 0x0000010A

     SE Offset     = 0xFFFFFFFC

     WriteReg\_20\_16 = 10

     WriteReg\_15\_11 = 31

     Function       = 0x3C

EX/MEM WRITE (written to by the EX stage):

     Control Signals:

         MemRead  = 1

         MemWrite = 0

         MemToReg = 1

         RegWrite = 1

     ALUResult   = 0x00000104

     SBValue     = 0x0000010A

     WriteRegNum = 10

EX/MEM READ (read by the MEM stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 1

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000108

     SBValue     = 0x00000102

     WriteRegNum = 2

MEM/WB WRITE (written to by the MEM stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000108

     LBDataValue = 0x00000000

     WriteRegNum = 2

MEM/WB READ (read by the WB stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     LBDataValue = 0x00000000

     WriteRegNum = 0

Registers:

----------

$0: 0x0

$1: 0x101

$2: 0x102

$3: 0x103

$4: 0x104

$5: 0x105

$6: 0x106

$7: 0x107

$8: 0x108

$9: 0x109

$10: 0x10A

$11: 0x10B

$12: 0x10C

$13: 0x10D

$14: 0x10E

$15: 0x10F

$16: 0x110

$17: 0x111

$18: 0x112

$19: 0x113

$20: 0x114

$21: 0x115

$22: 0x116

$23: 0x117

$24: 0x118

$25: 0x119

$26: 0x11A

$27: 0x11B

$28: 0x11C

$29: 0x11D

$30: 0x11E

$31: 0x11F

///////////////////

// Clock Cycle 5 //

///////////////////

Before we copy the write side of pipeline registers to the read side

--------------------------------------------------------------------

IF/ID WRITE (written to by the IF stage):

     Inst = 0x01224820  [add $9, $9, $2]

IF/ID READ (read by the ID stage):

     Inst = 0x01263820

ID/EX WRITE (written to by the ID stage):

     Control Signals:

         RegDst   = 1

         ALUSrc   = 0

         ALUOp    = 0b10

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ReadReg1Value  = 0x00000109

     ReadReg2Value  = 0x00000106

     SE Offset     = 0x00003820

     WriteReg\_20\_16 = 6

     WriteReg\_15\_11 = 7

     Function       = 0x20

ID/EX READ (read by the EX stage):

     Control Signals:

         RegDst   = 1

         ALUSrc   = 0

         ALUOp    = 0b10

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ReadReg1Value  = 0x00000104

     ReadReg2Value  = 0x00000103

     SE Offset     = 0x00001820

     WriteReg\_20\_16 = 3

     WriteReg\_15\_11 = 3

     Function       = 0x20

EX/MEM WRITE (written to by the EX stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x00000207

     SBValue     = 0x00000103

     WriteRegNum = 3

EX/MEM READ (read by the MEM stage):

     Control Signals:

         MemRead  = 1

         MemWrite = 0

         MemToReg = 1

         RegWrite = 1

     ALUResult   = 0x00000104

     SBValue     = 0x0000010A

     WriteRegNum = 10

MEM/WB WRITE (written to by the MEM stage):

     Control Signals:

         MemToReg = 1

         RegWrite = 1

     ALUResult   = 0x00000104

     LBDataValue = 0x00000004

     WriteRegNum = 10

MEM/WB READ (read by the WB stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000108

     LBDataValue = 0x00000000

     WriteRegNum = 2

Registers:

----------

$0: 0x0

$1: 0x101

$2: 0x102

$3: 0x103

$4: 0x104

$5: 0x105

$6: 0x106

$7: 0x107

$8: 0x108

$9: 0x109

$10: 0x10A

$11: 0x10B

$12: 0x10C

$13: 0x10D

$14: 0x10E

$15: 0x10F

$16: 0x110

$17: 0x111

$18: 0x112

$19: 0x113

$20: 0x114

$21: 0x115

$22: 0x116

$23: 0x117

$24: 0x118

$25: 0x119

$26: 0x11A

$27: 0x11B

$28: 0x11C

$29: 0x11D

$30: 0x11E

$31: 0x11F

///////////////////

// Clock Cycle 6 //

///////////////////

Before we copy the write side of pipeline registers to the read side

--------------------------------------------------------------------

IF/ID WRITE (written to by the IF stage):

     Inst = 0x81180000  [lw  $24, 0($8)]

IF/ID READ (read by the ID stage):

     Inst = 0x01224820

ID/EX WRITE (written to by the ID stage):

     Control Signals:

         RegDst   = 1

         ALUSrc   = 0

         ALUOp    = 0b10

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ReadReg1Value  = 0x00000109

     ReadReg2Value  = 0x00000102

     SE Offset     = 0x00004820

     WriteReg\_20\_16 = 2

     WriteReg\_15\_11 = 9

     Function       = 0x20

ID/EX READ (read by the EX stage):

     Control Signals:

         RegDst   = 1

         ALUSrc   = 0

         ALUOp    = 0b10

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ReadReg1Value  = 0x00000109

     ReadReg2Value  = 0x00000106

     SE Offset     = 0x00003820

     WriteReg\_20\_16 = 6

     WriteReg\_15\_11 = 7

     Function       = 0x20

EX/MEM WRITE (written to by the EX stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x0000020F

     SBValue     = 0x00000106

     WriteRegNum = 7

EX/MEM READ (read by the MEM stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x00000207

     SBValue     = 0x00000103

     WriteRegNum = 3

MEM/WB WRITE (written to by the MEM stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x00000207

     LBDataValue = 0x00000004

     WriteRegNum = 3

MEM/WB READ (read by the WB stage):

     Control Signals:

         MemToReg = 1

         RegWrite = 1

     ALUResult   = 0x00000104

     LBDataValue = 0x00000004

     WriteRegNum = 10

Registers:

----------

$0: 0x0

$1: 0x101

$2: 0x102

$3: 0x103

$4: 0x104

$5: 0x105

$6: 0x106

$7: 0x107

$8: 0x108

$9: 0x109

$10: 0x4

$11: 0x10B

$12: 0x10C

$13: 0x10D

$14: 0x10E

$15: 0x10F

$16: 0x110

$17: 0x111

$18: 0x112

$19: 0x113

$20: 0x114

$21: 0x115

$22: 0x116

$23: 0x117

$24: 0x118

$25: 0x119

$26: 0x11A

$27: 0x11B

$28: 0x11C

$29: 0x11D

$30: 0x11E

$31: 0x11F

///////////////////

// Clock Cycle 7 //

///////////////////

Before we copy the write side of pipeline registers to the read side

--------------------------------------------------------------------

IF/ID WRITE (written to by the IF stage):

     Inst = 0x81510010  [lw  $17, 16($10)]

IF/ID READ (read by the ID stage):

     Inst = 0x81180000

ID/EX WRITE (written to by the ID stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 1

         ALUOp    = 0b0

         MemRead  = 1

         MemWrite = 0

         MemToReg = 1

         RegWrite = 1

     ReadReg1Value  = 0x00000108

     ReadReg2Value  = 0x00000118

     SE Offset     = 0x00000000

     WriteReg\_20\_16 = 24

     WriteReg\_15\_11 = 0

     Function       = 0x00

ID/EX READ (read by the EX stage):

     Control Signals:

         RegDst   = 1

         ALUSrc   = 0

         ALUOp    = 0b10

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ReadReg1Value  = 0x00000109

     ReadReg2Value  = 0x00000102

     SE Offset     = 0x00004820

     WriteReg\_20\_16 = 2

     WriteReg\_15\_11 = 9

     Function       = 0x20

EX/MEM WRITE (written to by the EX stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x0000020B

     SBValue     = 0x00000102

     WriteRegNum = 9

EX/MEM READ (read by the MEM stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x0000020F

     SBValue     = 0x00000106

     WriteRegNum = 7

MEM/WB WRITE (written to by the MEM stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x0000020F

     LBDataValue = 0x00000004

     WriteRegNum = 7

MEM/WB READ (read by the WB stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x00000207

     LBDataValue = 0x00000004

     WriteRegNum = 3

Registers:

----------

$0: 0x0

$1: 0x101

$2: 0x102

$3: 0x207

$4: 0x104

$5: 0x105

$6: 0x106

$7: 0x107

$8: 0x108

$9: 0x109

$10: 0x4

$11: 0x10B

$12: 0x10C

$13: 0x10D

$14: 0x10E

$15: 0x10F

$16: 0x110

$17: 0x111

$18: 0x112

$19: 0x113

$20: 0x114

$21: 0x115

$22: 0x116

$23: 0x117

$24: 0x118

$25: 0x119

$26: 0x11A

$27: 0x11B

$28: 0x11C

$29: 0x11D

$30: 0x11E

$31: 0x11F

///////////////////

// Clock Cycle 8 //

///////////////////

Before we copy the write side of pipeline registers to the read side

--------------------------------------------------------------------

IF/ID WRITE (written to by the IF stage):

     Inst = 0x00624022  [sub $8, $3, $2]

IF/ID READ (read by the ID stage):

     Inst = 0x81510010

ID/EX WRITE (written to by the ID stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 1

         ALUOp    = 0b0

         MemRead  = 1

         MemWrite = 0

         MemToReg = 1

         RegWrite = 1

     ReadReg1Value  = 0x00000004

     ReadReg2Value  = 0x00000111

     SE Offset     = 0x00000010

     WriteReg\_20\_16 = 17

     WriteReg\_15\_11 = 0

     Function       = 0x10

ID/EX READ (read by the EX stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 1

         ALUOp    = 0b0

         MemRead  = 1

         MemWrite = 0

         MemToReg = 1

         RegWrite = 1

     ReadReg1Value  = 0x00000108

     ReadReg2Value  = 0x00000118

     SE Offset     = 0x00000000

     WriteReg\_20\_16 = 24

     WriteReg\_15\_11 = 0

     Function       = 0x00

EX/MEM WRITE (written to by the EX stage):

     Control Signals:

         MemRead  = 1

         MemWrite = 0

         MemToReg = 1

         RegWrite = 1

     ALUResult   = 0x00000108

     SBValue     = 0x00000118

     WriteRegNum = 24

EX/MEM READ (read by the MEM stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x0000020B

     SBValue     = 0x00000102

     WriteRegNum = 9

MEM/WB WRITE (written to by the MEM stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x0000020B

     LBDataValue = 0x00000004

     WriteRegNum = 9

MEM/WB READ (read by the WB stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x0000020F

     LBDataValue = 0x00000004

     WriteRegNum = 7

Registers:

----------

$0: 0x0

$1: 0x101

$2: 0x102

$3: 0x207

$4: 0x104

$5: 0x105

$6: 0x106

$7: 0x20F

$8: 0x108

$9: 0x109

$10: 0x4

$11: 0x10B

$12: 0x10C

$13: 0x10D

$14: 0x10E

$15: 0x10F

$16: 0x110

$17: 0x111

$18: 0x112

$19: 0x113

$20: 0x114

$21: 0x115

$22: 0x116

$23: 0x117

$24: 0x118

$25: 0x119

$26: 0x11A

$27: 0x11B

$28: 0x11C

$29: 0x11D

$30: 0x11E

$31: 0x11F

///////////////////

// Clock Cycle 9 //

///////////////////

Before we copy the write side of pipeline registers to the read side

--------------------------------------------------------------------

IF/ID WRITE (written to by the IF stage):

     Inst = 0x00000000  [Unknown command $0, $0, $0]

IF/ID READ (read by the ID stage):

     Inst = 0x00624022

ID/EX WRITE (written to by the ID stage):

     Control Signals:

         RegDst   = 1

         ALUSrc   = 0

         ALUOp    = 0b10

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ReadReg1Value  = 0x00000207

     ReadReg2Value  = 0x00000102

     SE Offset     = 0x00004022

     WriteReg\_20\_16 = 2

     WriteReg\_15\_11 = 8

     Function       = 0x22

ID/EX READ (read by the EX stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 1

         ALUOp    = 0b0

         MemRead  = 1

         MemWrite = 0

         MemToReg = 1

         RegWrite = 1

     ReadReg1Value  = 0x00000004

     ReadReg2Value  = 0x00000111

     SE Offset     = 0x00000010

     WriteReg\_20\_16 = 17

     WriteReg\_15\_11 = 0

     Function       = 0x10

EX/MEM WRITE (written to by the EX stage):

     Control Signals:

         MemRead  = 1

         MemWrite = 0

         MemToReg = 1

         RegWrite = 1

     ALUResult   = 0x00000014

     SBValue     = 0x00000111

     WriteRegNum = 17

EX/MEM READ (read by the MEM stage):

     Control Signals:

         MemRead  = 1

         MemWrite = 0

         MemToReg = 1

         RegWrite = 1

     ALUResult   = 0x00000108

     SBValue     = 0x00000118

     WriteRegNum = 24

MEM/WB WRITE (written to by the MEM stage):

     Control Signals:

         MemToReg = 1

         RegWrite = 1

     ALUResult   = 0x00000108

     LBDataValue = 0x00000102

     WriteRegNum = 24

MEM/WB READ (read by the WB stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x0000020B

     LBDataValue = 0x00000004

     WriteRegNum = 9

Registers:

----------

$0: 0x0

$1: 0x101

$2: 0x102

$3: 0x207

$4: 0x104

$5: 0x105

$6: 0x106

$7: 0x20F

$8: 0x108

$9: 0x20B

$10: 0x4

$11: 0x10B

$12: 0x10C

$13: 0x10D

$14: 0x10E

$15: 0x10F

$16: 0x110

$17: 0x111

$18: 0x112

$19: 0x113

$20: 0x114

$21: 0x115

$22: 0x116

$23: 0x117

$24: 0x118

$25: 0x119

$26: 0x11A

$27: 0x11B

$28: 0x11C

$29: 0x11D

$30: 0x11E

$31: 0x11F

///////////////////

// Clock Cycle 10 //

///////////////////

Before we copy the write side of pipeline registers to the read side

--------------------------------------------------------------------

IF/ID WRITE (written to by the IF stage):

     Inst = 0x00000000  [Unknown command $0, $0, $0]

IF/ID READ (read by the ID stage):

     Inst = 0x00000000

ID/EX WRITE (written to by the ID stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 0

         ALUOp    = 0b0

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ReadReg1Value  = 0x00000000

     ReadReg2Value  = 0x00000000

     SE Offset     = 0x00000000

     WriteReg\_20\_16 = 0

     WriteReg\_15\_11 = 0

     Function       = 0x00

ID/EX READ (read by the EX stage):

     Control Signals:

         RegDst   = 1

         ALUSrc   = 0

         ALUOp    = 0b10

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ReadReg1Value  = 0x00000207

     ReadReg2Value  = 0x00000102

     SE Offset     = 0x00004022

     WriteReg\_20\_16 = 2

     WriteReg\_15\_11 = 8

     Function       = 0x22

EX/MEM WRITE (written to by the EX stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x00000105

     SBValue     = 0x00000102

     WriteRegNum = 8

EX/MEM READ (read by the MEM stage):

     Control Signals:

         MemRead  = 1

         MemWrite = 0

         MemToReg = 1

         RegWrite = 1

     ALUResult   = 0x00000014

     SBValue     = 0x00000111

     WriteRegNum = 17

MEM/WB WRITE (written to by the MEM stage):

     Control Signals:

         MemToReg = 1

         RegWrite = 1

     ALUResult   = 0x00000014

     LBDataValue = 0x00000014

     WriteRegNum = 17

MEM/WB READ (read by the WB stage):

     Control Signals:

         MemToReg = 1

         RegWrite = 1

     ALUResult   = 0x00000108

     LBDataValue = 0x00000102

     WriteRegNum = 24

Registers:

----------

$0: 0x0

$1: 0x101

$2: 0x102

$3: 0x207

$4: 0x104

$5: 0x105

$6: 0x106

$7: 0x20F

$8: 0x108

$9: 0x20B

$10: 0x4

$11: 0x10B

$12: 0x10C

$13: 0x10D

$14: 0x10E

$15: 0x10F

$16: 0x110

$17: 0x111

$18: 0x112

$19: 0x113

$20: 0x114

$21: 0x115

$22: 0x116

$23: 0x117

$24: 0x102

$25: 0x119

$26: 0x11A

$27: 0x11B

$28: 0x11C

$29: 0x11D

$30: 0x11E

$31: 0x11F

///////////////////

// Clock Cycle 11 //

///////////////////

Before we copy the write side of pipeline registers to the read side

--------------------------------------------------------------------

IF/ID WRITE (written to by the IF stage):

     Inst = 0x00000000  [Unknown command $0, $0, $0]

IF/ID READ (read by the ID stage):

     Inst = 0x00000000

ID/EX WRITE (written to by the ID stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 0

         ALUOp    = 0b0

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ReadReg1Value  = 0x00000000

     ReadReg2Value  = 0x00000000

     SE Offset     = 0x00000000

     WriteReg\_20\_16 = 0

     WriteReg\_15\_11 = 0

     Function       = 0x00

ID/EX READ (read by the EX stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 0

         ALUOp    = 0b0

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ReadReg1Value  = 0x00000000

     ReadReg2Value  = 0x00000000

     SE Offset     = 0x00000000

     WriteReg\_20\_16 = 0

     WriteReg\_15\_11 = 0

     Function       = 0x00

EX/MEM WRITE (written to by the EX stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     SBValue     = 0x00000000

     WriteRegNum = 0

EX/MEM READ (read by the MEM stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x00000105

     SBValue     = 0x00000102

     WriteRegNum = 8

MEM/WB WRITE (written to by the MEM stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x00000105

     LBDataValue = 0x00000014

     WriteRegNum = 8

MEM/WB READ (read by the WB stage):

     Control Signals:

         MemToReg = 1

         RegWrite = 1

     ALUResult   = 0x00000014

     LBDataValue = 0x00000014

     WriteRegNum = 17

Registers:

----------

$0: 0x0

$1: 0x101

$2: 0x102

$3: 0x207

$4: 0x104

$5: 0x105

$6: 0x106

$7: 0x20F

$8: 0x108

$9: 0x20B

$10: 0x4

$11: 0x10B

$12: 0x10C

$13: 0x10D

$14: 0x10E

$15: 0x10F

$16: 0x110

$17: 0x14

$18: 0x112

$19: 0x113

$20: 0x114

$21: 0x115

$22: 0x116

$23: 0x117

$24: 0x102

$25: 0x119

$26: 0x11A

$27: 0x11B

$28: 0x11C

$29: 0x11D

$30: 0x11E

$31: 0x11F

///////////////////

// Clock Cycle 12 //

///////////////////

Before we copy the write side of pipeline registers to the read side

--------------------------------------------------------------------

IF/ID WRITE (written to by the IF stage):

     Inst = 0x00000000  [Unknown command $0, $0, $0]

IF/ID READ (read by the ID stage):

     Inst = 0x00000000

ID/EX WRITE (written to by the ID stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 0

         ALUOp    = 0b0

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ReadReg1Value  = 0x00000000

     ReadReg2Value  = 0x00000000

     SE Offset     = 0x00000000

     WriteReg\_20\_16 = 0

     WriteReg\_15\_11 = 0

     Function       = 0x00

ID/EX READ (read by the EX stage):

     Control Signals:

         RegDst   = 0

         ALUSrc   = 0

         ALUOp    = 0b0

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ReadReg1Value  = 0x00000000

     ReadReg2Value  = 0x00000000

     SE Offset     = 0x00000000

     WriteReg\_20\_16 = 0

     WriteReg\_15\_11 = 0

     Function       = 0x00

EX/MEM WRITE (written to by the EX stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     SBValue     = 0x00000000

     WriteRegNum = 0

EX/MEM READ (read by the MEM stage):

     Control Signals:

         MemRead  = 0

         MemWrite = 0

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     SBValue     = 0x00000000

     WriteRegNum = 0

MEM/WB WRITE (written to by the MEM stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 0

     ALUResult   = 0x00000000

     LBDataValue = 0x00000014

     WriteRegNum = 0

MEM/WB READ (read by the WB stage):

     Control Signals:

         MemToReg = 0

         RegWrite = 1

     ALUResult   = 0x00000105

     LBDataValue = 0x00000014

     WriteRegNum = 8

Registers:

----------

$0: 0x0

$1: 0x101

$2: 0x102

$3: 0x207

$4: 0x104

$5: 0x105

$6: 0x106

$7: 0x20F

$8: 0x105

$9: 0x20B

$10: 0x4

$11: 0x10B

$12: 0x10C

$13: 0x10D

$14: 0x10E

$15: 0x10F

$16: 0x110

$17: 0x14

$18: 0x112

$19: 0x113

$20: 0x114

$21: 0x115

$22: 0x116

$23: 0x117

$24: 0x102

$25: 0x119

$26: 0x11A

$27: 0x11B

$28: 0x11C

$29: 0x11D

$30: 0x11E

$31: 0x11F