# **Hex Buffer**

The MC14049B Hex Inverter/Buffer and MC14050B Noninverting Hex Buffer are constructed with MOS P-Channel and N-Channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic level conversion using only one supply voltage,  $V_{\rm DD}$ .

The input–signal high level ( $V_{IH}$ ) can exceed the  $V_{DD}$  supply voltage for logic level conversions. Two TTL/DTL loads can be driven when the devices are used as a CMOS–to–TTL/DTL converter ( $V_{DD}$  = 5.0 V,  $V_{OL} \leq$  0.4 V,  $I_{OL} \geq$  3.2 mA).

Note that pins 13 and 16 are not connected internally on these devices; consequently connections to these terminals will not affect circuit operation.

## **Features**

- High Source and Sink Currents
- High-to-Low Level Converter
- Supply Voltage Range = 3.0 V to 18 V
- V<sub>IN</sub> can exceed V<sub>DD</sub>
- Meets JEDEC B Specifications
- Improved ESD Protection On All Inputs
- These Devices are Pb-Free and are RoHS Compliant

## MAXIMUM RATINGS (Voltages Referenced to V<sub>SS</sub>)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage Range	-0.5 to +18.0	V
V <sub>in</sub>	Input Voltage Range (DC or Transient)	-0.5 to +18.0	V
V <sub>out</sub>	Output Voltage Range (DC or Transient)	-0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub>	Input Current (DC or Transient) per Pin	±10	mA
l <sub>out</sub>	Output Current (DC or Transient) per Pin	±45	mA
P <sub>D</sub>	Power Dissipation, per Package (Note 1) (Plastic) (SOIC)	825 740	mW
T <sub>A</sub>	Ambient Temperature Range	-55 to +125	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8-Second Soldering)	260	°C

1. Temperature Derating: See Figure 3.

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields referenced to the  $V_{SS}$  pin only. Extra precautions must be taken to avoid applications of any voltage higher than the maximum rated voltages to this high–impedance circuit. For proper operation, the ranges  $V_{SS} \leq V_{in} \leq 18$  V and  $V_{SS} \leq V_{out} \leq V_{DD}$  are recommended.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.



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## MARKING DIAGRAMS

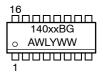


PDIP-16 P SUFFIX CASE 648





SOIC-16 D SUFFIX CASE 751B





TSSOP-16 DT SUFFIX CASE 948F





SOEIAJ-16 F SUFFIX CASE 966



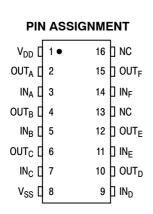
xx = Specific Device Code A = Assembly Location

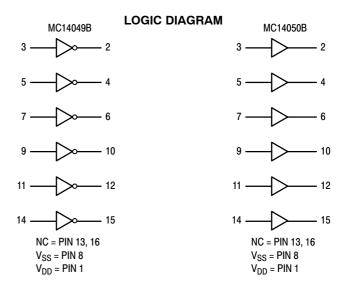
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or = Pb-Free Indicator

(Note: Microdot may be in either location)

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.





## **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC14049BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14049BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14049BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC14049BFELG	SOEIAJ-16 (Pb-Free)	2000 Units / Tape & Reel
MC14050BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14050BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14050BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC14050BDTG	TSSOP-16* (Pb-Free)	96 Units / Rail
MC14050BDTR2G	TSSOP-16* (Pb-Free)	2500 Units / Tape & Reel
MC14050BFELG	SOEIAJ-16 (Pb-Free)	2000 Units / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*</sup>This package is inherently Pb-Free.

# **ELECTRICAL CHARACTERISTICS** (Voltages Referenced to V<sub>SS</sub>)

			.,	- 5	5°C		+ 25°C		+ 12	.5°C	
Characterist	ic	Symbol	V <sub>DD</sub> Vdc	Min	Max	Min	Typ (Note 2)	Max	Min	Max	Unit
Output Voltage V <sub>in</sub> = V <sub>DD</sub>	"0" Level	V <sub>OL</sub>	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
V <sub>in</sub> = 0	"1" Level	V <sub>OH</sub>	5.0 10 15	4.95 9.95 14.95		4.95 9.95 14.95	5.0 10 15		4.95 9.95 14.95		Vdc
Input Voltage $ (V_O = 4.5 \text{ Vdc}) $ $ (V_O = 9.0 \text{ Vdc}) $ $ (V_O = 13.5 \text{ Vdc}) $	"0" Level	V <sub>IL</sub>	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ Vdc})$ $(V_O = 1.0 \text{ Vdc})$ $(V_O = 1.5 \text{ Vdc})$	"1" Level	V <sub>IH</sub>	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- - -	3.5 7.0 11	- - -	Vdc
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source	I <sub>OH</sub>	5.0 10 15	- 1.6 - 1.6 - 4.7	- - -	- 1.25 - 1.30 - 3.75	- 2.5 - 2.6 - 10	- - -	- 1.0 - 1.0 - 3.0	- - -	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	Sink	I <sub>OL</sub>	5.0 10 15	3.75 10 30	- - -	3.2 8.0 24	6.0 16 40	- - -	2.6 6.6 19	- - -	mAdc
Input Current		l <sub>in</sub>	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Capacitance (Vin =	= 0)	C <sub>in</sub>	-	-	_	-	10	20	-	-	pF
Quiescent Current (Per	Package)	I <sub>DD</sub>	5.0 10 15	- - -	1.0 2.0 4.0	- - -	0.002 0.004 0.006	1.0 2.0 4.0	- - -	30 60 120	μAdc
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, per package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching		I <sub>T</sub>	5.0 10 15			$I_T = (3)$	1.8 μΑ/kHz) f 3.5 μΑ/kHz) f 5.3 μΑ/kHz) f	+ I <sub>DD</sub>			μAdc

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
 The formulas given are for the typical characteristics only at + 25°C
 To calculate total supply current at loads other than 50 pF:

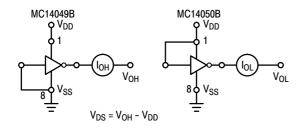
$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

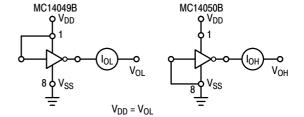
Where:  $I_T$  is in  $\mu A$  (per Package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts, f in kHz is input frequency and k = 0.002.

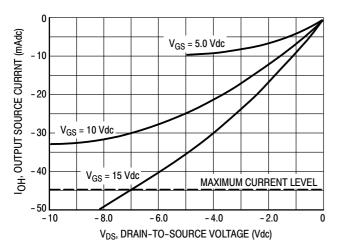
# AC SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50 \text{ pF}, T_A = +25^{\circ}\text{C}$ )

Characteristic	Symbol	V <sub>DD</sub> Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time	t <sub>TLH</sub>	5.0		100	100	ns
$t_{TLH} = (0.7 \text{ ns/pF}) C_L + 65 \text{ ns}$ $t_{TLH} = (0.25 \text{ ns/pF}) C_L + 37.5 \text{ ns}$		5.0 10	_	100 50	160 80	
$t_{TLH} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$		15	_	40	60	
Output Fall Time	t <sub>THL</sub>					ns
$t_{THL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$		5.0	-	40	60	
$t_{THL} = (0.06 \text{ ns/pF}) C_L + 17 \text{ ns}$		10	-	20	40	
$t_{THL} = (0.04 \text{ ns/pF}) C_L + 13 \text{ ns}$		15	-	15	30	
Propagation Delay Time	t <sub>PLH</sub>					ns
$t_{PLH} = (0.33 \text{ ns/pF}) C_L + 63.5 \text{ ns}$		5.0	_	80	140	
$t_{PLH} = (0.19 \text{ ns/pF}) C_L + 30.5 \text{ ns}$		10	-	40	80	
$t_{PLH} = (0.06 \text{ ns/pF}) C_L + 27 \text{ ns}$		15	-	30	60	
Propagation Delay Time	t <sub>PHL</sub>					ns
$t_{PHL} = (0.2 \text{ ns/pF}) C_L + 30 \text{ ns}$		5.0	-	40	80	
$t_{PHL} = (0.1 \text{ ns/pF}) C_L + 15 \text{ ns}$		10	-	20	40	
$t_{PHL} = (0.05 \text{ ns/pF}) C_L + 12.5 \text{ ns}$		15	_	15	30	

- 5. The formulas given are for the typical characteristics only at 25°C.
  6. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.







**Figure 1. Typical Output Source Characteristics** 

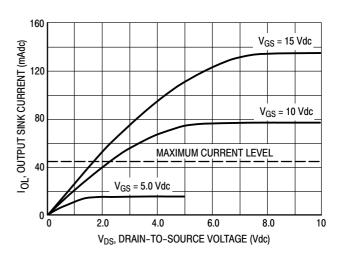


Figure 2. Typical Output Sink Characteristics

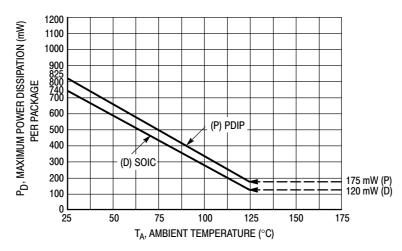


Figure 3. Ambient Temperature Power Derating

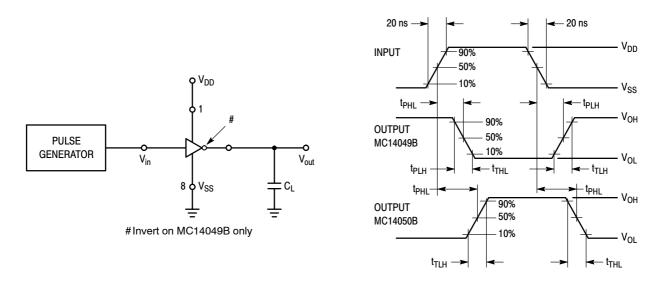
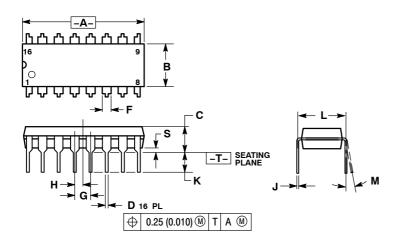


Figure 4. Switching Time Test Circuit and Waveforms

# **PACKAGE DIMENSIONS**

PDIP-16 **P SUFFIX** PLASTIC DIP PACKAGE CASE 648-08 ISSUE T

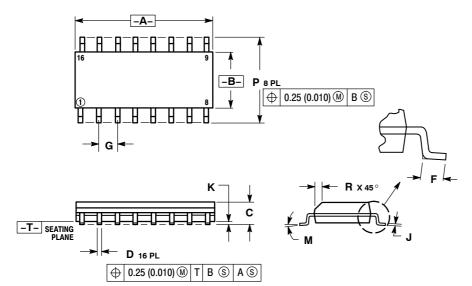


- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.740	0.770	18.80	19.55
В	0.250	0.270	6.35	6.85
С	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100	BSC	2.54	BSC
Н	0.050	BSC	1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
М	0°	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

# **PACKAGE DIMENSIONS**

## SOIC-16 **D SUFFIX** PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE K



- NOTES:

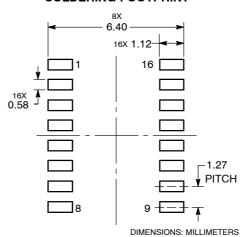
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  2. CONTROLLING DIMENSION: MILLIMETER.

  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTEINING AND B DO NOT INCLUDE MOLD PROTEINING AND B DO NOT INCLUDE MOLD
- PROTRUSION.
  MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

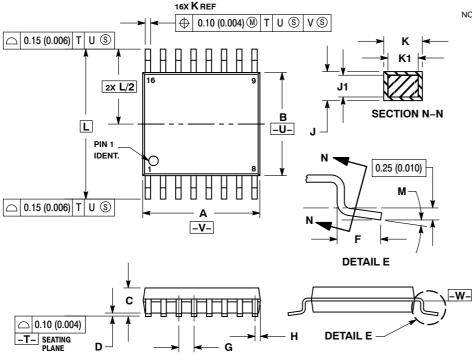
## **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### PACKAGE DIMENSIONS

## TSSOP-16 **DT SUFFIX** PLASTIC TSSOP PACKAGE CASE 948F-01 **ISSUE B**



#### NOTES:

- JIES:

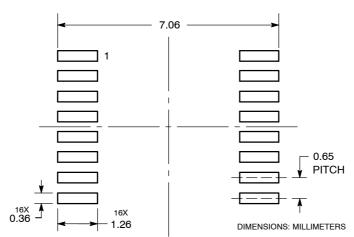
  1. DIMENSIONING AND TOLERANCING PER
  ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD
  FLASH. PROTRUSIONS OR GATE BURRS.
  MOLD FLASH OR GATE BURRS SHALL NOT
  EXCEED 15 (2008) DED SIDE.
- MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
- DAMIDAR PHOTRUSION. ALLOWABLE
  DAMBAR PROTRUSION SHALL BE 0.08
  (0.003) TOTAL IN EXCESS OF THE K
  DIMENSION AT MAXIMUM MATERIAL
  CONDITION.
- CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
O		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026 BSC	
Н	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
Κ	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252	BSC
M	0°	8°	0°	8 °

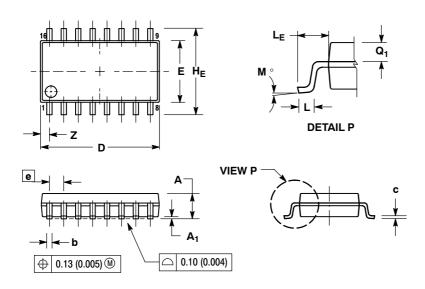
#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### PACKAGE DIMENSIONS

## SOEIAJ-16 **F SUFFIX** PLASTIC EIAJ SOIC PACKAGE CASE 966-01 **ISSUE A**



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

  CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS D AND E DO NOT INCLUDE
  MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.

  DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE
  BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

	MILLIMETERS		INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
C	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
Е	5.10	5.45	0.201	0.215
е	1.27 BSC		0.050	BSC
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10°	0 °	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z		0.78		0.031

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