National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM741-X REV 1A0

Original Creation Date: 08/07/95
Last Update Date: 10/22/99
Last Major Revision Date: 10/07/99

OPERATIONAL AMPLIFIER

General Description

The LM741 is a general purpose operational amplifier which features improved performance over industry standards such as the LM709. It is a direct, plug-in replacement for the LM709, LM101, MC1439 and LM748 in most applications.

The amplifier offers many features which make application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

Industry Part Number

LM741

Prime Die

LM741

NS Part Numbers

LM741H/883
LM741J/883
LM741W/883
LM741WG/883

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage		±22V
Power Dissipation (Note 2)		500mW
Differential Input Voltage		±30V
Input Voltage (Note 3)		±15V
Output Short Circuit Duration		Continuous
Operating Temperature Range		-55 C to +125 C
Storage Temperature Range		-65 C to +150 C
Maximum Junction Temperature		150 C
Lead Temperatuer (Soldering, 10 seconds)		300 C
Thermal Resistance ThetaJA		
Metal Can	(Still Air)	167 C/W
Metal Can	(500LF/Min Air Flow)	100 C/W
CERDIP	(Still Air)	TBD
CERDIP	(500LF/Min Air Flow)	TBD
CERPACK	(Still Air)	228 C/W
CERPACK	(500LF/Min Air Flow)	154 C/W
CERAMIC SOIC	(Still Air)	228 C/W
CERAMIC SOIC	(500LF/Min Air Flow)	154 C/W
ThetaJC		
Metal Can		44 C/W
CERDIP		TBD
CERPACK		27 C/W
CERAMIC SOIC		27 C/W
Package Weight (Typcial)		
Metal Can		TBD
CERDIP		TBD
CERPACK		TBD
CERAMIC SOIC		TBD
ESD Tolerance (Note 4)		400V

Note 1: Absolute maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperature and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) /ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: Human body model, 1.5K Ohms in series with 100pF.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Vcm = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage	Vcm = -12V			-5	5	mV	1
					-6	6	mV	2, 3
		Vcm = 12V			-5	5	mV	1
					-6	6	mV	2, 3
					-5	5	mV	1
					-6	6	mV	2, 3
		+Vcc = ±5V			-5	5	mV	1
					-6	6	mV	2, 3
Vio(adj)-	Offset Null					-6	mV	1, 2, 3
Vio(adj)+	Offset Null				6		mV	1, 2, 3
Iio	Input Offset Current	Vcm = -12V			-200	200	nA	1
					-500	500	nA	2, 3
		Vcm = 12V			-200	200	nA	1
					-500	500	nA	2, 3
					-200	200	nA	1
					-500	500	nA	2, 3
		Vcc = ±5V			-200	200	nA	1
					-500	500	nA	2, 3
+Iib	Input Bias Current	Vcm = -12V			0	500	nA	1
					0	1500	nA	2, 3
		Vcm = 12V			0	500	nA	1
					0	1500	nA	2, 3
					0	500	nA	1
					0	1500	nA	2, 3
		Vcc = ±5V			0	500	mA	1
					0	1500	nA	2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Vcm = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
-Iib	Input Bias Current	Vcm = -12V			0	500	nA	1
					0	1500	nA	2, 3
		Vcm = 12V			0	500	nA	1
					0	1500	nA	2, 3
					0	500	nA	1
					0	1500	nA	2, 3
		Vcc = ±5V			0	500	nA	1
					0	1500	nA	2, 3
Icc	Power Supply Current					2.8	mA	1
						2.5	mA	2
						3.5	mA	3
Avs+	Open Loop Voltage Gain	Rl = 2K, Vo = 0 to 10V	3		50		V/mV	1
			3		25		V/mV	2, 3
Avs-	Open Loop Voltage Gain	Rl = 2K, Vo = 0 to -10V	3		50		V/mV	1
			3		25		V/mV	2, 3
PSRR+	Power Supply Rejection Ratio	+Vcc = 15V to 5V, -Vcc = -15V			77		dB	1, 2, 3
PSRR-	Power Supply Rejection Ratio	-Vcc = -15V to -5V, +Vcc = +15V			77		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	-12V ≤ Vcm ≤ 12V			70		dB	1, 2, 3
Ios+	Output Short Circuit Current				-45	-5	mA	1, 2
					-50	-5	mA	3
Ios-	Output Short Circuit Current				5	45	mA	1, 2
					5	50	mA	3
Vopp+	Output Voltage Swing	Rl = 10K Ohms			12		V	1, 2, 3
		Rl = 2K Ohms			10		V	1, 2, 3
		Vcc = ±20V, Rl = 10K Ohms			16		V	1, 2, 3
		Vcc = ±20V, Rl = 2K Ohms			15		V	1, 2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Vcm = 0

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vopp-	Output Voltage Swing	Rl = 10K Ohms				-12	V	1, 2, 3
		Rl = 2K Ohms				-10	V	1, 2, 3
		Vcc = ±20V, Rl = 10K Ohms				-16	V	1, 2, 3
		Vcc = ±20V, Rl = 2K Ohms				-15	V	1, 2, 3
Rin	Input Resistance		2		0.3		MOhm	1
Vin	Input Voltage Range	Vcc = ±15V	1		±12		V	1, 2, 3
Vout	Output Voltage Swing	Vcc = ±5V	2		±2		V	1, 2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = ±15V, Vcm = 0

Sr+	Slew Rate	Vin = -5V to 5V, Av =1, Rl = 2K Ohms				0.2	V/uS	7
Sr-	Slew Rate	Vin = 5V to -5V, Av =1, Rl = 2K Ohms				0.2	V/uS	7
tr	Rise Time	Test on LTX, Rl = 2K Ohms, Av = 1, Cl = 100pF				1	uS	7
os	Overshoot	Test on LTX, Rl = 2K Ohms, Av = 1, Cl = 100pF				30	%	7
Gbw	Gain Bandwidth	Vin = 50Vrms, F = 20KHz, Rl = 2K			250		KHz	

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = ±15V, Vcm = 0V. "Deltas not required on B-Level product. Deltas required for S-Level product ONLY as specified on Internal Processing Instructions (IPI)."

Vio	Input Offset Voltage				-1	1	mV	1
Iio	Input Offset Current				-20	20	nA	1
Iib+	Input Bias Current				-50	50	nA	1
Iib-	Input Bias Current				-50	50	nA	1

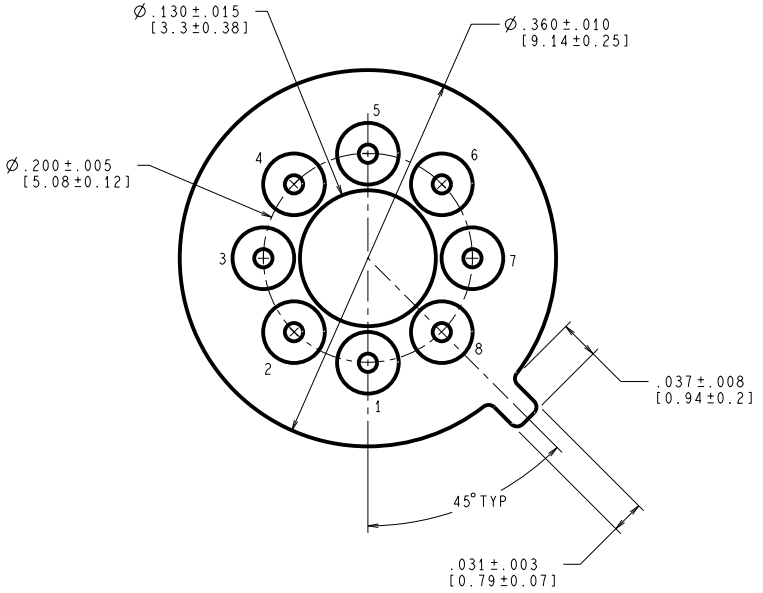
Note 1: Guaranteed by CMRR, Iib, Iio, Vio
Note 2: Guaranteed parameter not tested.
Note 3: Datalog reading in K = V/mV.

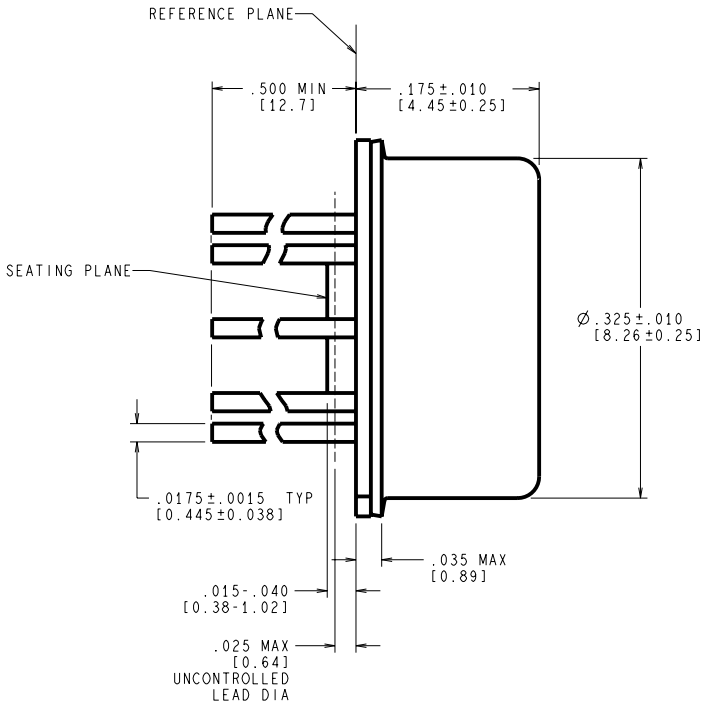
Graphics and Diagrams

GRAPHICS#	DESCRIPTION
05309HRB2	CERDIP (J), 14 LEAD (B/I CKT)
08337HRB2	CERPACK (W), 10 LEAD (B/I CKT)
09384HRA4	METAL CAN, (H) TO-99,8 LEAD,.200 DIA P.C.(B/I CKT)
09413HRB1	CERDIP (J), 8 LEAD (B/I CKT)
H08CRF	METAL CAN (H), TO-99, 8LD, .200 DIA P.C. (P/P DWG)
J08ARL	CERDIP (J), 8 LEAD (P/P DWG)
P000278A	METAL CAN (H), TO-99, 8 LD, .200 DIA P.C. (PINOUT)
P000280A	CERPACK (W), 10 LEAD (PINOUT)
P000291A	CERDIP (J), 8 LEAD (PINOUT)
P000466A	CERAMIC SOIC (WG), 10 LEAD (PINOUT)
W10ARG	CERPACK (W), 10 LEAD (P/P DWG)
WG10ARC	CERAMIC SOIC (WG), 10 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE & REDRAW PER CURRENT STANDARD; UPDATE MIL/AERO STAMP & TITLE.	11002	06/22/95	MS/





CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

MIL-I-38535
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEADS TO BE LOCATED WITHIN .007 IN/ 0.18 mm OF THEIR TRUE POSITIONS RELATIVE TO A MAXIMUM WIDTH TAB.
2. STANDARD METAL CAN TYPE: SOLID BASE WITH CERAMIC STANDOFF.
3. APPLIES TO MIL-AERO AND LINEAR PRODUCTS.
4. REFERENCE JEDEC REGISTRATION TO-99, JEDEC PUBLICATION No.95.

APPROVALS	DATE
DRAWN: MARTA SUCHY	06/22/95
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

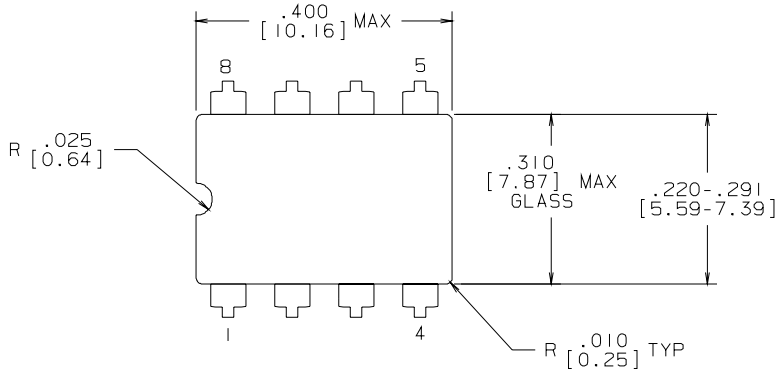
METAL CAN, TO-99, 8 LEAD, .200 DIA P.C.

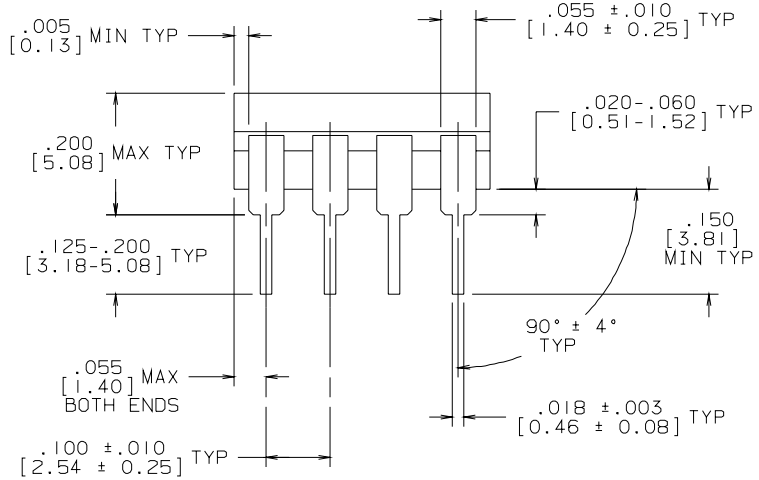
PROJECTION — INCH [MM]

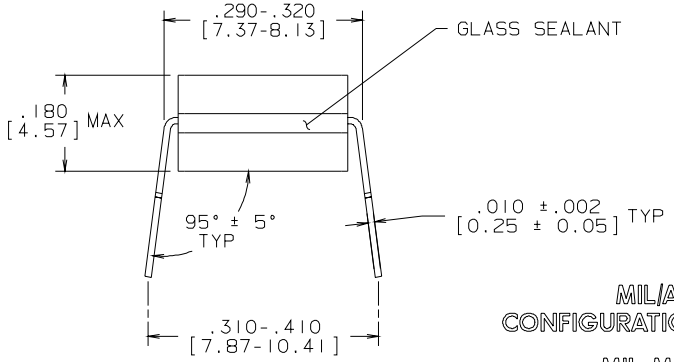
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-H08C	F

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
L	REVISE PER CURRENT STD; REDRAW	10002	09/21/93	TL/







MIL/AERO
CONFIGURATION CONTROL

MIL-M-38510
CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AA, DATED 04/1981.

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN T. LEQUANG	09/21/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

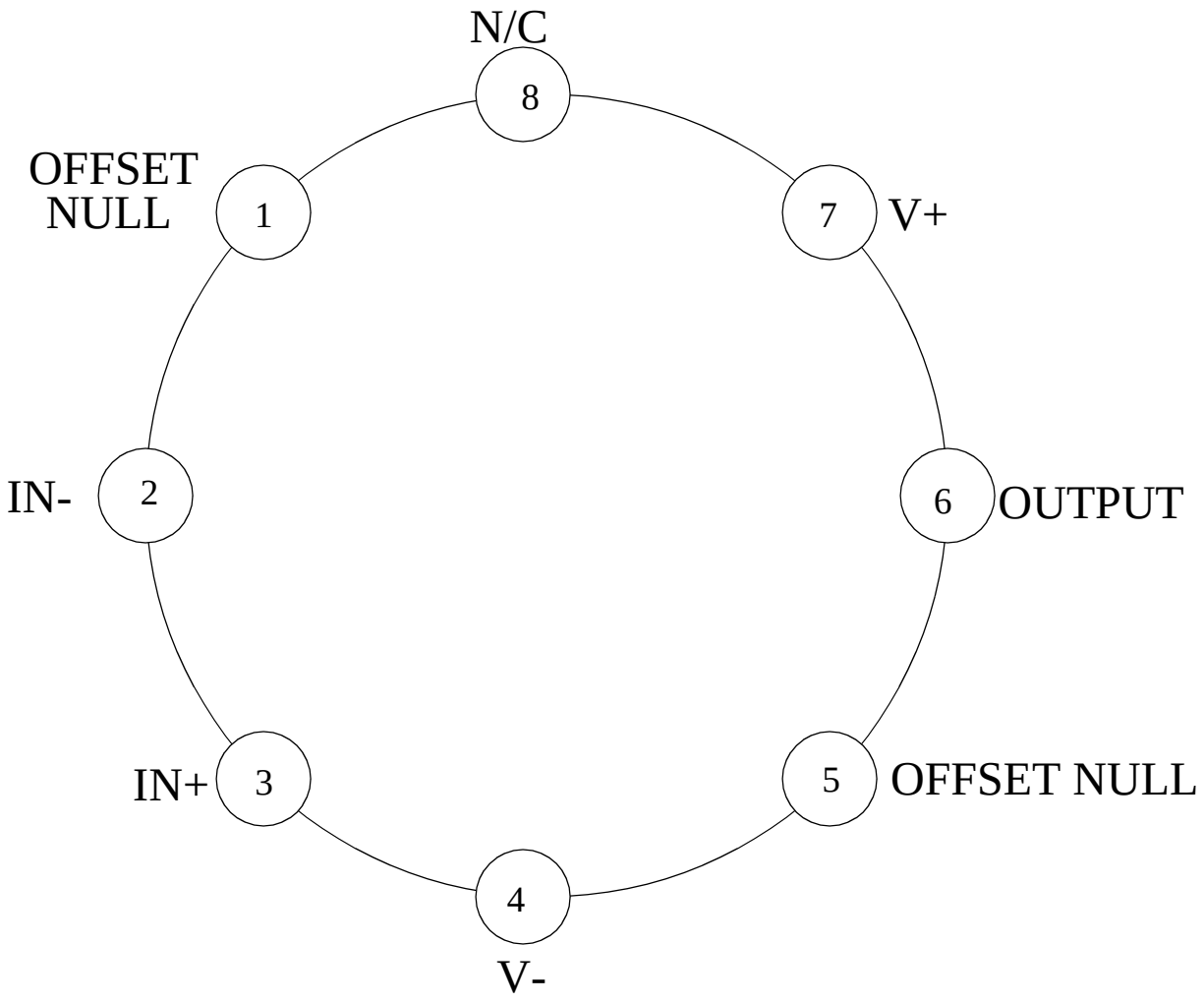
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 8 LEAD

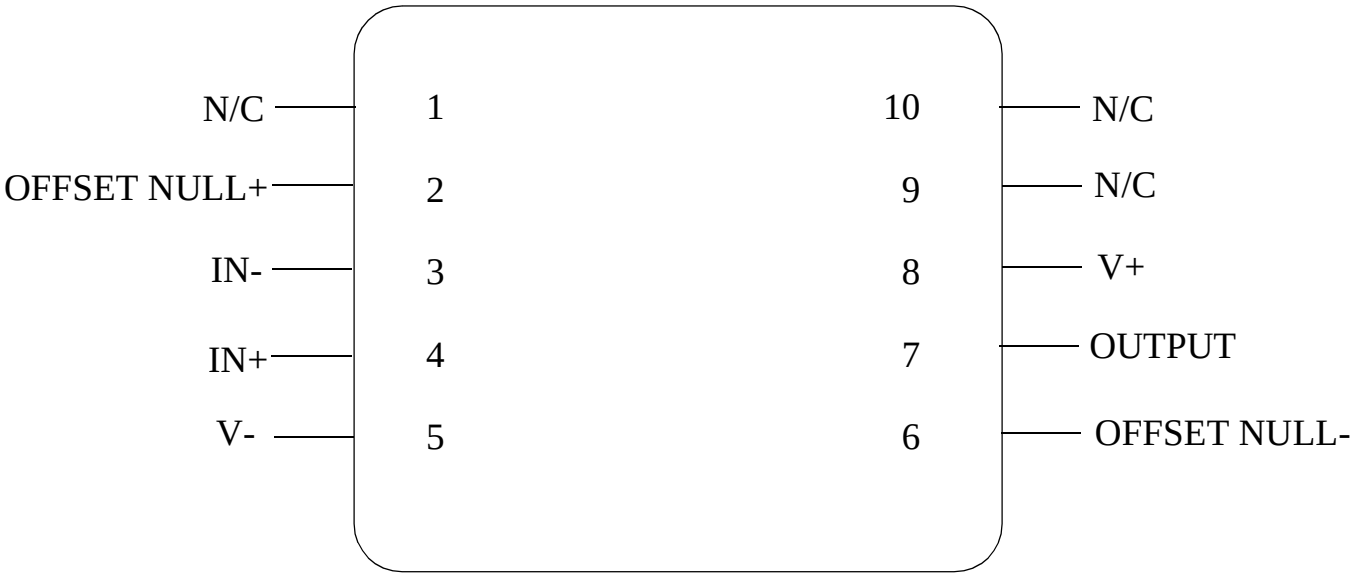
SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J08A	L

DO NOT SCALE DRAWING | SHEET 1 OF 1



LM741H
8 - PIN METAL CAN
CONNECTION DIAGRAM
TOP VIEW
P000278A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM741W

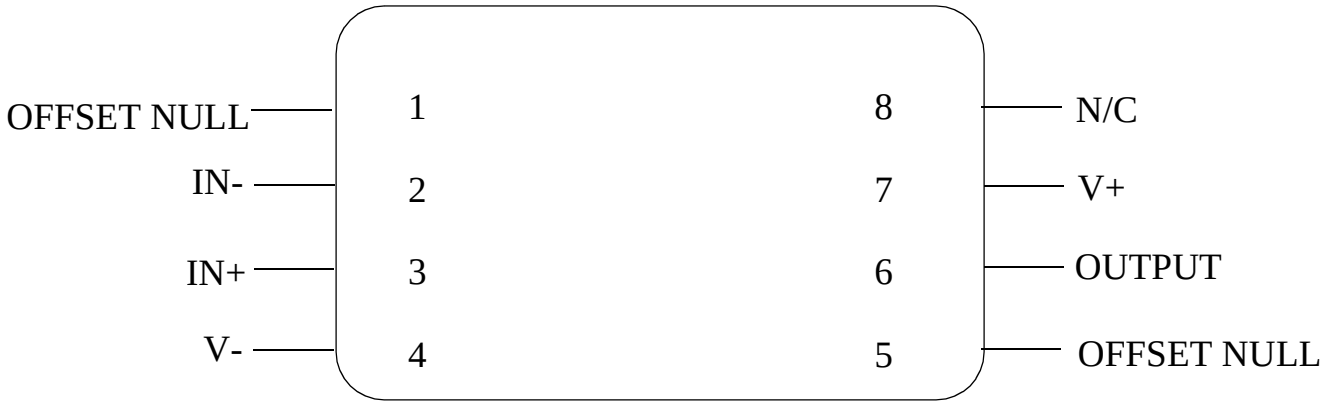
10 - LEAD CERPACK

CONNECTION DIAGRAM

TOP VIEW

P000280A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM741J

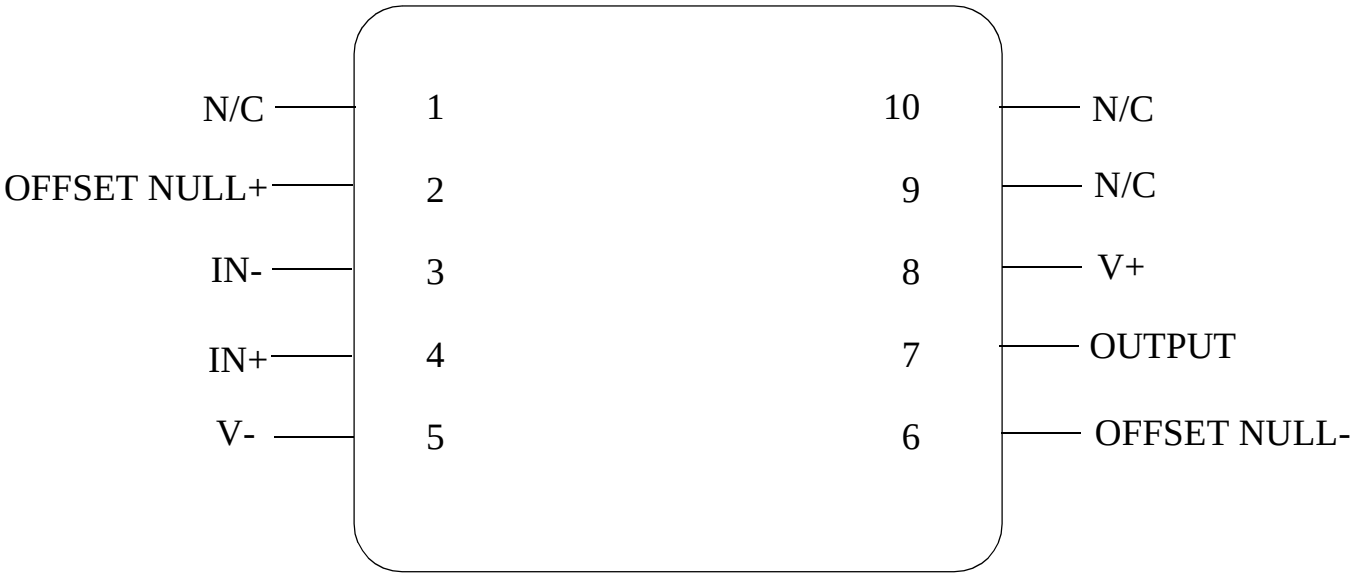
8 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000291A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050



LM741WG

10 - LEAD CERAMIC SOIC

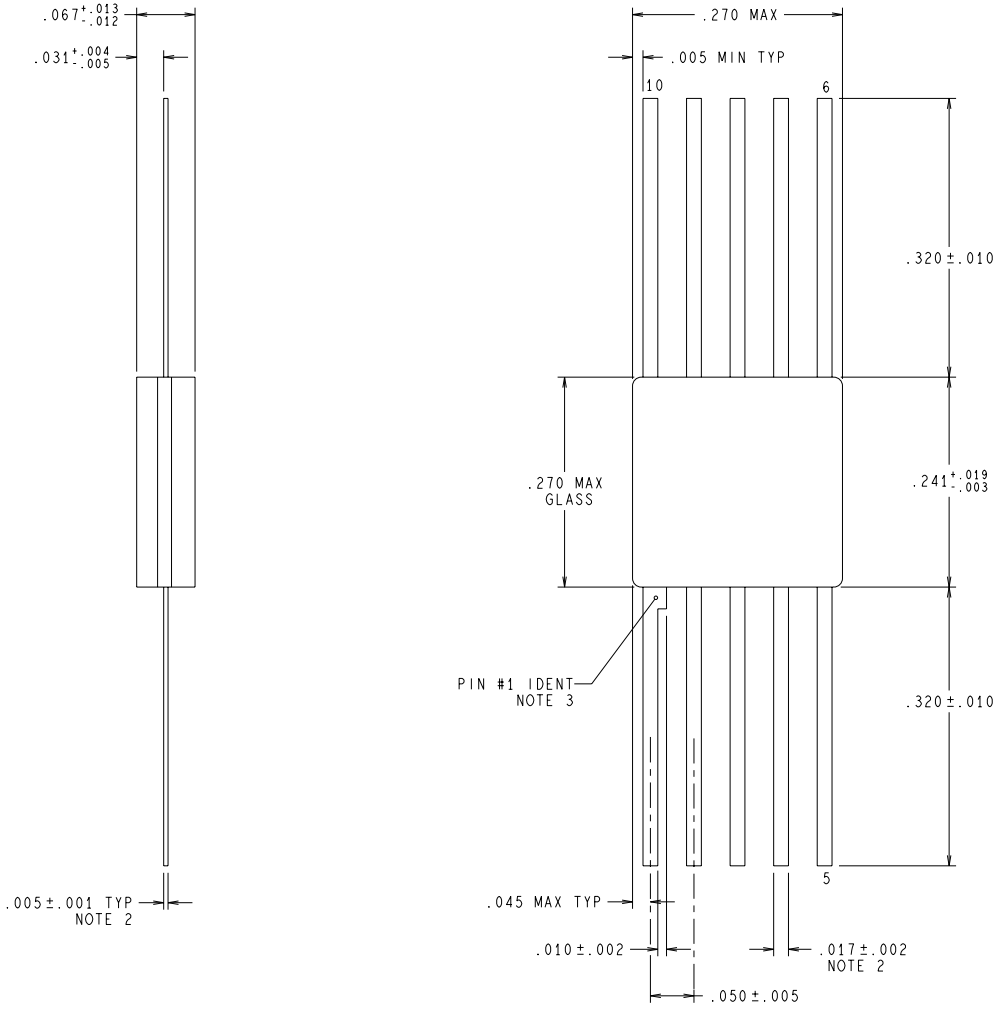
CONNECTION DIAGRAM

TOP VIEW

P000466A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE AND REDRAW PER NEW STANDARD.	10510	07/28/94	DEG/AEP
G	.017±.002 WAS .017±.020.	10654	10/21/94	DEG/



NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. MAXIMUM LIMIT MAY BE INCREASED BY .003 INCHES AFTER LEAD FINISH APPLIED.
3. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
4. REFERENCE JEDEC REGISTRATION MO-003, VARIATION AG, DATED 06/01/76.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: D.E.Grady	07/28/94
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

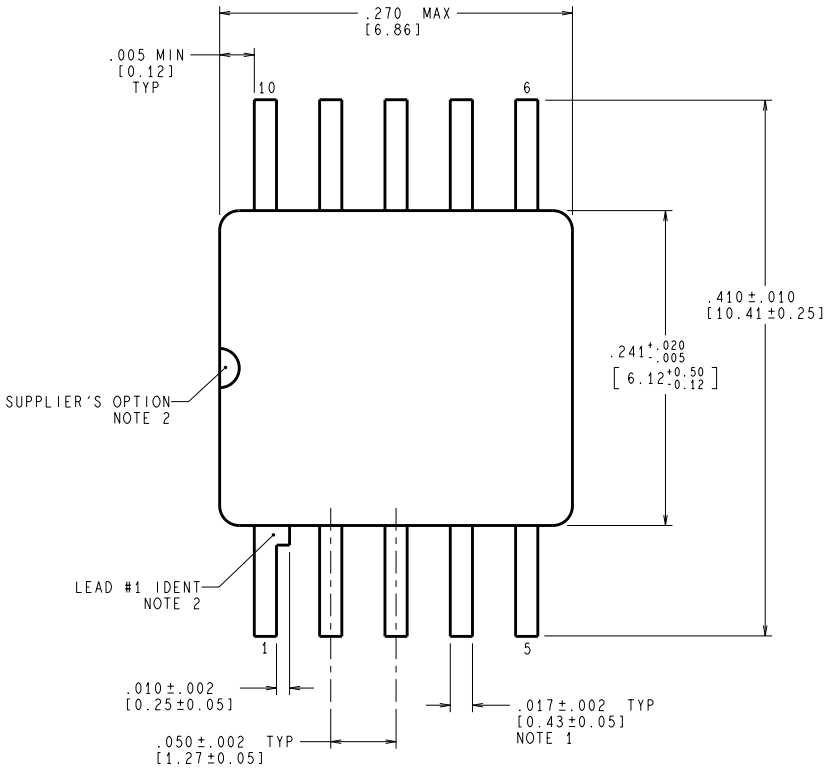
CERPACK, 10 LEAD

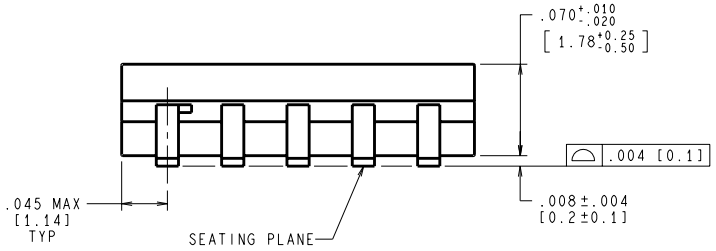
PROJECTION — INCH [MM]

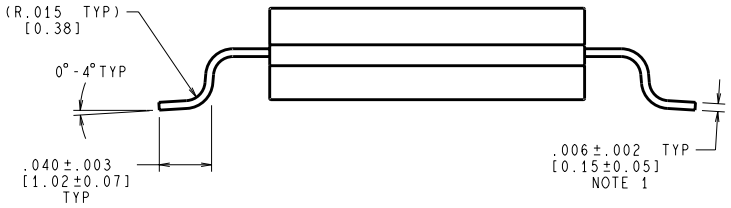
SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-W10A	G

DO NOT SCALE DRAWING — SHEET 1 of 1

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11374	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002 DIM .040±.003 WAS .037±.003	11441	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11838	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 10 LEAD, GULL WING

PROJECTION
INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG10A	C

DO NOT SCALE DRAWING | SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A0	M0003575	10/22/99	Rose Malone	Update MDS to full Release: MNLM741-X, Rev. 0BL to MNLM741-X, Rev. 1A0. Update to electrical parameters PSRR+ and PSRR-.