DUAL 'D' - TYPE FLIP-FLOP

- SET-RESET CAPABILITY
- STATIC FLIP-FLOP OPERATION - RETAINS STATE INDEFINITELY WITH CLOCK LEVEL EITHER "HIGH" OR "LOW"
- MEDIUM-SPEED OPERATION - 16 MHz (TYP.) CLOCK TOGGLE RATE AT 10V
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 4013B** (extended temperature range) and **HCF 4013B** (intermediate temperature range) are monolithic integrated circuits, available in 14-lead dual in-line plastic or ceramic package, ceramic flat package and plastic micropackage.
The **HCC/HCF 4013B** consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_i	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

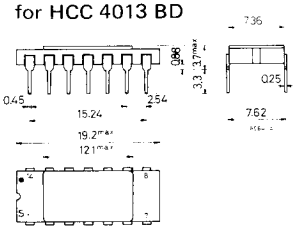
* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

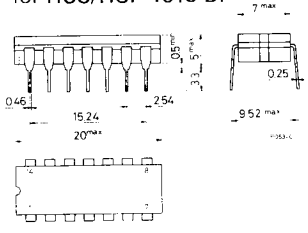
HCC 4013 BD for dual in-line ceramic package
HCC 4013 BF for dual in-line ceramic package, frit seal
HCC 4013 BK for ceramic flat package
HCF 4013 BE for dual in-line plastic package
HCF 4013 BF for dual in-line ceramic package, frit seal
HCF 4013 BM for plastic micropackage

MECHANICAL DATA (dimensions in mm)

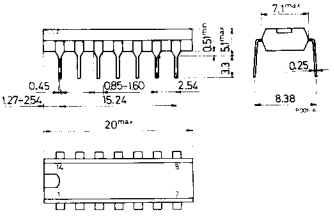
Dual in-line ceramic package for HCC 4013 BD



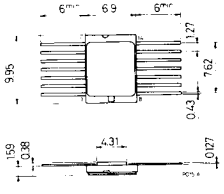
Dual in-line ceramic package for HCC/HCF 4013 BF



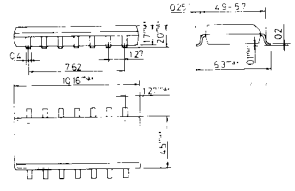
Dual in-line plastic package for HCF 4013 BE



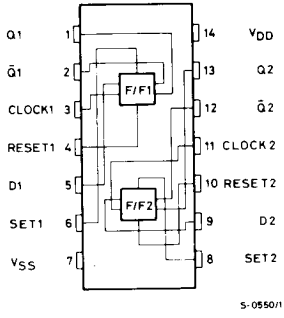
Ceramic flat package for HCC 4013 BK



Plastic micropackage for HCF 4013 BM



CONNECTION DIAGRAM

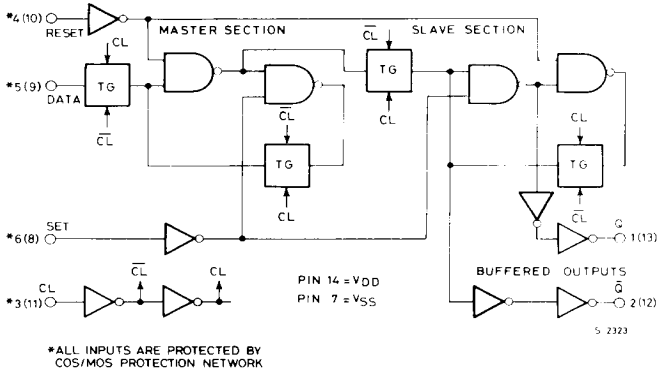


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

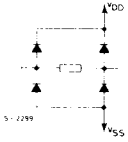
LOGIC DIAGRAM AND TRUTH TABLE

(one of two identical flip-flops)



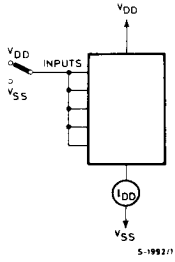
CL▲	D	R	S	Q	$\bar{Q}$	
⌒	0	0	0	0	1	
⌒	1	0	0	1	0	
⌣	X	0	0	Q	$\bar{Q}$	NO CHANGE
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

LOGIC 0=LOW ▲ =LEVEL CHANGE
LOGIC 1=HIGH X =DON'T CARE
N(N)=FF1/FF2 TERMINAL ASSIGNEMENT

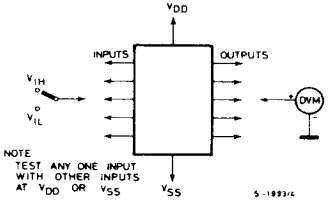


TEST CIRCUITS

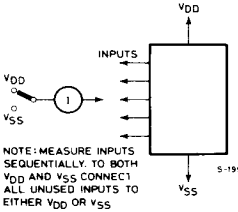
Quiescent device current



Noise immunity



Input leakage current



STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}*		25°C			T_{High}*		
							Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_L	Quiescent current	HCC types	0/ 5			5		1		0.02	1		30	μA
			0/10			10		2		0.02	2		60	
			0/15			15		4		0.02	4		120	
			0/20			20		20		0.04	20		600	
		HCF types	0/ 5			5		4		0.02	4		30	
			0/10			10		8		0.02	8		60	
			0/15			15		16		0.02	16		120	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		$\pm 10^{-5}$	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		$\pm 10^{-5}$	±0.3		± 1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = - 55°C for **HCC** device: -40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

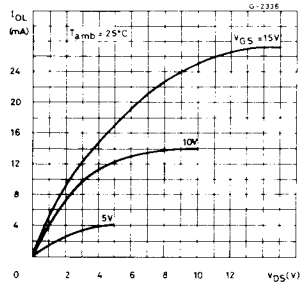
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, typical temperature coefficient for all V_{DD} = 0.3%/°C values, all input rise and fall time = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time (clock to Q or $\overline{Q}$ outputs)	5		150	300	ns
		10		65	130	
		15		45	90	
t_{PLH}	Propagation delay time (Set to Q or Reset to $\overline{Q}$)	5		150	300	ns
		10		65	130	
		15		45	90	
t_{PHL}	Propagation delay time (Set to $\overline{Q}$ or Reset to Q)	5		200	400	ns
		10		85	170	
		15		60	120	
t_{THL}, t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
f_{CL}*	Maximum clock input frequency	5	3.5	7		MHz
		10	8	16		
		15	12	24		
t_W	Clock pulse width	5	140	70		ns
		10	60	30		
		15	40	20		
t_r,t_f**	Clock input rise or fall time	5			15	μs
		10			4	
		15			1	
t_W	Set or reset pulse width	5	180	90		ns
		10	80	40		
		15	50	25		
t_{setup}	Data setup time	5	40	20		ns
		10	20	10		
		15	15	7		

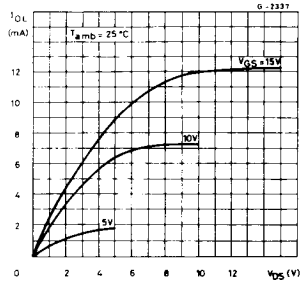
* Input t_r, t_f = 5 ns.

** If more than one unit is cascaded in a parallel clocked operation, t_r should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

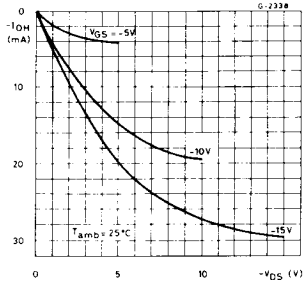
Typical output low (sink) current characteristics



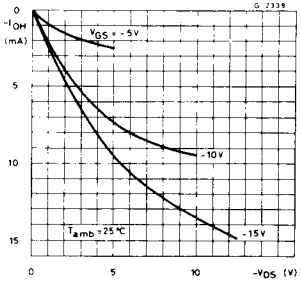
Minimum output low (sink) current characteristics



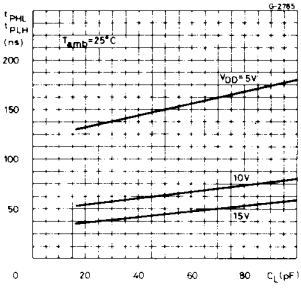
Typical output high (source) current characteristics



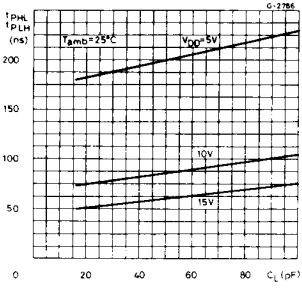
Minimum output high (source) current characteristics



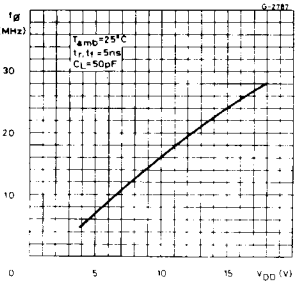
Typical propagation delay time vs. load capacitance (CLOCK or SET to Q CLOCK or RESET to $\overline{Q}$)



Typical propagation delay time vs. load capacitance (SET to $\overline{Q}$ or RESET to Q)



Typical maximum clock frequency vs. supply voltage



Typical power dissipation device vs. frequency