Homework 4 Report

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1. Briefly explain what each step does in the APR flow.
   A. Design setup
      引入 design 的 netlist 檔案，引入 LEF 製程檔案，設定 power ground 的 net 名稱；multi-mode, multi-corner 設定，用來做時序分析；並生成 IO 配置檔。
   B. Floorplan
      做一些 IC 平面空間的初始設定，設定 core utilization，決定 core 跟 cells 面積的比率。
   C. Powerplan
      設定 power 線的參數，生成 power rings 跟 stripe，設定 rings 的型態和層數，並設定 stripe 組數和間隔。
   D. Placement
      做初步的 standard cell 擺放，並進行 congestion analysis 分析這樣的 placement 是否會導致 routing 壅塞。
   E. ClockTreeSynthesis
      生成 clocktree 並且在生成前後進行 timing 的分析，包含 setup time 及 hold time。
   F. Route
      給所有的 cell 進行繞線，並且在完成後要進行 timing 分析。
   G. Filler Adding
      在沒有 cell 的空間要填入 filler。
2. What is the purpose of these generated files in hw4/apr/netlist/ ?
   A. CHIP.v
      可以用來做 post-layout simulation 的 netlist。
   B. CHIP_layout.sdc
      設置各種 design constraint，create_clock,create_generated_clock 設定 clk 頻率，set_input_delay, set_output_delay 設定 io pin 的 delay，set_max_fanout,set_max_capacitance, set_max_transition 設定違反 design rule 的標準。
   C. CHIP_layout.sdf

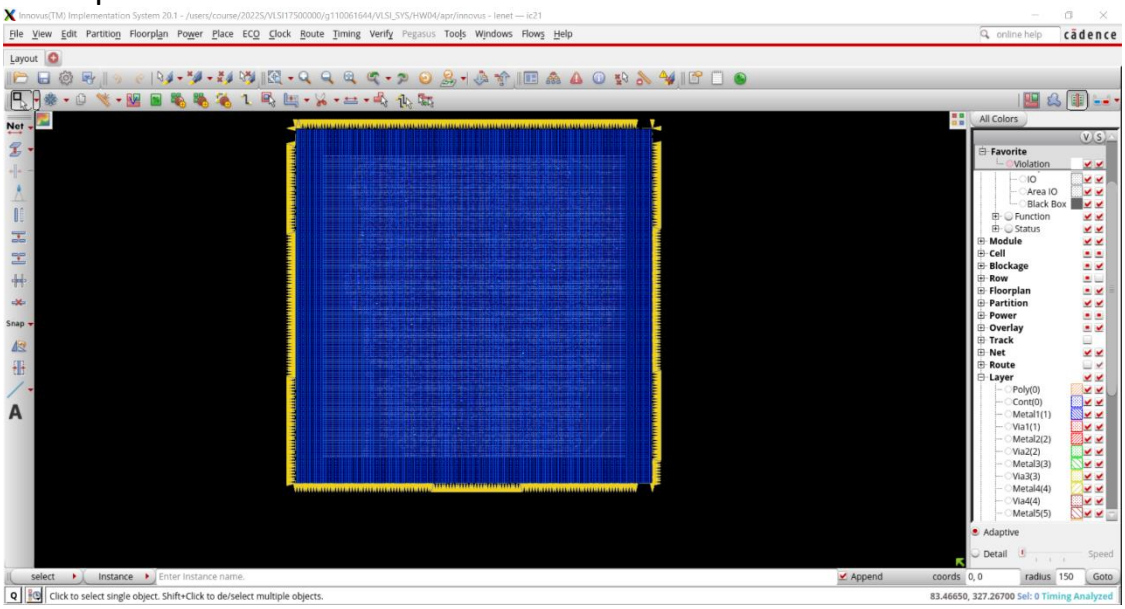
紀錄電路中的 delay。

D. CHIP_layout.gds
Layout 檔案。

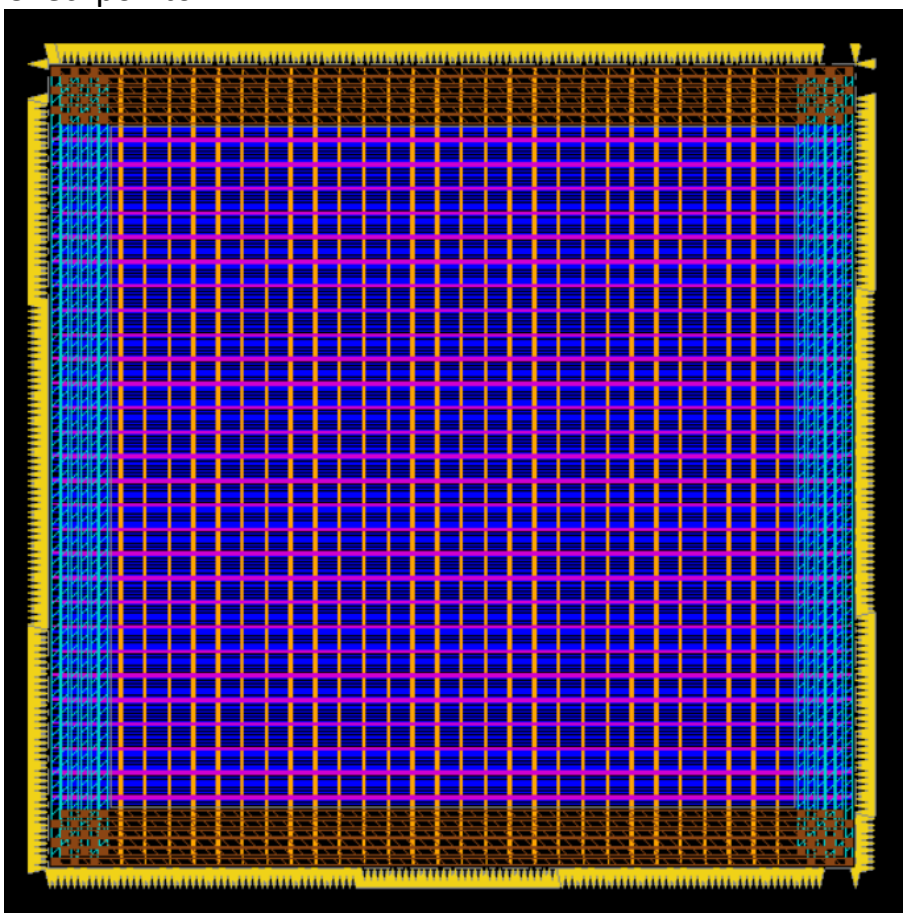
E. CHIP_layout.gz
RC extraction file

3. Please explain why the RTL simulation (make sim) doesn't need an SDF file, but the pre-layout (make syn) and post-layout simulation (make post) require this file.
因為 RTL simulation 並沒有使用合成出來的電路去模擬他只是 behavioral 的模擬，而 pre-layout 是合成出來的電路需要考慮 cell 的 delay，post-layout 則還需要另外考慮 routing 的 delay，因此他們需要 sdf 這個檔案，因為這個檔案記錄著電路中的 delay 資訊。
4. Please compare three kinds of power analysis in your report. Also, try to explain why they have different results.
pre_layout_power_report.rpt
用 gate level simulation 的波型，和合成出來的 netlist(lenet_syn.v)進行分析。
post_sim_power_report.rpt
用 post layout simulation 的波型，和 routing 完的電路(CHIP.v)進行分析。
pre_sim_power_report.rpt
用 RTL simulation 的波型，和 routing 完的電路(CHIP.v)進行分析。
5. You should include the screenshots of every checkpoint.

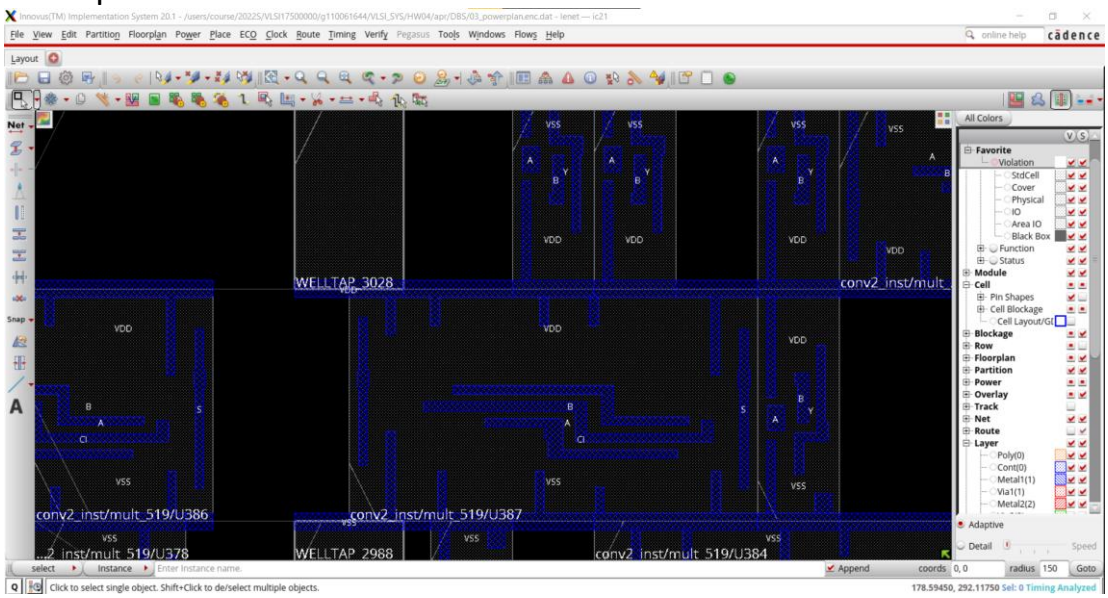
Checkpoint01



Checkpoint02



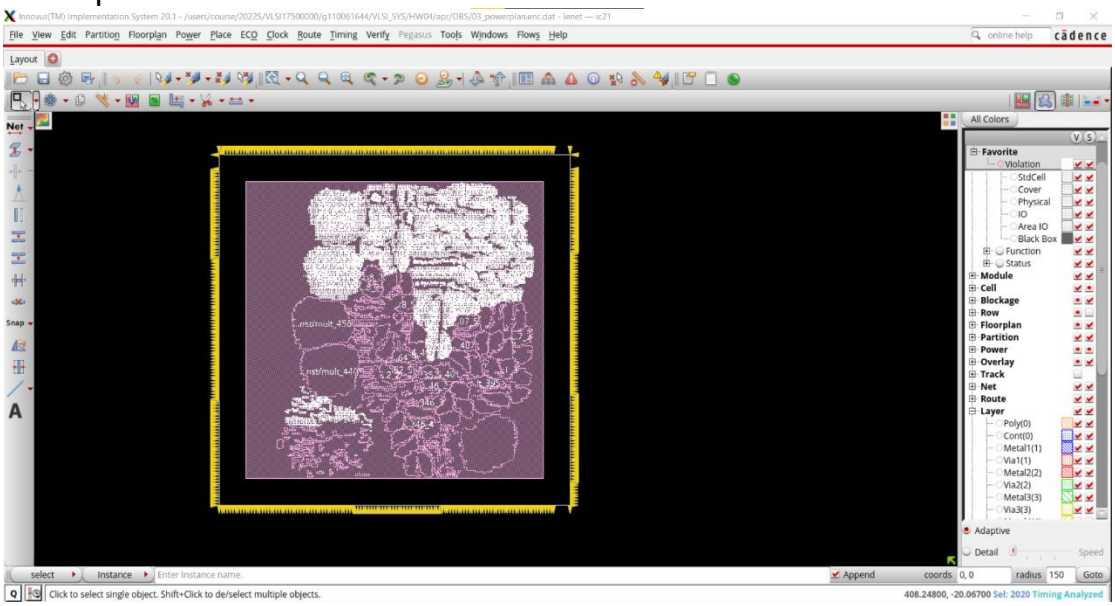
Checkpoint03



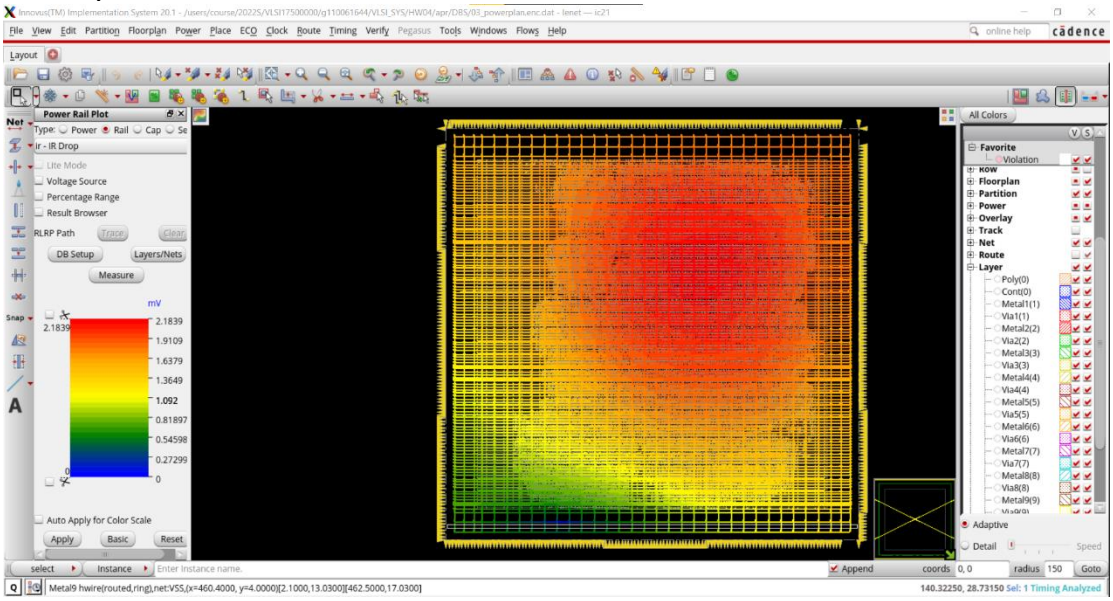
Q: How do standard cells connect with power/ground pins?

如上圖有將 pin 名稱顯示出來

Checkpoint04



Checkpoint05



Q: What is the worst IR drop? 2.1839mV

Checkpoint06

```
Reporting Utilizations.....

Core utilization  = 54.812929
Effective Utilizations
Average module density = 0.529.
Density for the design = 0.529.
       = stdcell_area 228421 sites (78120 um^2) / alloc_area 431963 sites (147731 um^2).
Pin Density = 0.2311.
            = total # of pins 104108 / total area 450443.
*** Message Summary: 0 warning(s), 0 error(s)

0
innovus 11>
```

Checkpoint07

```
Loading snapshot worklib.tb_lenet:v ..................... Done
*Verdi* Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi_R-2020.12, Linux, 11/19/2020
(C) 1996 - 2020 by Synopsys, Inc.
*Verdi* : Create FSDB file 'lenet_post.fsdb'
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
Reset System
Compute start
Compute finished, start validating result...
=====================
Image             [PASS]
Conv 1 activation [PASS]
Conv 2 activation [PASS]
Conv 3 activation [PASS]
FC   1 activation [PASS]
FC   2 activation [PASS]
>>> Congratulation! All result are correct
  [Post-layout gate-level simulation]
Clock Period:          12 ns,Total cycle count:       23729 cycles
=====================
Simulation finish
Simulation complete via $finish(1) at time 285990332 PS + 0
./lenet_tb.v:202         $finish;
ncsim> exit
[g110061644@ic21 sim]$
```

Checkpoint08

```
[g110061644@ic55 lec]$ ./run_lec.bat
C: unknown locale
// Warning: Using '0_lec_all.do' as filename
                        CONFORMAL (R)
                Version 11.10-s440 (27-Sep-2012) (64 bit executable)
   Copyright (c) Cadence Design Systems, Inc., 1997-2012. All Rights Reserved


This program is proprietary and confidential information belonging to
Cadence Design Systems, Inc., and may be used and disclosed only as authorized
in a license agreement controlling such use and disclosure.

// Check out Conformal_Ultra 11.1 license
// Check out Conformal_Asic 11.1 license
// Command: dofile 0_lec_setup.do
// Command: set system mode setup
// Command: set log file lec.log -replace
// Command: setenv TOP_DESIGN lenet
Set variable 'TOP_DESIGN' as 'lenet'
// Command: read design -file golden.f -golden -verilog2k
// Note: Process verilog command file golden.f
// Parsing file ../../syn/netlist/lenet_syn.v ...
// Parsing file /theda21_2/library/GPDK045/cur/gsclib045/verilog/slow_vdd1v2_basicCells.v ...
// Golden root module is set to 'lenet'
// Warning: (RTL14) Signal has input but it has no output (occurrence:34)
// Warning: (VLG7) Nets are renamed after removing backslash (occurrence:714)
// Note: (HRC3.5b) Open output port connection is detected (occurrence:74)
// Note: Read VERILOG design successfully
// Command: read design -file revised.f -revised
// Note: Process verilog command file revised.f
// Parsing file ../netlist/CHIP.v ...
// Parsing file /theda21_2/library/GPDK045/cur/gsclib045/verilog/slow_vdd1v2_basicCells.v ...
// Revised root module is set to 'lenet'
// Warning: (RTL2.5) Undriven net is detected (occurrence:3)
// Warning: (RTL2.13) Undriven pin is detected (occurrence:10)
// Warning: (RTL14) Signal has input but it has no output (occurrence:40)
// Warning: (VLG7) Nets are renamed after removing backslash (occurrence:685)
// Note: (HRC3.5b) Open output port connection is detected (occurrence:76)
// Warning: (HRC3.10a) An input port is declared, but it is not completely used in the module (occurrence:931)
// Warning: There are 13 undriven nets in Revised
// Warning: There are 10 undriven pins in Revised
// Note: Read VERILOG design successfully
// Command: set flatten model -gated_clock
// Command: set flatten model -seq_constant
// Command: set root module $TOP_DESIGN -golden
// Warning: Golden root module is already at 'lenet'
// Command: set root module $TOP_DESIGN -revised
// Warning: Revised root module is already at 'lenet'
// Command: dofile 0_lec_compare.do
// Command: set system mode lec
// Processing Golden ...
// Modeling Golden ...
// Processing Revised ...
// Modeling Revised ...
// Balanced modeling (auto) mapped 2726 out of 2726 DFF/DLATs
// (F28) Converted 328 internal output port(s) to inout port(s)
// Mapping key points ...
================================================================================
Mapped points: SYSTEM class
```

```
================================================================================
Mapped points: SYSTEM class
--------------------------------------------------------------------------------
Mapped points     PI     PO     DFF       Total
--------------------------------------------------------------------------------
Golden            291    209    1363      1863
--------------------------------------------------------------------------------
Revised           291    209    1363      1863
================================================================================
// Command: map key point
// Mapping key points ...
================================================================================
Mapped points: SYSTEM class
--------------------------------------------------------------------------------
Mapped points     PI     PO     DFF       Total
--------------------------------------------------------------------------------
Golden            291    209    1363      1863
--------------------------------------------------------------------------------
Revised           291    209    1363      1863
================================================================================
// Command: analyze multiplier -cdp_info
// Command: analyze datapath -merge -share -effort medium -verbose
// Command: add compare point -all
// 1572 compared points added to compare list
// Command: compare
================================================================================
Compared points      PO     DFF       Total
--------------------------------------------------------------------------------
Equivalent           209    1363      1572
================================================================================
// Command: analyze abort -compare
There is no abort/specified point to be analyzed.
// Command: report unmap point -notmapped
There is no unmapped point
// Command: usage
CPU time     : 5.06    seconds
Memory usage : 291.21  M bytes
// Command: report compare data -nonequivalent
0 Non-equivalent point(s) reported
0 compared point(s) reported
================================================================================
Compared points      PO     DFF       Total
--------------------------------------------------------------------------------
Equivalent           209    1363      1572
================================================================================
// Command: exit -force
[g110061644@ic55 lec]$
```

Checkpoint09

```
Warning: Some timing arcs have been disabled for breaking timing loops or because of constant propagation. Use the 'report_disable_timing' command to get the
list of these disabled timing arcs. (PTE-003)
Information: Checking 'out_of_table_range'.
Warning: There are 1762 out_of_range ramps.
Warning: There are 34161 out_of_range loads.
Information: Checking 'missing_table'.
Information: Checking 'missing_function'.
0
update_power
Information: Running time_based power analysis... (PWR-601)
Information: Reading vcd file '/users/course/2022S/VLSI17500000/g110061644/VLSI_SYS/HW04/sim/lenet_syn.fsdb'
fsdb2vcd - fsdb to vcd converter, Release Verdi_R-2020.12 (RH Linux x86_64/64bit) -- Thu Nov 19 03:16:38 PDT 2020

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FSDB Writer, Release Verdi_P-2019.06-SP2-5, RH Linux x86_64/64bit, 05/28/2022
(C) 1996 - 2022 by Synopsys, Inc.
Information: The waveform options are:
              File name:      primetime_px.fsdb
              File format:    fsdb
              Time interval:  0.001ns
              Hierarchical level:     all

Information: Power analysis is running, please wait ...

 Last event time =   285966 ns
fsdb2vcd: /users/course/2022S/VLSI17500000/g110061644/VLSI_SYS/HW04/sim/lenet_syn.fsdb is converted to stdout successfully.
Information: analysis is done for time window (0ns - 285990ns)

Information: Total simulation time = 285990.000000 ns
1
report_power  -hier > report_power_hier.rpt
report_power  > pre_layout_power_report.rpt
exit

Timing updates: 1 (1 implicit, 0 explicit) (0 incremental, 1 full, 0 logical)
Noise updates: 0 (0 implicit, 0 explicit) (0 incremental, 0 full)
Maximum memory usage for this session: 1534.65 MB
CPU usage for this session: 486 seconds
Elapsed time for this session: 719 seconds
Diagnostics summary: 1 warning, 10 informationals

Thank you for using pt_shell!
[g110061644@ic55 pre_layout]$
```

Checkpoint10

```
Warning: Some timing arcs have been disabled for breaking timing loops or because of constant propagation. Use the 'report_disable_timing' command to get the list of these dis
abled timing arcs. (PTE-003)
Information: Checking 'out_of_table_range'.
Warning: There are 2 out_of_range ramps.
Warning: There are 33584 out_of_range loads.
Information: Checking 'missing_table'.
Information: Checking 'missing_function'.
0
update_power
Information: Running time_based power analysis... (PWR-601)
Information: Reading vcd file '/users/course/2022S/VLSI17500000/g110061644/VLSI_SYS/HW04/sim/lenet_post.fsdb'
fsdb2vcd - fsdb to vcd converter, Release Verdi_R-2020.12 (RH Linux x86_64/64bit) -- Thu Nov 19 03:16:38 PDT 2020

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FSDB Writer, Release Verdi_P-2019.06-SP2-5, RH Linux x86_64/64bit, 05/28/2022
(C) 1996 - 2022 by Synopsys, Inc.
Information: The waveform options are:
               File name:      primetime_px.fsdb
               File format:    fsdb
               Time interval:  0.001ns
               Hierarchical level:     all

Information: Power analysis is running, please wait ...

 Last event time =   285979 ns
fsdb2vcd: /users/course/2022S/VLSI17500000/g110061644/VLSI_SYS/HW04/sim/lenet_post.fsdb is converted to stdout successfully.
Information: analysis is done for time window (0ns - 285990ns)

Information: Total simulation time = 285990.332000 ns
1
report_power  -hier > report_power_hier.rpt
report_power  > post_sim_power_report.rpt
exit

Timing updates: 1 (1 implicit, 0 explicit) (0 incremental, 1 full, 0 logical)
Noise updates: 0 (0 implicit, 0 explicit) (0 incremental, 0 full)
Maximum memory usage for this session: 1546.49 MB
CPU usage for this session: 841 seconds
Elapsed time for this session: 1317 seconds
Diagnostics summary: 1 warning, 11 informationals

Thank you for using pt_shell!
[g110061644@ic55 post_sim_waveform]$
```

Checkpoint11

```
Information: Total number of synthesis invariant points = 1664 , annotated synthesis invariant points = 392, annotation_ratio = 23.56%
1
check_power
Warning: Some timing arcs have been disabled for breaking timing loops or because of constant propagation. Use the 'report_disable_timing' command to get the list of these dis
abled timing arcs. (PTE-003)
Information: Building multi voltage information for entire design. (MV-022)
Information: Checking 'out_of_table_range'.
Warning: There are 2 out_of_range ramps.
Warning: There are 33584 out_of_range loads.
Information: Checking 'missing_table'.
Information: Checking 'missing_function'.
0
update_power
Information: Clock clk is selected as the reference clock for cycle accurate peak power analysis of the current design. (PWR-280)
Information: Running time_based power analysis... (PWR-601)
Information: Reading vcd file '/users/course/2022S/VLSI17500000/g110061644/VLSI_SYS/HW04/sim/lenet.fsdb'
fsdb2vcd - fsdb to vcd converter, Release Verdi_R-2020.12 (RH Linux x86_64/64bit) -- Thu Nov 19 03:16:38 PDT 2020

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FSDB Writer, Release Verdi_P-2019.06-SP2-5, RH Linux x86_64/64bit, 05/28/2022
(C) 1996 - 2022 by Synopsys, Inc.
Information: The waveform options are:
               File name:      primetime_px.fsdb
               File format:    fsdb
               Time interval:  10ns
               Hierarchical level:     all

Information: Power analysis is running, please wait ...

 Last event time =   331782 ns
fsdb2vcd: /users/course/2022S/VLSI17500000/g110061644/VLSI_SYS/HW04/sim/lenet.fsdb is converted to stdout successfully.
Information: analysis is done for time window (0ns - 332106ns)
Warning: Switching activity for constant net fc_inst/n190 is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/n191 is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/n191 is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/n192 is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/FE_OFN512_n188 is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/FE_OFN512_n188 is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/N101 is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/N101 is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/N104 is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/sub_81/FE_OFN897_FE_RN_1 is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[25] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[18] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[20] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[13] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[28] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[30] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[23] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[16] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[11] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[26] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[19] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[21] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[14] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[29] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[31] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[24] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[17] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[12] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[27] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[22] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[15] is reset by SAIF/VCD.  (PSW-208)
Warning: Switching activity for constant net fc_inst/add_0_root_add_0_root_add_75_2/carry[10] is reset by SAIF/VCD.  (PSW-208)
Information: Total simulation time = 332106.000000 ns
1
report_power  -hier > report_power_hier.rpt
report_power  > pre_sim_power_report.rpt
exit

Timing updates: 1 (1 implicit, 0 explicit) (0 incremental, 1 full, 0 logical)
Noise updates: 0 (0 implicit, 0 explicit) (0 incremental, 0 full)
Maximum memory usage for this session: 1524.85 MB
CPU usage for this session: 468 seconds
Elapsed time for this session: 466 seconds
Diagnostics summary: 53 warnings, 12 informationals

Thank you for using pt_shell!
[g110061644@ic55 pre_sim_waveform]$
```