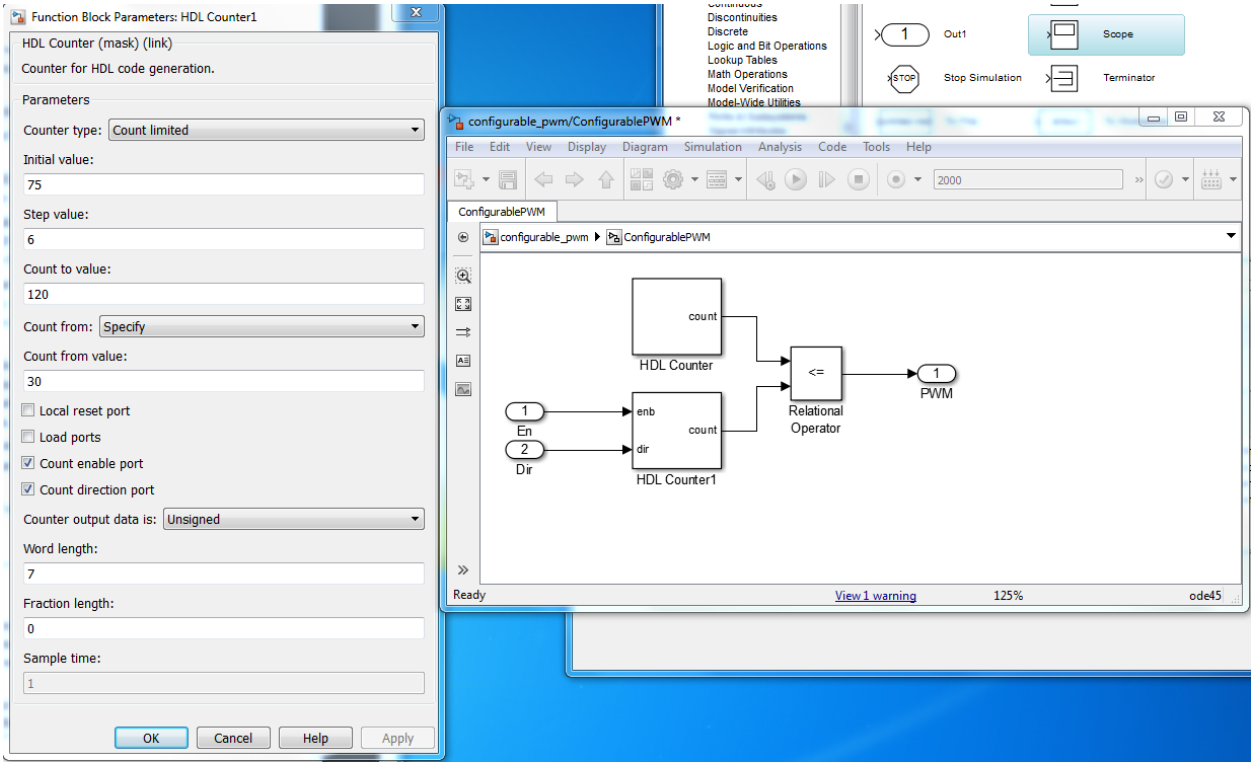
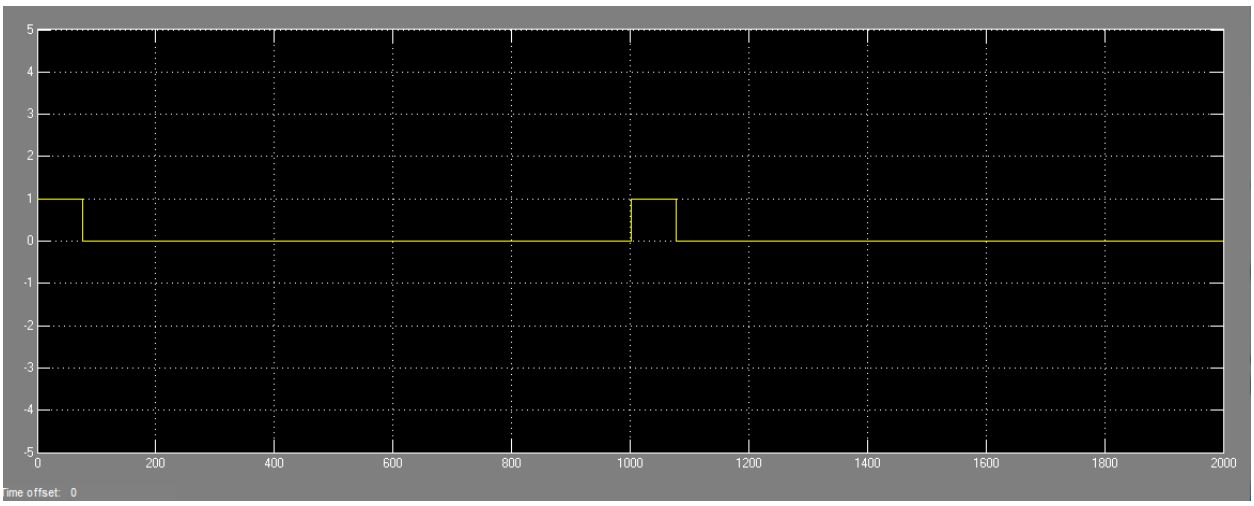
Evan Noyes and Henry Gridley
Lab Report 10

Assignment 1

a)



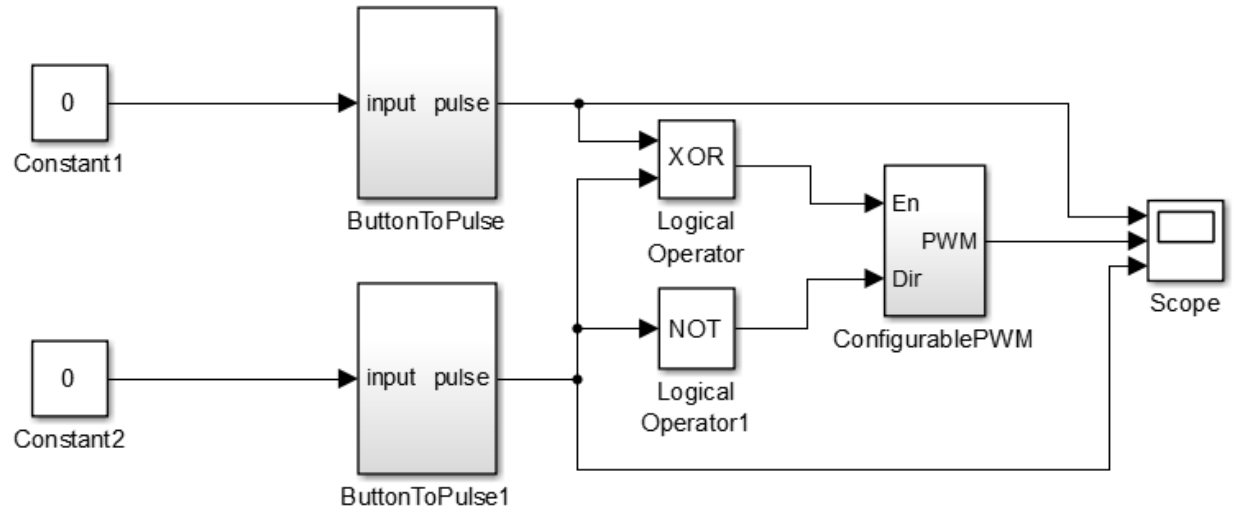
b)



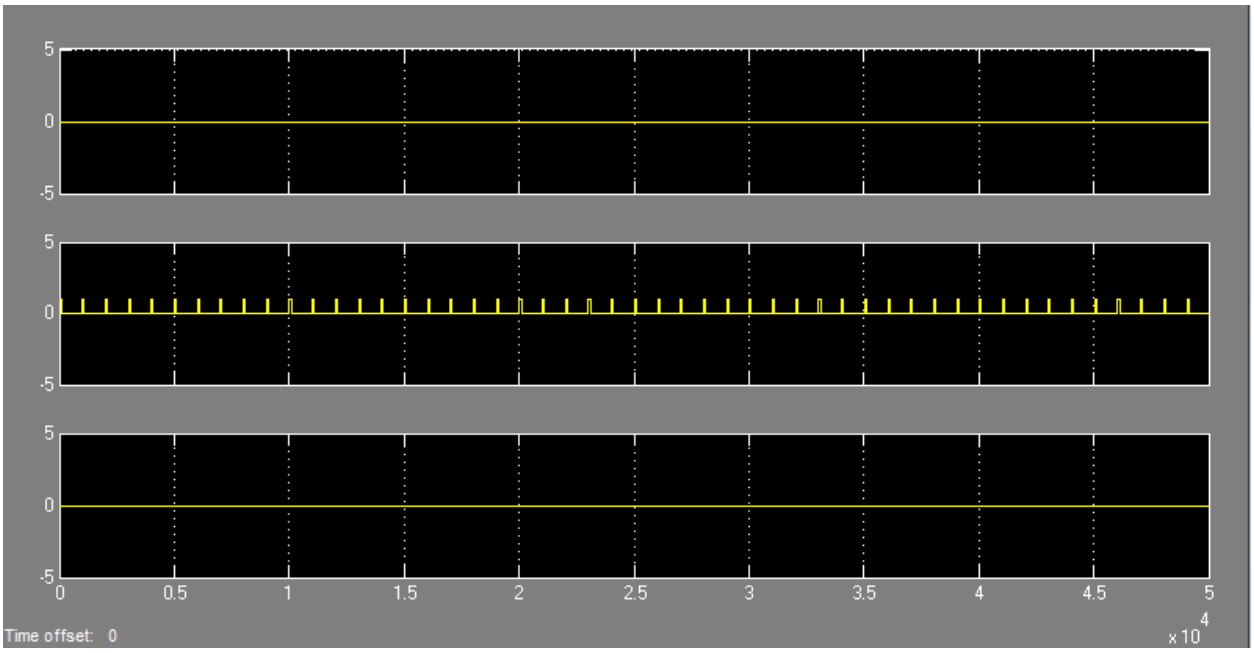
Every 1000 clock cycles the system produces a pulse with a width of 75 cycles, the default specified by the counter. This width is changed when signals are given to the inputs

Assignment 2

a)



b)



Here you can see the pulse cycles in the middle row, which will remain at a constant width since there is no input

c)

Before pulse:
- 0 => 1 Transition: **1.2012**
- 1 => 0 Transition: **1.2088**
- Total Width: **76 cycles**

After pulse:
- 0 => 1 Transition: **1.3013**
- 1 => 0 Transition: **1.3095**
- Total Width: **82 cycles**

We see a **+6 increase** in pulse width, consistent with the increment on our counter

d)

Before pulse:
- 0 => 1 Transition: **1.2012**
- 1 => 0 Transition: **1.2088**
- Total Width: **76 cycles**

After pulse:
- 0 => 1 Transition: **1.3013**
- 1 => 0 Transition: **1.3083**
- Total Width: **70 cycles**

We see a **-6 decrease** in pulse width, consistent with the increment on our counter

Assignment 3