EE P 592 / EE 579A

Electromagnetic Compatibility

HW2

Q1 [5 pts]: Show the detailed steps to get (derive) the equation shown in T6 slide 3 for V_N from the equivalent circuit model shown on the same slide.

Q2 [15 pts]: For the digital circuit shown in Figure 1, two CMOS gates are connected via a transmission line (a long PCB trace). The driving gate (source) pushes a 5V step to the receiver gate (load). Due to the impedance mismatches, signal integrity (SI) issues arise. The source gate impedance is 1/5 Zc and the load gate impedance is 5Zc. Assuming Zc = 55Ω, the propagation delay T_D is 1μsec,

(a) Calculate the source and load voltage reflection coefficients.
(b) Using the time domain graphing method, sketch $V_L(t)$ up to 10 T_D.
(c) Re-sketch $V_L(t)$, using the formula and compare with (b)
(d) Using **LTSPICE**, simulate the circuit and plot $V_L(t)$ and $V_{in}(t)$
(e) To reduce SI issue, we need to match the driver/receiver to the TL. First using a series termination at the source side, what should be the value of this resistance? Add the value to your circuit model and re-simulate. What can you conclude regarding the received signal VL(t) and the signal Vin(t) compared to the case in (d) (i.e. without termination matching).
(f) Repeat (e) but now using a load parallel termination. What can see say comparing series and parallel matching terminations with respect to the obtained waveforms VL(t) and Vin(t).
(g) In general, as a design engineer, what would be the voltage rating of the receiving (load) gate in order for it to withstand the worst-case voltage levels?

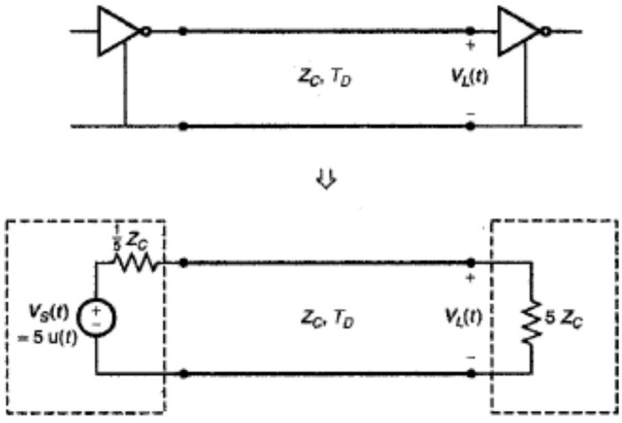


Figure 1

Q3 [13 pts]: For the transmission line shown in **Figure 2**, f = 5MHz, v= $3x10^8$ m/s, L = 78 m, Z_c=50Ω, Vs = 50 e^{j0} V, Z_s = 20 – j30 Ω, Z_L = 200 – j500 Ω. Determine,

(a) The line length in wavelengths
(b) The voltage reflection coefficient at the source and load sides
(c) The input impedance to the line (Zin)
(d) The time domain voltages at the input of the line and at the load side
(e) The average power delivered to the load
(f) The VSWR
(g) Construct an **LTSPICE** model to simulate this problem and verify all your previous answers from the simulated values.

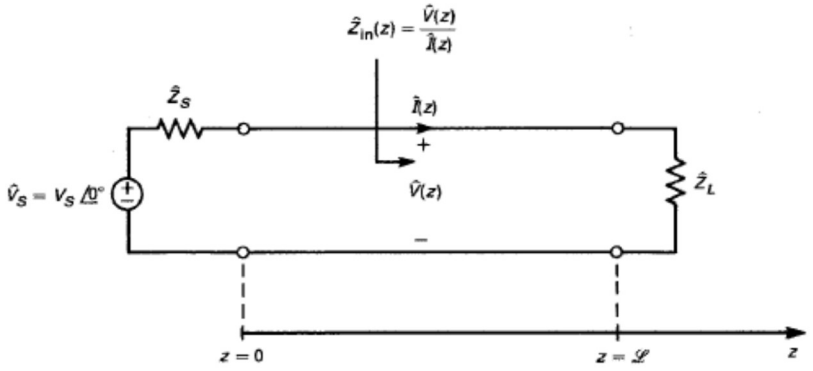


Figure 2

Q4 [10 pts]: An ideal common mode choke windings perfectly symmetric and having no losses) is constructed as shown in Figure 3. When we connect terminals **AB**, the impedance seen looking into **ab** is 300 000∠90° Ω at 50 MHz. When we connect terminals **Ab**, the impedance at 50MHz seen looking into **aB** is 1000 000 ∠90° Ω.

(a) Determine the self and mutual inductances of this choke
(b) Construct an **LTSPICE** model that confirms the results (i.e. plot the impedance as a function of frequency)

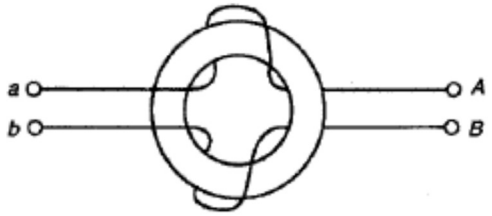


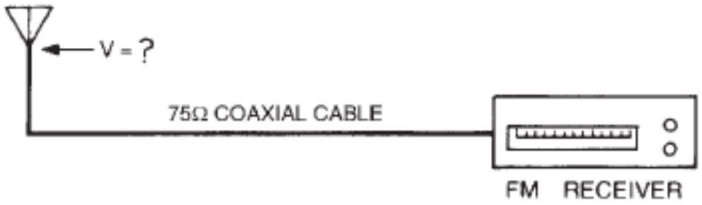
Figure 3

Q5 [7 pts]:

Figure 4 shows an FM antenna connected to an FM receiver by a 75Ω matched coaxial cable. The required SNR at the input terminals of the receiver to have good reception is 18dB, and the noise figure of the receiver is 8dB.

(a) If the cable connecting the antenna to the receiver has 6dB of insertion loss, what signal voltage is required at the point where the antenna connects to the cable, to have good signal quality? The noise bandwidth of the receiver is 50KHz.

(b) Why do you think this voltage in part (a) is considerable smaller than that required by the TV as considered in example 5.3 (see class example)



<u>Submission Notes</u>:

(1) submit a PDF file for your solutions including ALL figures, plots, circuit models, etc.

(2) Attach the LTSPICE files as separate files for each problem that asks for such a solution/model/file, name them according to the problem number, i.e. "HW2_Q2_b_Student_name".

(3) submit ALL files through Canvas for assignment 2.