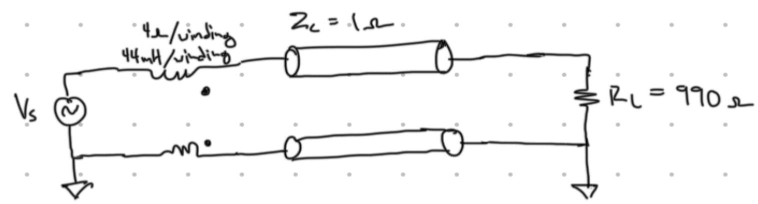
Q1

EE P 592 / EE 579A
Electromagnetic Compatibility
HW3

Q1 [8 pts]: A common-mode choke is placed in series with a transmission line that connects a low impedance source to a 900Ω load. The transmission line conductors each have a 1Ω resistance. Each winding of the common-mode choke has an inductance of 0.044H and a resistance of 4Ω.

(a) Above what frequency will the choke have a negligible effect on the signal transmission?
(b) How much attenuation (in dB) does the choke provide to a ground differential noise voltage at 60Hz, 180 Hz and 300Hz.

EMC_T7_Sharawi.pdf
Topic: Grounding



Assume identical windings so that $L_1 = L_2 = M$ } Slide 22
Also, $Z_c << R_L$ so Z_c can be ignored

a) For signal frequencies greater than $\omega = 5R_{c2}/L_2$, virtually all the current will go via the second conductor and not the ground plane.

Since $L_1 = L_2 = M$ the following formula $V_s = j\omega(L_1+L_2)I_s - 2j\omega M I_s + (R_{c2}+R_L)I_s$ simplifies to $I_s = \frac{V_s}{(R_{c2}+R_L)}$

Then since $R_{c2} << R_L$ it simplifies to $I_s = V_s/R_L$, again only when signal frequency is greater than $\omega = 5R_{c2}/L_2$

Question:
· Does the transmission line resistance factor into the common mode choke frequency formula?

$$\omega = 5R_{c2}/L_2$$

$$2\pi f = 5R_{c2}/L_2$$

$$\boxed{f = \frac{5R_{c2}}{2\pi L_2} = \frac{5(4\Omega+1\Omega)}{2\pi(44mH)} = \frac{5(5)}{(\pi)(0.088)} = 90.43 \text{ Hz}}$$

b) Lecture 7, slide 24 $V_N = \dfrac{V_G R_{c2}/L}{j\omega + R_{c2}/L}$

$$A_{dB} = 20\log_{10}\left(\left|\frac{V_N(f)}{V_G(f)}\right|\right) = 20\log_{10}\left|\frac{\left(\frac{V_G R_{c2}/L}{j\omega + (R_{c2}/L)}\right)}{V_G}\right| = 20\log_{10}\left(\left|\frac{R_{c2}}{j\omega L + R_{c2}}\right|\right)$$

$$A_{dB}(60Hz) = 20\log_{10}\left(\frac{(4+1)}{j(2\pi(60)(0.044)) + (4+1)}\right) = 20\log_{10}\left|\frac{5}{5+j16.59}\right| = 20\log_{10}\left(\frac{5}{17.33}\right) = -10.80\text{ dB}$$

$$A_{dB}(180Hz) = 20\log_{10}\left(\frac{(4+1)}{j(2\pi(180)(0.044)) + (4+1)}\right) = 20\log_{10}\left|\frac{5}{5+j49.76}\right| = 20\log_{10}\left(\frac{5}{49.46}\right) = -19.91\text{ dB}$$

$$A_{dB}(300Hz) = 20\log_{10}\left(\frac{(4+1)}{j(2\pi(300)(0.044)) + (4+1)}\right) = 20\log_{10}\left|\frac{5}{5+j82.94}\right| = 20\log_{10}\left(\frac{5}{83.08}\right) = -24.4\text{ dB}$$

Q2

Q2 [10 pts]: For the Differential amplifier shown in Figure 1, R1 and R2 are 1% resistors with values of 4.7 kΩ and 270 kΩ, respectively.

(a) Calculate the Differential mode (DM) input impedance.
(b) What is the differential mode gain?
(c) Calculate the common-mode (CM) input impedance?
(d) What is the common mode gain?
(e) What will be the value of the CMRR?

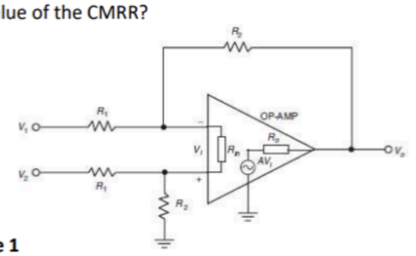


Figure 1

EMC_T8_Shorawi.pdf
Topic: Filtering and balancing

S6; if the load resistors have tolerance of +/- x%, the max variation (unbalance) will be 2x%. because path 1 resistance can be R + ΔR (tolerance) versus path 2 R − ΔR (tolerance).

Let $\Delta R_L / R_L = 2p$ (value not %).

If $R_L \gg \Delta R_L$ then $CMRR = 20\log\left(\left(\frac{1}{2p}\right)\left(R_L/R_s\right)\right)$ dB

a) S9; $R_{in(DM)} = 2R_1 = 2(4.7k) = 9.4\,k\Omega$

b) S9; $A_{DM} = \frac{-R_2}{R_1} = \frac{-270}{4.7} = -57.45$

c) S9; $R_{in(cm)} = \frac{270 + 4.7}{2} = 137.35\,k\Omega$

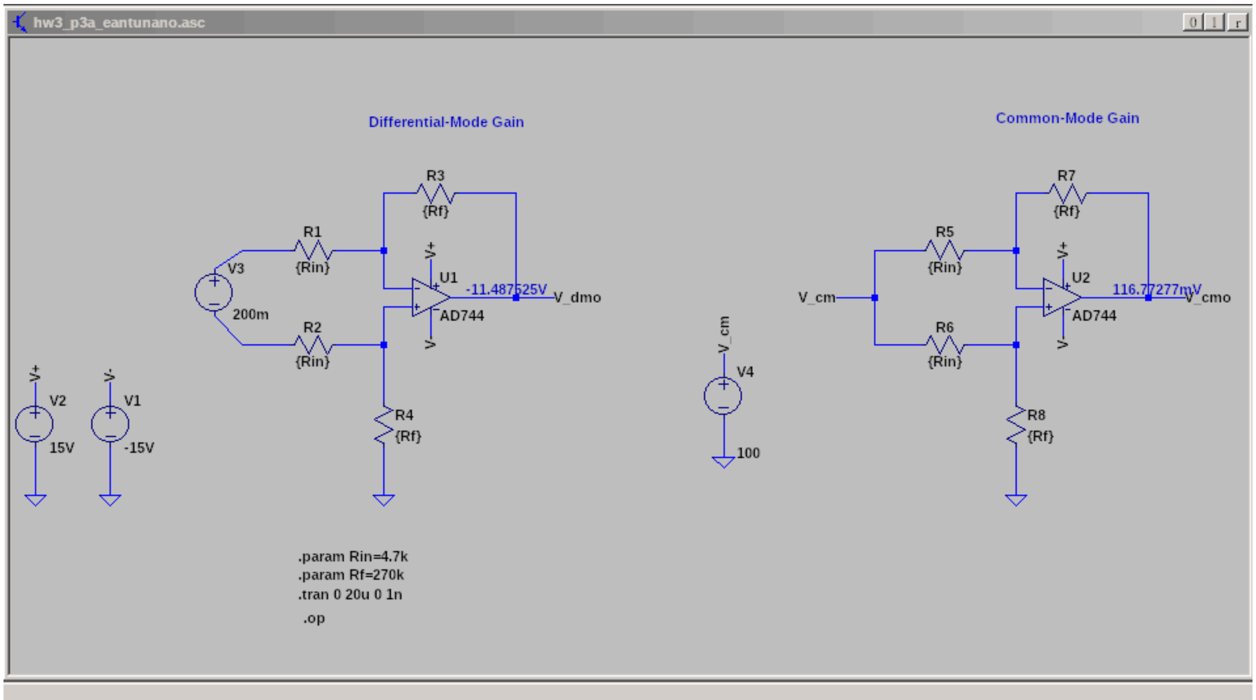
d) S10; $A_{cm} = \frac{V_{out}}{V_{cm}} = \frac{\Delta R_2}{R_2}(A_{DM}) = \frac{\Delta R_2}{R_1} = \frac{(2p)(R_2)}{R_1} = \frac{270(2)(0.01)}{4.7} = 1.15$

e) S11; CMRR can be found by substituting V_{in} for V_{DM} giving

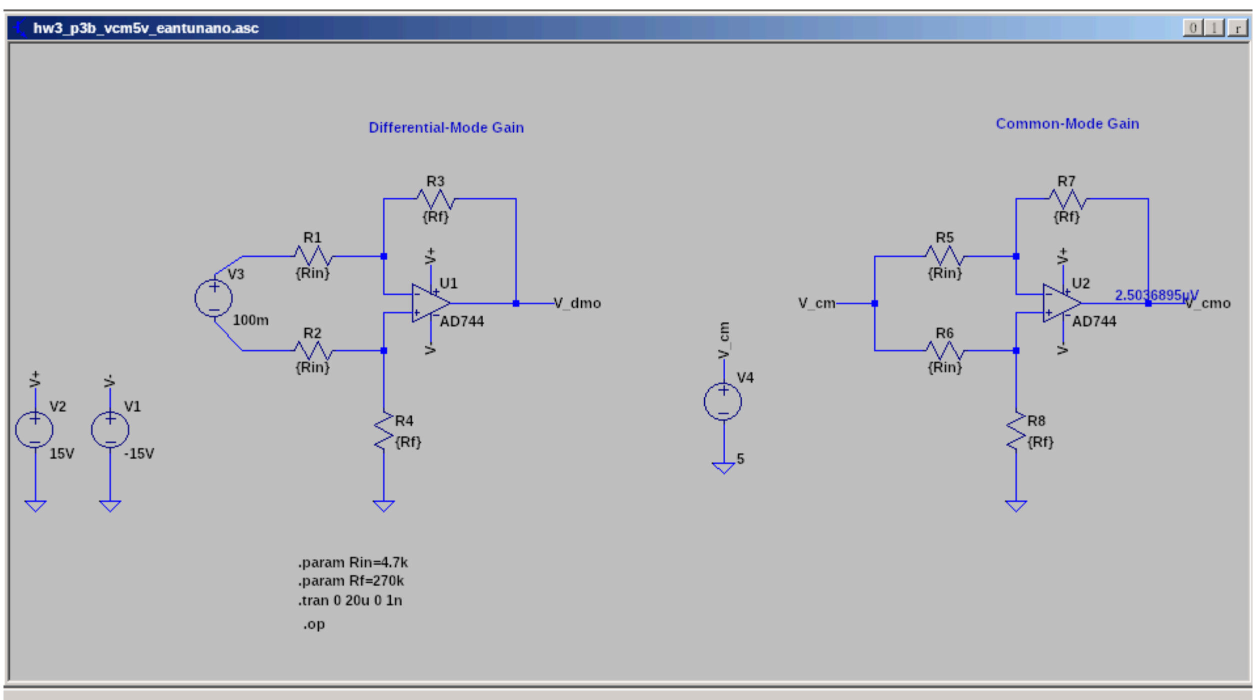
$$CMRR = 20\log\left(\frac{V_{cm}}{V_{in}}\right) = 20\log\left(\frac{R_2}{\Delta R_2}\right) = 20\log\left(\frac{1}{2p}\right)\,dB = 20\log\left[\frac{1}{2(0.01)}\right] = 33.98\,dB$$

Q3

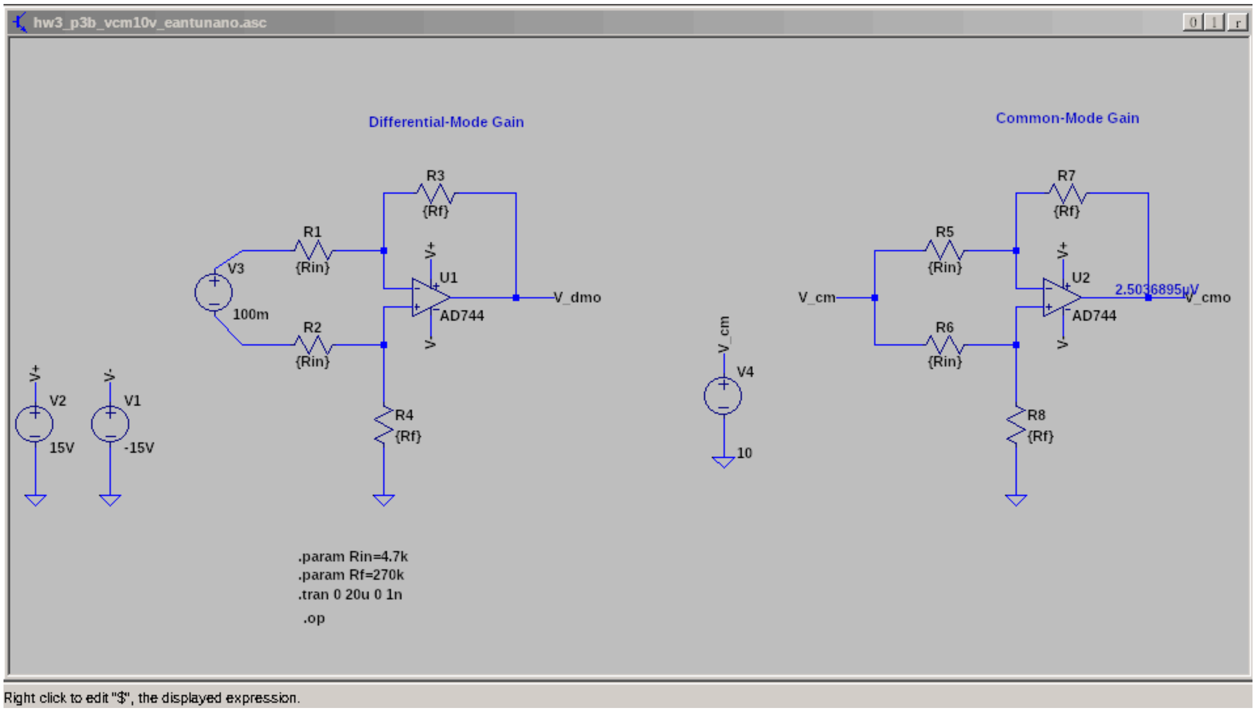
Part A



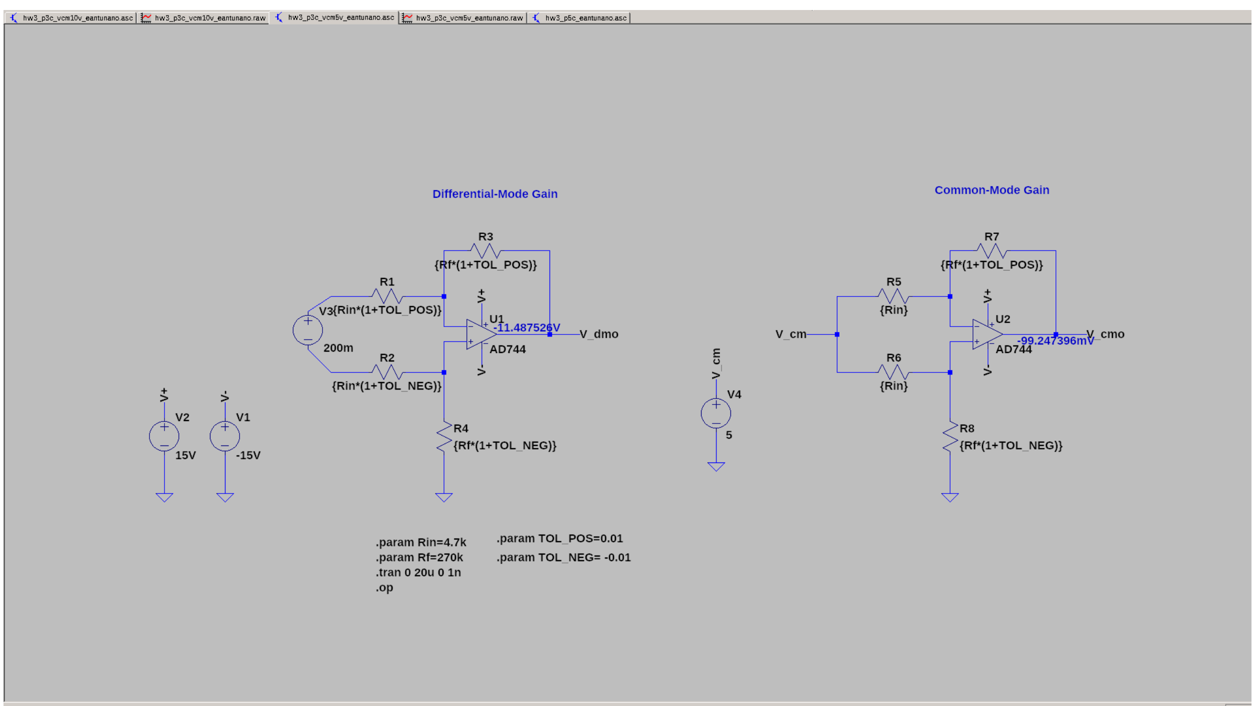
Part B 5V



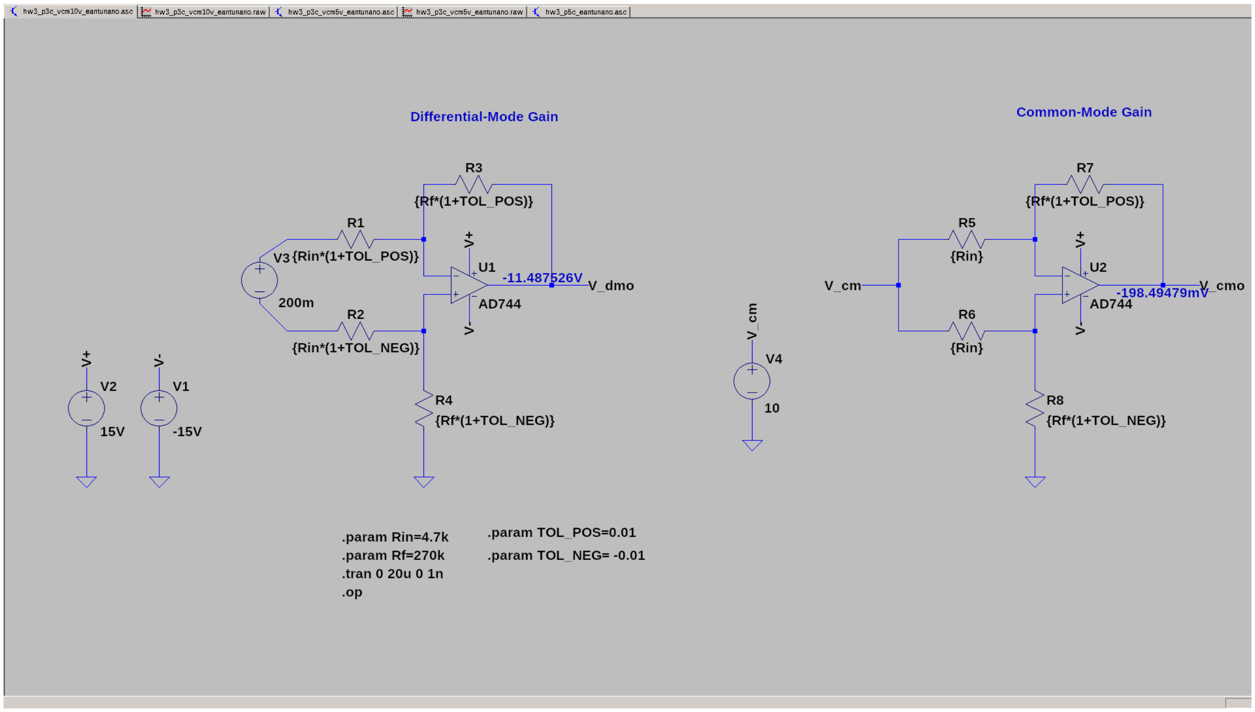
Part B 10V



Part C 5V



Part C 10V



Q3 [7 pts]: In **LTSPICE**, build the circuit shown in Figure 1 (using an AD744 op-amp) with the values of R1 and R2 as specified by the question.

(a) Find the DM gain and the CM gain via the application of V_{DM}=0.2 and V_{CM}=100.
(b) Using the application note attached for CMRR calculation in simulation models (on moodle), Find the idea CMRR of the circuit in part (a) (use ΔVin=5V, i.e. one case 10V the other 5V).
(c) Apply a resistor tolerance of 1% such that you ADD 1% to R2 values and you subtract 1% from R1 values. Simulate and calculate the CMRR value obtained from your simulation model (again using the method in the application note provided on moodle).
(d) Explain the results your obtained in (b) and (c) with respect to the ideal calculation.

[**Hint**: Check the data sheet of the amplifier to know some of its features as well as its biasing levels]

Sll; $\text{CMRR} = 20\log\left(\frac{V_{cm}}{V_{in}}\right) = 20\log\left(\frac{R_2}{\Delta R_2}\right) = 20\log\left(\frac{1}{2p}\right)\text{dB}$

Spice model V_{dm_o} Spice model V_{cm_o}

a) $A_{DM} = \left|\frac{V_o}{V_{in}}\right| = \left|\frac{-11.49}{0.2}\right| = 57.45 \qquad A_{cm} = \left|\frac{V_o}{V_{in}}\right| = \left|\frac{0.117}{100}\right| = 0.00117$

From app. note: b) $\text{CMRR} = \frac{\Delta V_{in}}{\Delta V_{out}}\left(1+\frac{R_2}{R_1}\right) = 20\log\left(\frac{10\text{ V} - 5\text{ V}}{2.5\,\mu V - 1.25\,\mu V}\left(1+\frac{270k}{4.7k}\right)\right)$

Spice model V_{cm_o}

$= 167.38\text{ dB}$

c) $\text{CMRR} = \frac{\Delta V_{in}}{\Delta V_{out}}\left(1+\frac{R_2}{R_1}\right) = 20\log\left(\frac{10\text{ V} - 5\text{ V}}{198.49\,mV - 99.25\,mV}\left(1+\frac{270k(1+0.01)}{4.7k(1+0.01)}\right)\right) = 69.38\text{ dB}$

Spice model V_{cm_o}

d) The CMRR dips significantly in part c because the variation in resistors R_f cause the A_{cm} to increase. In part b), the ideal case, A_{cm} is kept as close to zero as possible, which following $20\log(V_{cm}/V_{dm})$ dB keeps a high CMRR. With tolerances, a larger A_{cm} decreases the CMRR since A_{dm} remains constant even if R_f changes.

Q4

Q4 [10 pts]: A large microprocessor draws a total transient current of 10A from a 3.3V supply. The logic has a rise/fall time of 1nS. It is desirable to limit the Vcc to ground noise voltage peaks to 250mV, and each decoupling capacitor has 5nH of series inductance. The decoupling will be done with a multiplicity of equal value capacitors and should be effective at all frequencies above 20MHz.

(a) Sketch the value of the target impedance versus frequency
(b) What is the minimum number of decoupling capacitors required to fulfil the requirements?
(c) What should be the minimum value of each of these capacitors?
(d) Could larger value capacitors be used just as effectively? S30; increasing the value of the overall capacitance can decrease the overall impedance, which is the recommended technique

Question:

S32, for the target impedance would the antiresonance spikes be acceptable if they exceeded the target impedance even if the resonance dips were under the target impedance curve?

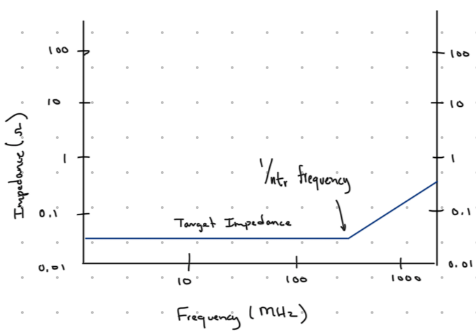
a) S33; example solution

Assume correction factor $k = 2$

$$Z_t = k\left(\frac{dV}{dI}\right)$$

$$Z_t = (2)\left(\frac{250 \cdot 10^{-3}}{10}\right) = 0.05\,\Omega = 50\,m\Omega$$

corner frequency $\frac{1}{\pi t_r} = \frac{1}{\pi(1 \times 10^{-9})} = 318\,MHz$



b) S32, minimum number of caps (n) to achieve a certain target impedance

$n = \frac{2L}{Z_t t_r}$ where the inductance L is the total inductance (cap, traces, IC, leads)

Z_t = target impedance

t_r = rise time

$$n = \frac{2(5 \times 10^{-9})}{(50m)(1 \times 10^{-9})} = 200 \text{ caps}$$

c) S33; example solution

$$Z_c = \frac{1}{\omega C} \longrightarrow C = \frac{1}{\omega Z_c}$$

Z_c = target impedance
ω = lowest freq of interest
C = total capacitance

$$C = \frac{1}{(20 \times 10^6)(50 \times 10^{-3})2\pi} = 159\,nF$$

$$\frac{C}{n} = \frac{159\,nF}{200} = 795\,pF \text{ per cap}$$

d) Purely for this problem, higher value caps would be effective. The only drawback is that the resonance frequency's overall impedance would reach a minimum at a lower frequency with fewer large caps and a constant overall capacitance. The signals rise/fall time would be lower.

Q5

S13;

Instead of using R_2, two buffer amplifiers can be added to the inputs of a standard amplifier to improve CMRR

The benefit of the amplifier is that there's a single resistor value for gain control (kR_f)

Output voltage for amplifier $V_o = (V_2 - V_1)\left(1 + \frac{2R_f}{kR_f}\right)\left(\frac{R_1}{R_1}\right)$

$$CMRR: 20\log\left(\frac{A_{Dm}}{A_{cm}}\right) = 20\log\left(\frac{A_{Dm}}{2p}\right) = 20\log\left(\frac{1+\frac{2}{k}}{2p}\right) \text{ dB}$$

For the <u>same tolerance</u> resistors in a differential amp, an instrumentation one will provide a CMRR that is $20\log(A_{Dm})$ higher.

a) $$A_{DC} = \frac{V_o}{V_2 - V_1} = \left(1 + \frac{2(1000)}{100}\right) = 1 + 20 = 21$$

b) S13;

$100 = k(1000)$

$k = 0.1$

$$CMRR = 20\log\left(\frac{1+\frac{2}{k}}{2p}\right) = 20\log\left(\frac{1+\frac{2}{0.1}}{2(0.01)}\right) =$$

$$\boxed{CMRR = 60.42 \text{ dB}}$$

c) $$A_{Dm} = \frac{V_o}{V_i} = \left|\frac{-4.16\text{ V}}{200\text{ mV}}\right| = 20.8$$

Is it $\frac{R_1(+\%)}{R_1(-\%)}$ for an instrumentation amplifier?

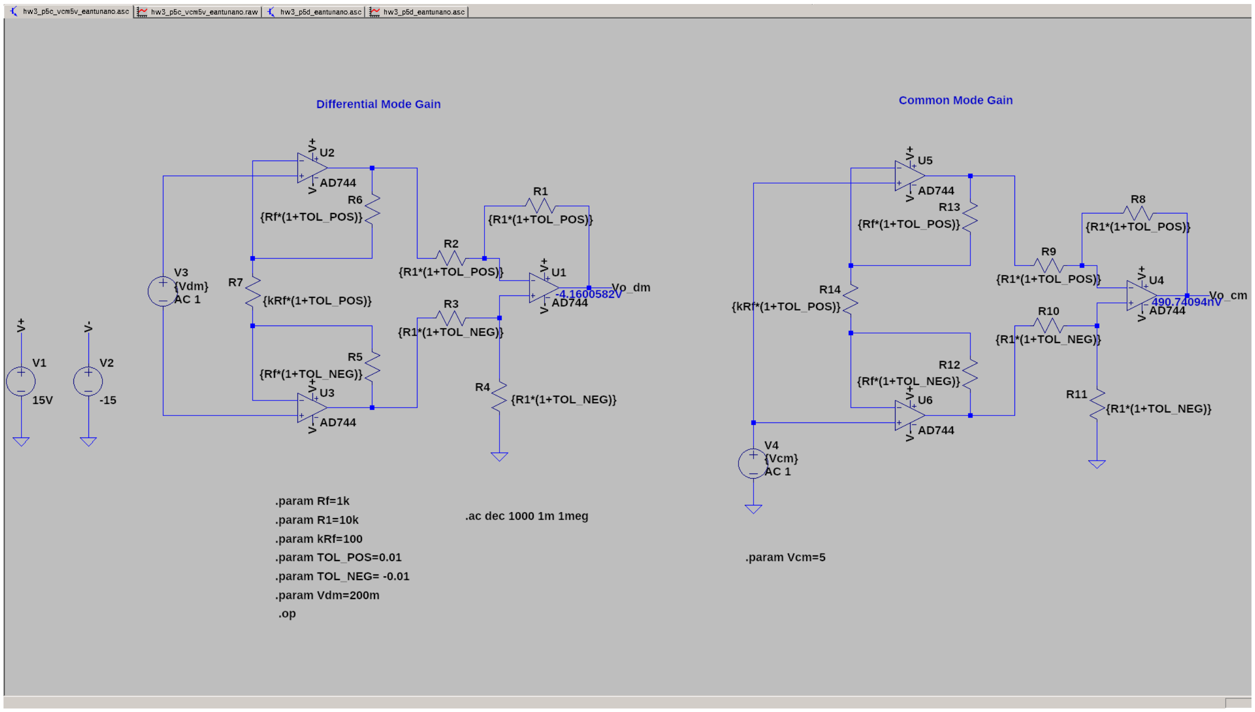
$$CMRR = \frac{\Delta V_{in}}{\Delta V_{out}}\left(1 + \frac{R_2}{R_1}\right) = 20\log\left(\frac{10\text{ V} - 5\text{ V}}{(948.56 - 490.74\text{ nV}}\left(1 + \frac{10k(1+0.01)}{10k(1-0.01)}\right)\right) = 146.87 \text{ dB}$$

Spice model V_{cm}-0

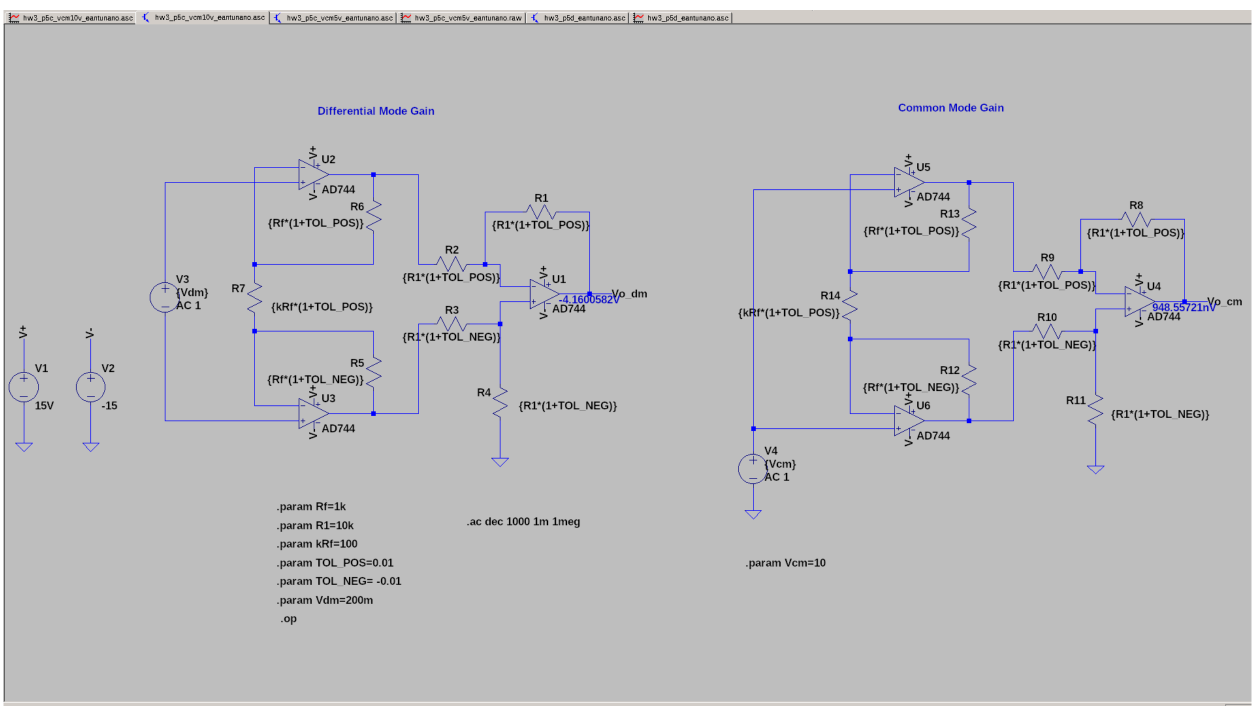
d) -3dB point @ 649.49 kHz for A_{Dm}

3dB point @ 23.667 Hz for A_{cm}

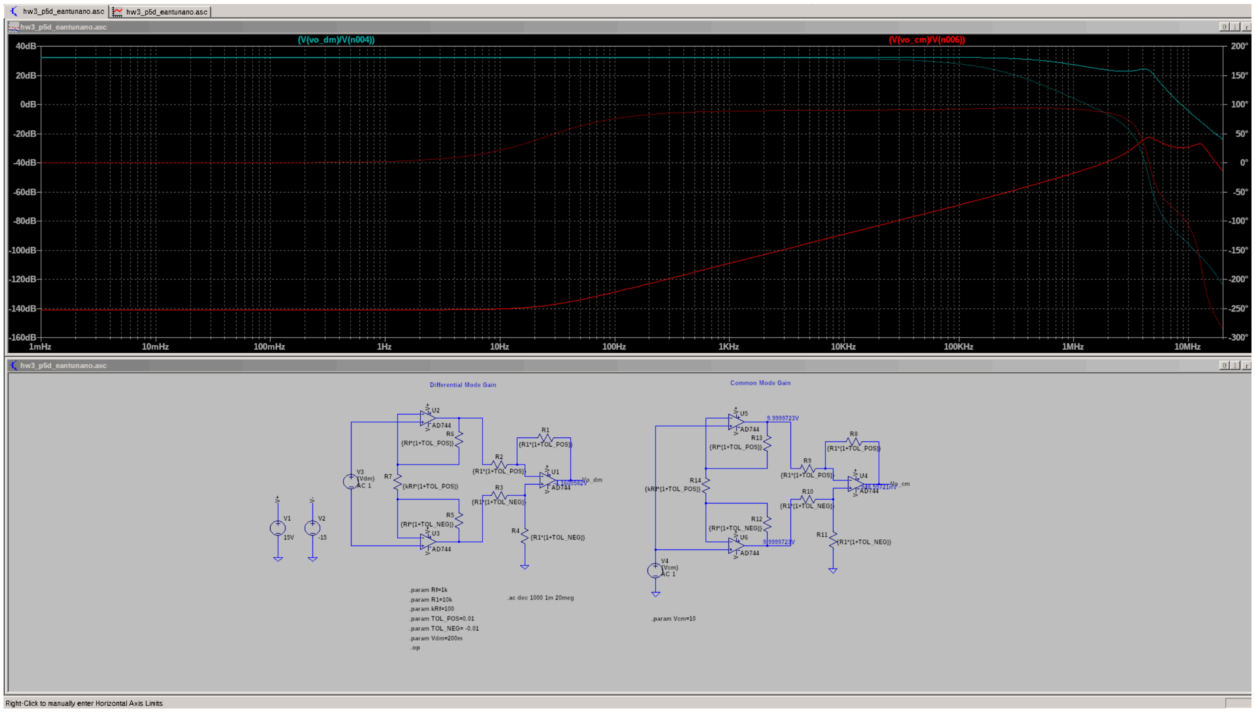
Part C 5V



Part C 10V



Part D



hw3_p5d_eantunano.asc
V(vo_dm)/V(n004)
V(vo_cm)/V(n006)
40dB
20dB
0dB
-20dB
-40dB
-60dB
-80dB
-100dB
-120dB
-140dB
-160dB
1mHz
10mHz
100mHz
1Hz
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
10MHz
200°
150°
100°
50°
0°
-50°
-100°
-150°
-200°
-250°
-300°
Differential Mode Gain
Common Mode Gain
.param Rf=1k
.param R1=10k
.param kRf=100
.param TOL_POS=0.01
.param TOL_NEG= -0.01
.param Vdm=200m
.op
.ac dec 1000 1m 20meg
.param Vcm=10
Right-Click to manually enter Horizontal Axis Limits