EE P 592 / EE 579A

Electromagnetic Compatibility

HW3

Q1 [8 pts]: A common-mode choke is placed in series with a transmission line that connects a low impedance source to a 900Ω load. The transmission line conductors each have a 1Ω resistance. Each winding of the common-mode choke has an inductance of 0.044H and a resistance of 4Ω.

(a) Above what frequency will the choke have a negligible effect on the signal transmission?

(b) How much attenuation (in dB) does the choke provide to a ground differential noise voltage at 60Hz, 180 Hz and 300Hz.

Q2 [10 pts]: For the Differential amplifier shown in Figure 1, R1 and R2 are 1% resistors with values of 4.7 kΩ and 270 kΩ, respectively.

(a) Calculate the Differential mode (DM) input impedance.

(b) What is the differential mode gain?

(c) Calculate the common-mode (CM) input impedance?

(d) What is the common mode gain?

(e) What will be the value of the CMRR?

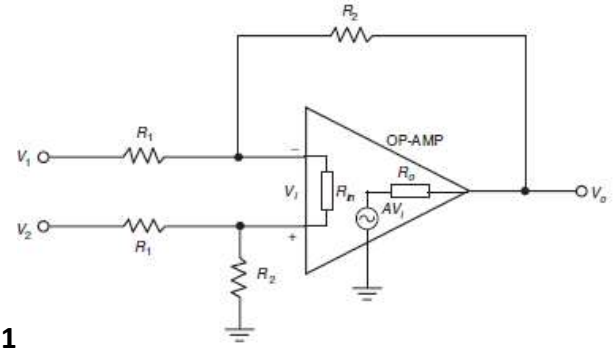

Figure 1

Q3 [7 pts]: In **LTSPICE**, build the circuit shown in Figure 1 (using an AD744 op-amp) with the values of R1 and R2 as specified by the question.

(a) Find the DM gain and the CM gain via the application of V_{DM}=0.2 and V_{CM}=100.

(b) Using the application note attached for CMRR calculation in simulation models (on moodle), Find the idea CMRR of the circuit in part (a) (use ΔVin=5V, i.e. one case 10V the other 5V).

(c) Apply a resistor tolerance of 1% such that you ADD 1% to R2 values and you subtract 1% from R1 values. Simulate and calculate the CMRR value obtained from your simulation model (again using the method in the application note provided on moodle).

(d) Explain the results your obtained in (b) and (c) with respect to the ideal calculation.

[**Hint**: Check the data sheet of the amplifier to know some of its features as well as its biasing levels]

Q4 [10 pts]: A large microprocessor draws a total transient current of 10A from a 3.3V supply. The logic has a rise/fall time of 1nS. It is desirable to limit the Vcc to ground noise voltage peaks to 250mV, and each decoupling capacitor has 5nH of series inductance. The decoupling will be done with a multiplicity of equal value capacitors and should be effective at all frequencies above 20MHz.

(a) Sketch the value of the target impedance versus frequency
(b) What is the minimum number of decoupling capacitors required to fulfil the requirements?
(c) What should be the minimum value of each of these capacitors?
(d) Could larger value capacitors be used just as effectively?

Q5 [15 pts]: **Figure 2** shows an Instrumentation amplifier with Rf = 1kΩ, kRf = 100Ω, and R1 = 10 kΩ. All resistors are with 1% tolerances.

(a) Calculate the Differential mode gain?
(b) Calculate the CMRR?
(c) In **LTSPICE**, build a model of this Instrumentation amplifier with AD744 op-amps from the library provided. Then, verify the value of the DM gain as well as the CMRR. For CMRR, let ALL R1's, the top side Rf and kRf have +ve 1% tolerance, while the bottom side Rf has -ve 1%. After the simulations (again for CMRR calculation, follow the application note), Compare with parts (a) and (b).
(d) Plot the gain (in dB) versus frequency for this amplifier (with the tolerances in part (c)) and identify the frequency within which its gain is stable, the value of the gain in dB and identify the frequency where the gain crosses the 3dB point. [Hint: you need AC analysis for this part]

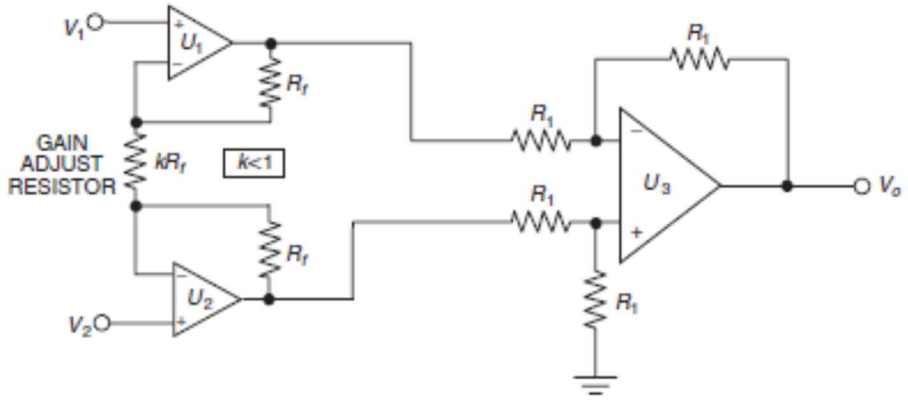

Figure 2

Submission Notes:

(1) submit a PDF file for your solutions including ALL figures, plots, circuit models, etc.
(2) Attach the LTSPICE files as separate files for each problem that asks for such a solution/model/file, name them according to the problem number, i.e. "HW3_Q2_b_Student_Name".
(3) Send the PDF file along with the individual circuit files in Canvas.