Electromagnetic Compatibility (EMC)

Topic 8

Balancing and Filtering

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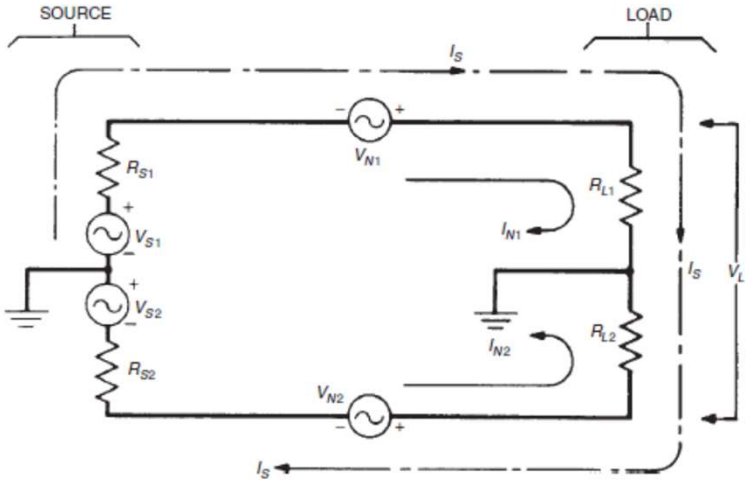
Balancing

- A circuit is considered Balanced if it consists of two conductors that have the same non-zero impedance with respect to a reference (i.e. ground) and all other conductors
- The purpose of Balancing is to have the same noise pick up in both conductors, and thus make them cancel at the load side
- If the impedances of the two conductors are not equal, the system is not balanced (unbalanced)
- Using transformers or differential amplifiers are two possible approaches to providing a Balanced termination
- Telephone lines are balanced and use twisted pairs.
- Consider the system shown,
  - if Rs1 = Rs2 then the source is Balanced
  - If RL1 = RL2 then the load is Balanced
  - If both above conditions are satisfied, then the System is Balanced
- Balancing is with respect to the impedances not the induced voltages



I_S is source differential current

I_N is noise common mode current

Apply KVL:

$$V_L = I_{N1}R_{L1} - I_{N2}R_{L2} + I_S\left(R_{L1} + R_{L2}\right)$$

$$if\ I_{N1} = I_{N2} \text{ and } R_{L1} = R_{L2}, \text{ then}$$

$$V_L = I_S\left(R_{L1} + R_{L2}\right)$$

- Figure A shows a Balanced circuit with inductive noise voltages (V_1 and V_2), and capacitive noise current (I1 and I2).
- The ground potential differences between the load and source is represented by V_{CM}
- If the two conductors are adjacent to one another, or are a twisted pair, then noise voltages V_1 and V_2 will cancel at the load (why?)
- For capacitive coupling at ports 1 and 2 at the load side, consider Figure B for better illustration.
- As we saw in the cabling section (T6), noise voltages from adjacent sources (conductor 3) to the victim lines at lines 1 and 2 induced via capacitive coupling are (refer to Figure B):

$$V_{N1} = j\omega R_{C1} C_{13} V_3$$

$$V_{N2} = j\omega R_{C2} C_{23} V_3$$

- If the circuit is Balanced, Rc1 = Rc2. And if the two conductors are in close proximity, then C13=C32.
- Thus VN1=VN2, and they will cancel at the load!
- A Balanced twisted-pair will protect against magnetic and electric field couplings!

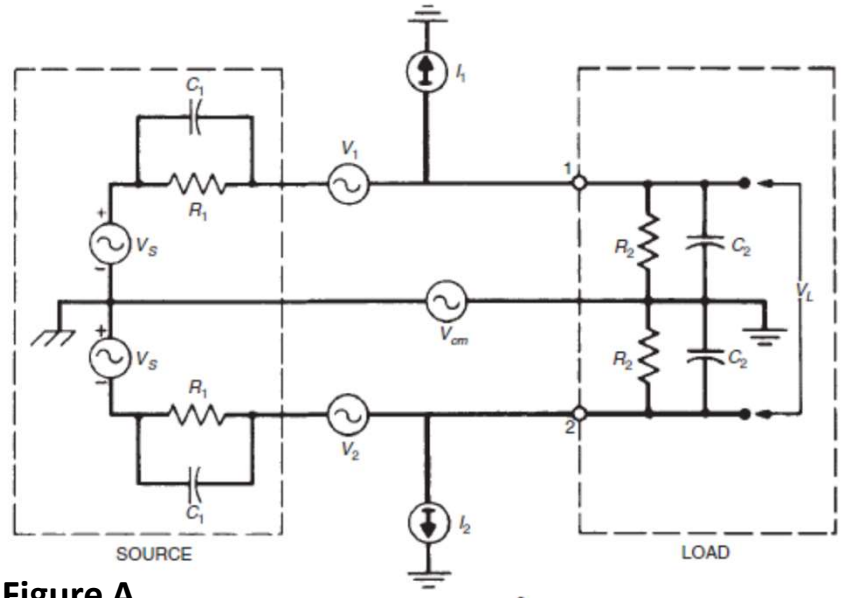


Figure A

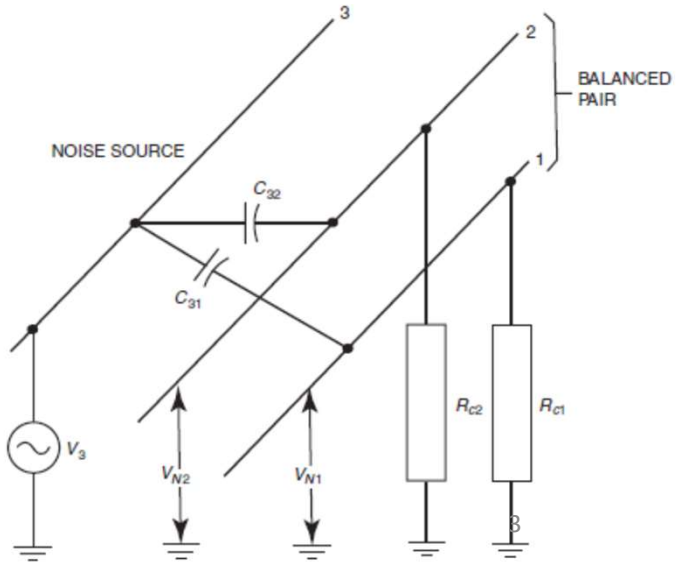


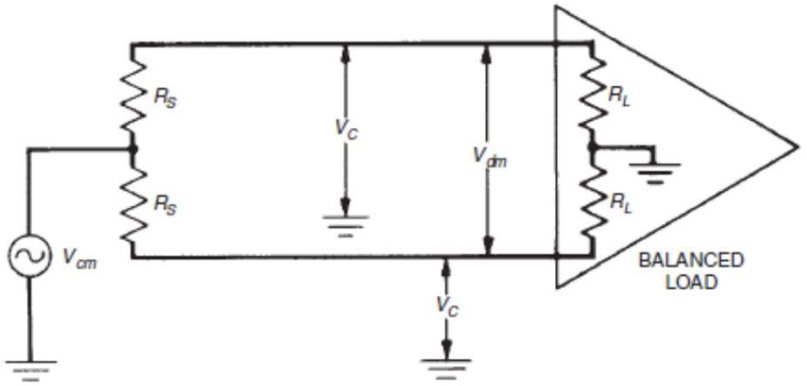
Figure B

Common Mode Rejection Ratio (CMRR)

- Is a metric to quantify the effectiveness of a Balanced circuit in rejecting common mode noise voltages
- Consider the circuit shown, if we have perfect Balance, we will have no differential mode voltage at the input of the amplifier (**due to common mode source**).
- In practical circuits, the Balance is not perfect and some small levels of V_{DM} are observed (due to a CM source).
- The CMRR, or Balance, is defined as

$$CMRR = 20\log\left(\frac{V_{CM}}{V_{DM}}\right) \quad \text{dB}$$

- The greater the CMRR the better and the greater the CM noise reduction obtained

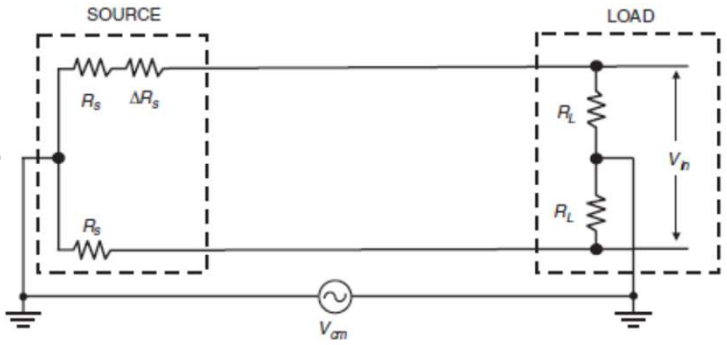


- If source resistance Rs is much smaller than the load one (which is a practical case), then V_c at the load side will almost equal V_{cm}, thus we can relate the two voltages as

$$CMRR = 20\log\left(\frac{V_c}{V_{DM}}\right) \quad \text{dB}$$

- In a real world scenario, unbalance due to load, source, cable and any parasitics will occur.
- We need to consider resistive and reactive unbalance

- In many practical scenarios, the load is Balanced, but the source is not!
- The CMRR caused by an unbalanced source resistance ΔRs can be determined by referring to the shown figure, as



$$CMRR = 20\log\left(\frac{\left(R_L + R_s + \Delta R_s\right)\left(R_L + R_s\right)}{R_L \Delta R_s}\right) \quad \text{dB}$$

- If RL >> Rs+ ΔRs , which is usually the situation, we have

$$CMRR = 20\log\left(\frac{R_L}{\Delta R_s}\right) \quad \text{dB}$$

- For example, consider that RL= 10K, ΔRs = 10, then CMRR is 60 dB.
- The effect of the source unbalance can be reduced via:
  - Reducing the common mode voltage
  - Reducing the source unbalance ΔRs
  - Increasing the common mode load impedance RL

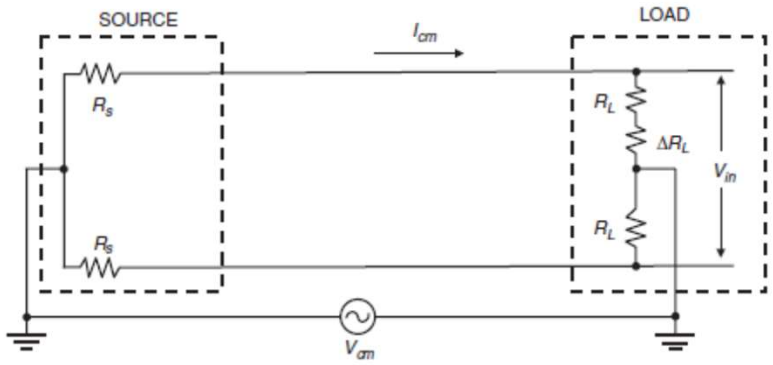
- If the unbalance is at the load side, as shown in the figure to the side, we have

$$CMRR = 20\log\left(\frac{\left(R_L + R_s + \Delta R_L\right)\left(R_L + R_s\right)}{R_s \Delta R_L}\right) \quad \text{dB}$$

- If RL >> Rs, then we get

$$CMRR = 20\log\left(\frac{\left(R_L + \Delta R_L\right)}{\Delta R_L}\left(\frac{R_L}{R_s}\right)\right) \quad \text{dB}$$

- Thus, the larger the ratio of RL/Rs the greater the noise rejection, regardless of ΔRL.
- So, a low source impedance with a large load impedance will provide the largest CMRR (ideally, zero source impedance and infinite load one)
- We can conclude that a large load impedance will always maximize CMRR for the cases of source or load unbalance. This is because an infinite load impedance will have no current flowing and no noise voltage drop will occur.



- If the load resistors have tolerance of +/- x%, the maximum variation (unbalance) will be 2x%
- Let ΔRL/RL= 2p (value not percentage). If RL >> ΔRL, then we can write

$$\boxed{CMRR = 20\log\left(\left(\frac{1}{2p}\right)\left(\frac{R_L}{R_s}\right)\right) \quad \text{dB}}$$

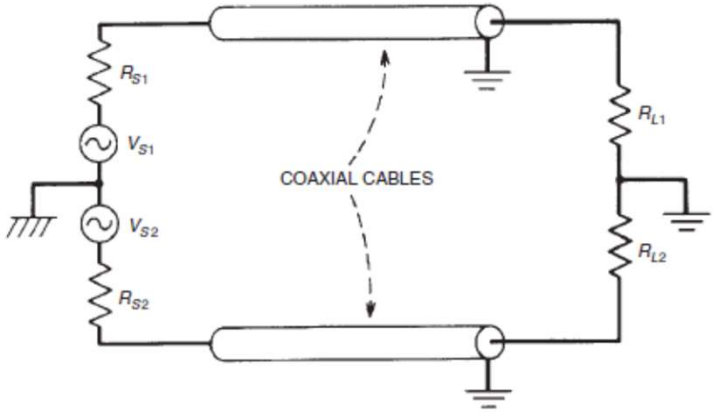
Cable Balance

- In cables, both resistance and reactance of each conductor must be balanced.
- In many cases, circuit unbalances are higher than the cable ones.
- When high CMRR values are required, i.e. 100dB or more, or when using long cable lengths, then cable balancing becomes important
- Resistive unbalances of cables are small and usually ignored.
- Capacitive unbalances are usually of the order of 3-5%. At low frequencies, they can be ignored. At higher frequencies, consider such unbalances in your model and calculations.
- Inductive unbalances are almost non-existent for braided shield cables if properly terminated (as we saw before)
- Foil shield based cables might have more inductive unbalance at lower frequencies and needs to be treated with care. But due to the skin effect at higher frequencies, the inductive unbalance becomes less problematic in such cables. Some issues of foil shield based cables are due to the end of cable drain wire termination that is inevitable.
- **Remember, effects of Shielding and Balancing are additive. Shielding can reduce the amount of CM pickup in the signal conductors, while the Balancing reduces the portion of the CM voltage that is converted to DM voltage that is coupled to the load**.

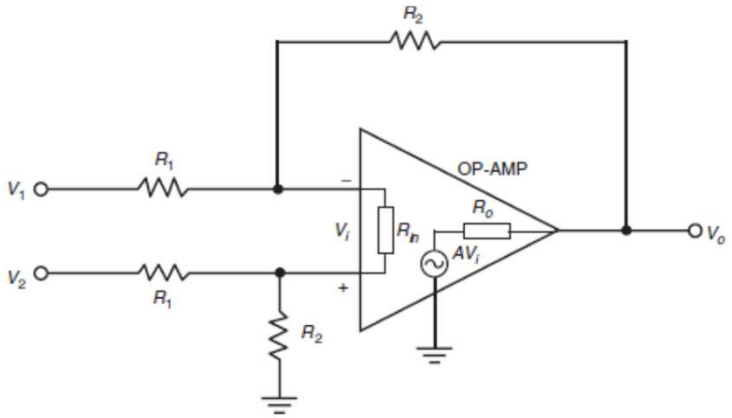
System Balance

- A **twisted pair** cable is inherently a **Balanced configuration**. Twisted pairs of shielded twisted pairs are often used as the connecting cables in a balanced system.

- A **coaxial cable** on the other hand is **not a Balanced configuration**. If we want to use a coaxial cable in a balanced system, then we need two cables to be used as shown in the figure



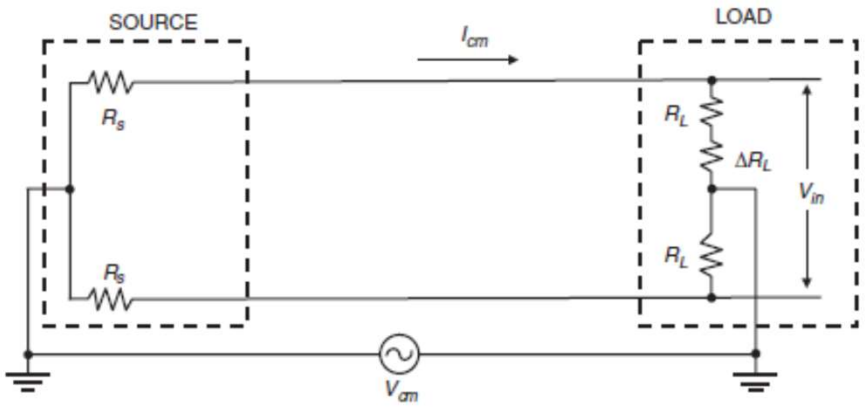
Differential Amplifiers

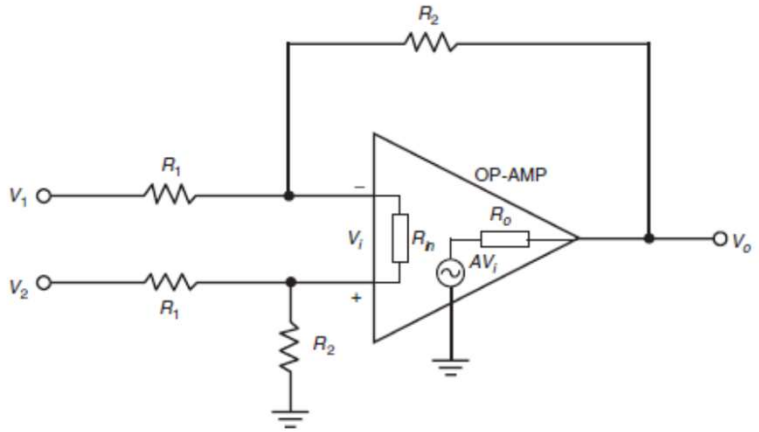


- An Op-Amp has a differential input and a single-ended output
- An ideal Op-Amp has:
  - Very large gain A (~ ∞)
  - Very large (~∞) input resistance between (+) and (-) Rin
  - Zero output resistance Ro
  - An infinite CMRR
- Practical Op-Amps have DC gain A ~ 100 000, Rin ~ MΩ, Ro ~ few Ω and CMRR~70-80dB
- For an inverting differential amplifier as the one shown, we have (please check detailed derivation note on website):

$$A_{DM} = -\frac{R_2}{R_1} \qquad R_{in(CM)} = \frac{(R_1 + R_2)}{2}$$

$$R_{in(DM)} = 2R_1$$





- Assume the differential amplifier (right) is connected to a Balanced source, and let RL (left) equal to R1+R2 (right). Then we have

$$V_{in}(left) = I_{CM}\Delta\left(R_1 + R_2\right) = V_1 - V_2$$

$$I_{CM} = \frac{V_{CM}}{\left(Rs + \Delta\left(R_L\right) + R_L\right)} = \frac{V_{CM}}{\left(Rs + \Delta\left(R_1 + R_2\right) + \left(R_1 + R_2\right)\right)}$$

- When R2 >> R1, R2 >> Δ(R1+R2) and R2 >> Rs, then $V_{in} = \frac{\Delta R_2}{R_2} V_{CM} = V_1 - V_2$
- The differential amplifier output becomes $V_{out} = \frac{\Delta R_2}{R_2}\left(A_{DM} V_{CM}\right)$
- Thus, the CM gain is,

$$A_{CM} = \frac{V_{out}}{V_{CM}} = \frac{\Delta R_2}{R_2}\left(A_{DM}\right) = \frac{\Delta R_2}{R_2}\left(\frac{R_2}{R_1}\right) = \frac{\Delta R_2}{R_1}$$

$$A_{CM} = \frac{V_{out}}{V_{CM}} = \frac{\Delta R_2}{R_2}\left(A_{DM}\right) = \frac{\Delta R_2}{R_2}\left(\frac{R_2}{R_1}\right) = \frac{\Delta R_2}{R_1}$$

- The worst case tolerance in R_2 is $2\Delta R_2$. Representing the tolerance as p (as before),

$$A_{CM} = \frac{V_{out}}{V_{CM}} = \frac{\Delta R_2}{R_2}\left(A_{DM}\right) = 2p\left(\frac{R_2}{R_1}\right) = \frac{2pR_2}{R_1}$$

- The CMRR can be found by substituting V_{in} for V_{DM}, giving,

$$\boxed{CMRR = 20\log\left(\frac{V_{CM}}{V_{in}}\right) = 20\log\left(\frac{R_2}{\Delta R_2}\right) = 20\log\left(\left(\frac{1}{2p}\right)\right) \quad \text{dB}}$$

- When we use matched resistors with low tolerance values and a balanced source, the CMRR of the amplifier get high

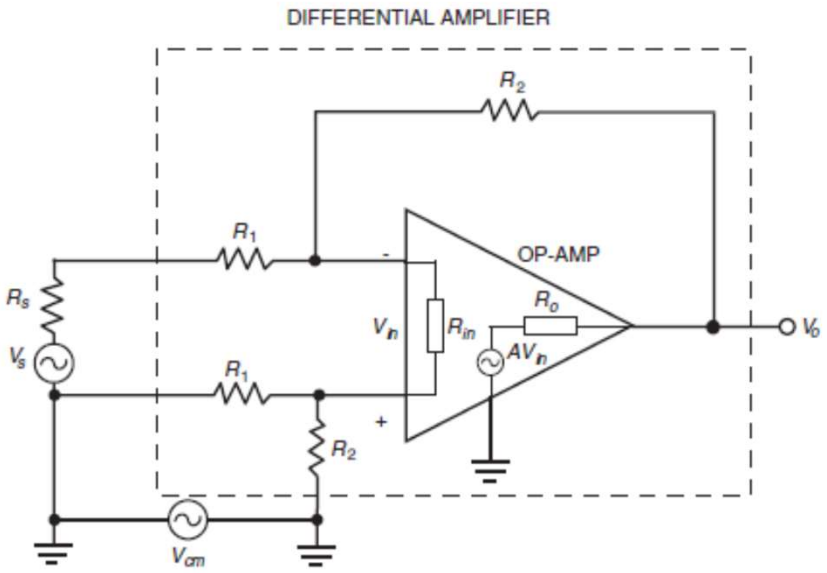
- For example, using a balanced source, and resistor tolerances of 0.1% are used for R1 and R2 (p=0.001), then CMRR will be 54dB.

- If the differential amplifier is driven by an unbalanced source we saw before (slide 5) that

$$CMRR = 20\log\left(\frac{R_L}{\Delta R_s}\right) \quad \text{dB}$$

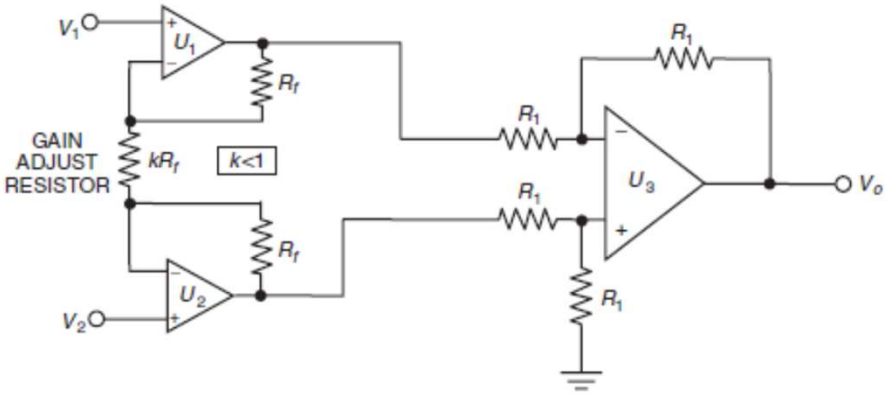
- Which for a differential amplifier becomes (remember assumptions from before, i.e. R2 >> R1)

$$CMRR = 20\log\left(\frac{R_2}{R_s}\right) \quad \text{dB}$$



- For example, if Rs = 500Ω and R2 = 100kΩ, then CMRR is 46dB.
- So, the best way to increase the CMRR of a differential amplifier driven from an unbalanced source is to increase the amplifier CM input impedance to a value of several hundred kΩs or several MΩs.
- Be aware that increasing the resistor value also increases its thermal noise contribution! So a balance should be targeted!

Instrumentation Amplifiers



- Instead of increasing the load impedances (R2), we can add two high-impedance buffer amplifiers to the inputs of a standard differential amplifier to improve the CMRR.
- We will then get an Instrumentation Amplifier as shown.
- This amplifier has the advantage of have a single resistor value for Gain Control (kR_f)
- The output voltage for this amplifier is (see PDF note)

$$V_o = (V_2 - V_1)\left(1 + \frac{2R_f}{kR_f}\right)\left(\frac{R_1}{R_1}\right)$$

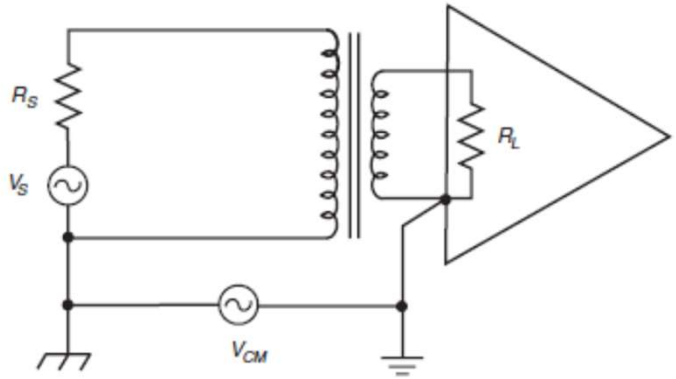
- The CMRR becomes

$$CMRR = 20\log\left(\frac{A_{DM}}{A_{CM}}\right) = 20\log\left(\frac{A_{DM}}{2p}\right) = 20\log\left(\frac{1+\frac{2}{k}}{2p}\right) \quad \text{dB}$$

- For the same tolerance resistors in a differential amplifier, an instrumentation one will give a CMRR that is $20\log(A_{DM})$ higher. If 0.1% tolerances, and A_{DM}=100, the **instrumentation amplifier** provides **94dB** of CMRR compared to **54dB differential** one!

Transformer coupled inputs

- Using a transformer will improve the CMRR because as we saw before it will reduce the CM noise.



Input Cable Shield Termination

- As we discussed in T7, cable shields are normally grounded at both ends. But, when using high CM input impedance amplifier circuits (i.e. Instrumentation amplifier), the input of shielded cable is one connected to the source ground only, the load side is not.
- If the load shield side is grounded, the input high impedance of the amplifier will be shunted via the capacitor to ground, thus lowering its impedance and degrading CMRR. Grounding at the source will shunt the source resistance which is by default low, so this is recommended.
- This approach might increase the radiated emissions in high frequency circuits. Thus a trade off should be made. Be aware!

- To demonstrate such an effect of cable shield grounding on CMRR, consider a high input impedance differential amplifier that is fed from a 600 Ω unbalanced source through a shielded cable that has a capacitance of 30pF/ft. If the cable is 100ft. long, the total cable capacitance is 3nF. If the cables shield is grounded at the amplifier end, then the cable capacitance will shunt the amplifier input impedance, thus not being able to exceed the capacitive reactance of the cable.
- Thus, at 1000Hz, the CMRR will not exceed

$$CMRR \le 20\log\left(\frac{R_L}{\Delta R_s}\right) = 20\log\left(\frac{1}{2\pi f C \Delta R_s}\right) = 20\log\left(\frac{1}{2\pi(1000)\left(3\times10^{-9}\right)(600)}\right) = 39 \text{ dB}$$

- Note that RL >> Zc, thus Zc will dominate (they are in parallel!)
- So regardless of the input impedance of the amplifier (load), the cable capacitance will dominate.
- If the input impedance of the amplifier is 2MΩ, and if the cable was grounded at the source side, then the obtained CMRR will be of the order

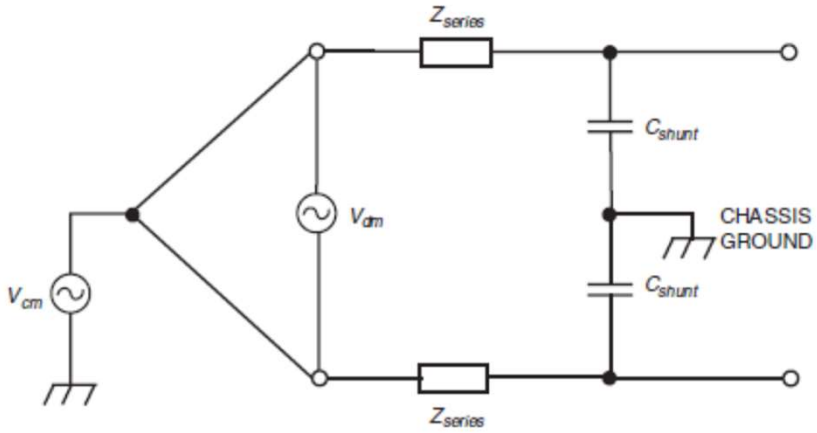
$$CMRR = 20\log\left(\frac{R_L}{\Delta R_s}\right) = 20\log\left(\frac{2\times10^6}{600}\right) = 70.5 \text{ dB}$$

Filtering

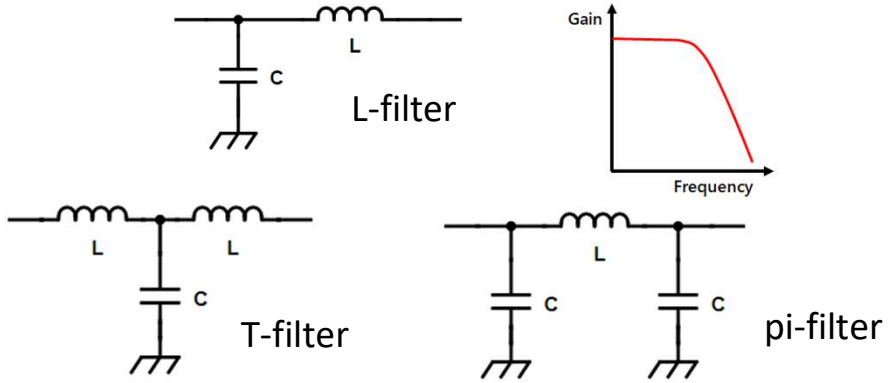
- Filters can be for DM or CM signals.
- Signal line or DM filters are well understood in literature.
- CM filters are used to supress the noise on the cables while passing the desired DM signal.
- Three reasons why CM filters are more difficult to design that DM ones:
  - We usually do not know the source impedance
  - We usually do not know the load impedance
  - The filter should not disturb the desired signal (DM) on the cable
- For CM signals, the source is the noise generated by the circuit, and the load is usually some cable that behaves as a radiator (antenna), with an unknown impedance that usually varies with frequency, cable length, and cable routing, among other variables.
- The impedance of the ground plane in a PCB is taken as the source impedance of a CM signal (thus low value) and the load impedance is that of the cable.
- For a CM filter not to disturb the DM (desired) signals, the DM passband of the filter must be: - the highest frequency present (for narrow band signals)

  - the $1/(\pi\ tr)$ frequency of the signal (for wideband signals)

- Signal filters should be placed as close as possible to the source or driver (clock line filters, etc)
- CM filters should be located as close as possible to where the cable leaves or enters the enclosure.
- The figure shown shows a CM filter consisting of a series and a shunt components. They are placed on the two lines; the signal conductor and its return path.
- The CM source, sees 2C (two times) the capacitance as they are in parallel, while the DM source sees ½ C (because the two caps are in series for the DM signal). Thus more filtering to the CM compared to DM.
- The CM source sees Zseries/2 (parallel combination), while the DM signal sees 2 Zseries, thus 4 times the CM values. This is NOT GOOD! We want the Zseries to have more effect on the CM signal not the DM signal. Thus, the **solution** is to use a Common-Mode Choke for this series impedance, as it presents a ZERO impedance for DM signals and only affects CM signals as we saw earlier.



- CM filters are low-pass-filters (LPF) that can be constructed with 1, 2 or 3 elements
- Single-element filters:
  - A single series element
  - A single shunt element
- Multi-element Filters:
  - An L-filter (one series and one shunt)
  - A T-filter (two series and one shunt)
  - A pi-filter (two shunt and one series)



- Advantages of single-element filters is that they need 1-element only, but they cannot provide sharp stop band attenuation where multi-element filters can provide.
- The shunt element in the filter is almost always a capacitor, with a value based on the frequency range of the filter. The series element can be a resistor, an inductor or a ferrite. Inductors are used for lower frequencies (~30MHz) while ferrites are used for higher ones. But be aware of the resonances of such elements (see T5).
- If the source impedance is Low (as is the case usually), and the load impedance is high, an L-shaped filter is used with its high impedance element (inductor) connected to the source side and the shunt capacitor connected to its load side would be an effective connection, because filtering occurs due to impedance mismatches.

- To have an effective single element filter, a series impedance filter must have an impedance larger than the sum of the source and load impedances. While a shunt filter element should have an impedance less than the parallel combination of the source and load impedances.
- Three cases:

(1) Both source and load impedances are LOW → A series impedance filter element will be effective

(2) Both source and load impedances are HIGH → a shunt capacitor will be effective

(3) One of the impedances (source or load) is Low and the other is High → multi-element filter should be used

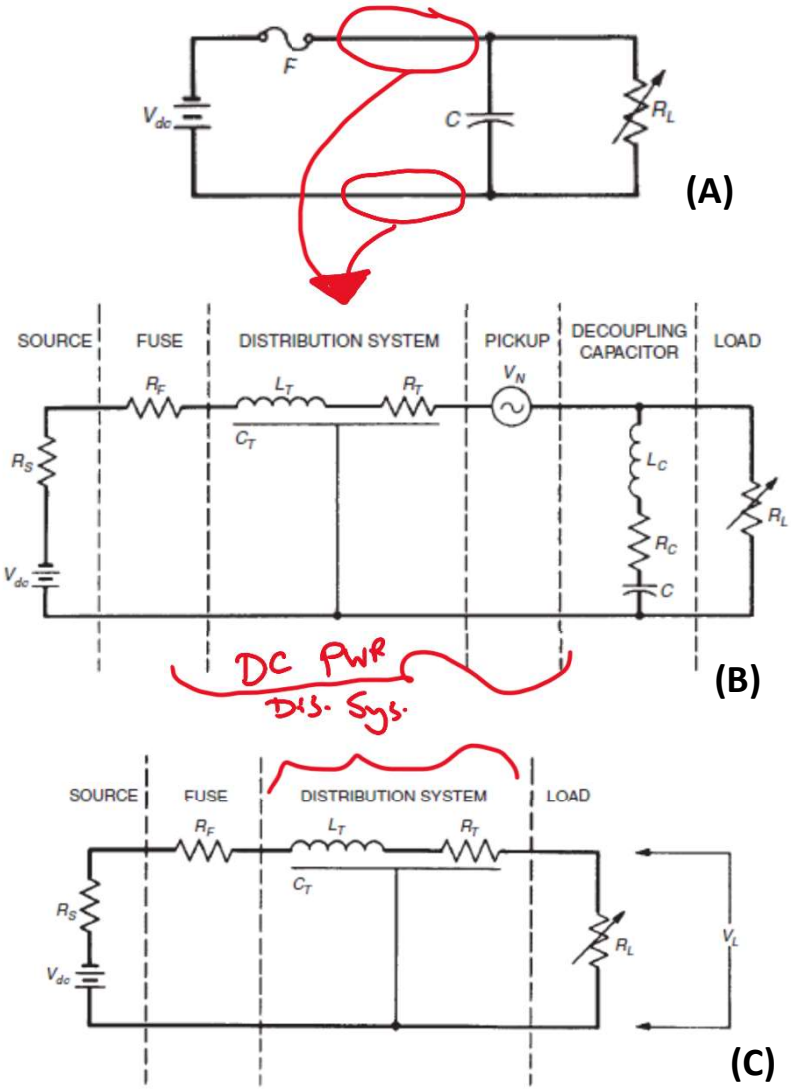
- Note that CM filters need to be applied to ALL the cables/conductors leaving or entering the equipment enclosure. The use of Ferrite cores will allow the use of ONE CORE that can have all conductors run through, and thus provide an economical solution (check your laptop cables, and other electronics for such a cylinder)

Power Supply Decoupling

- The DC power supply distribution system is common to many circuits within the system.
- It should not be a channel for coupling noise between connected circuits
- The DC power distribution system should supply a nearly constant DC voltage to ALL connected loads and circuits under varying load currents. In addition, any noise generated at the load side, should not generate a noise signal on the DC power distribution network (bus)
- Ideally, a power supply is a zero impedance source of voltage. In practice, they have finite impedance values (should be as low as possible). In addition, the conductors connected to the distribution network adds to this impedance.
- Local decoupling capacitors are used next to loads to remove high frequency noise from being fed into the DC power distribution system, and also provide a localized source of DC power reducing peak current surges that might propagate within the network, so they act as local sources of current.

- Figure (A) shows a typical power distribution system with a local decoupling capacitor (C).
- In the detailed circuit in (B), the noise voltage picked up by this circuit from other adjacent ones is given by V_N, and the decoupling capacitor is represented by its practical model with some internal resistance and inductance (leads).
- To reduce V_N, we saw in previous lectures how that can be done (CM noise reduction via cable shield grounding, reducing ground loops, CM filters, etc).
- The response of a decoupling capacitor is based on a sudden change in the current demand due to the switching of the load (i.e. $C = \Delta I/(\Delta V/\Delta t)$).
- Removing V_N and C, we simplify (as in (C)) the problem as:
  - (1) Determine the static or DC performance of the system
  - (2) Determine the transient or noise performance of the system
- from (1), we can write (L is shorted at DC and C is open),

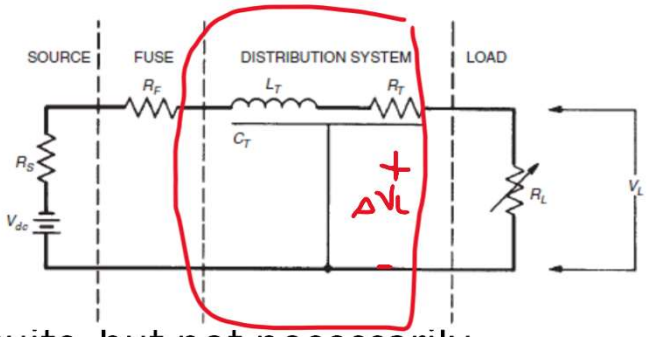
$$V_{L(\min)} = V_{DC(\min)} - I_{L(\max)}\left(R_s + R_F + R_T\right)_{\max}$$



- for (2), the instantaneous voltage change in the DC distribution network across the load will be,

$$\Delta V_L = \Delta I_L Z_0$$

$$Z_0 = \sqrt{\frac{L_T}{C_T}}$$



- This instantaneous current change assumption is correct in digital circuits, but not necessarily true for analog ones (you need to check your system and circuits).
- We can see that for best performance, noise performance, the characteristic impedance (Z0) of the power distribution network should be as low as possible (typically 1Ω or less)
- To reduce inductance, use rectangular cross sectional conductors instead of round ones, and return currents as close as possible to their corresponding ones (reduce ground loop areas).
- The optimum power distribution system line would be one with parallel flat conductors, as wide as possible (i.e. power and ground planes in a PCB), placed one on top of the other and as close as possible.
- For parallel flat conductors 0.25in wide, and separated by 0.005in with epoxy glass (FR-4) substrate, we have an impedance of $Z_0 \approx \frac{377}{\sqrt{\varepsilon_r}}\left(\frac{0.005}{0.25}\right) = 3.55\Omega$
- Thus, we place decoupling caps to reduce the impedances at the load locations

Low-frequency analog circuit decoupling

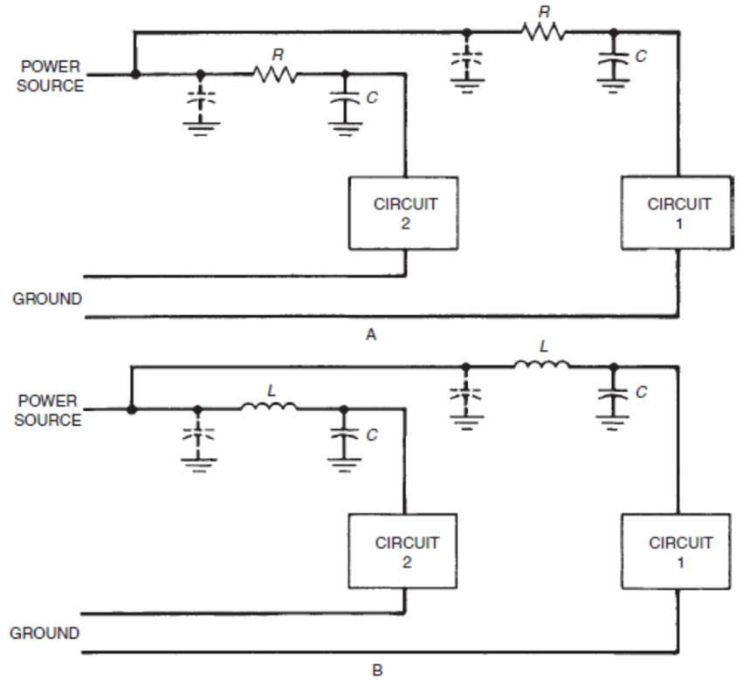
- Resistor-capacitor, and inductor capacitor decoupling networks can be used to isolate circuits from the power supply, to eliminate coupling between circuits and the keep power supply noise from entering the circuit.
- L-C filters are preferred over and provide more filtering compared to R-C ones, as R-C ones suffer from voltage drops across the resistors. While R-C filters can be more effective for noise reduction, as the noise is dissipated as head in R. Dissipating noise in L might increase radiation emissions!
- The resonant frequency of L-C filters is:

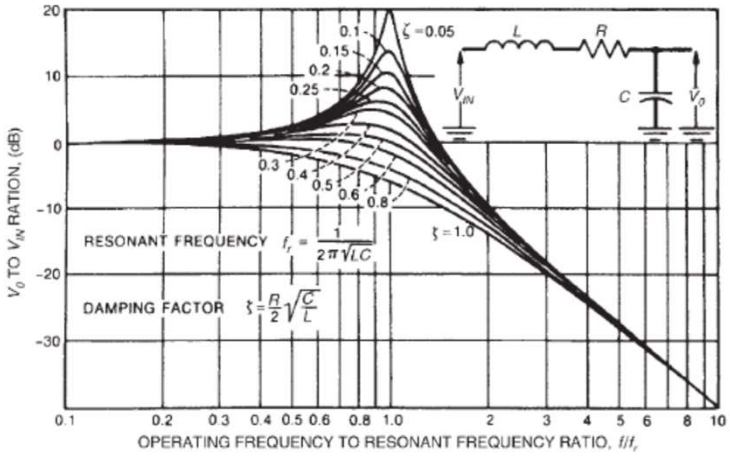
$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

- The output signal from the filter can have a higher level from the entering one if damping factor was not designed properly.

$$\zeta = \frac{R}{2}\sqrt{\frac{C}{L}}$$

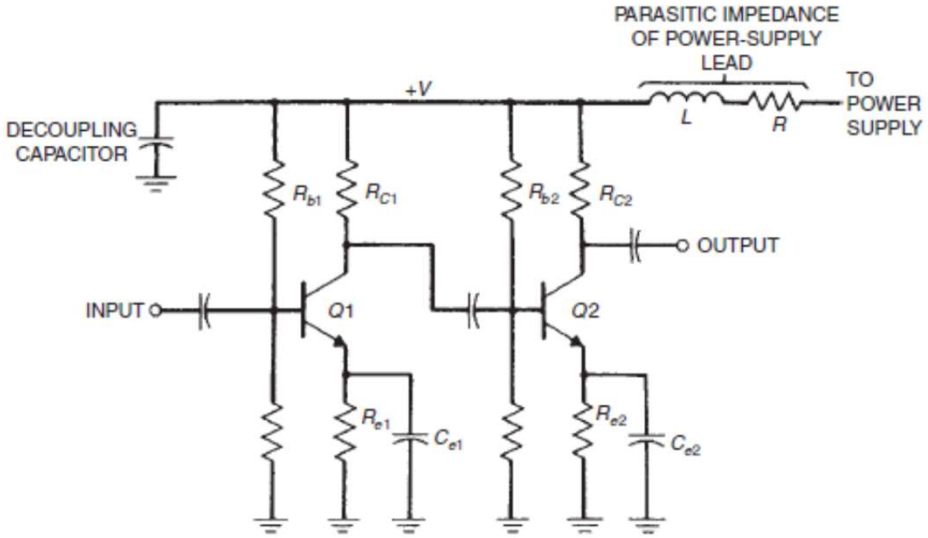
- A second capacitor can improve the filtering capability (dashed)





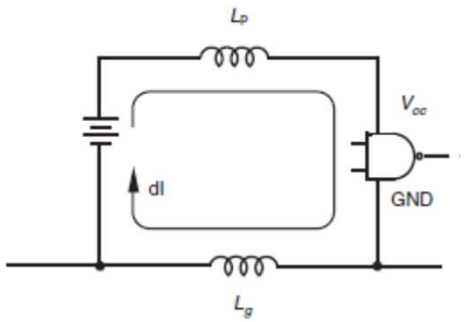
Amplifier decoupling

- It is hard to guarantee that the AC impedance between the power supply and ground is zero unless a decoupling capacitor is placed between the power supply and ground at the amplifier.
- This capacitor should serve as a short circuit across the frequency range over which the amplifier operates.

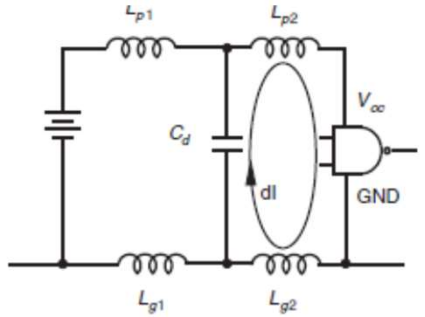


Power Distribution Network (PDN)

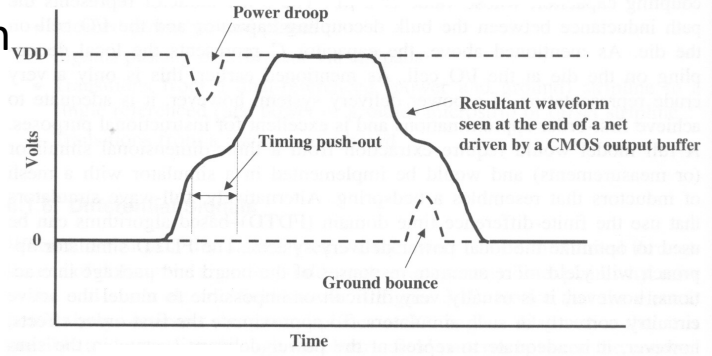
- An Ideal PDN will:
  (1) Supply constant DC voltage to the loads
  (2) Not propagate any AC noise generated by loads
  (3) Will have 0 AC impedance between power and GND
- Power supplies can be based on voltage regulator modules (VRMs) in digital systems
- When the I/O switches, it requires a fast current supply from the VRM, i.e. power distribution network (PDN) circuits.
- If the series inductance L_p+L_g of the VRM is large enough (along with its return ground path), it will look like an open circuit (why?), and the demand for current by the I/O will not be satisfied, thus causing a Power Droop/Ground Bounce (low→ high, and high → low) in the output pulse.
- This will DIVASTATE the SI!
- We will use decoupling capacitors (C_d) to alleviate this problem.



A



B



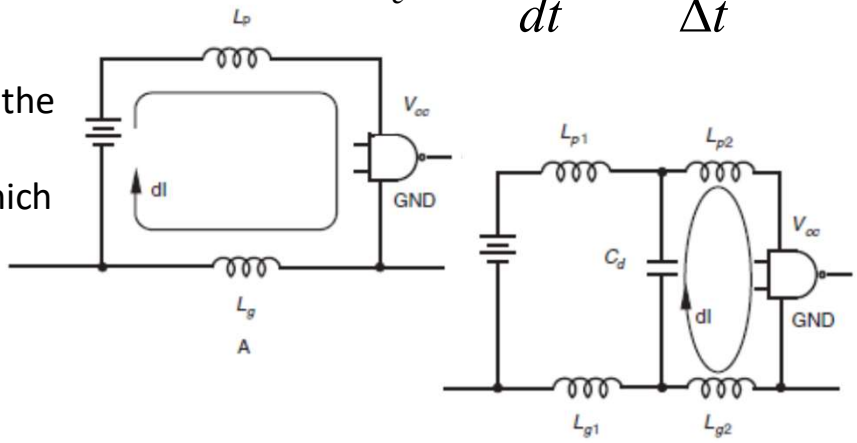
Telltale sign of a power delivery problem.

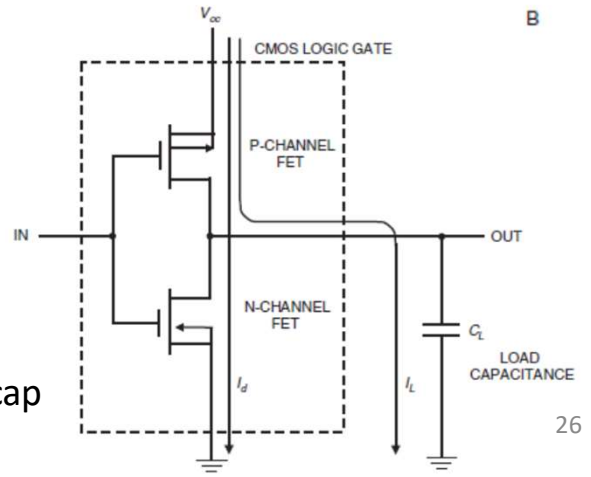
- The voltage transient (voltage drop + noise) can be reduced by either decreasing the inductance (L_g+L_p) or reducing the rate of change of the current that is flowing in these inductances.
- The loop area also can enhance noise pickup as we saw before
- Thus, a decoupling capacitor can serve as:
  (1) A source of charge (voltage) that is close to the IC that can provide the fast transient currents with a low-impedance path
  (2) It can provide a low AC impedance between PWR and GND rails which can short out AC noise from the loads (ICs)
  (3) Breaks the large loop created by long return current paths
- Two different power supply transient currents occur when digital ICs switch:
  - Transient load current (I_L), when the gate charges the load capacitance
  - Dynamic internal current (I_d), when the two transistors at the output stage changes (one closes, and the other opens) and momentarily conduct together
- For n-loads connected, we will have $I_L = \frac{nC_L V_{cc}}{t_r}$
- For n-gates switching, we will have $I_d = \frac{nC_{pd} V_{cc}}{t_r}$

C_{pd}: power dissipation cap per gate

$$V_L = L\frac{di}{dt} = L\frac{\Delta i}{\Delta t}$$

$$i_c = C\frac{dv}{dt} = C\frac{\Delta v}{\Delta t}$$

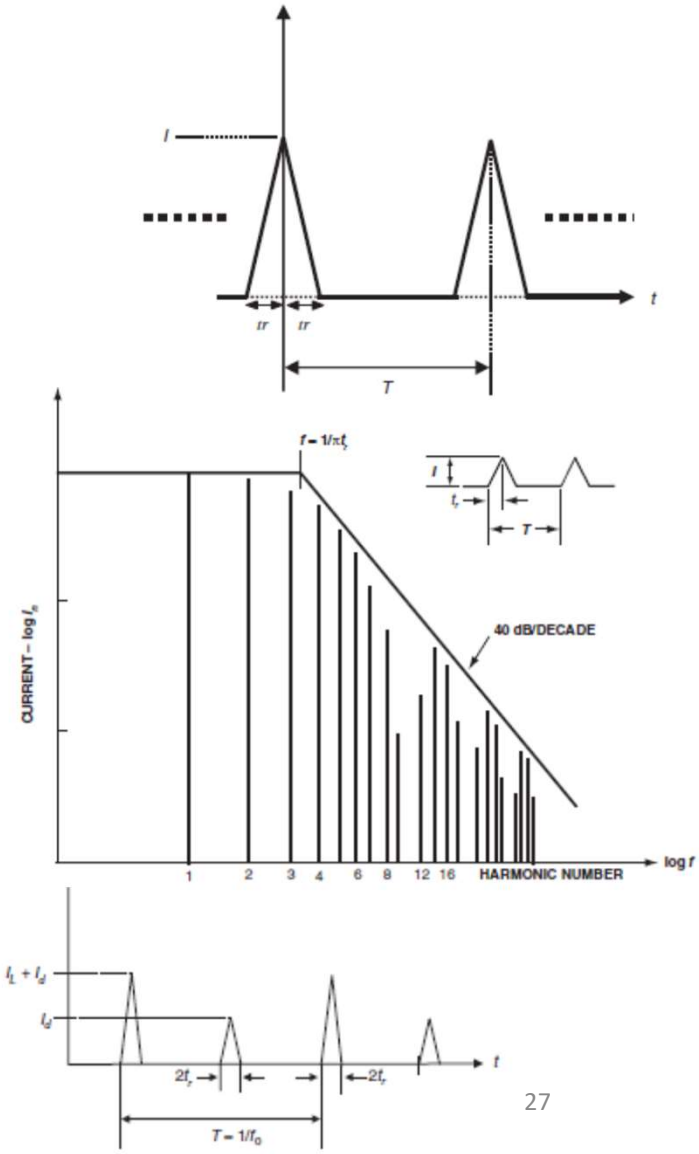




- The waveshape of the transient currents (load or dynamic) can be approximated by a triangular wave as shown.
- The nth harmonic of such a triangular wave is found from,

$$I_n = \frac{2It_r}{T}\left(\frac{\sin\left(\frac{n\pi t_r}{T}\right)}{\frac{n\pi t_r}{T}}\right)^2$$

- The log scale spectrum of such a triangular wave with $t_r/T = 0.1$ is shown in the figure to the right.
- Note that above the frequency $f = 1/(\pi t_r)$ the harmonics fall off with 40dB per decade rate, and both even and odd harmonics exist.
- Note that for a $t_r/T = 0.1$, the fundamental will only contain 20% of the current
- Note that the total transient current is $I_L + I_d$. Load currents occur at the fundamental frequency while the dynamic ones occur at twice the fundamental.

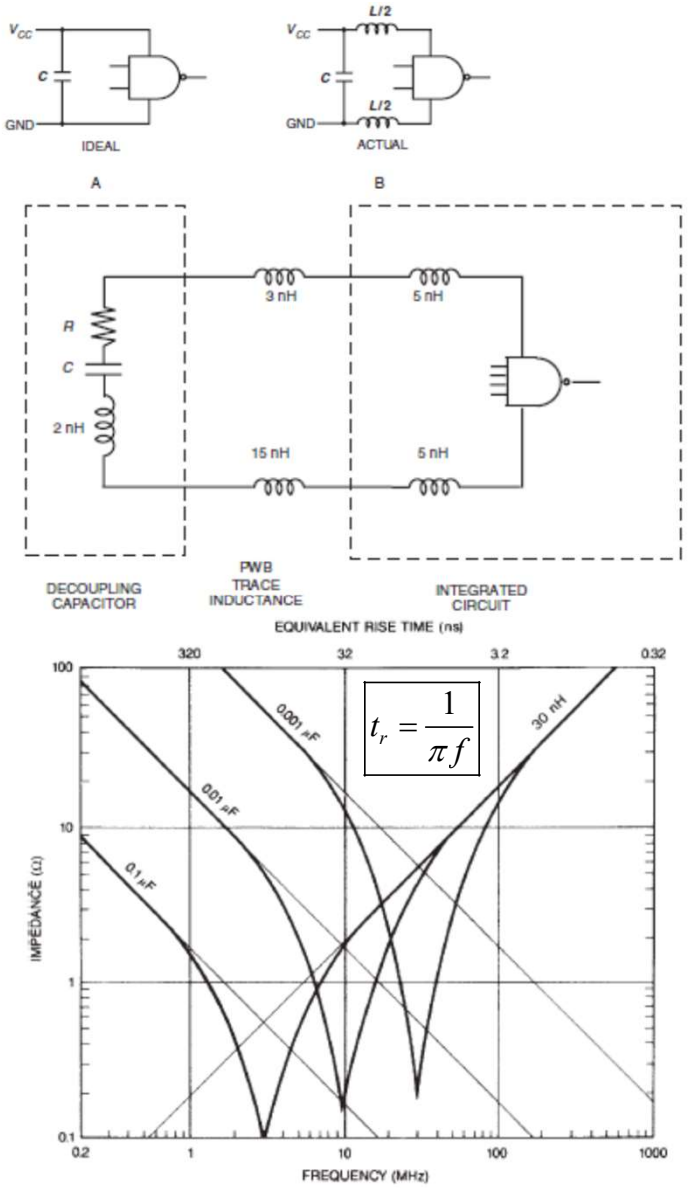


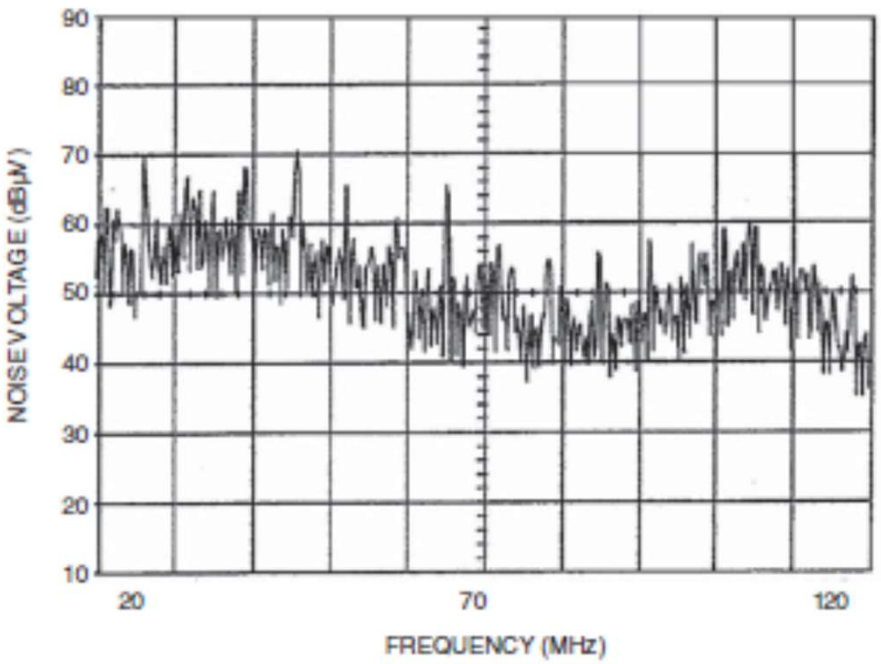
Decoupling Capacitors:

- Ineffective decoupling can lead to excessive power bus noise as well as excessive radiated emissions.
- We should always consider that the decoupling capacitor has its own inductance, in addition to the board inductance and the component (IC) lead inductance.
- As a designer, you have control to some extent of the PCB inductance, others you cannot change.
- The decoupling capacitor will resonate with the total inductance, and thus provide a very low impedance at resonance. Resonance is found using,

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

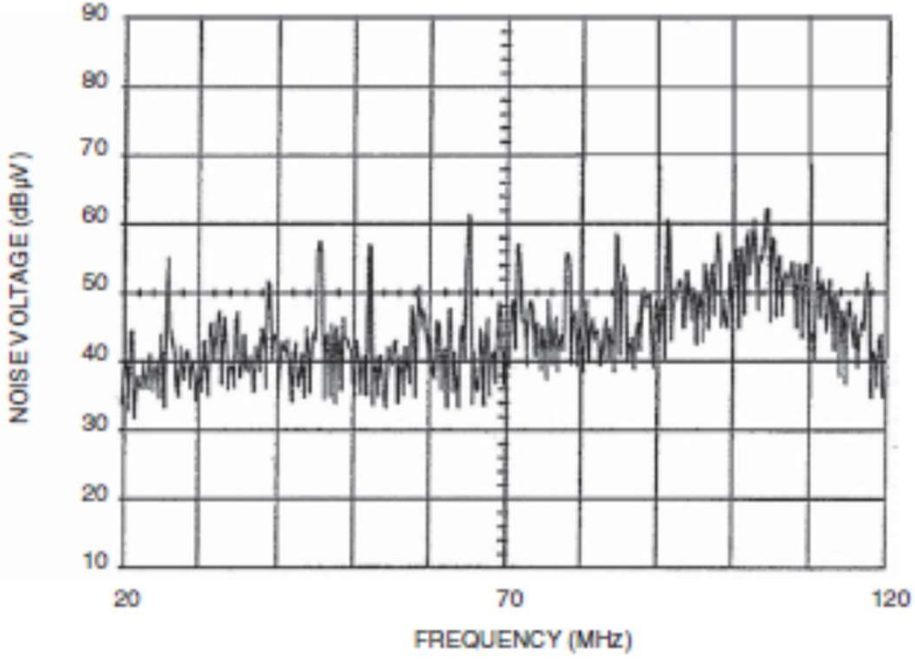
- At resonance, C cancels L, and only the small series resistance stays.
- The figure shows that multiple decoupling capacitors with various values are used to cover higher frequencies and bring down the impedance



- 

WITHOUT DECOUPLING CAPACITORS

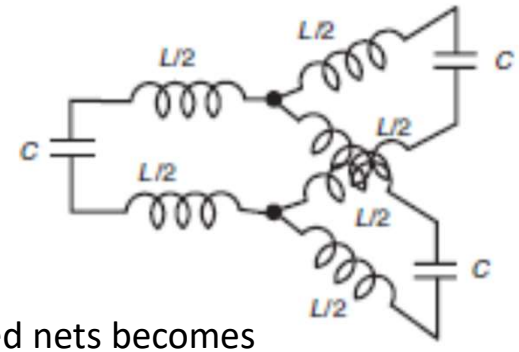
A



WITH DECOUPLING CAPACITORS

B

- Three approaches for multi-cap decoupling:
  (1) Multiple caps of same values
  (2) Multiple caps of two different values
  (3) Multiple caps of many different values



(1) Multiple caps of same value

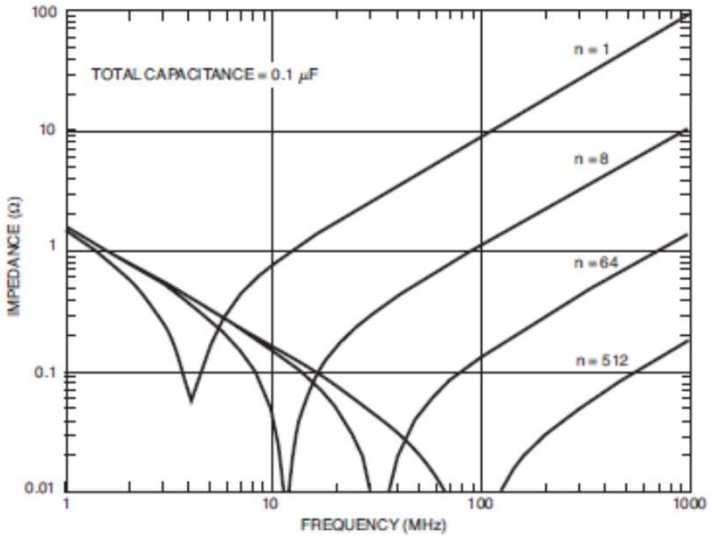
- Connected in parallel, so

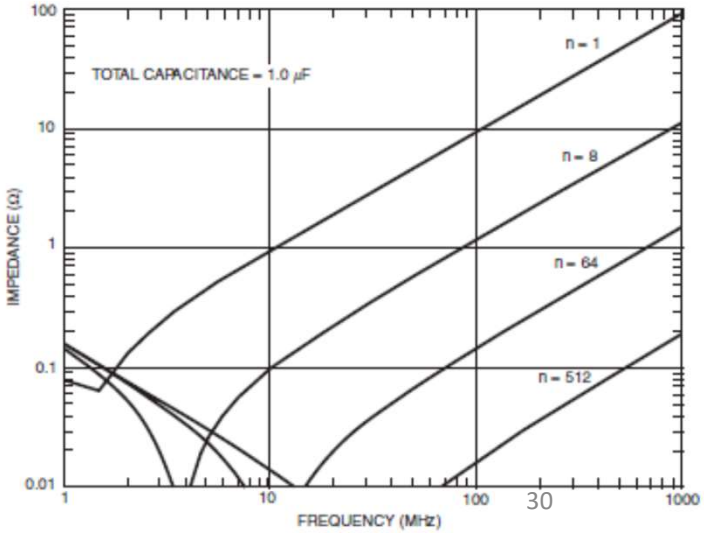
  $C_T = n\ C$

- The inductance value of parallel connected nets becomes

  $L_T = L/n$

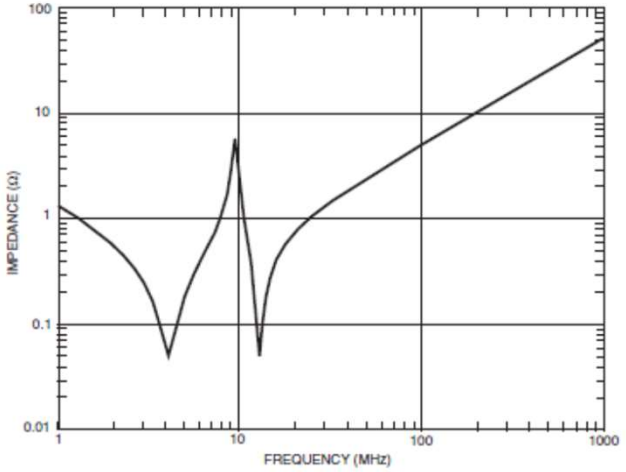
- Note that high frequency impedance is reduced noticeably, but low impedance one is not
- Increasing the value of the overall capacitance can decrease the overall impedance (see the 0.1µF and 1µF graphs to the right).
- This is a **recommended technique** as it can provide low target impedance as we will see soon.





(2) Multiple Caps of two different values

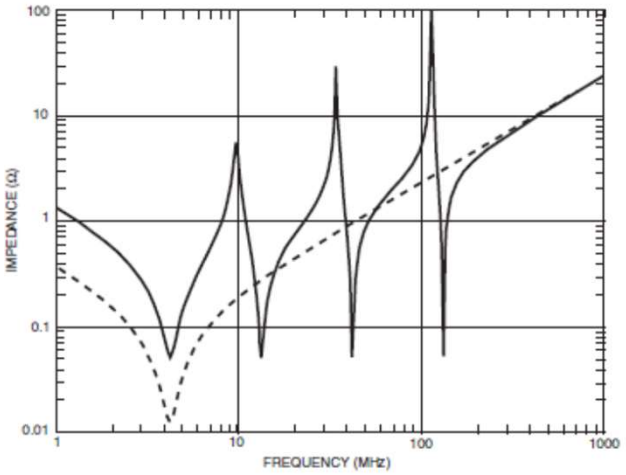
- This was the idea to have a large valued Cap to provide low frequency decoupling while the small valued Cap will provide high frequency decoupling
- This combination will provide two resonances, but an antiresonance in between
- If any of the high speed clock or signal harmonics falls within this antiresonance band, it will degrade performance as noise and low impedance decoupling will be deteriorated.
- This antiresonance will be more profound when the Caps are an order of magnitude apart.



Impedance versus frequency for a decoupling network consisting of a 0.1 and a 0.01-µF capacitor, both in series with 15 nH of inductance.

(3) Multiple Caps of Many different values

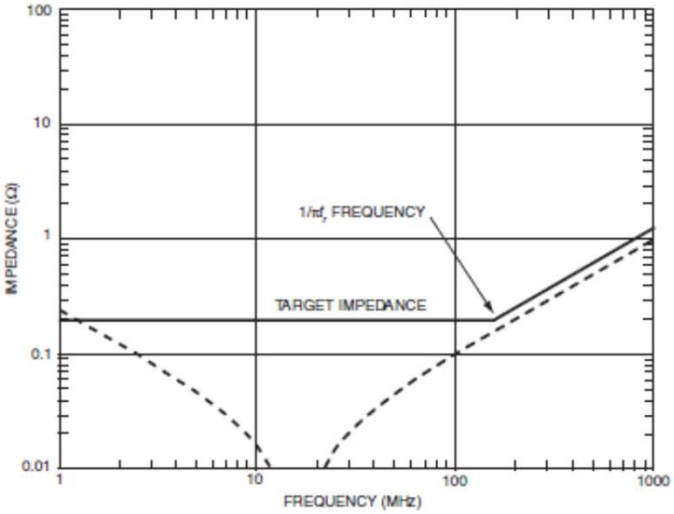
- This is a **recommended technique**.
- Multiple resonances will be obtained and thus multiple impedance dips (low values)
- Additional impedance spikes (antiresonances occur)



Impedance versus frequency for a decoupling network consisting of **a 0.1, a 0.01, and a 0.001 µF plus a 100-pF capacitor (solid line),** and a network that consists of **four 0.1-µF capacitors (dashed line).** For both networks, the capacitors are in series with 15 nH of inductance.

Target Impedance

- The impedance of the decoupling network should be kept under a certain target value within the frequency range of interest, this is the Target impedance.
- Using a Target impedance that is constant across the frequency of operation is very restrictive and usually not necessary.
- Remember that the amplitude of the harmonics of the triangular wave fall off at a rate of 40dB/decade above the $1/(\pi t_r)$ point, thus the target impedance can rise above this frequency point without affecting much the noise voltage
- Assuming that we allow the **Target impedance (Z_t)** to rise at a rate of 20dB/decade above the corner frequency ($1/(\pi t_r)$), then the noise will still be attenuated with the other 20dB/decade. This will relax the design process.
- The minimum # of caps (n) to achieve a certain Target impedance is,
- The inductance in this formula is the total inductance (Cap, traces, IC leads)
- We can ignore the internal inductance internal to the IC.



Target impedance (solid line). Impedance of a decoupling network consisting of 64, 0.01µF capacitors, each in series with 10 nH of inductance (dashed line).

$$n = \frac{2L}{Z_t t_r}$$

- The low-frequency Zt is often found by considering the magnitude of the total transient current and the allowable variation on the supply voltage. k is a correction factor (~2).

$$\boxed{Z_t = k\frac{dV}{dI}}$$

Example:

Consider a large IC, with tr = 2ns, 5V supply and want to keep 5% variation. Assume total transient current of 2.5A. Assume k=2 and each decoupling Cap has 10nH series inductance.

Then, the low frequency $Z_t = k\frac{dV}{dI} = 2\times\frac{0.05*5}{2.5} = 200m\Omega$, will be valid until $\frac{1}{\pi t_r} = \frac{1}{\pi\times 2\times 10^{-9}} = 159MHz$

This target impedance is shown as the straight line in the previous slide figure. Beyond this corner frequency, Z_t can increase at a rate of 20dB/decade (remember, spectrum is decreasing at 40dB/dec)

To meet the Z_t = 200mΩ, we find that we need $n = \frac{2L}{Z_t t_r} = \frac{2\times 10\times 10^{-9}}{0.2\times 2\times 10^{-9}} = 50$

If 2MHz is the lowest frequency of interest, the total decoupling capacitance should be

$$Z_C = \frac{1}{\omega C} \rightarrow C = \frac{1}{Z_t\omega} \rightarrow C = \frac{1}{0.2\times 2\times 10^6} \approx 400nF$$

Thus, each cap out of 50 will have the value of 400nF/50 = 8nF for each Cap.

→ The total capacitance should also satisfy the transient current criteria given by: $\boxed{C \geq \frac{dIdt}{dV}}$

NEXT TIME

- Shielding …