DRV8842-EP DC Motor Driver IC

1 Features

- Single H-Bridge Current-Control Motor Driver
  - Drives One DC Motor, One Coil of a Stepper Motor, or Other Actuators
  - Five-Bit Winding Current Control Allows Up to 32 Current Levels
  - Low MOSFET On-Resistance
- 5-A Maximum Drive Current at 24 V, 25°C
- Built-In 3.3-V Reference Output
- Industry-Standard PWM Control Interface
- 8.2-V to 45-V Operating Supply Voltage Range
- Thermally Enhanced Surface Mount Package
- Supports Defense, Aerospace, and Medical Applications
  - Controlled Baseline
  - One Assembly and Test Site
  - One Fabrication Site
  - Available in Military (–55°C to 125°C) Temperature Range
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability

2 Applications

- Printers
- Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics

3 Description

The DRV8842-EP provides an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device has one H-bridge driver, and is intended to drive one DC motor, one coil of a stepper motor, or other loads. The output driver block consists of N-channel power MOSFETs configured as an H-bridge. The DRV8842-EP can supply up to 5-A peak or 3.5-A RMS output current (with proper heatsinking at 24 V and 25°C).

Separate inputs to independently control each half of the H-bridge are provided.

Internal shutdown functions are provided for overcurrent protection, short circuit protection, undervoltage lockout, and over-temperature.

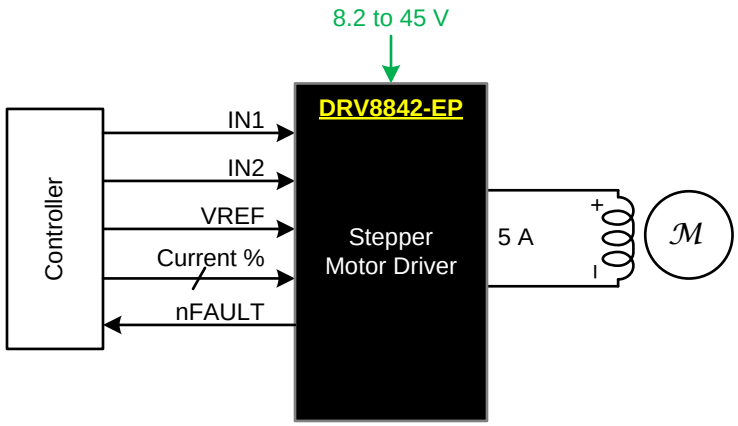
The DRV8842-EP is available in a 28-pin HTSSOP package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

Device Information[1]

ORDER NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8842MPWPREP	HTSSOP (28)	9.70 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



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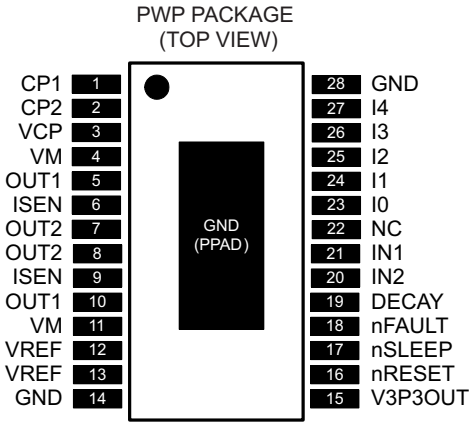
5 Revision History

DATE	VERSION	NOTES
July 2014	*	Initial Release

6 Pin Configuration and Functions



Pin Functions

PIN		I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
GND	14	—	Device ground	
	28			
VM	4	—	Bridge A power supply	Connect to motor supply (8.2 to 45 V). Both pins must be connected to same supply.
	11			
V3P3OUT	15	O	3.3-V regulator output	Bypass to GND with a 0.47-µF, 6.3-V ceramic capacitor. Can be used to supply VREF.
CP1	1	IO	Charge pump flying capacitor	Connect a 0.01-µF 50-V capacitor between CP1 and CP2.
CP2	2	IO	Charge pump flying capacitor	
VCP	3	IO	High-side gate drive voltage	Connect a 0.1-µF 16-V ceramic capacitor and a 1-MΩ resistor to VM.
CONTROL				
IN1	21	I	Input 1	Logic input controls state of OUT1. Internal pulldown.
IN2	20	I	Input 2	Logic input controls state of OUT2. Internal pulldown.
I0	23	I	Current set inputs	Sets winding current as a percentage of full-scale. Internal pulldown.
I1	24	I		
I2	25	I		
I3	26	I		
I4	27	I		
DECAY	19	I	Decay mode	Low = slow decay, open = mixed decay, High = fast decay. Internal pulldown and pullup.
nRESET	16	I	Reset input	Active-low reset input initializes the logic and disables the H-bridge outputs. Internal pulldown.
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown.
VREF	12	I	Current set reference input	Reference voltage for winding current set. Both pins must be connected together on the PCB.
	13			
STATUS				
nFAULT	18	OD	Fault	Logic low when in fault condition (over-temperature, overcurrent)
OUTPUT				
ISEN	6	IO	Bridge ground / Isense	Connect to current sense resistor. Both pins must be connected together on the PCB.
	9			

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
OUT1	5	O	Bridge output 1	Connect to motor winding. Both pins must be connected together on the PCB.
	10			
OUT2	7	O	Bridge output 2	Connect to motor winding. Both pins must be connected together on the PCB.
	8			

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1] [2]

		MIN	MAX	UNIT
$V_{(VM)}$	Power supply voltage	–0.3	47	V
	Digital pin voltage	–0.5	7	V
$V_{(VREF)}$	Input voltage	–0.3	4	V
	ISEN pins	–0.3	0.8	V
	Peak motor drive output current, t < 1 µs		Internally limited	A
	Continuous motor drive output current[3]		5	A
	Continuous total power dissipation		See *Thermal Information*	
T_J	Operating virtual junction temperature range	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–60	150	°C
$V_{(ESD)}$ [1]	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[2]	–500	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[3]	–250	1500	

(1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by assembly line electrostatic discharges into the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. *Pins listed as 1 kV may actually have higher performance.*
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. *Pins listed as 250 V may actually have higher performance.*

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range[1]	8.2		45	V
$V_{(VREF)}$	VREF input voltage[2]	1		3.5	V
I_{V3P3}	V3P3OUT load current	0		1	mA
f_{PWM}	Externally applied PWM frequency	0		100	kHz
T_J	Operating virtual junction temperature range	–55		125	°C

(1) All V_M pins must be connected to the same supply voltage.
(2) Operational at $V_{(VREF)}$ between 0 and 1 V, but accuracy is degraded.

7.4 Thermal Information

THERMAL METRIC[1]		DRV8842-EP PWP 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	35.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[3]	15.6	
$R_{\theta JB}$	Junction-to-board thermal resistance[4]	13.5	
ψ_{JT}	Junction-to-top characterization parameter[5]	0.4	
ψ_{JB}	Junction-to-board characterization parameter[6]	13.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance[7]	1.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

7.5 Electrical Characteristics

over recommended operating junction temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V, f_{PWM} < 50 kHz		5	8	mA
I_{VMQ}	VM sleep mode supply current	V_M = 24 V		10	20	µA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising		7.8	8.4	V
V3P3OUT REGULATOR						
V_{3P3}	V3P3OUT voltage	IOUT = 0 to 1 mA	3.1	3.3	3.5	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2.2		5.25	V
V_{HYS}	Input hysteresis		0.3	0.45	0.65	V
I_{IL}	Input low current	VIN = 0	–20		20	µA
I_{IH}	Input high current	VIN = 3.3 V		33	100	µA
R_{PD}	Internal pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
DECAY INPUT						
V_{IL}	Input low threshold voltage	For slow decay (brake) mode	0		0.8	V
V_{IH}	Input high threshold voltage	For fast decay (coast) mode	2			V
I_{IN}	Input current				±40	µA
R_{PU}	Internal pullup resistance (to 3.3 V)			130		kΩ
R_{PD}	Internal pulldown resistance			80		kΩ
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_M = 24 V, I_O = 1 A		0.13	0.17	Ω
$R_{DS(ON)}$	LS FET on resistance	V_M = 24 V, I_O = 1 A		0.13	0.17	Ω
I_{OFF}	Off-state leakage current		–79		96	µA
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		5			A
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
CURRENT CONTROL						
I_{REF}	VREF input current	$V_{(VREF)}$ = 3.3 V	–3		3	µA
V_{TRIP}	ISENSE trip voltage	$V_{(VREF)}$ = 3.3 V, 100% current setting	635	660	685	mV
ΔI_{TRIP}	Current trip accuracy (relative to programmed value)	$V_{(VREF)}$ = 3.3 V, 5% current setting	–25%		25%	
		$V_{(VREF)}$ = 3.3 V, 10% to 34% current setting	–15%		15%	
		$V_{(VREF)}$ = 3.3 V, 38% to 67% current setting	–10%		10%	
		$V_{(VREF)}$ = 3.3 V, 71% to 100% current setting	–5%		5%	
A_{ISENSE}	Current sense amplifier gain	Reference only		5		V/V

7.6 Motor Driver Timing Requirements

		MIN	TYP	MAX	UNIT
f_{PWM}	Internal current control PWM frequency		50		kHz
t_{BLANK}	Current sense blanking time		3.75		µs
t_R	Rise time	30		220	ns
t_F	Fall time	30		220	ns

7.7 Typical Characteristics

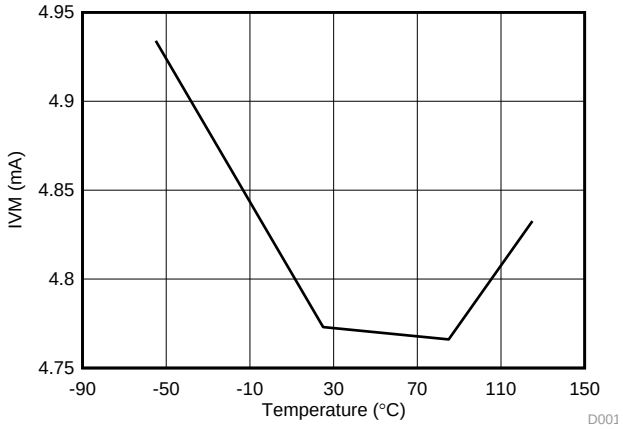


Figure 1. IVM vs Temperature

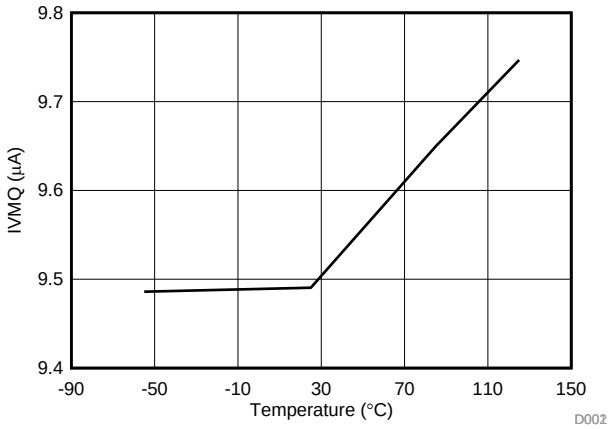


Figure 2. IVMQ vs Temperature

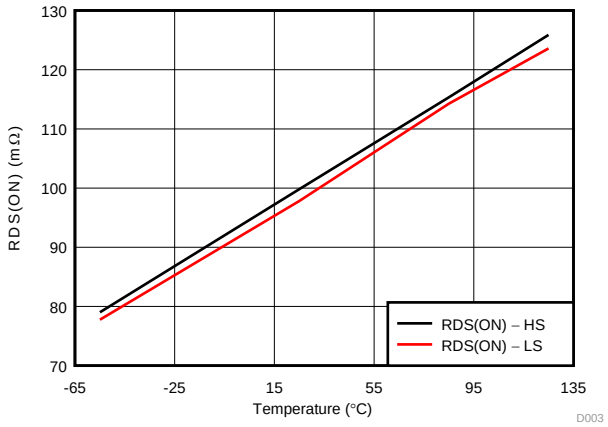


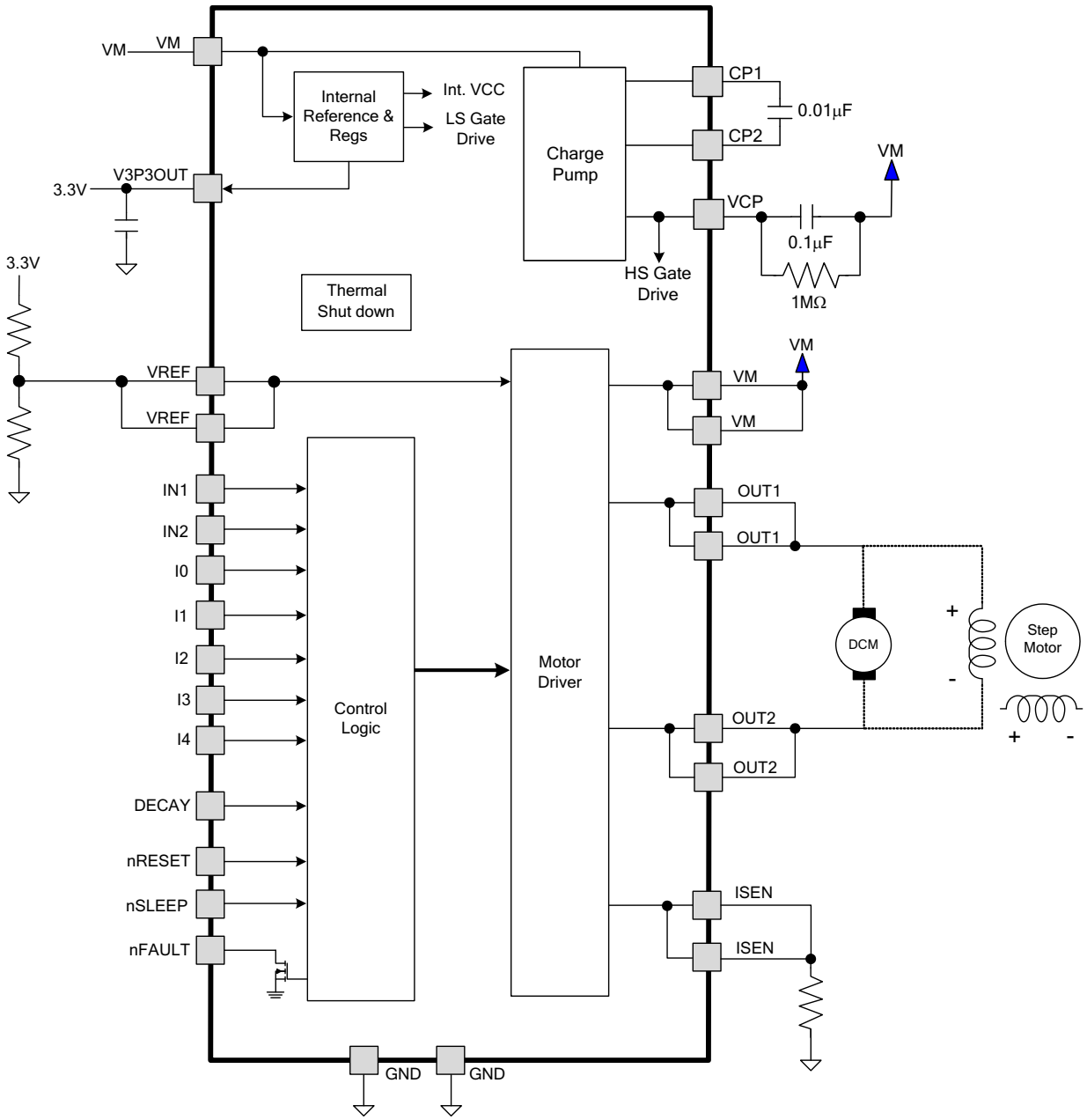
Figure 3. $R_{DS(ON)}$ vs Temperature

8 Detailed Description

8.1 Overview

The DRV8842-EP provides an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device has one H-bridge driver, and is intended to drive one DC motor, one coil of a stepper motor, or other loads. The output driver block consists of N-channel power MOSFETs configured as an H-bridge. The DRV8842-EP can supply up to 5-A peak or 3.5-A RMS output current (with proper heatsinking at 24 V and 25°C).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 PWM Motor Drivers

The DRV8842-EP contains one H-bridge motor driver with current-control PWM circuitry. Figure 4 shows a block diagram of the motor control circuitry.

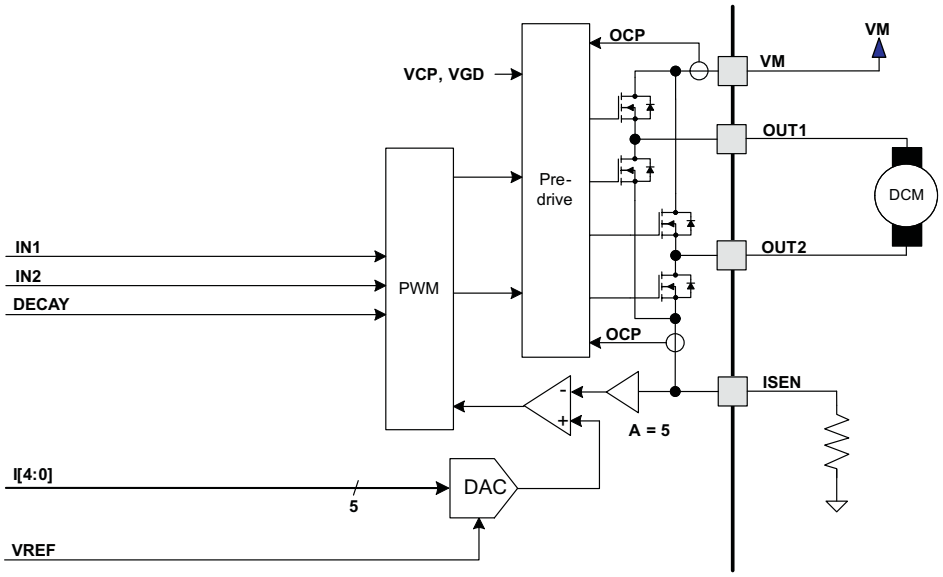


Figure 4. Motor Control Circuitry

Note that there are multiple VM, ISEN, OUT, and VREF pins. All like-named pins must be connected together on the PCB.

8.3.2 Bridge Control

The IN1 and IN2 input pins directly control the state of the OUT1 and OUT2 outputs. Either input can also be used for PWM control of the load. Table 1 shows the logic.

Table 1. H-Bridge Logic

IN1	IN2	OUT1	OUT2
0	0	L	L
0	1	L	H
1	0	H	L
1	1	H	H

The control inputs have internal pulldown resistors of approximately 100 kΩ.

8.3.3 Current Regulation

The maximum current through the load is regulated by a fixed-frequency PWM current regulation, or current chopping. When the H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. After the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

For DC motors, current regulation is used to limit the start-up and stall current of the motor. Speed control is typically performed by providing an external PWM signal to the IN1 or IN2 input pins.

If the current regulation feature is not needed, it can be disabled by connecting the ISEN pins directly to ground and the VREF pins to V3P3.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the ISEN pins, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the VREF pins, and is scaled by a 5-bit DAC that allows current settings of 0% to 100% in an approximately sinusoidal sequence.

The full-scale (100%) chopping current is calculated in Equation 1.

$$I_{CHOP} = \frac{V_{(VREF)}}{5 \times R_{ISENSE}} \quad (1)$$

Example:

If using a 0.25-Ω sense resistor and the VREF pins are 2.5 V, the full-scale (100%) chopping current is 2.5 V / (5 × 0.25 Ω) = 2 A.

Five input pins (I0 through I4) are used to scale the current in the bridge as a percentage of the full-scale current set by the VREF input pin and sense resistance. The I0 through I4 pins have internal pulldown resistors of approximately 100 kΩ. The function of the pins is shown in Table 2.

Table 2. Pin Functions

I[4..0]	RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)
0x00h	0%
0x01h	5%
0x02h	10%
0x03h	15%
0x04h	20%
0x05h	24%
0x06h	29%
0x07h	34%
0x08h	38%
0x09h	43%
0x0Ah	47%
0x0Bh	51%
0x0Ch	56%
0x0Dh	60%
0x0Eh	63%
0x0Fh	67%
0x10h	71%
0x11h	74%
0x12h	77%
0x13h	80%
0x14h	83%
0x15h	86%
0x16h	88%
0x17h	90%
0x18h	92%
0x19h	94%
0x1Ah	96%
0x1Bh	97%
0x1Ch	98%
0x1Dh	99%
0x1Eh	100%
0x1Fh	100%

8.3.4 Blanking Time

After the current is enabled in an H-bridge, the voltage on the ISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 µs. Note that the blanking time also sets the minimum on-time of the PWM.

8.3.5 nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge driver. All inputs are ignored while nRESET is active.

Driving nSLEEP low puts the device into a low-power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state, all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational. Note that nRESET and nSLEEP have internal pulldown resistors of approximately 100 kΩ. These signals need to be driven to logic high for device operation.

8.3.6 Protection Circuits

The DRV8842-EP is fully protected against undervoltage, overcurrent, and overtemperature events.

8.3.6.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The device remains disabled until either nRESET pin is applied, or VM is removed and reapplied.

Overcurrent conditions on both high-side and low-side devices (that is, a short to ground, supply, or across the motor winding) all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the I_{SENSE} resistor value or VREF voltage.

8.3.6.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. After the die temperature has fallen to a safe level, operation automatically resumes.

8.3.6.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the UVLO threshold voltage, all circuitry in the device is disabled and internal logic is reset. Operation resumes when V_M rises above the UVLO threshold.

8.3.7 Thermal Protection

The DRV8842-EP has TSD as described in *Thermal Shutdown (TSD)*. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

8.3.8 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, *PowerPAD™ Thermally Enhanced Package* and TI application brief SLMA004, *PowerPAD™ Made Easy*, available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

8.4 Device Functional Modes

8.4.1 Decay Mode

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until it reaches the PWM current chopping threshold (see Figure 5, case 1). The current flow direction shown indicates the state when the IN1 pin is high and the IN2 pin is low.

After the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, after the PWM chopping current level is reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches 0, the bridge is disabled to prevent any reverse current flow. Figure 5 case 2 shows fast decay mode.

In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge (see Figure 5, case 3).

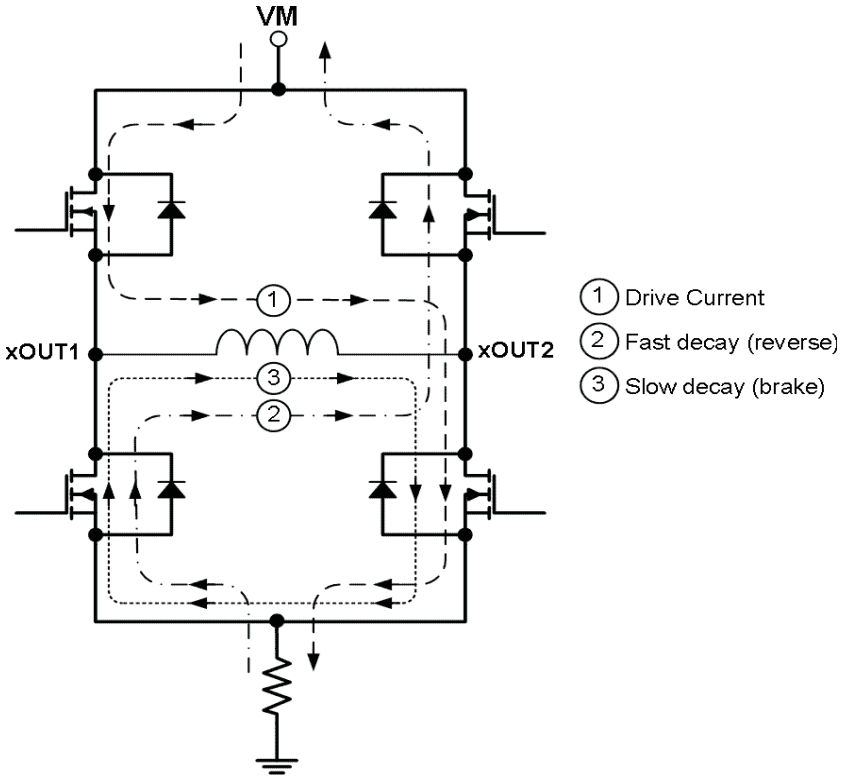


Figure 5. Decay Mode

The DRV8842-EP supports fast decay, slow decay, and a mixed decay mode. Slow, fast, or mixed decay mode is selected by the state of the DECAY pin. Logic low selects slow decay. Open selects mixed decay operation. And, logic high sets fast decay mode. The DECAY pin has both an internal pullup resistor of approximately 130 kΩ and an internal pulldown resistor of approximately 80 kΩ. This sets the mixed decay mode if the pin is left open or undriven.

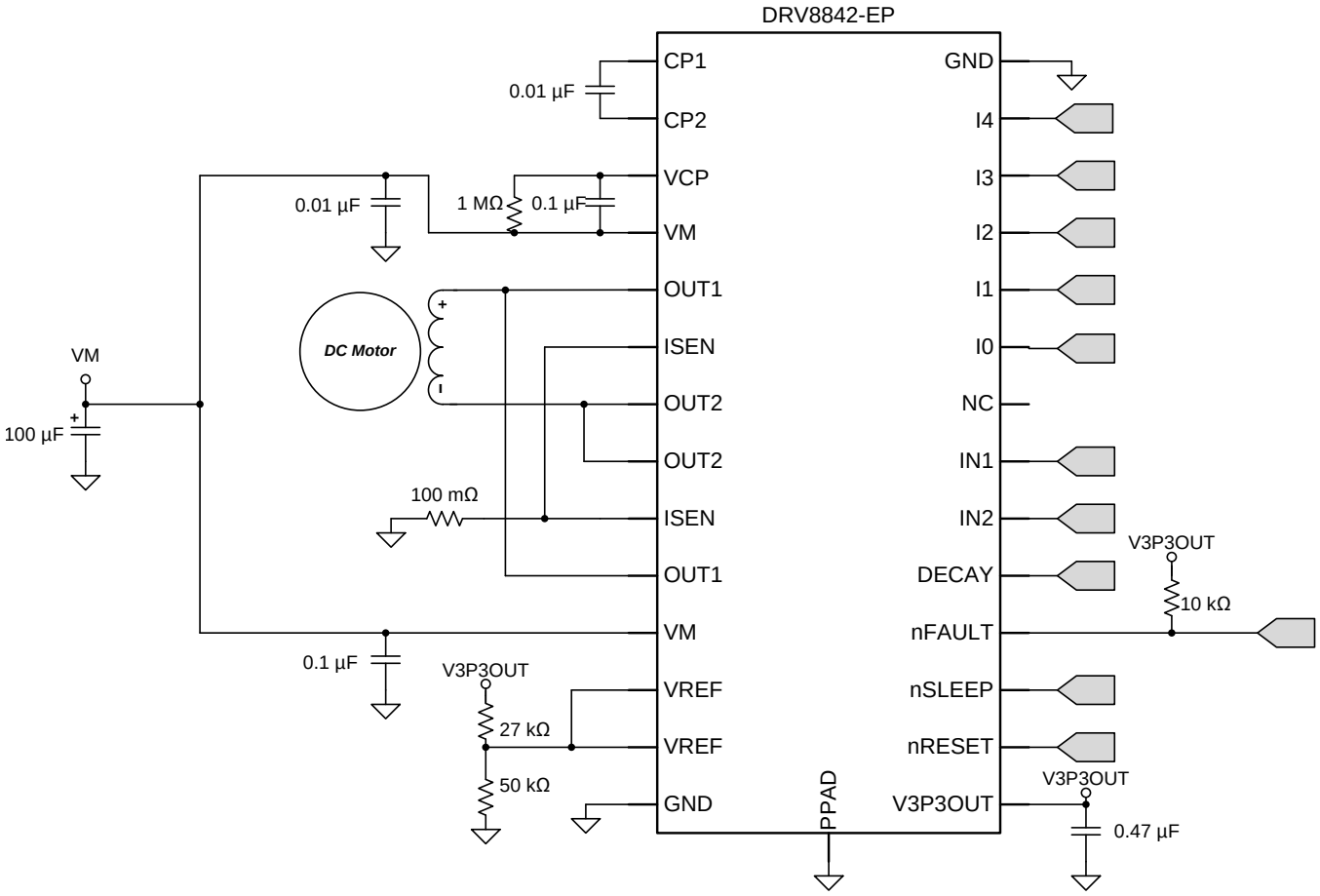
Mixed decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period.

9 Application and Implementation

9.1 Application Information

The DRV8842-EP is used in DC motor control. This integrated driver drives up to a 5-A peak with precise winding current control. The motor is controlled through a PWM interface and device faults are reported through the nFAULT pin. The following design is a common application of the DRV8842-EP.

9.2 Typical Application



9.2.1 Design Requirements

Design Parameters	Reference	Example Value
Supply voltage	VM	24 V
Motor winding resistance	R_L	13.23 Ω
Motor winding inductance	I_L	4.03 mH
Motor type	BDC	Brushed DC motor
Sense resistor	R_{SENSE}	100 mΩ
Full-scale current	I_{FS}	3.5 A

9.2.2 Detailed Design Procedure

9.2.2.1 Power Dissipation

Average power dissipation in the DRV8842-EP when running a DC motor can be roughly estimated by Equation 2.

$$P = 2 \times R_{DS(ON)} \times \left(I_{OUT}\right)^2 \quad (2)$$

where

- P is the power dissipation of one H-bridge
- $R_{DS(ON)}$ is the resistance of each FET
- I_{OUT} is the RMS output current being applied to each winding

I_{OUT} is equal to the average current drawn by the DC motor. Note that at start-up and fault conditions, this current is much higher than normal running current; also consider the peak currents and their duration. The factor of 2 is due to two FETs conducting winding current (one high side and one low side) at any instant.

The maximum amount of power that can be dissipated in the device depends on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when sizing the heatsink.

9.2.2.2 Current Regulation Considerations

For the DRV8842-EP, the set full-scale current (I_{FS}) is the maximum current that can be driven. This quantity depends on the VREF analog voltage and the sense resistor value (R_{SENSE}). The gain of DRV8842-EP is set for 5 V/V. This value can be adjusted from 0% to 100% through the use of the relative current bits I[4:0].

$$I_{FS}\ (A) = \frac{V_{(VREF)}\ (V)}{A_V \times R_{SENSE}\ (\Omega)} = \frac{V_{(VREF)}\ (V)}{5 \times R_{SENSE}\ (\Omega)} \quad (3)$$

To achieve I_{FS} = 3.5 A with R_{SENSE} of 0.1 Ω, $V_{(VREF)}$ should be 1.75 V, and I[4:0] should be 0x1F.

9.2.2.3 Slow, Fast, and Mixed Decay Modes

The DRV8842-EP supports three different decay modes: slow decay, fast decay, and mixed decay. The current through the motor winding is regulated using a fixed-frequency PWM scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8842-EP places the winding in one of the three decay modes until the PWM cycle has expired. After, a new drive phase starts.

The blanking time, T_{BLANK}, defines the minimum drive time for the current chopping. I_{TRIP} is ignored during T_{BLANK}, so the winding current may overshoot the trip level.

9.2.3 Application Curves

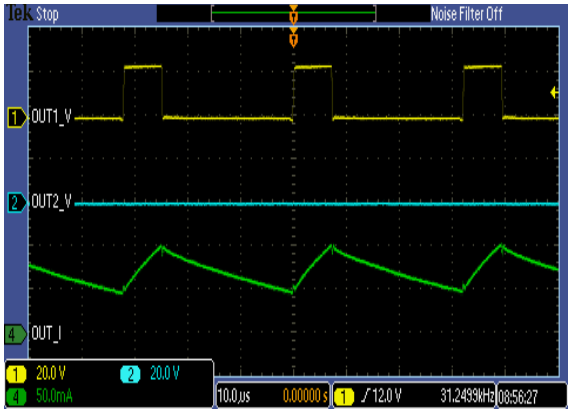


Figure 6. 25% Duty Cycle, Forward Direction

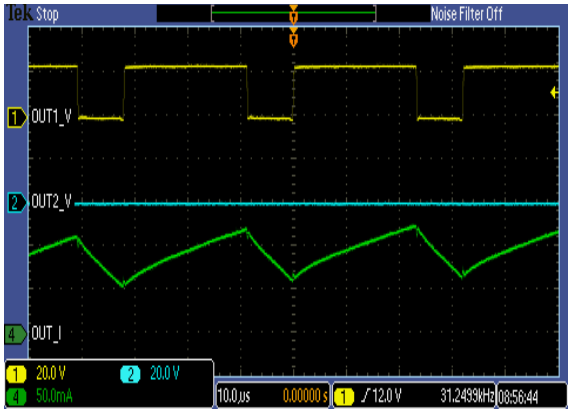


Figure 7. 75% Duty Cycle, Forward Direction

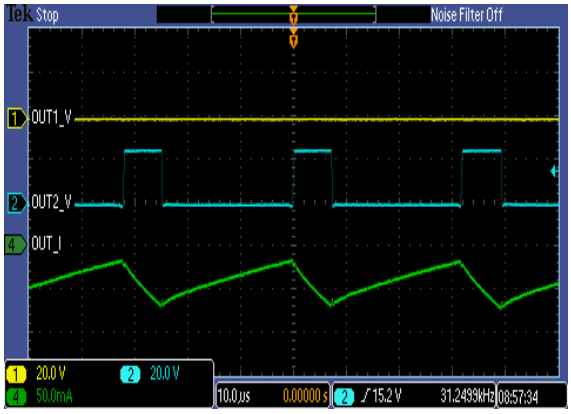


Figure 8. 25% Duty Cycle, Reverse Direction

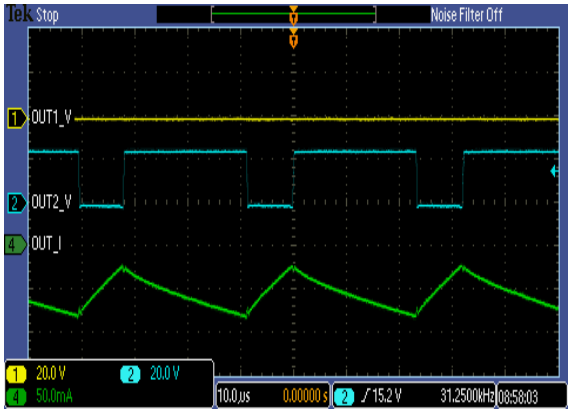


Figure 9. 75% Duty Cycle, Reverse Direction

10 Power Supply Recommendations

The DRV8842-EP is designed to operate from an input voltage supply (VM) range between 8.2 and 45 V. Two 0.1-µF ceramic capacitors rated for VM must be placed as close as possible to the VM pins respectively (one on each pin). In addition to the local decoupling caps, additional bulk capacitance is required and must be sized according to the application requirements.

10.1 Bulk Capacitance

Bulk capacitance sizing is an important factor in motor drive system design. It depends on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. The designer should size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

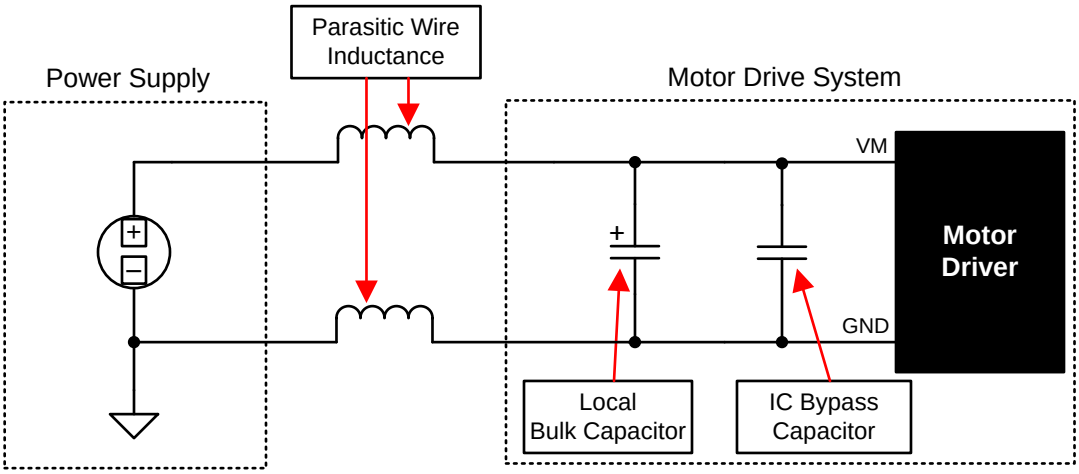


Figure 10. Setup of Motor Drive System With External Power Supply

10.2 Power Supply and Logic Sequencing

There is no specific sequence for powering-up the DRV8842-EP. It is okay for digital input signals to be present before VM is applied. After VM is applied to the DRV8842-EP, the device begins operation based on the status of the control pins.

11 Layout

11.1 Layout Guidelines

The VM pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1-µF rated for VM. This capacitor should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

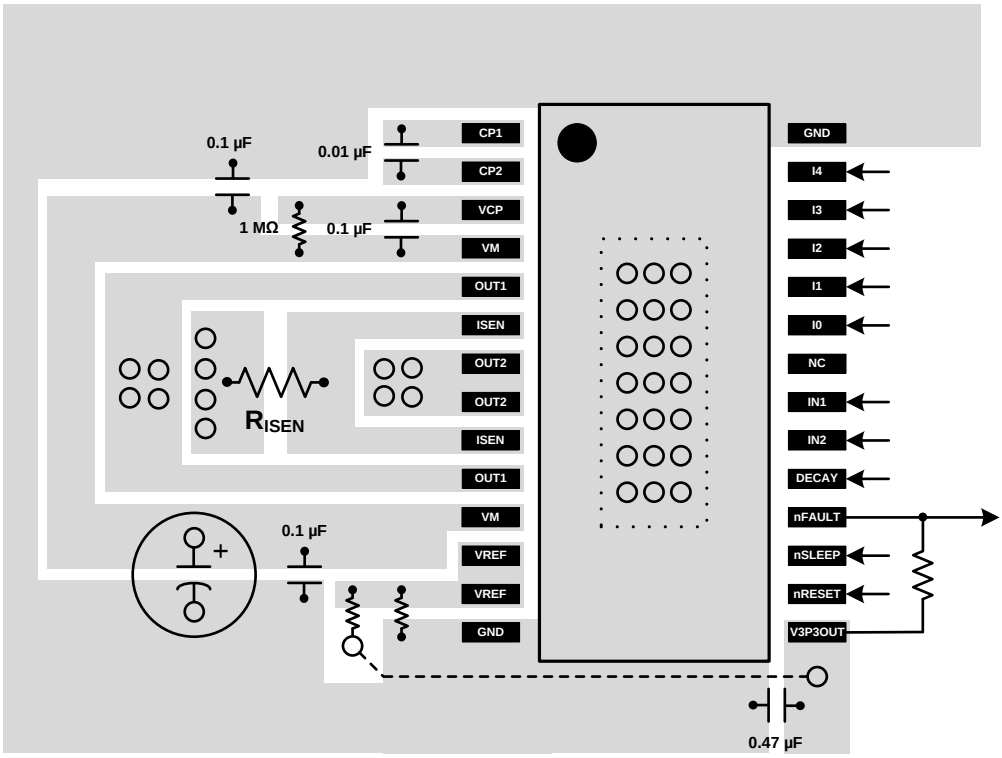
The VM pins must be bypassed to ground using an appropriate bulk capacitor. This component may be an electrolytic and should be located close to the DRV8842-EP.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. TI recommends a value of 0.01-µF rated for VM. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 0.1-µF rated for 16 V. Place this component as close to the pins as possible. Also, place a 1-MΩ resistor between VCP and VM.

Bypass V3P3 to ground with a ceramic capacitor rated 6.3 V. Place this bypass capacitor as close to the pin as possible.

11.2 Layout Example



12 Device and Documentation Support

12.1 Trademarks

PowerPAD is a trademark of Texas Instruments.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8842MPWPREP	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	DRV8842EP	Samples
V62/14615-01XE	ACTIVE	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	DRV8842EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DRV8842-EP :

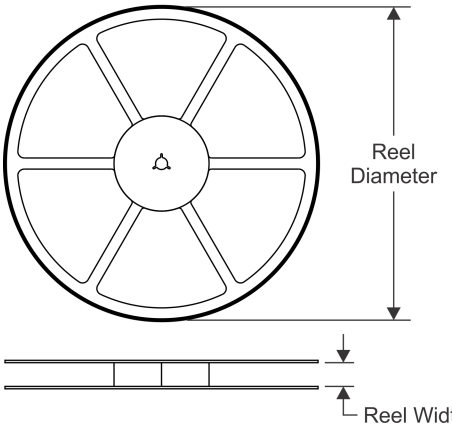
- Catalog: DRV8842

NOTE: Qualified Version Definitions:

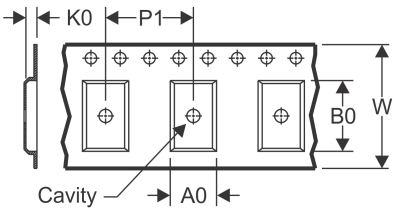
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

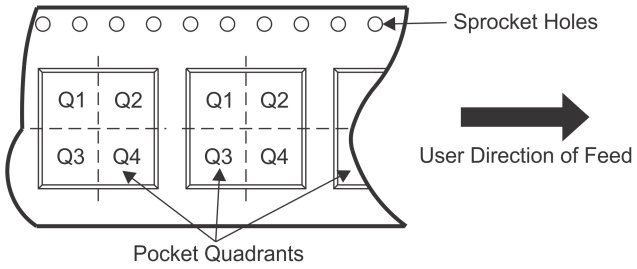


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

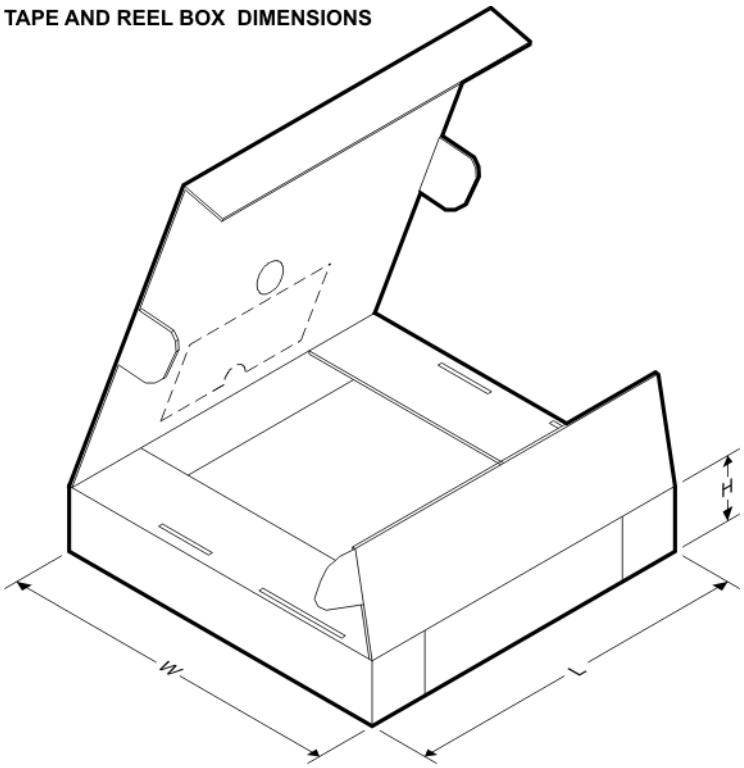
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8842MPWPREP	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8842MPWPREP	HTSSOP	PWP	28	2000	350.0	350.0	43.0

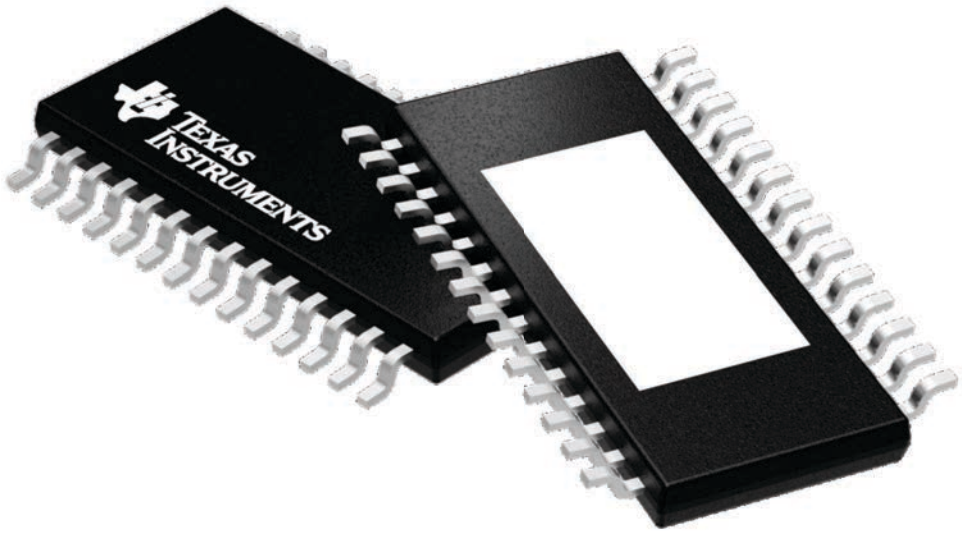
GENERIC PACKAGE VIEW

PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

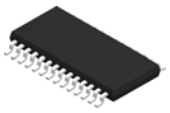


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224765/A

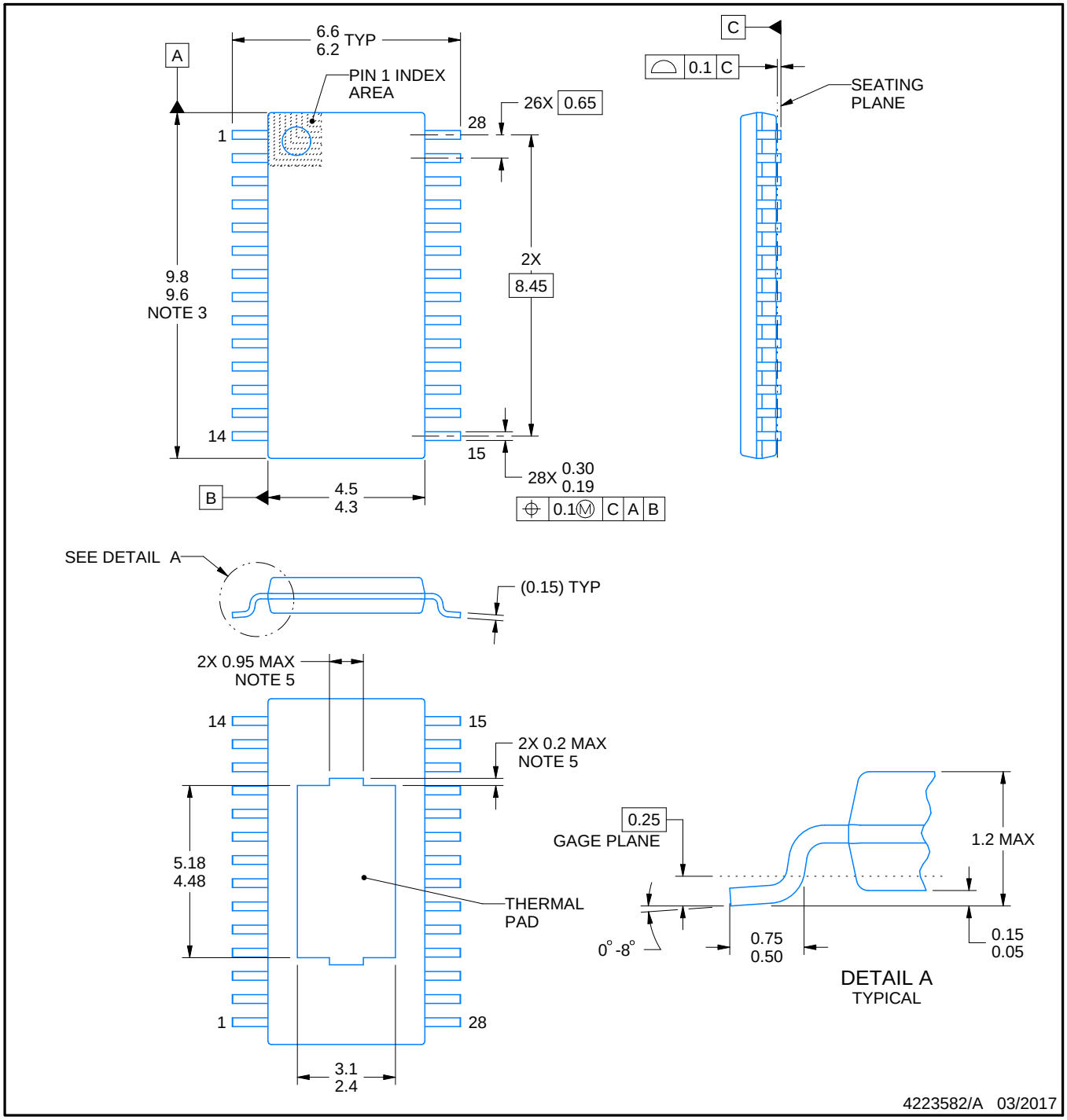
PACKAGE OUTLINE

PWP0028C



PowerPAD™ TSSOP - 1.2 mm max height

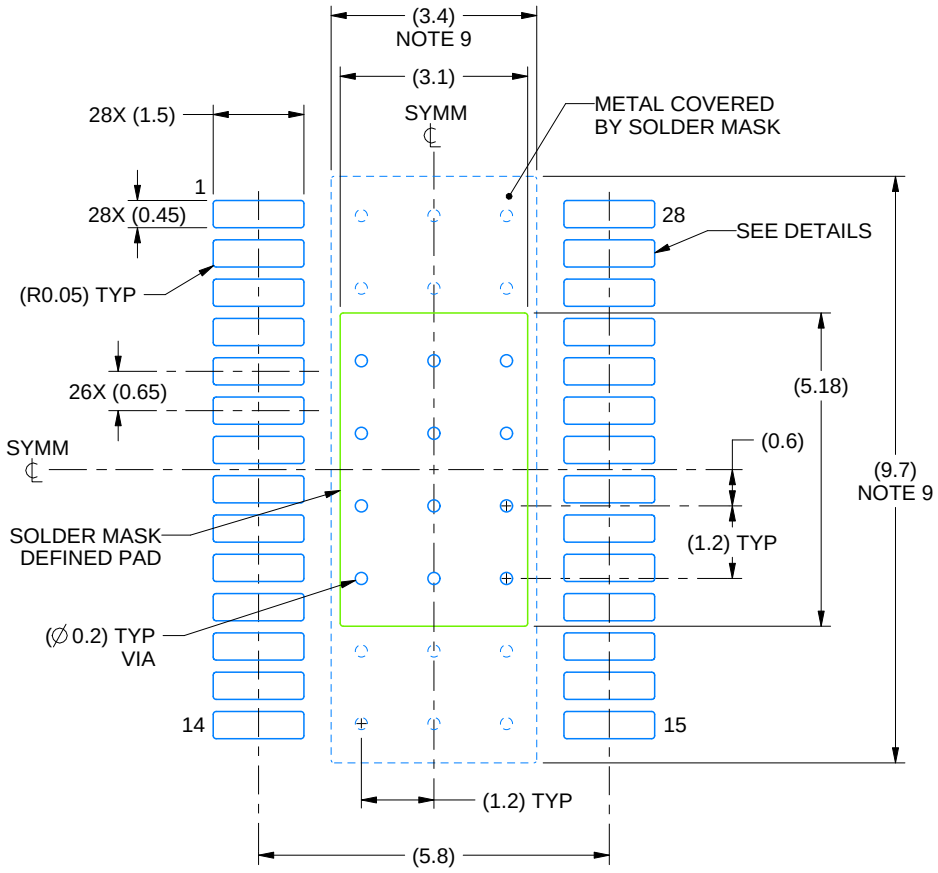
SMALL OUTLINE PACKAGE



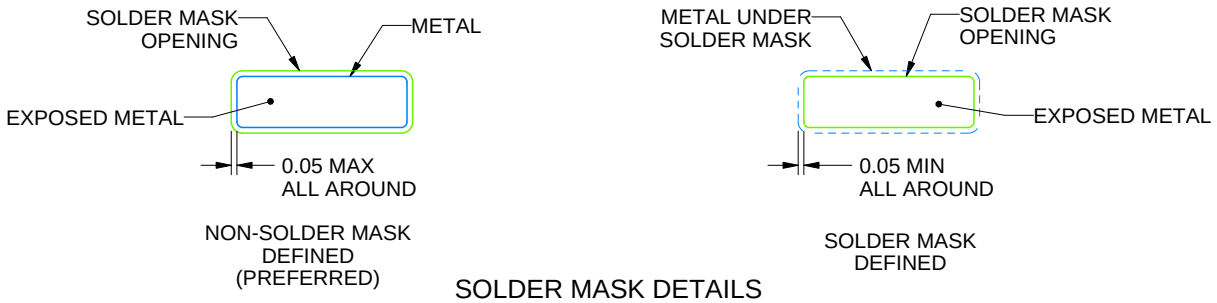
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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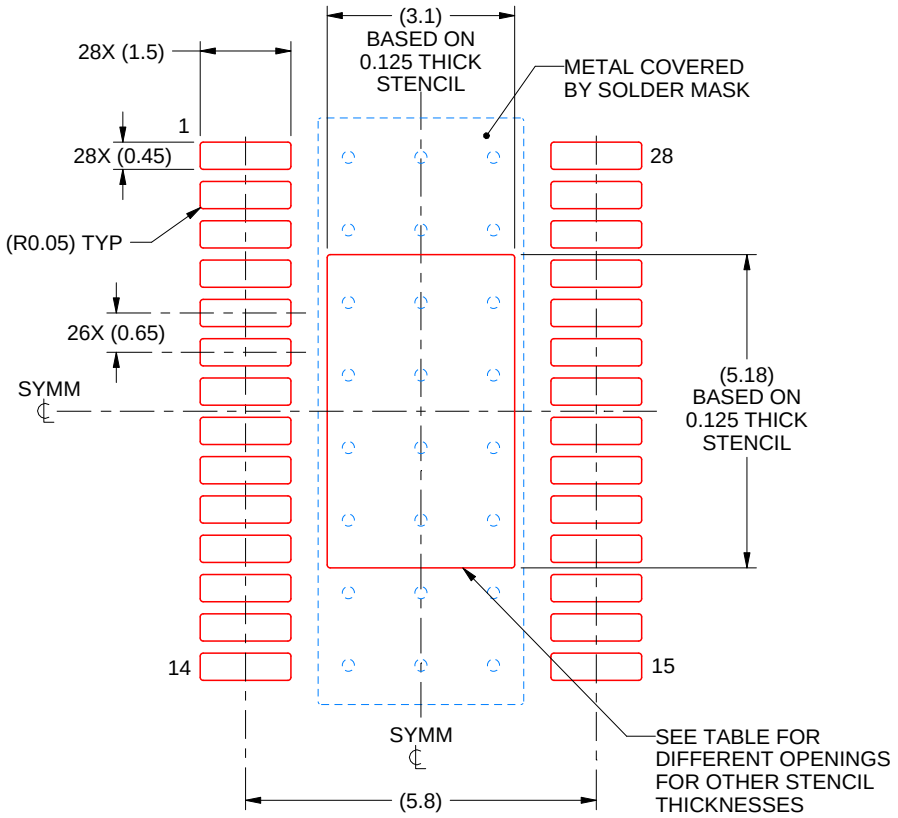
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 5.79
0.125	3.10 X 5.18 (SHOWN)
0.15	2.83 X 4.73
0.175	2.62 X 4.38

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265