

Chapter 2

A Review of Hardware Platforms for Whitespace Communication

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Abstract Designing a hardware platform for white space Technology is a complex task. The IEEE 802.22 standard for white space communications imposes tight specifications that require powerful CPUs and FPGAs as well as compliance with strict RF regulations. In addition, a commercial product needs to be produced at a low cost. In this chapter, we examine the specifications that directly impact the design of white space communications hardware. We then explore the various hardware platforms that are commercially available and identify their strengths and weaknesses. The hardware platforms that will be discussed here are the USRP N210, the Nuand BladeRF, Zepeto SDR and the HackRF board. These platforms are costly considering the component cost of the hardware supplied and have been designed with different goals and hence don't meet the full white space communication requirements. However, these boards can be used as a yardstick for the design of a white space hardware and useful inferences can be drawn by observing their merits and de-merits.

The IEEE 802.22 specification for TV white space communications imposes tight specifications [1]. The 802.22 standard is based on OFDMA modulation for downstream and upstream links with the ability to channel bond adjacent TV channels should more bandwidth be required. The standard supports modulation schemes up to 64QAM, producing a data rate of 19 Mbps per 6MHz TV channel. The standard also makes use of a geo-location spectrum database or an Eigen Value method of Spectrum Sensing to detect other primary users.

These specifications require a platform with a powerful CPU and FPGA as well as compliance with strict RF power and spectral mask regulations. At the same time, a commercial product has to be low-cost. In this Chapter, we first examine the specifications that directly impact the design of white space communication hardware. We then explore the various hardware platforms that are commercially

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Table 2.1 Frequencies of operation: each of these channels have a bandwidth of 6 MHz

Device type	Frequency bands (MHz)
All TVBDs	512–608
	614–698
Only for communication between fixed TVBDs	54–60
	76–88
	174–216
	470–512

In total, there are 47 available channels of operation

available and identify their strengths and weaknesses. The hardware platforms that will be discussed here are the USRP N210, the Nuand BladeRF, Zepto SDR and the HackRF board [2–5]. These platforms are costly considering the component cost of the hardware supplied and have been designed with different goals and hence don’t meet the full white space communication requirements. However, these boards can be used as a yardstick for the design of a white space hardware and useful inferences can be drawn by observing their merits and de-merits

2.1 Key Specifications

In this section, we shall briefly discuss the impact of some of the key Whitespace Communications specifications on the hardware design aspects. These specifications have been noted from the FCC and the IEEE 802.22 documents [1, 6].

2.1.1 Bandwidth of Operation

The first specification is the bandwidth of operation. As per the Whitespace regulations defined by FCC, the allowed channels have been shown in Table 2.1, [6]. The allowed frequency bands are part of the VHF and the UHF spectrum. This specification directly impacts the choice of the Radio Frequency hardware of the system. The choice of the RF hardware shall not only decide the operational bandwidth of the system but it will also play a part in deciding the price of the system.

2.1.2 Transmit Power

Another specification emerging from the FCC regulations is the maximum transmit power. It says that maximum Equivalent Isotropically Radiated Power (EIRP) of the system shall be less than 4 W (36 dBm). The choice of transmit power class of the system as shown in Table 2.2 shall decide the choice of the high power amplifier. General trend is that higher the power rating of the amplifier, higher is the price of the amplifying device.

Table 2.2 In-Band power: these specifications define the maximum limits of In-Band power levels and spectral densities radiated by the different classes of TVBDs

Device type	Typical conducted power output (dBm)	Typical antenna gain (dBi)	Absolute maximum EIRP (dBm)	Max power spectral density, PSD (in 100 KHz band) (in dBm EIRP)	Power control
Fixed-devices	30	6	36	12.6	Required
Personal/Portable device (operating @ adjacent channel to TV channels)	20	0	20	−1.4	Required
Sensing-only devices	–	–	–	−0.4	–
All other personal/portable devices	20	0	20	2.6	Required

2.1.3 Computational Specifications

The IEEE 802.22 WRAN architecture defines many computationally intensive tasks. These tasks require powerful processing units as well as onboard memory elements. Some of these tasks are as follows:

- **OFDM and OFDMA:** The specification defines 2,048 point FFTs for the transmit OFDM and receive OFDMA which are highly computationally intensive. The OFDM/OFDMA specifications are shown in Table 2.3.
- **Spectrum Sensing:** The spectrum sensing sensitivity specifications defined by the FCC are shown in Table 2.4. In order to sense the spectrum at such sensitivities, the system requires to implement efficient spectrum sensing algorithms. The spectrum sensing algorithms like the Eigen Value based sensing necessitate generation of huge covariance matrices and fast iterative calculations. Such tasks require sufficient memory as well as computational elements.
- **Control and Management:** Apart from the above resource intensive tasks, the control and the management plane defined in the Protocol Reference Model (PRM) of the IEEE 802.22 also requires storing and running of many routines at the same time.

Hence, the Hardware designer needs to ensure that necessary steps have been taken to provide enough memory and computational resources to perform the above mentioned tasks. The designer also needs to optimize the design of the radio frequency

Table 2.3 OFDM requirements

Property of OFDM	Value	Remark
Total number of sub-carriers (N_{FFT})	2048	–
Number of guard sub-carriers (N_G)	368	(184, 1, 183)
Number of used sub-carriers ($N_t = N_d + N_p$)	1680	–
Number of data sub-carriers (N_d)	1440	–
Number of pilot sub-carriers (N_p)	240	–
Data sub-carriers/channel	24	Total of 28 subcarriers/channel
Pilot sub-carriers/channel	4	
Total number of channels	60	–
Length of cyclic prefix	74.7	in usecs (to compensate for unequal channel fadings)
Total size of the guard bands	1.08	in MHz

Table 2.4 Interference avoidance, spectrum sensing: sensitivity specifications

Signal type	Sensitivity-threshold (dBm)	Integration bandwidth	Detector type
ATSC, digital TV	–114	6 MHz	Average
NTSC, analog TV	–114	200 kHz	Average
Wireless microphone	–114	100 kHz	Average

hardware subsystems. The design decisions shall impact both the price and performance of the system. After having discussed some of the key specifications (from hardware perspective), we shall now move on to discuss some of the currently available SDR platforms.

2.2 USRP N210

The USRP(Universal Software Radio Peripheral) N210 is an SDR platform from Ettus Research, Fig. 2.1. Its a complete system which includes digital and RF subsystems allowing users to use this piece of hardware for various applications. Packed with high speed FPGA, dual ADC's, DAC's and Ethernet connections, its very powerful for data streaming to and from host processors. The USRP also provides seamless integration with the GNU radio which makes it an convenient platform for rapid prototyping [2].

The notable feature are:

- Xilinx Spartan 3A-DSP 3400 FPGA: Comprises of 54 K logic cells.
- Interfaces: Gigabit ethernet, 2 Gbps expansion interface, RF interfaces with SMA connectors etc.
- ADC/DACs: The USRP comes with high speed dual 100 Msps 14-bit ADCs and dual 400 Msps 16-bit DAC.
- Software compatibility: GNU Radio, LAB VIEW and Simulink.



Fig. 2.1 USRP N210—Ettus research. Photo courtesy—<https://www.ettus.com/product/details/UN210-KIT>

- Other features: DC—6 GHz operation bandwidth, fully coherent MIMO capability, 2.5 ppm TCXO reference.

2.2.1 Hardware Architecture

The Hardware Architecture of the USRP is shown in Fig. 2.2. As we can see, the Spartan 3A-DSP FPGA forms the core of the USRP N210 system. The control and management is handled by a softcore microblaze processor. At the backend, it is connected to one ethernet PHY and at the front end, it is connected to the high-speed dual ADCs and DACs. The FPGA is also connected to a MIMO expansion header. Two USRP have to be connected to form a 2×2 MIMO configuration.

The USRP without connecting to the RF daughter board consumes around 8 Watts of power. With the WBX daughter card designed to work with the USRP, it can transmit a maximum RF power of 15 dBm. The WBX has a receive noise figure of 5 dB [7].

2.2.2 Merits

The merits of the USRP N210 are as follows:

1. The board has standard connectors and standard interfaces which makes it a ready to use commercial platform.
2. The processing bandwidth is 100 MHz which is very useful for spectrum sensing kind of applications.
3. Since, it integrates well with GNU Radio, fast prototyping capability of this board is a great advantage [8].
4. It does not have unnecessary extra-peripherals and hence, very application specific.

2.2.3 De-Merits

The USRP N210 has many de-merits:

1. Spartan 3A-DSP is a low end FPGA.
2. By implementing a softcore processor like the micro blaze consumes a third of its space leaving out very less space for other blocks.
3. Absense of on-board RAMs make it almost impossible to perform much signal processing on the board.
4. Priced at about 1,800 USD, it is not a very cheap platform.

2.3 NUAND Blade RF Board

The NUAND Blade RF board is an open source USB 3.0 software defined radio (SDR) board, Fig. 2.3. It contains a micro processor, an FPGA for configurable logic and the LMS6002D RF transceiver [3]. It has SMA connectors which have to connect to an RF front end. This board is capable for MIMO operation. The platform runs Linux, Windows, Mac and has GNU Radio software support [8].

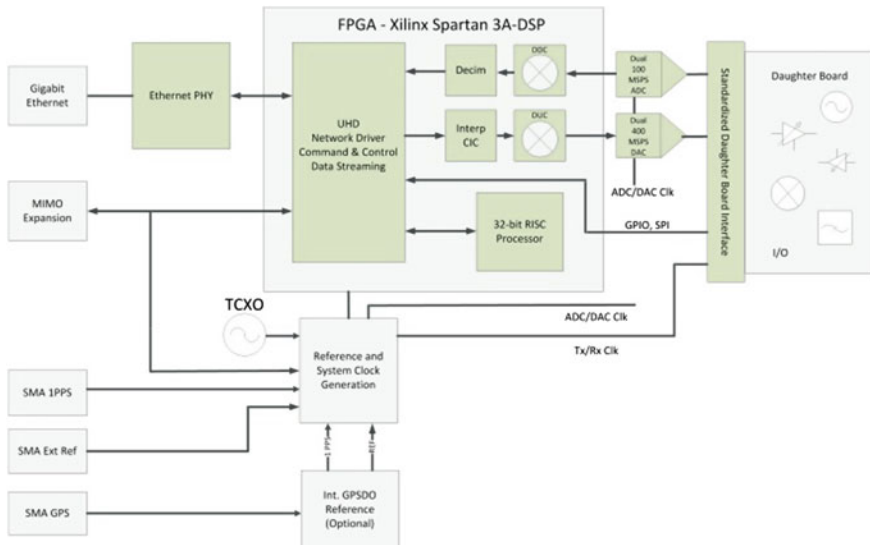


Fig. 2.2 USRP N210—hardware architecture. Photo courtesy—https://www.ettus.com/content/files/07495_Ettus_N200-210_DS_Flyer_HR_1.pdf

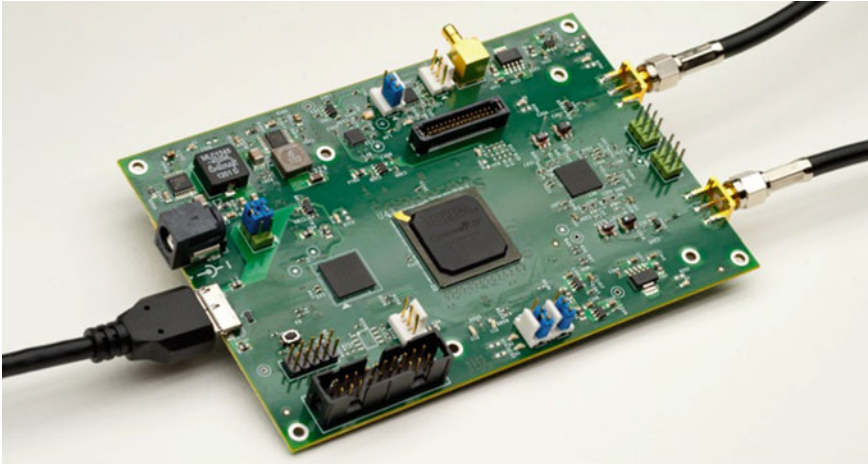


Fig. 2.3 NUAND—bladeRF board. Photo courtesy—<http://nuand.com/>

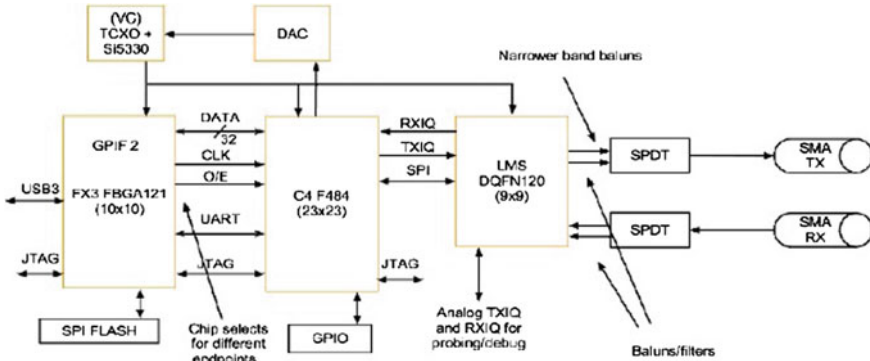


Fig. 2.4 NUAND—bladeRF hardware architecture. Photo courtesy—<http://nuand.com/bladeRF.pdf>

2.3.1 Hardware Architecture

The bladeRF board has a processing core which is the ARM A-9 microprocessor, a programmable logic IC which is the Altera Cyclone-4 FPGA and the LMS6002D RF transceiver. The FPGA provides the interface between the ARM and the transceiver. Its RF section does not provide Fig. 2.4 any duplexing facilities. It just makes the transmit and the receive outputs available at two SMA connectors. This board can be powered by USB and has a 512 MB embedded SRAM. The transceiver is configured through the SPI interface from the Cyclone-4 FPGA [9]. The board comes with external JTAG interfaces for both the processor and the FPGA for the debug and configuration.



Fig. 2.5 Zepto SDR. Photo courtesy—<http://www.nutaq.com/en/products/zeptosdr>

2.3.2 Merits

The board has the following merits:

1. Priced at 650 USD, it is a cost effective board which has all elements for a radio frequency system functionality.
2. GNU Radio support [8].
3. With 115 KLE (K logic elements), it offers high amount of onboard programmable resources.
4. High Speed USB 3.0 functionality.
5. Small form factor of 5" by 3.5"

2.3.3 De-Merits

Inspite of the obvious merits, the NUAND bladeRF has the following de-merits:

1. Absence of ethernet functionality. In order to interface the board with packetized networks, an additional board has to be connected.
2. Absence of a duplexing system for transmit and receive ports.
3. Peak output power of 6 dBm is low.

2.4 Zepto SDR Board

The Zepto SDR board from Nutaq is a complete SDR product which houses two separate boards Fig. 2.5. One is the Zedboard from Digilent and the Radio420S board from Nutaq. The Zedboard and the Radio420S board are interfaced using the FMC connectors. While the Zedboard forms the digital processing core of the Zepto

SDR platform, the Radio420S board forms the air interface subsystem. Now, we shall discuss both the boards in greater detail [4].

2.4.1 ZedBoard

The ZedBoard is a very low cost Xilinx Zynq7000 development platform, Fig. 2.6 [10]. It is a very generic board which allows one to use it for a wide range applications. Due to its expandable features, the Zedboard is very convenient for rapid prototyping. The notable feature of the Zedboard are [11]:

- Xilinx XC7Z020-1CLG484CES Zynq-7000 AP SoC: It can be configured through QSPI flash, cascaded JTAG and SD card.
- Memory: 512 MB DDR3 and 126 Mb QSPI flash.
- Interfaces: USB JTAG, 10/100/1G Ethernet, USB OTG 2.0, SD Card, Digilent PMOD Headers, LPM FMC (FPGA Mezzanine card) header and so on.
- Display or Audio: The Zedboard comes with various display or audio connectors like HDMI, VGA, OLED display, audio line in, line out and microphone.

2.4.1.1 Hardware Architecture

The hardware architecture of the ZedBoard is shown in Fig. 2.7. Even though we shall discuss the Zynq-7000 SoC architecture in greater detail later, we would just like to mention that the SoC is partitioned into programmable logic (PL) and processing system (PS) elements. The processing system consists of the embedded dual core ARM Cortex A-9 processors with NEON floating point arithmetic logic units (ALUs). The programmable logic blocks have standard Xilinx FPGA elements like configurable logic blocks (CLBs), DSP slices, RAM block and so on. There are also multiplexed IO pins which can be accessed either from the PS or the PL blocks. However, the MIOs refer to the PS pins and EMIO refer to the PL pins. As we can observe from Fig. 2.7, all the control, configuration and memory interfaces like USB UART, Ethernet PHYs, DDR3, SD card, clocks, resets etc are connected to the processing system or its MIOs. The application related peripherals like the FMC, general purpose IOs (GPIOs), audio and video interfaces are connected to the programmable logic [12].

The ZedBoard has a 10-Layer PCB stackup [13]. As we can see in Fig. 2.8, there are six signal layers. Three important aspects of the ZedBoard PCB design are noticeable from this stackup:

1. The two sets of internal signal layers are not standard striplines because each set has two signal layers placed adjacently to each other.
2. The internal signal layers are coupled to power planes as well instead of being coupled to just grounds.
3. Due to low layer count, each power supply does not have a single plane. Instead, planes have been split to accommodate for all the various power supplies.

As a result of these three design aspects, the cost of the ZedBoard PCB is very low.

2.4.1.2 Merits

Following are the merits of the ZedBoard:

1. Very Low Cost, less than 400 USD.
2. Very Generic and can cater to wide variety of applications due to its expandability and various features.
3. A convenient platform to learn and evaluate all capabilities of the Zynq7000 SoC.
4. Standard FMC interface for connection to daughter boards.

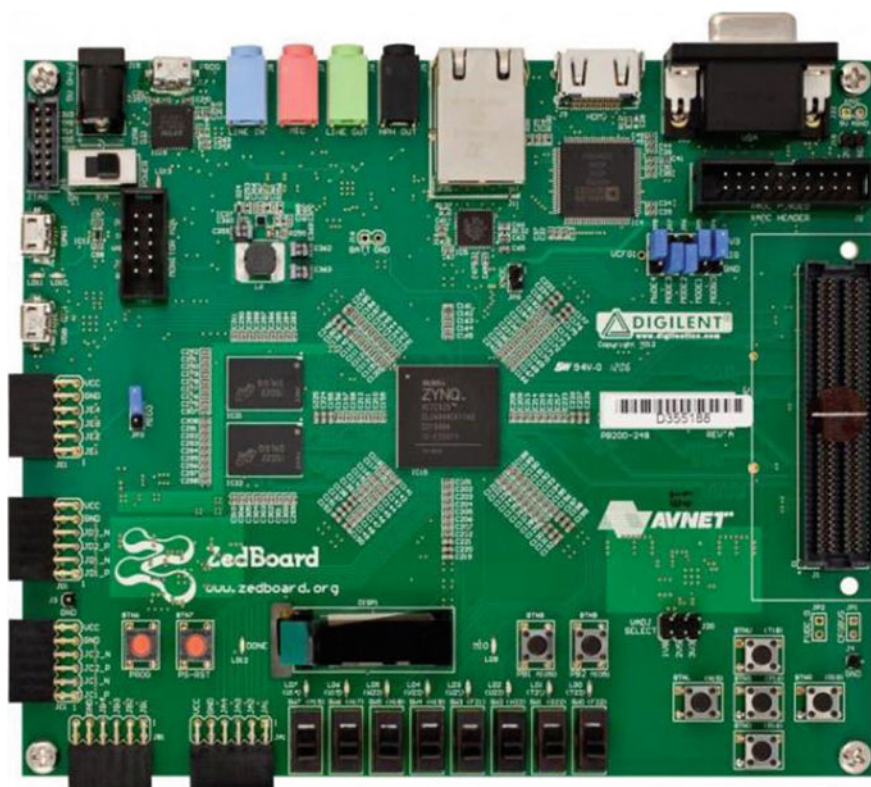


Fig. 2.6 Zedboard—hardware architecture. Photo courtesy—<http://www.zedboard.org>

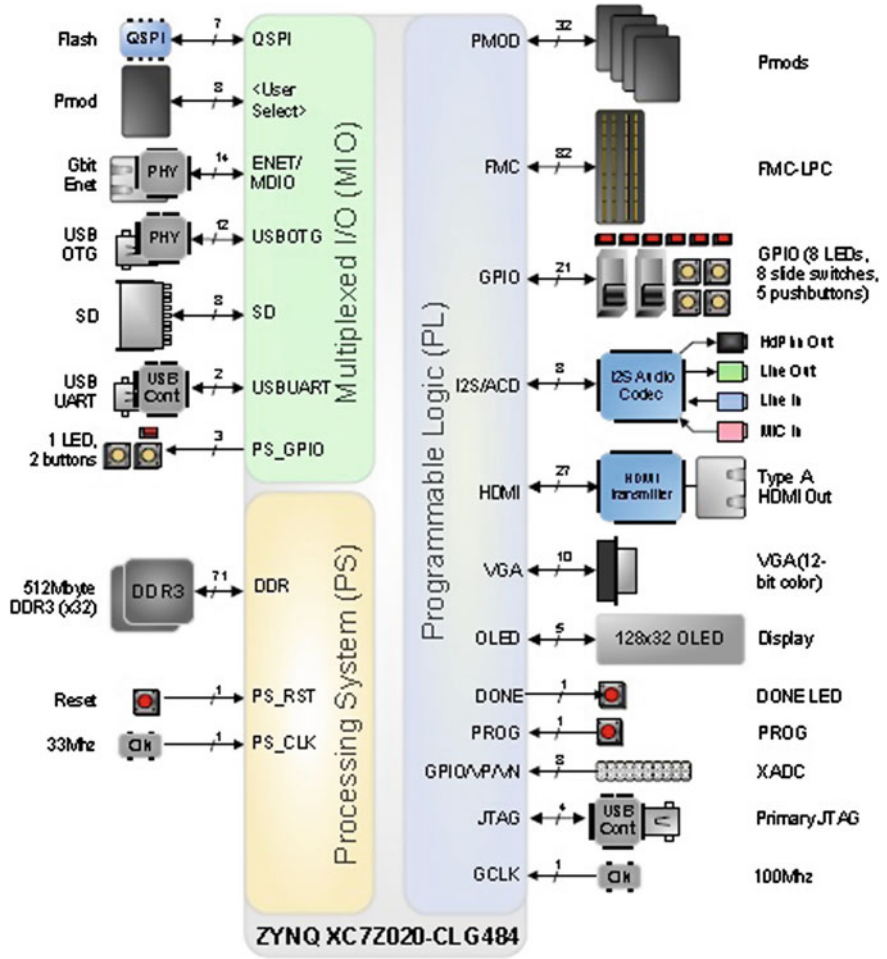


Fig. 2.7 Zedboard. Photo courtesy—ZedBoard (Zynq Evaluation and Development) hardware users guide

2.4.1.3 De-Merits

Following are the de-merits of the ZedBoard:

1. Not application specific as its meant to be an evaluation board.
2. Additional plugin boards have to be used if the final goal is to have a complete communication or radar system.
3. Due to many peripherals and connectors which consume a lot of space, the size of the board(5.3" by 6.3") is large when compared to more application specific modules.



Fig. 2.8 Zedboard—layer stackup. Photo courtesy—ZedBoard, power distribution and decoupling system

2.4.2 NUTAQ Radio420S Board

The Radio420S FPGA mezzanine card (FMC) is a software defined radio (SDR) RF transceiver module which uses the Lime Micro LMS6002D SoC, Fig. 2.9. It is a multi-mode module which supports time division duplex (TDD) as well as frequency division duplex (FDD) modes. The board has an operating frequency of 300 MHz–3 GHz with an instantaneous bandwidth of 1.5–28 MHz. The board has to be connected through an FMC connector to a digital motherboard for configuration and data transfer [14]. This board is aimed for communication applications like MIMO systems, cognitive radios, WiMAX, White Space, Wi-Fi, GSM, WCDMA and so on.

2.4.2.1 Hardware Architecture

The board has a simple hardware architecture. It contains the RF transceiver LMS6002D whose all the digital control and data line are connected to the low pin count (LPC) FMC connector. It has a selectable clock reference input. There are two RF output connectors, one for transmit and the other for receive. The outputs are connected through a set of baluns which convert the various differential transmit/receive outputs/inputs to 50 Ω single-ended outputs/inputs respectively [15].

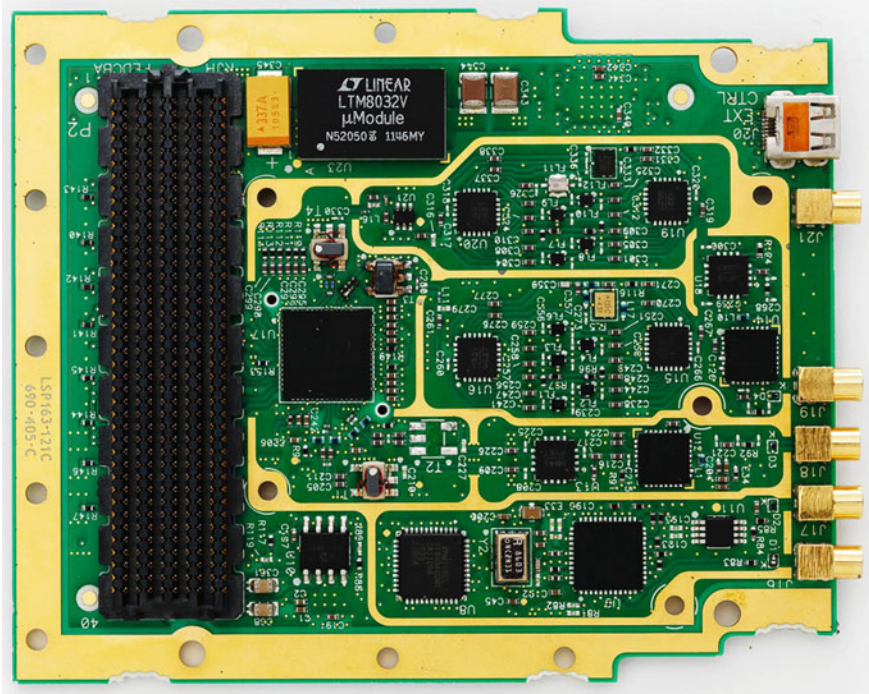


Fig. 2.9 NUTAQ—Radio420S. Photo courtesy—<http://nutaq.com/en/products/view/+nutaq-radio420x>

2.4.2.2 Merits

The merits of the NUTAQ Radio420X board are:

1. Simple design.
2. Utilizes all the features of the LMS6002D SoC.
3. Standard FMC connector for interfacing with motherboards.

2.4.2.3 De-Merits

1. Lacks proper frontend section. Even though its TDD and FDD compatible but implementation of those features would require a further RF frontend board.
2. Low output power for an RF module. The peak Output power is only 10dBm.
3. The FMC connector consumes a major portion of the board space.
4. Again like the Zedboard, its too generic and not a particular application or communication standard oriented board.

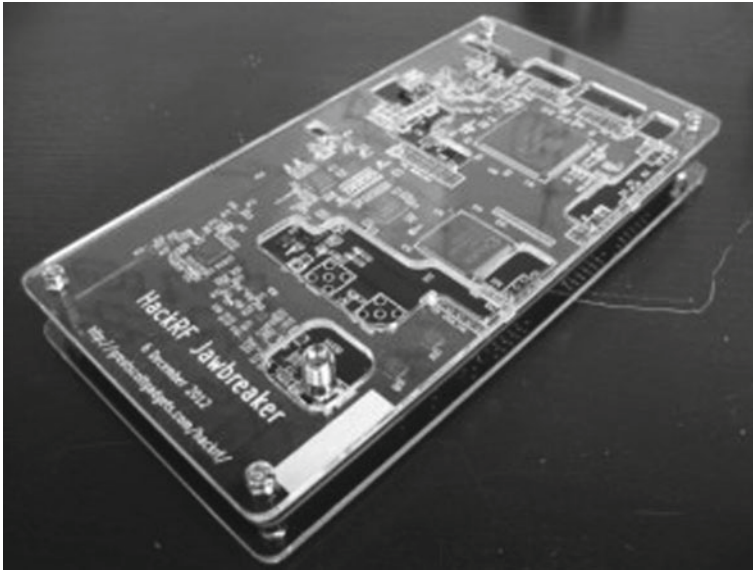


Fig. 2.10 HackRF SDR platform. Photo courtesy—<http://www.rtl-sdr.com/hackrf-vs-bladerf-vs-usrp/>

2.5 HackRF SDR Platform

The HackRF is a very new SDR platform platform which offers wideband performance at an extremely cheap cost, Fig. 2.10. The HackRF SDR platform consists of a CPLD device along with a wideband RF transceiver. This platform aims to provide widest band of operation at the cheapest price when compared to all other SDR platforms [5].

2.5.1 Hardware Architecture

The HackRF Hardware consists of a heterogeneous architecture with an ARM-based microcontroller and a CPLD which form the digital core of the platform. The microcontroller is the LPC43XX from NXP semiconductors [16]. It also contains a very wideband transceiver section capable of operating from 30 MHz to 6 GHz. The primary digital interface is the USB 2.0 and hence, has been designed primarily for use with a USB-attached host computer.

Table 2.5 Comparison

	USRP N210	Nuand blade RF	Zepto SDR	Hack RF
Operational bandwidth	DC—6 GHz	300 MHz–3 GHz	300 MHz–3 GHz	30 Mhz–6 GHz
Instantaneous bandwidth	100 MHz	28 MHz	28 MHz	20 MHz
Computational	Spartan-3A DSP FPGA	Altera Cyclone-4 FPGA	Zynq-7020	CPLD
Interfaces	USB 2.0	USB 3.0	2 Gbps Ethernet, HDMI, UART-USB, JTAG-USB, USB-OTG etc	USB 2.0
Sample size (ADC/DAC)	12 bit	12 bit	12 bit	8 bit
Price	High	Low	Highest	Lowest

2.5.2 Merits

The various positive points of the HackRF board are:

1. At 300 USD it aims to be the lowest priced SDR platform.
2. Very wide bandwidth of operation of 30 MHz–6 GHz.
3. Instantaneous bandwidth of 20 MHz.
4. The HackRF integrates with the GNU Radio framework.
5. The HackRF designs have been completely open-sourced.

2.5.3 De-Merits

Inspite of the many positives, it has many drawbacks. They are:

1. Absense of Ethernet functionality which is an integral part of a communication system.
2. For implementation of baseband elements, the HackRF only has a CPLD whose capabilities are very limited.
3. The digital IOs of the ADC/DACs are only 8-bit wide which means that the dynamic range of the platform would be low.
4. There are no onboard memory elements apart from the CPLD.
5. The development of this platform is still ongoing and hence, is not a matured product.

2.6 Chapter Summary

In this chapter, we discussed some implications of the Whitespace Technology specifications on the hardware design. Then, we identified and discussed four currently available SDR platforms. While the HackRF and the BladeRF are very low cost platforms, they are still in their development phases and hence, the products are not very matured yet. Also, they are not computationally very powerful and do not have much onboard memory elements. However, the USRP N210 and the Zepto SDR are commercial platforms and hence, very expensive. At 2295 USD, the Zepto SDR is a very powerful platform computationally. It incorporates the latest Zynq device from Xilinx and is packed with loads of other features along with 2 Gbps Ethernet facility. The USRP N210, on the other hand with a low-end FPGA and limited feature set is very expensive at 1,800 USD. Its high price is due to the fact that USRP series platforms are among the oldest commercially available SDR platforms leading to their immense popularity. It also has a very wideband performance when compared to the Zepto SDR and the Blade RF. However, from a Whitespace Technology perspective, this feature is not required as the operational bands are in the VHF and the UHF regions of the spectrum. To sum up, even though none of these platforms are optimized for Whitespace Communications, they can be used for prototyping and testing various functionalities while the hardware is being developed. The key features of the SDR platforms that we have discussed above have been summarized in Table 2.5.

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White Space Communication

Advances, Developments and Engineering Challenges

Mishra, A.K.; Johnson, D.L. (Eds.)

2015, XII, 295 p. 159 illus., 125 illus. in color.,

Hardcover

ISBN: 978-3-319-08746-7