EE502 - Advanced Computer Architecture
Paper Critique 1

1 Summary of Technical Contributions

Microarchitecture advances to increase single threaded performance in turn lead to excessive power consumption. This increased can be countered by improvements in process technology, architecture, and microarchitecture. To measure the improvements, 6 Intel processors from different generations are used. The processors are brought at par by, e.g. shutting of extra cores of processors which had more cores and the same environment and variables are used for all the tests. Livermore Loops benchmark suite, a collection of compute intensive kernels is used for benchmarking the results. Several billion iterations are run of the kernel which as between 13 to 83 instructions with the processor warmed up before the runs and each core running an instance of the kernel to amplify dynamic power consumption. Energy consumption is calculated my multiplying average power (measured in watts) by duration of computation, and energy efficiency is its reciprocal, more specifically: $\frac{\mathbf{1}}{\mathbf{energy}} = \mathbf{frac1durationxpower} = \frac{\mathbf{performance}}{\mathbf{power}}$. Register scrambling, a technique to alter and mix register level instructions of a kernel is used to estimate how much change in performance will affect the energy efficiency, as more scrambled the instructions are, the more decrease in performance is noticed.

2 Opinion/Weaknesses/Strengths

The processors used have different frequencies and fabrication sizes which affect clock cycles and the amount of heat generated and more heated a component gets, the more performance it looses. From 2007 and 2013, and pipelining has become more aggressive and this can affect the results. It cannot be assumed that all processors have been brought onto the same level. Moreover the processors were put on full load during tests, but to test it under real world conditions,instructions should be a mix which could stall the processor often, and the average of full and half load performance should be taken, as normally a processor is not always running on full load. The results also do not clearly state which micro architectural feature was more powerful in each processor and how much improvement each processor gained.

The paper justifies the technique(s) used well, touches major aspects and outlines what has been achieved. The future work area are also sited clearly and this paper opens new gateways for future research and experiments.

The paper does not make an effort to include the semantics to rate it as a generalized results as the code run on the processors was from a specific domain and so was the environment and the compiler. A mix of environments, compilers and kernels should have been used and the gain or drop in efficiency should have been pitted against when the same piece of code would have been run under normal, non-supervised conditions.

3 Comment on how the current approach can be improved

Temperature sensors can be used to pick up temperature readings of all cores. Putting load on a core means it would draw more energy, but a heated processor looses it performance and does not perform like a cooled processor.

The benchmark tests should be run while the processor is below a given threshold of temperature and also when it is above a given threshold of temperature and the average of readings should be taken. This would also help uncover another mystery that does a heated up processor actually draw in more energy when a certain amount of load is out on it. Also a mix of different conditions/environments, compilers and kernels should be used to generalize the results, and as the newer processors have more clock speed, smaller fabrication size and more aggressive pipelining; they certainly outperform the older processors, therefore the newer ones should be run more advanced processor/power intensive tests.

4 Questions

1. How do the authors/this paper justify that energy consumption of processors with different clock speeds and different fabrication sizes can be compared. These cannot be ignored when comparing energy/performance levels how do the calculations incorporate/adjust the energy each transistor requires to fulfil its functionality and produce output at different processor utilization levels.

2. How does using the same ISA, same environment and same kernel do justice to the results as different generations of processors are being used? The ISA, the environment, and the kernel being used could give one processor an edge over the other.

3. How can the paper generalize the results when different processors can have different arrangement of physical cores, caches, registers and transistors, which can affect the results and give one processor an unfair advantage over the other. Physical arrangement of components can also lead to a change in power consumption.